实验一（2）：双2选1多路选择器（层次化设计）

* 实验原理：根据2位选择信号输出输入信号a1或输入信号a2或输入信号a3,通过实例化实验一的模块实现。
* 设计过程：

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 输入 | | | | | 输出 |
| A1 | A2 | A3 | S0 | S1 | outy |
| 0/1 | 0/1 | 0/1 | 0 | 0 | A1 |
| 0/1 | 0/1 | 0/1 | 0 | 1 | A2 |
| 0/1 | 0/1 | 0/1 | 1 | 0 | A1 |
| 0/1 | 0/1 | 0/1 | 1 | 1 | A3 |

代码：

module mux221A(a1,a2,a3,s0,s1,outy);

input a1,a2,a3,s0,s1;

output outy;

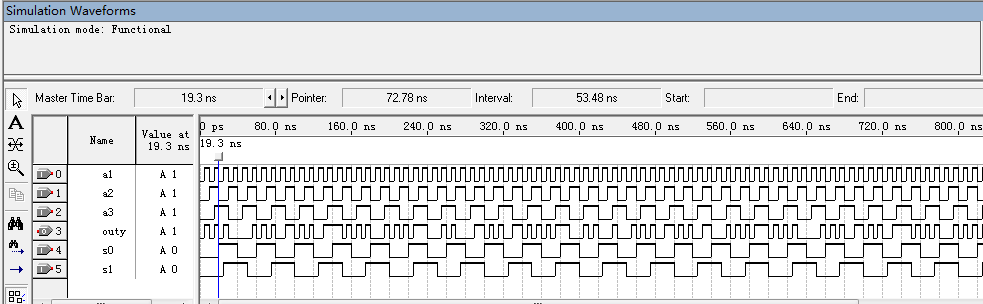
wire tmp;

mux21 u1(a2,a3,s0,tmp);

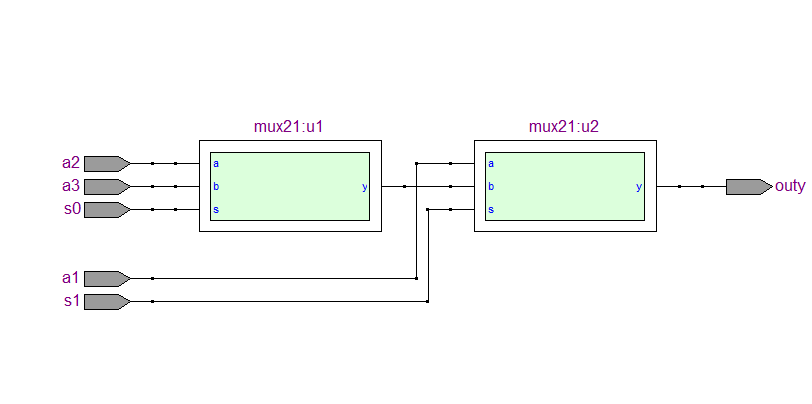
mux21 u2(a1,tmp,s1,outy);

endmodule

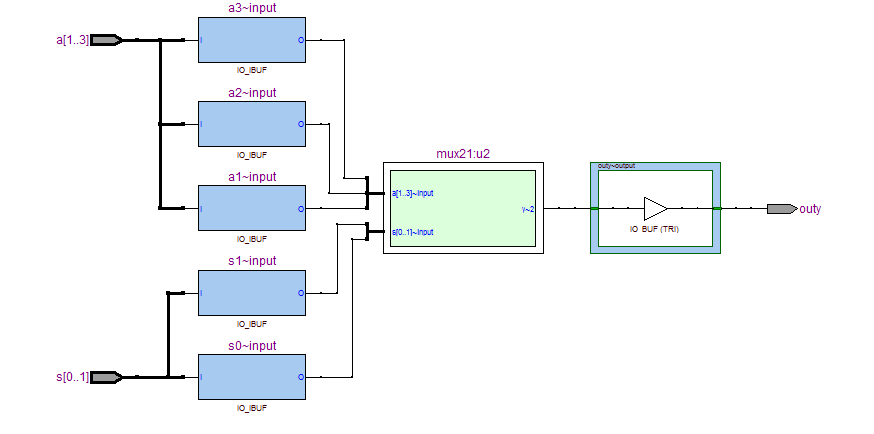
* 仿真波形



* RTL



* 门电路



* 实验分析：

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 输入 | | | | | 输出 |
| A1 | A2 | A3 | S0 | S1 | outy |
| 0/1 | 0/1 | 0/1 | 0 | 0 | A1 |
| 0/1 | 0/1 | 0/1 | 0 | 1 | A2 |
| 0/1 | 0/1 | 0/1 | 1 | 0 | A1 |
| 0/1 | 0/1 | 0/1 | 1 | 1 | A3 |

**实验三：双2选1多路选择器（行为描述）**

* 实验原理：根据2位选择信号输出输入信号a1或输入信号a2或输入信号a3,通过case语句实现。
* 设计：

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 输入 | | | | | 输出 |
| A1 | A2 | A3 | S0 | S1 | outy |
| 0/1 | 0/1 | 0/1 | 0 | 0 | A1 |
| 0/1 | 0/1 | 0/1 | 0 | 1 | A2 |
| 0/1 | 0/1 | 0/1 | 1 | 0 | A1 |
| 0/1 | 0/1 | 0/1 | 1 | 1 | A3 |

代码：

module mux221B(a1,a2,a3,s0,s1,outy);

input a1,a2,a3,s0,s1;

output outy;

reg outy;

always@(\*)

begin

case({s0,s1})

2'b00:outy<=a1;

2'b01:outy<=a2;

2'b10:outy<=a1;

2'b11:outy<=a3;

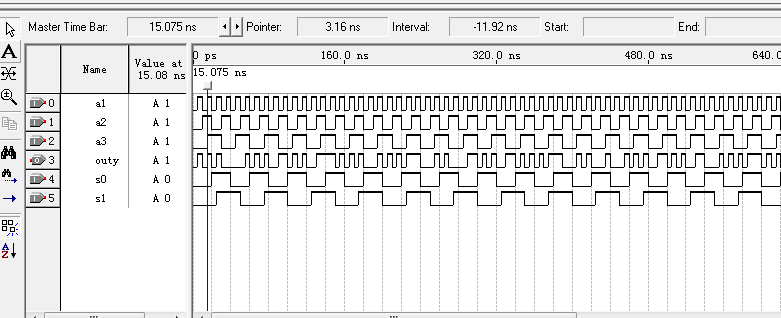
default:outy<=a1;

endcase

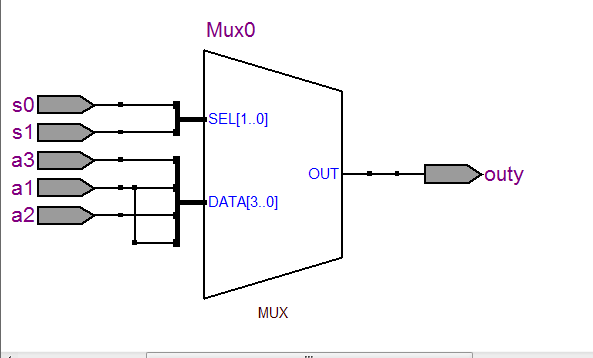
end

endmodule

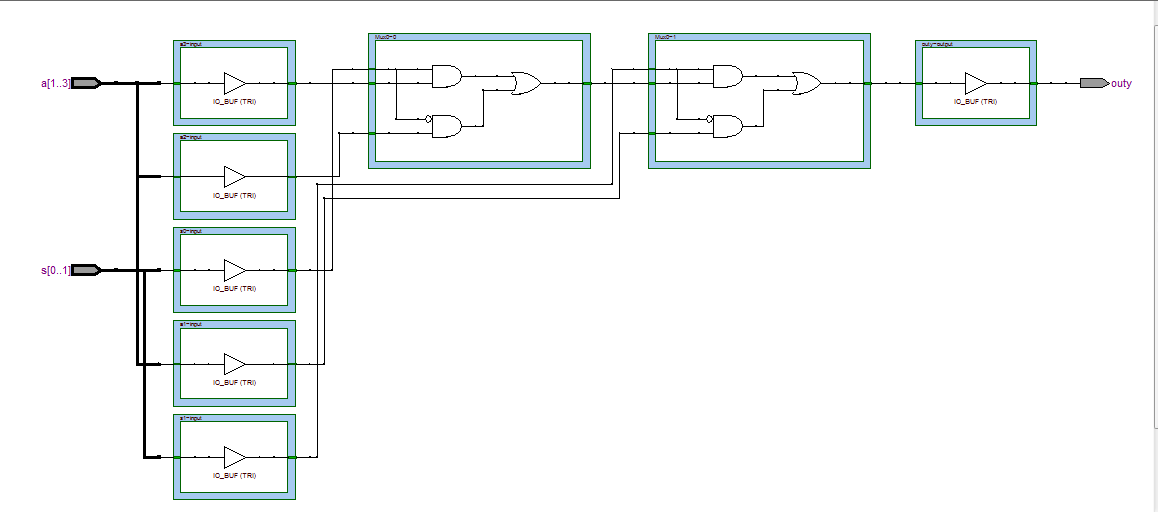
* 仿真波形



* RTL



* 门电路



* 实验分析:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 输入 | | | | | 输出 |
| A1 | A2 | A3 | S0 | S1 | outy |
| 0/1 | 0/1 | 0/1 | 0 | 0 | A1 |
| 0/1 | 0/1 | 0/1 | 0 | 1 | A2 |
| 0/1 | 0/1 | 0/1 | 1 | 0 | A1 |
| 0/1 | 0/1 | 0/1 | 1 | 1 | A3 |