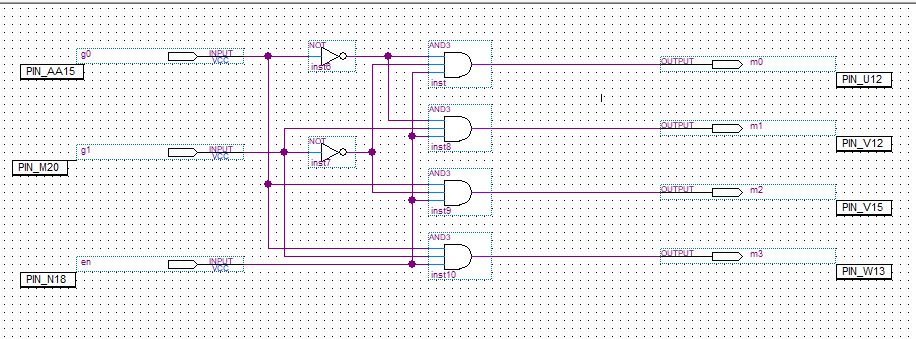
EDA实验三

实验目的：使用VHDL设计一个带使能的24译码器,0代表灯亮，不译码，1代表灯灭，译码。

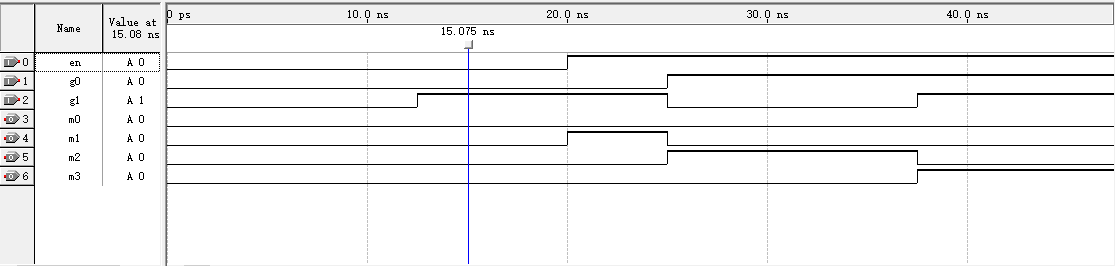
实验设计：

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Input | | | output | | | |
| En | G1 | G0 | M3 | M2 | M1 | M0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 |

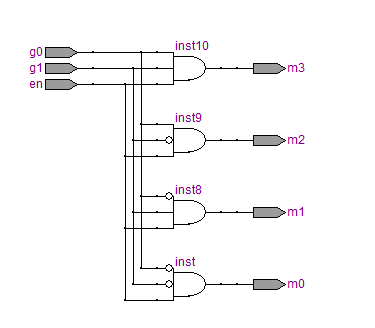
电路图：



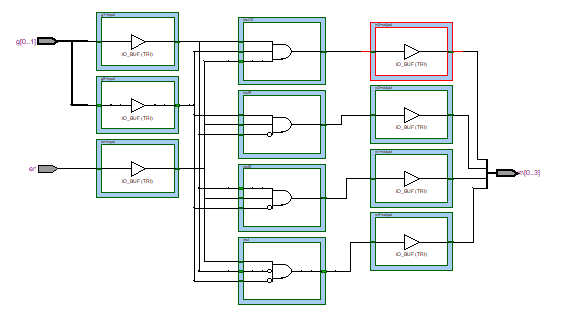
仿真：



RTL：



门电路：



实物图：

