**电子设计自动化（EDA）实验报告**

实验九

1. 实验内容

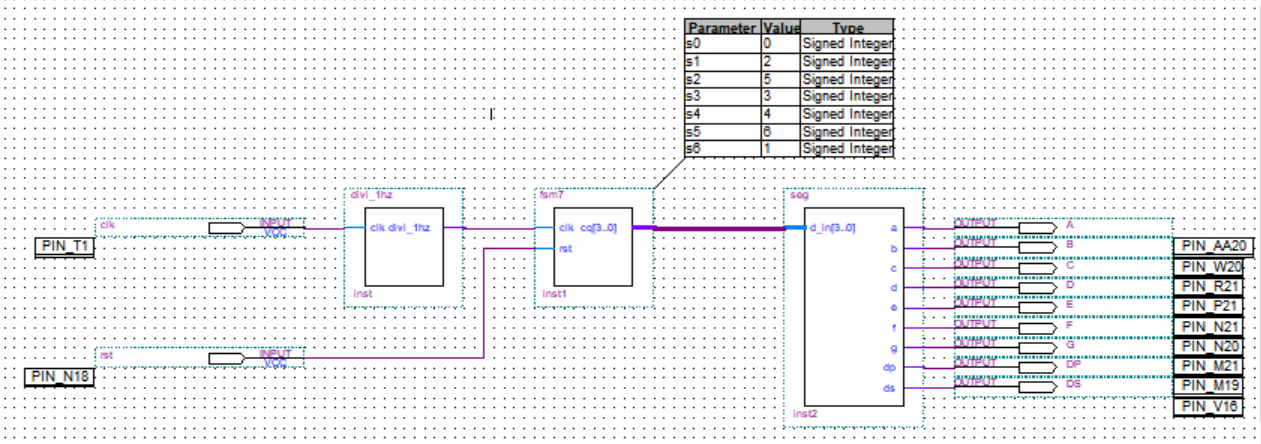
使用状态机设计任意编码计数器，在数码管上显示7进制计数器：0，2，5，3，4，6，1。

1. 实验原理

使用状态机设置7个状态，分别输出0，2，5，3，4，6，1

1. 代码

顶层文件



状态机：

module fsm7(clk,rst,cq);

input clk,rst;

output reg [3:0] cq;

parameter s0=0,s1=2,s2=5,s3=3,s4=4,s5=6,s6=1;

reg[2:0] c\_st,n\_st;

//state machine

always @(posedge clk or negedge rst)

begin

if(!rst) c\_st<=s0;

else c\_st<=n\_st;

end

//output and next state

always@(\*)

begin

case(c\_st)

s0:begin cq<=0; n\_st<=s1; end

s1:begin cq<=2; n\_st<=s2; end

s2:begin cq<=5; n\_st<=s3; end

s3:begin cq<=3; n\_st<=s4; end

s4:begin cq<=4; n\_st<=s5; end

s5:begin cq<=6; n\_st<=s6; end

s6:begin cq<=1; n\_st<=s0; end

default:begin cq<=0; n\_st<=s0; end

endcase

end

endmodule

分频器：

module divi\_1hz(clk,divi\_1hz);

input clk;

output reg divi\_1hz;

reg [24:0] count\_reg1;

always@(posedge clk)

if(count\_reg1==25'd24999999) //（50Mhz / 1hz）/ 2 - 1

begin

divi\_1hz <= ~ divi\_1hz;

count\_reg1 <= 25'd0;

end

else

begin

count\_reg1 <= count\_reg1 + 25'd1;

end

endmodule

数码管显示：

module seg(d\_in,a,b,c,d,e,f,g,dp,ds);

input[3:0] d\_in;

output ds; //数码管使能信号，低电平有效

output a,b,c,d,e,f,g,dp;

reg [7:0] seg; //g,f,e,d,c,b,a,dp

assign ds = 0;

assign g = seg[7];

assign f = seg[6];

assign e = seg[5];

assign d = seg[4];

assign c = seg[3];

assign b = seg[2];

assign a = seg[1];

assign dp = seg[0];

always @(d\_in)

begin

case(d\_in)

4'b0000: seg = 8'b01111110; //g,f,e,d,c,b,a,dp

4'b0001: seg = 8'b00001100;//1

4'b0010: seg = 8'b10110110;//2

4'b0011: seg = 8'b10011110;//3

4'b0100: seg = 8'b11001100;//4

4'b0101: seg = 8'b11011010;//5

4'b0110: seg = 8'b11111010;//6

4'b0111: seg = 8'b00001110;//7

4'b1000: seg = 8'b11111110;//8

4'b1001: seg = 8'b11011110;//9

4'b1010: seg = 8'b11101110;//A

4'b1011: seg = 8'b11111000;//B

4'b1100: seg = 8'b01110010;//C

4'b1101: seg = 8'b10111100;//D

4'b1110: seg = 8'b11110010;//E

4'b1111: seg = 8'b11100010;//F

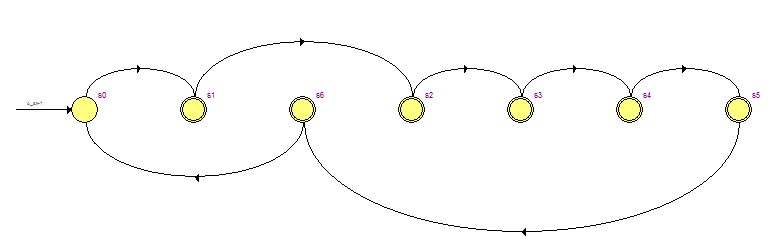
default: seg = 8'b00000000;//其他情况什么都不输出

endcase

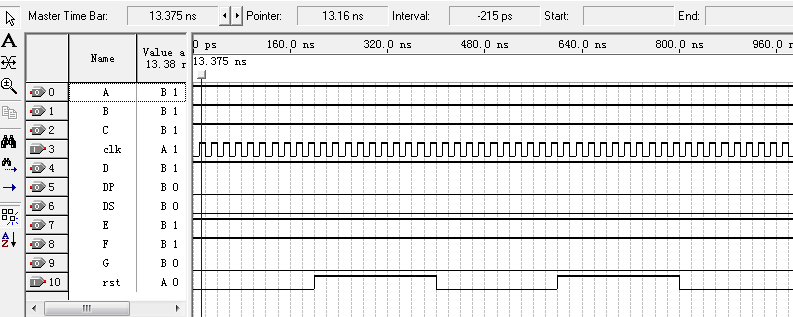
end

endmodule

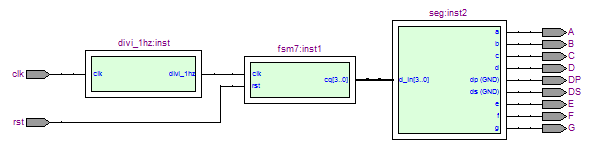
状态转换图：



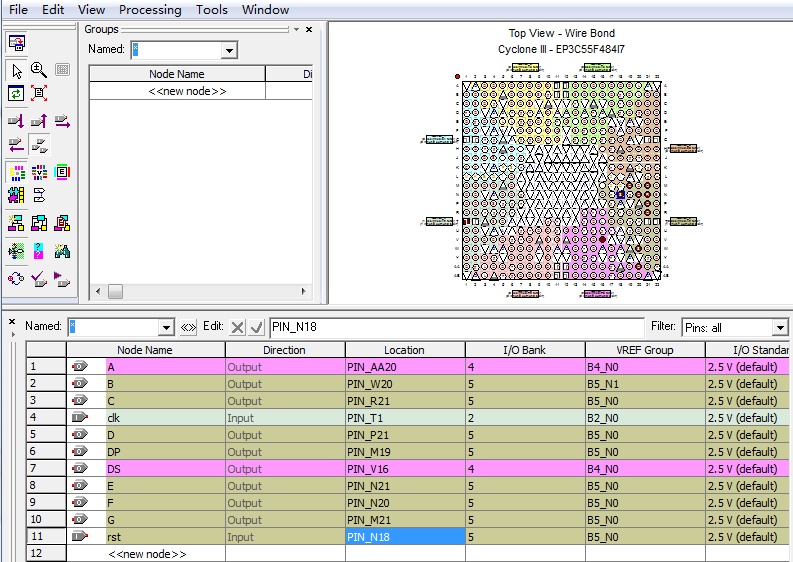
1. 仿真



1. RTL



1. 引脚绑定



1. 扩展：
   1. 实验内容
   2. 本实验通过实验平台上的八个共阴数码管，从左到右依次显示 8，7，6，5，4，3，2，1，并将拨码开关 SW1-SW8 作为使能输入，控制对应数码管显示功能的实现。时钟频率可以选 1K~100KHz
   3. 实验原理

使用状态机扫描7个数码管，只要频率足够快，就能在人眼上实现视觉暂留，同时显示。

* 1. 代码

module seven(clk,en,a,b,c,d,e,f,g,dp,sel);

input clk;

input [7:0]en;

output a,b,c,d,e,f,g;

output reg [7:0]sel;

output dp;

parameter [2:0]s1=000;

parameter [2:0]s2=001;

parameter [2:0]s3=010;

parameter [2:0]s4=011;

parameter [2:0]s5=100;

parameter [2:0]s6=101;

parameter [2:0]s7=110;

parameter [2:0]s8=111;

reg[7:0]data;

reg [2:0]current\_state;

reg [2:0]next\_state;

//reg [2:0]count;

always@(posedge clk)

begin

current\_state<=next\_state;

end

always@(posedge clk)

begin

case(current\_state)

s1:next\_state<=s2;

s2:next\_state<=s3;

s3:next\_state<=s4;

s4:next\_state<=s5;

s5:next\_state<=s6;

s6:next\_state<=s7;

s7:next\_state<=s8;

s8:next\_state<=s1;

default:next\_state=s1;

endcase

end

always@(posedge clk or negedge en)

begin

case(current\_state)

s1:

begin

if(en[0])

begin

sel<=8'b01111111;

data<=8'b00001100;

end

else

begin

sel<=8'b11111111;

data<=8'b00001100;

end

end

s2:

begin

if(en[1])

begin

sel<=8'b10111111;

data<=8'b10110110;

end

else

begin

sel<=8'b11111111;

data<=8'b10110110;

end

end

s3:

begin

if(en[2])

begin

sel<=8'b11011111;

data<=8'b10011110;

end

else

begin

sel<=8'b11111111;

data<=8'b10011110;

end

end

s4:

begin

if(en[3])

begin

sel<=8'b11101111;

data<=8'b11001100;

end

else

begin

sel<=8'b11111111;

data<=8'b11001100;

end

end

s5:

begin

if(en[4])

begin

sel<=8'b11110111;

data<=8'b11011010;

end

else

begin

sel<=8'b11111111;

data<=8'b11011010;

end

end

s6:

begin

if(en[5])

begin

sel<=8'b11111011;

data<=8'b11111010;

end

else

begin

sel<=8'b11111111;

data<=8'b11111010;

end

end

s7:

begin

if(en[6])

begin

sel<=8'b11111101;

data<=8'b00001110;

end

else

begin

sel<=8'b11111111;

data<=8'b00001110;

end

end

s8:

begin

if(en[7])

begin

sel<=8'b11111110;

data<=8'b11111110;

end

else

begin

sel<=8'b11111110;

data<=8'b11111110;

end

end

default:

begin

sel<=8'b11111111;

data<=8'b00000000;

end

endcase

end

assign a=data[1];

assign b=data[2];

assign c=data[3];

assign d=data[4];

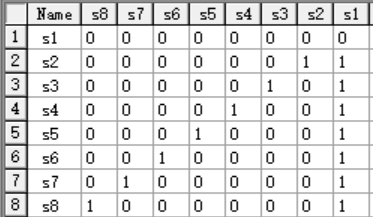
assign e=data[5];

assign f=data[6];

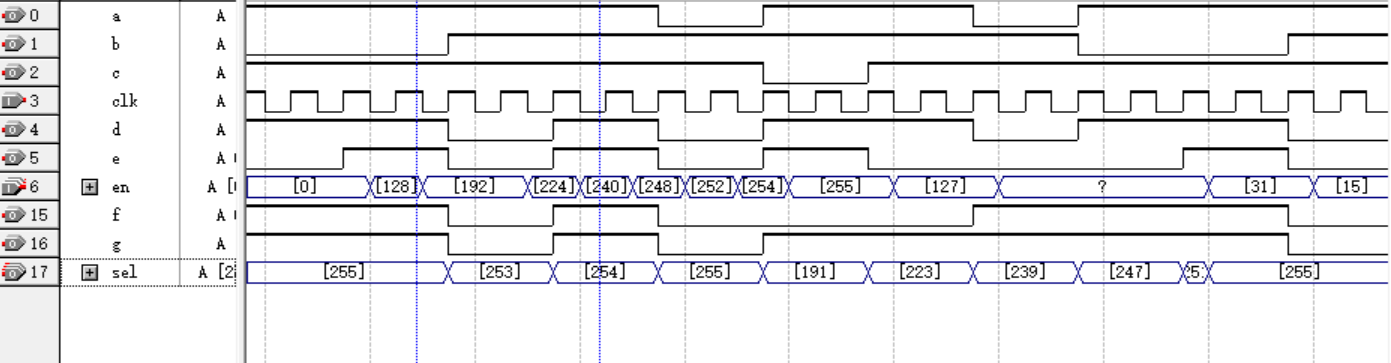
assign g=data[7];

assign dp=0;

endmodule



* 1. 仿真



* 1. RTL



* 1. 结果

在7个数码管上分别显示0，2，5，3，4，6，1.

忘记拍照了QAQ