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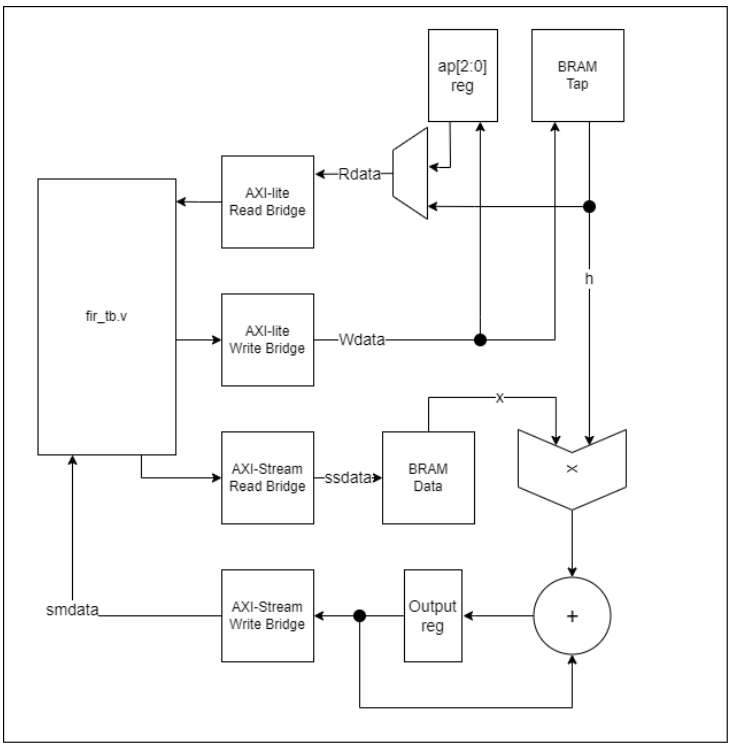
- Block Diagram：
  - Datapath：

Step 1：當 AXI-lite write 將 Tap parameter 送進 Bram tap 裡，若 waddr 是 00 就存入 ap_reg。

Step2：tb 檢查 Tap data，則我的 design 將 tap data 從 bram 讀出，並透過 AXI-lite read 傳回 tb。

Step3：當收到 ap_start，AXI-stream read 開始將 data 收進來並進行 fir 的乘加法累加，當累加完成後，output reg 將結果給 AXI-Stream write bridge。



  - Control signals：

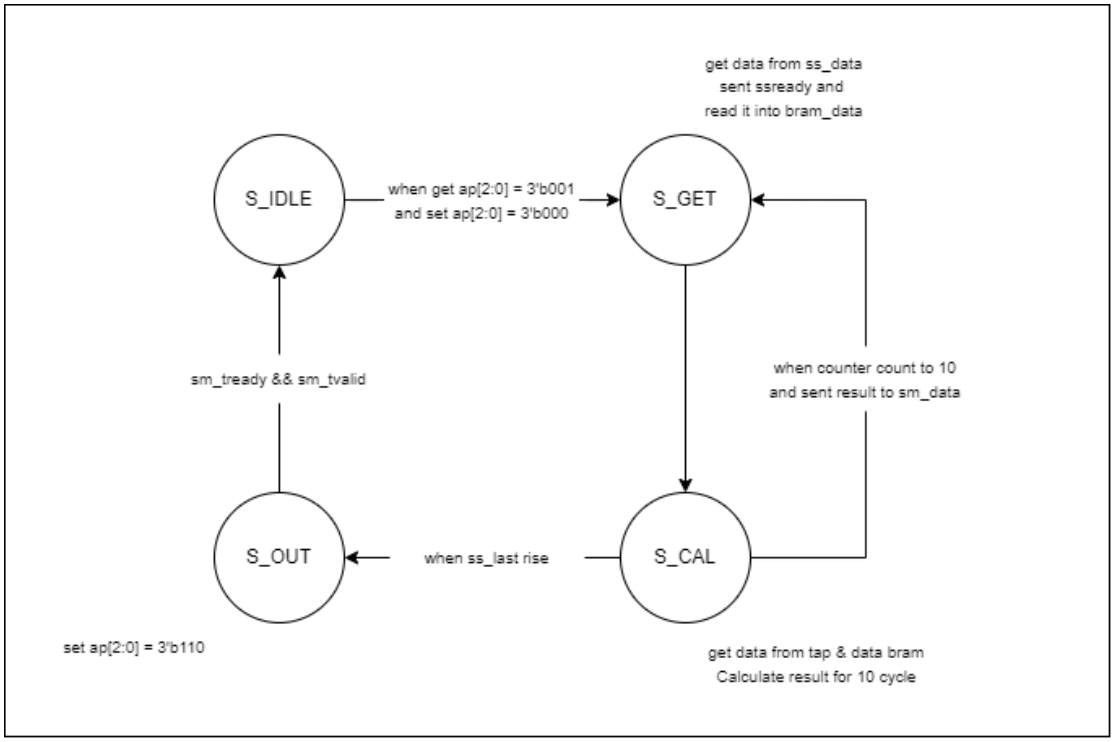
我將 Finite state machine 分成三部分，Fir、AXI-lite read、AXI-lite write，由於該 spec 的行為在同一時間中彼此控制不會重疊，因此這三個 FSM 彼此不用多做控制來避免重疊的事情發生。

- Fir FSM

  共有 4 個 state，S_IDLE 時，Fir 電路尚未啟動，當 ap_start 訊號起動，將 state 移至 S_GET。

  S_GET 用來將 x[i] data 從 AXI-stream read 傳進來，同時存入 bram_data，並同時將上次算好的 fir 結果給 AXI-stream write。

  S_CAL 用來計算 fir，利用 counter 計數 11 個 cycle 將 fir 用相乘累加的方式完成，完成後將 state 回到 S_GET 收下一筆 x[] data，而當 ss_last 升起時，代表沒資料可收了，state 移至 S_OUT。



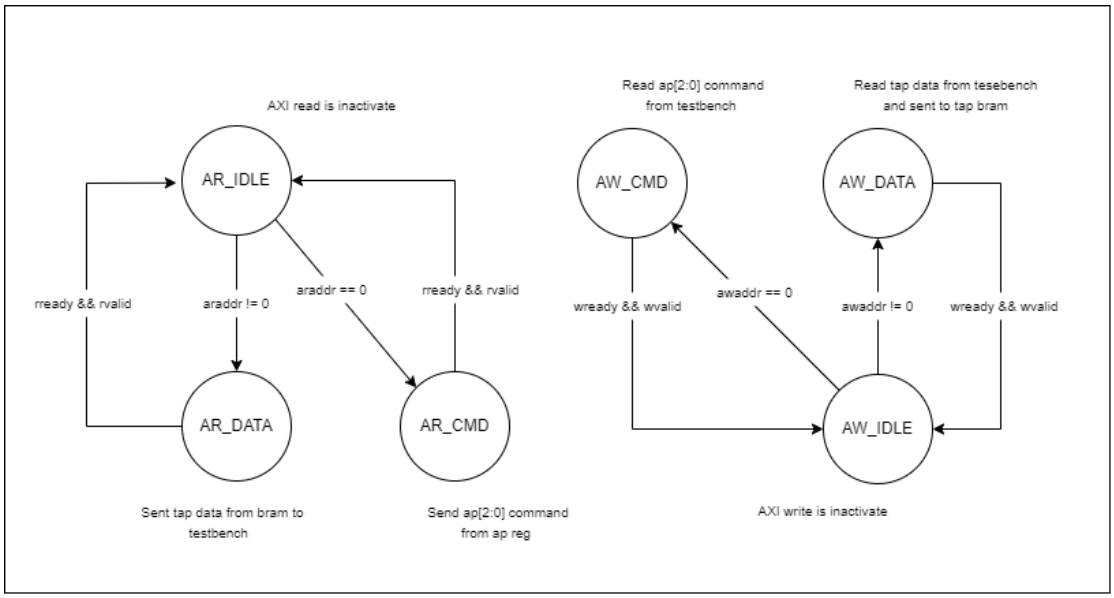
- AXI write & read FSM：

  這兩個的行為模式非常相近，但為了分出 write read，才產生兩個 FSM。

  AW_IDLE、AR_IDLE：為 AXI 未啟動的狀態。

  AW_DATA、AR_DATA：當 AXI 收到不是 0x00 的 address，也就是收 Tap parameter / data length，這個 state 用來區分 ap 指令與 tap parameter，以利控制線使用。

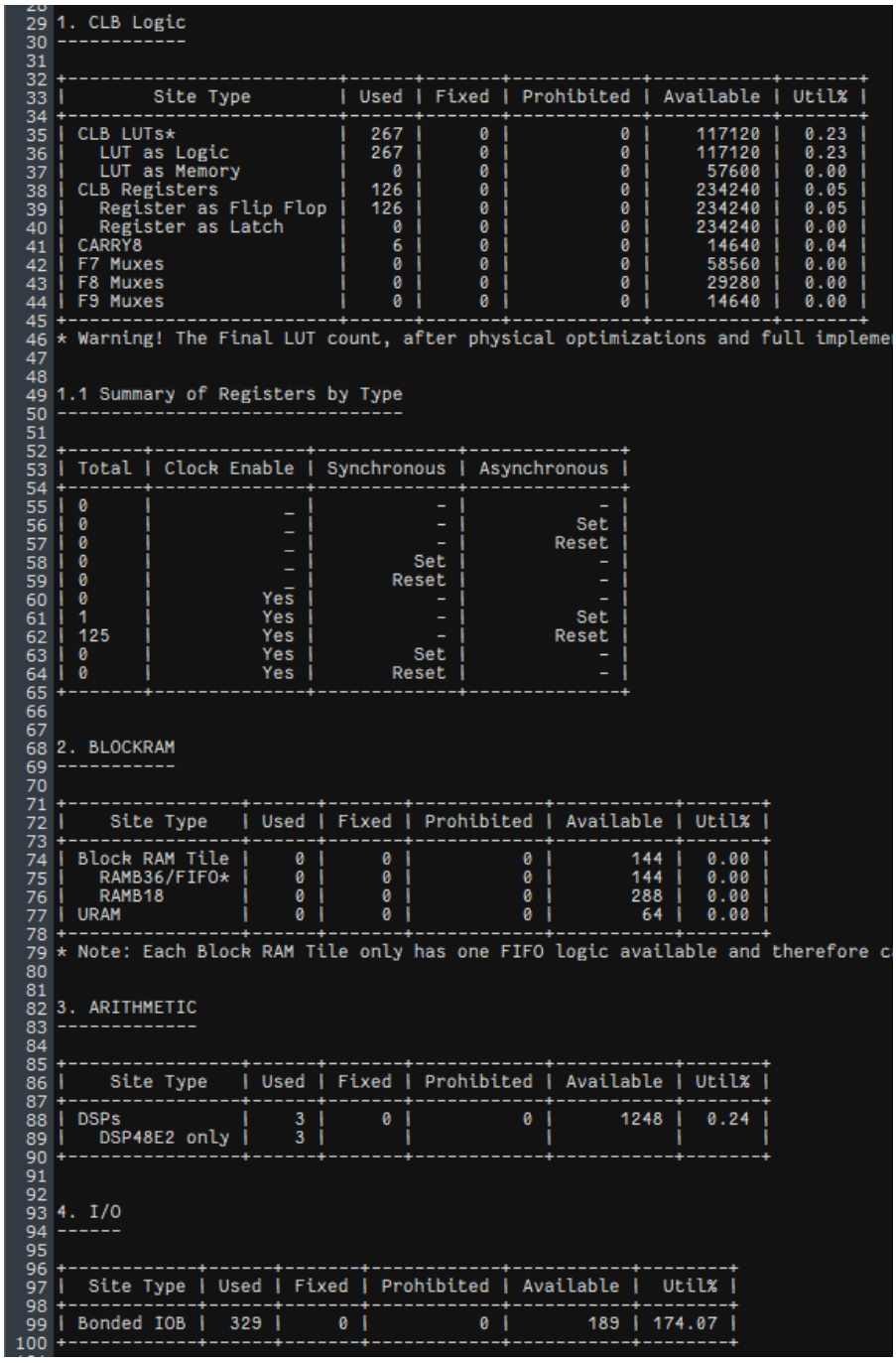
  AW_CMD、AR_CMD：AXI addr 為 0x00，AR_CMD 把 design 裡的 ap reg 傳回給 testbench，AW_CMD 則是讀 testbench 送過來的 ap 指令。



- Describe operation：
  - How to receive data-in and tap parameters and place into SRAM：
    我的想法是將Tap-parameter在SRAM的位置是固定的，再透過一些方法把X從SRAM中拿出相對應的資料，為此當tap parameter從AXI-lite write進來時，只需與SRAM對接，並address做offset就好了。
    而X[i] data則是用了First in First out的想法，用一個reg去記下最後一個data在SRAM中的位置，當新的X[i]資料來時將其複寫，此時下一個位置就會是新的最後一個位置，此時reg就更新，而這行為模式像是counter一樣。
  - How to access shiftram and tapRAM to do computation：
    那 SRAM 並沒有 shift 的功能，若我們利用 address 的方法模擬 shift 的作法則是非常耗時的，因為我們必須把每個 address 的資料讀出來在寫回去下一個位置(2*n cycle per shift | n 為 fir 中 coefficient 的長度)，，並且每次乘法都要執行此動作，花的 cycle 數是非常可觀的，為此我們改用控制 address 的方式得到我們要的結果。
    首先，SRAM data 會延後一個 cycle 才會把結果值 output 出去，因此最快完成一個 fir 點的 cycle 數為 n+1，此外我們還得用 AXI-stream 將新的 X[i] data 讀進來並存回去，使 SRAM access cycle 也剛好 n+ 1(n read and 1 write)。
    完整流程是：我先將 X[i]從 AXI 讀出，並寫入 SRAM，同時 tap SRAM 讀 T[10]的值，但要下個 cycle 才能得到 T[10]的值因此 X[i]的值要先存入暫存器中，下個 cycle 時，SRAM address 讀第二筆的 X 跟 Tap，同時做第一筆的乘加…以此類推，做到第 11 筆 data 為止。

- How ap_done is generated：
  當fir process完成、最後一筆資料送到tb後，ap_done拉起，而正是此時S_OUT state要轉到S_IDLE state，利用這條件我把design中ap reg的ap-done 與ap_idle flag拉起，並等到AXI read送第一次address = 0的read動作完成後，再將ap_done降下，而ap_idle仍然為0，直到AXI write更改ap_start時在歸零。

- Resource usage: including FF, LUT, BRAM



```
1. CLB Logic
------------

+-------------------------+------+-------+------------+-----------+-------+
|        Site Type        | Used | Fixed | Prohibited | Available | Util% |
+-------------------------+------+-------+------------+-----------+-------+
| CLB LUTs*               |  267 |     0 |          0 |    117120 |  0.23 |
|   LUT as Logic          |  267 |     0 |          0 |    117120 |  0.23 |
|   LUT as Memory         |    0 |     0 |          0 |     57600 |  0.00 |
| CLB Registers           |  126 |     0 |          0 |    234240 |  0.05 |
|   Register as Flip Flop |  126 |     0 |          0 |    234240 |  0.05 |
|   Register as Latch     |    0 |     0 |          0 |    234240 |  0.00 |
| CARRY8                  |    6 |     0 |          0 |     14640 |  0.04 |
| F7 Muxes                |    0 |     0 |          0 |     58560 |  0.00 |
| F8 Muxes                |    0 |     0 |          0 |     29280 |  0.00 |
| F9 Muxes                |    0 |     0 |          0 |     14640 |  0.00 |
+-------------------------+------+-------+------------+-----------+-------+
* Warning! The Final LUT count, after physical optimizations and full impleme

1.1 Summary of Registers by Type
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+-------+--------------+-------------+--------------+
| Total | Clock Enable | Synchronous | Asynchronous |
+-------+--------------+-------------+--------------+
| 0     |            _ |           - |            - |
| 0     |            _ |           - |          Set |
| 0     |            _ |           - |        Reset |
| 0     |            _ |         Set |            - |
| 0     |            _ |       Reset |            - |
| 0     |          Yes |           - |            - |
| 1     |          Yes |           - |          Set |
| 125   |          Yes |           - |        Reset |
| 0     |          Yes |         Set |            - |
| 0     |          Yes |       Reset |            - |
+-------+--------------+-------------+--------------+


2. BLOCKRAM
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+----------------+------+-------+------------+-----------+-------+
|    Site Type   | Used | Fixed | Prohibited | Available | Util% |
+----------------+------+-------+------------+-----------+-------+
| Block RAM Tile |    0 |     0 |          0 |       144 |  0.00 |
|   RAMB36/FIFO* |    0 |     0 |          0 |       144 |  0.00 |
|   RAMB18       |    0 |     0 |          0 |       288 |  0.00 |
| URAM           |    0 |     0 |          0 |        64 |  0.00 |
+----------------+------+-------+------------+-----------+-------+
* Note: Each Block RAM Tile only has one FIFO logic available and therefore c


3. ARITHMETIC
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+----------------+------+-------+------------+-----------+-------+
|    Site Type   | Used | Fixed | Prohibited | Available | Util% |
+----------------+------+-------+------------+-----------+-------+
| DSPs           |    3 |     0 |          0 |      1248 |  0.24 |
|   DSP48E2 only |    3 |       |            |           |       |
+----------------+------+-------+------------+-----------+-------+


4. I/O
------

+------------+------+-------+------------+-----------+--------+
|  Site Type | Used | Fixed | Prohibited | Available |  Util% |
+------------+------+-------+------------+-----------+--------+
| Bonded IOB |  329 |     0 |          0 |       189 | 174.07 |
+------------+------+-------+------------+-----------+--------+
```

```
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:09 ; elapsed = 00:00:10 .
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start RTL Component Statistics
---------------------------------------------------------------------------------
Detailed RTL Component Info :
+---Adders :
           2 Input   32 Bit       Adders := 1
           2 Input   12 Bit       Adders := 1
           3 Input    5 Bit       Adders := 2
           2 Input    4 Bit       Adders := 4
+---Registers :
                     32 Bit    Registers := 3
                      7 Bit    Registers := 1
                      4 Bit    Registers := 3
                      3 Bit    Registers := 2
                      1 Bit    Registers := 2
+---Multipliers :
                    32x32  Multipliers := 1
+---Muxes :
           4 Input   32 Bit        Muxes := 1
           2 Input   32 Bit        Muxes := 8
           2 Input   12 Bit        Muxes := 2
           4 Input   12 Bit        Muxes := 1
           2 Input    7 Bit        Muxes := 3
           3 Input    7 Bit        Muxes := 1
           2 Input    5 Bit        Muxes := 1
           2 Input    4 Bit        Muxes := 5
           3 Input    4 Bit        Muxes := 1
           4 Input    3 Bit        Muxes := 1
           3 Input    2 Bit        Muxes := 2
           4 Input    2 Bit        Muxes := 3
           2 Input    2 Bit        Muxes := 6
           2 Input    1 Bit        Muxes := 19
           3 Input    1 Bit        Muxes := 3
---------------------------------------------------------------------------------
Finished RTL Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Part Resource Summary
---------------------------------------------------------------------------------
Part Resources:
DSPs: 1248 (col length:96)
BRAMs: 288 (col length: RAMB18 96 RAMB36 48)
---------------------------------------------------------------------------------
Finished Part Resource Summary
---------------------------------------------------------------------------------
```

- Timing Report：

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.529 ns	Worst Hold Slack (WHS):	0.002 ns	Worst Pulse Width Slack (WPWS):	2.725 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	179	Total Number of Endpoints:	179	Total Number of Endpoints:	127

All user specified timing constraints are met.

本次實驗可合成的最小 cycle time 為 6ns

■ Setup longest timing path –0.512ns (require – arrival time) ：

```
Max Delay Paths
--------------------------------------------------------------------------------------
Slack (MET) :             0.529ns  (required time - arrival time)
  Source:                 coe_cnt_reg[1]/C
                            (rising edge-triggered cell FDCE clocked by axis_clk  {rise@0.000ns fall@3.000ns period=6.000ns})
  Destination:            acc_reg_reg[31]/D
                            (rising edge-triggered cell FDCE clocked by axis_clk  {rise@0.000ns fall@3.000ns period=6.000ns})
  Path Group:             axis_clk
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            6.000ns  (axis_clk rise@6.000ns - axis_clk rise@0.000ns)
  Data Path Delay:        5.335ns  (logic 4.135ns (77.507%)  route 1.200ns (22.493%))
  Logic Levels:           15  (CARRY8=3 DSP_A_B_DATA=1 DSP_ALU=2 DSP_M_DATA=1 DSP_MULTIPLIER=1 DSP_OUTPUT=2 DSP_PREADD_DATA=1 LUT2=2 LUT3=1 LUT6=1)
  Clock Path Skew:        -0.145ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    3.202ns = ( 9.202 - 6.000 )
    Source Clock Delay      (SCD):    3.910ns
    Clock Pessimism Removal (CPR):    0.562ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns
```

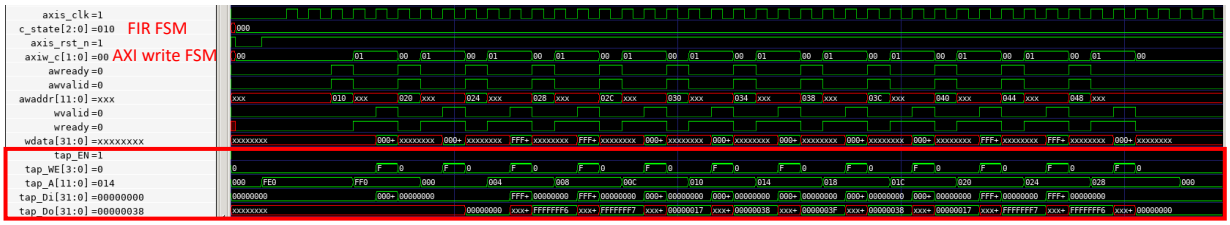
```
    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock axis_clk rise edge)
                                                    0.000     0.000 r
                                                    0.000     0.000 r  axis_clk (IN)
                         net (fo=0)                 0.000     0.000    axis_clk_IBUF_inst/I
                                                                   r  axis_clk_IBUF_inst/INBUF_INST/PAD
                         INBUF (Prop_INBUF_PAD_O)   1.026     1.026 r  axis_clk_IBUF_inst/INBUF_INST/O
                         net (fo=1, unplaced)       0.000     1.026    axis_clk_IBUF_inst/OUT
                                                                   r  axis_clk_IBUF_inst/IBUFCTRL_INST/I
                         IBUFCTRL (Prop_IBUFCTRL_I_O)
                                                    0.000     1.026 r  axis_clk_IBUF_inst/IBUFCTRL_INST/O
                         net (fo=1, unplaced)       0.256     1.282    axis_clk_IBUF
                                                                   r  axis_clk_IBUF_BUFG_inst/I
                         BUFGCE (Prop_BUFGCE_I_O)   0.044     1.326 r  axis_clk_IBUF_BUFG_inst/O
                         net (fo=126, unplaced)     2.584     3.910    axis_clk_IBUF_BUFG
                         FDCE                                       r  coe_cnt_reg[1]/C
  -------------------------------------------------------------------    -------------------
                         FDCE (Prop_FDCE_C_Q)       0.114     4.024 r  coe_cnt_reg[1]/Q
                         net (fo=79, unplaced)      0.194     4.218    coe_cnt[1]
                                                                   r  mul_result_i_1/I1
                         LUT6 (Prop_LUT6_I1_O)      0.188     4.406 f  mul_result_i_1/O
                         net (fo=2, unplaced)       0.252     4.658    mul_result__0/B[16]
                                                                   f  mul_result__0/DSP_A_B_DATA_INST/B[16]
                         DSP_A_B_DATA (Prop_DSP_A_B_DATA_B[16]_B2_DATA[16])
                                                    0.216     4.874 r  mul_result__0/DSP_A_B_DATA_INST/B2_DATA[16]
                         net (fo=1, unplaced)       0.000     4.874    mul_result__0/DSP_A_B_DATA.B2_DATA<16>
                                                                   r  mul_result__0/DSP_PREADD_DATA_INST/B2_DATA[16]
                         DSP_PREADD_DATA (Prop_DSP_PREADD_DATA_B2_DATA[16]_B2B1[16])
                                                    0.097     4.971 r  mul_result__0/DSP_PREADD_DATA_INST/B2B1[16]
                         net (fo=1, unplaced)       0.000     4.971    mul_result__0/DSP_PREADD_DATA.B2B1<16>
                                                                   r  mul_result__0/DSP_MULTIPLIER_INST/B2B1[16]
                         DSP_MULTIPLIER (Prop_DSP_MULTIPLIER_B2B1[16]_U[43])
                                                    0.773     5.744 f  mul_result__0/DSP_MULTIPLIER_INST/U[43]
                         net (fo=1, unplaced)       0.000     5.744    mul_result__0/DSP_MULTIPLIER.U<43>
                                                                   f  mul_result__0/DSP_M_DATA_INST/U[43]
                         DSP_M_DATA (Prop_DSP_M_DATA_U[43]_U_DATA[43])
                                                    0.067     5.811 r  mul_result__0/DSP_M_DATA_INST/U_DATA[43]
                         net (fo=1, unplaced)       0.000     5.811    mul_result__0/DSP_M_DATA.U_DATA<43>
                                                                   r  mul_result__0/DSP_ALU_INST/U_DATA[43]
                         DSP_ALU (Prop_DSP_ALU_U_DATA[43]_ALU_OUT[47])
                                                    0.727     6.538 f  mul_result__0/DSP_ALU_INST/ALU_OUT[47]
                         net (fo=1, unplaced)       0.000     6.538    mul_result__0/DSP_ALU.ALU_OUT<47>
                                                                   f  mul_result__0/DSP_OUTPUT_INST/ALU_OUT[47]
                         DSP_OUTPUT (Prop_DSP_OUTPUT_ALU_OUT[47]_PCOUT[47])
                                                    0.167     6.705 r  mul_result__0/DSP_OUTPUT_INST/PCOUT[47]
                         net (fo=1, unplaced)       0.014     6.719    mul_result__1/PCIN[47]
                                                                   r  mul_result__1/DSP_ALU_INST/PCIN[47]
                         DSP_ALU (Prop_DSP_ALU_PCIN[47]_ALU_OUT[0])
                                                    0.739     7.458 f  mul_result__1/DSP_ALU_INST/ALU_OUT[0]
                         net (fo=1, unplaced)       0.000     7.458    mul_result__1/DSP_ALU.ALU_OUT<0>
                                                                   f  mul_result__1/DSP_OUTPUT_INST/ALU_OUT[0]
                         DSP_OUTPUT (Prop_DSP_OUTPUT_ALU_OUT[0]_P[0])
                                                    0.146     7.604 r  mul_result__1/DSP_OUTPUT_INST/P[0]
                         net (fo=2, unplaced)       0.258     7.862    mul_result__1_n_105
                                                                   r  acc_reg[23]_i_18/I0
                         LUT2 (Prop_LUT2_I0_O)      0.083     7.945 r  acc_reg[23]_i_18/O
                         net (fo=1, unplaced)       0.021     7.966    acc_reg[23]_i_18_n_0
                                                                   r  acc_reg_reg[23]_i_11/S[1]
                         CARRY8 (Prop_CARRY8_S[1]_CO[7])
                                                    0.269     8.235 r  acc_reg_reg[23]_i_11/CO[7]
                         net (fo=1, unplaced)       0.006     8.241    acc_reg_reg[23]_i_11_n_0
                                                                   r  acc_reg_reg[31]_i_14/CI
                         CARRY8 (Prop_CARRY8_CI_O[1])
                                                    0.106     8.347 r  acc_reg_reg[31]_i_14/O[1]
                         net (fo=1, unplaced)       0.216     8.563    mul_result__3[25]
                                                                   r  acc_reg[31]_i_12/I1
                         LUT2 (Prop_LUT2_I1_O)      0.058     8.621 r  acc_reg[31]_i_12/O
                         net (fo=1, unplaced)       0.021     8.642    acc_reg[31]_i_12_n_0
                                                                   r  acc_reg_reg[31]_i_5/S[1]
                         CARRY8 (Prop_CARRY8_S[1]_O[7])
                                                    0.327     8.969 r  acc_reg_reg[31]_i_5/O[7]
                         net (fo=1, unplaced)       0.151     9.120    acc_reg0[31]
                                                                   r  acc_reg[31]_i_2/I0
                         LUT3 (Prop_LUT3_I0_O)      0.058     9.178 r  acc_reg[31]_i_2/O
                         net (fo=1, unplaced)       0.067     9.245    p_1_in[31]
                         FDCE                                       r  acc_reg_reg[31]/D
  -------------------------------------------------------------------    -------------------
```

```
  -------------------------------------------------------------------    -------------------

                        (clock axis_clk rise edge)
                                                     6.000     6.000 r
                                                     0.000     6.000 r  axis_clk (IN)
                        net (fo=0)                   0.000     6.000    axis_clk_IBUF_inst/I
                                                                    r  axis_clk_IBUF_inst/INBUF_INST/PAD
                        INBUF (Prop_INBUF_PAD_O)     0.518     6.518 r  axis_clk_IBUF_inst/INBUF_INST/O
                        net (fo=1, unplaced)         0.000     6.518    axis_clk_IBUF_inst/OUT
                                                                    r  axis_clk_IBUF_inst/IBUFCTRL_INST/I
                        IBUFCTRL (Prop_IBUFCTRL_I_O)
                                                     0.000     6.518 r  axis_clk_IBUF_inst/IBUFCTRL_INST/O
                        net (fo=1, unplaced)         0.206     6.724    axis_clk_IBUF
                                                                    r  axis_clk_IBUF_BUFG_inst/I
                        BUFGCE (Prop_BUFGCE_I_O)     0.039     6.763 r  axis_clk_IBUF_BUFG_inst/O
                        net (fo=126, unplaced)       2.439     9.202    axis_clk_IBUF_BUFG
                        FDCE                                        r  acc_reg_reg[31]/C
                        clock pessimism              0.562     9.765
                        clock uncertainty           -0.035     9.729
                        FDCE (Setup_FDCE_C_D)        0.044     9.773    acc_reg_reg[31]
  -------------------------------------------------------------------
                        required time                          9.773
                        arrival time                          -9.245
  -------------------------------------------------------------------
                        slack                                  0.529
```

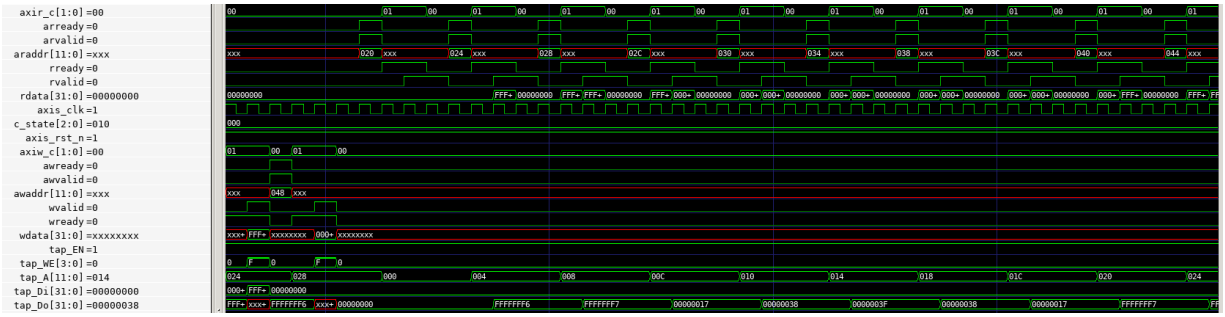
- Hold min timing path：

```
Min Delay Paths
--------------------------------------------------------------------------------------
Slack (MET) :             0.002ns  (arrival time - required time)
  Source:                 cnt_reg[2]/C
                            (rising edge-triggered cell FDCE clocked by axis_clk  {rise@0.000ns fall@3.000ns period=6.000ns})
  Destination:            cnt_reg[3]/D
                            (rising edge-triggered cell FDCE clocked by axis_clk  {rise@0.000ns fall@3.000ns period=6.000ns})
  Path Group:             axis_clk
  Path Type:              Hold (Min at Fast Process Corner)
  Requirement:            0.000ns  (axis_clk rise@0.000ns - axis_clk rise@0.000ns)
  Data Path Delay:        0.191ns  (logic 0.120ns (62.827%)  route 0.071ns (37.173%))
  Logic Levels:           1  (LUT5=1)
  Clock Path Skew:        0.145ns (DCD - SCD - CPR)
    Destination Clock Delay (DCD):    2.124ns
    Source Clock Delay      (SCD):    1.684ns
    Clock Pessimism Removal (CPR):    0.294ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock axis_clk rise edge)
                                                      0.000     0.000 r
                                                      0.000     0.000 r  axis_clk (IN)
                         net (fo=0)                   0.000     0.000    axis_clk_IBUF_inst/I
                                                                     r  axis_clk_IBUF_inst/INBUF_INST/PAD
                         INBUF (Prop_INBUF_PAD_O)     0.449     0.449 r  axis_clk_IBUF_inst/INBUF_INST/O
                         net (fo=1, unplaced)         0.000     0.449    axis_clk_IBUF_inst/OUT
                                                                     r  axis_clk_IBUF_inst/IBUFCTRL_INST/I
                         IBUFCTRL (Prop_IBUFCTRL_I_O)
                                                      0.000     0.449 r  axis_clk_IBUF_inst/IBUFCTRL_INST/O
                         net (fo=1, unplaced)         0.098     0.547    axis_clk_IBUF
                                                                     r  axis_clk_IBUF_BUFG_inst/I
                         BUFGCE (Prop_BUFGCE_I_O)     0.023     0.570 r  axis_clk_IBUF_BUFG_inst/O
                         net (fo=126, unplaced)       1.114     1.684    axis_clk_IBUF_BUFG
                         FDCE                                        r  cnt_reg[2]/C
  -------------------------------------------------------------------    -------------------
                         FDCE (Prop_FDCE_C_Q)         0.084     1.768 r  cnt_reg[2]/Q
                         net (fo=6, unplaced)         0.053     1.821    cnt[2]
                                                                     r  cnt[3]_i_2/I3
                         LUT5 (Prop_LUT5_I3_O)        0.036     1.857 r  cnt[3]_i_2/O
                         net (fo=1, unplaced)         0.018     1.875    cnt[3]_i_2_n_0
                         FDCE                                        r  cnt_reg[3]/D
  -------------------------------------------------------------------    -------------------

                         (clock axis_clk rise edge)
                                                      0.000     0.000 r
                                                      0.000     0.000 r  axis_clk (IN)
                         net (fo=0)                   0.000     0.000    axis_clk_IBUF_inst/I
                                                                     r  axis_clk_IBUF_inst/INBUF_INST/PAD
                         INBUF (Prop_INBUF_PAD_O)     0.721     0.721 r  axis_clk_IBUF_inst/INBUF_INST/O
                         net (fo=1, unplaced)         0.000     0.721    axis_clk_IBUF_inst/OUT
                                                                     r  axis_clk_IBUF_inst/IBUFCTRL_INST/I
                         IBUFCTRL (Prop_IBUFCTRL_I_O)
                                                      0.000     0.721 r  axis_clk_IBUF_inst/IBUFCTRL_INST/O
                         net (fo=1, unplaced)         0.118     0.839    axis_clk_IBUF
                                                                     r  axis_clk_IBUF_BUFG_inst/I
                         BUFGCE (Prop_BUFGCE_I_O)     0.026     0.865 r  axis_clk_IBUF_BUFG_inst/O
                         net (fo=126, unplaced)       1.259     2.124    axis_clk_IBUF_BUFG
                         FDCE                                        r  cnt_reg[3]/C
                         clock pessimism             -0.294     1.829
                         FDCE (Hold_FDCE_C_D)         0.044     1.873    cnt_reg[3]
  -------------------------------------------------------------------
                         required time                         -1.873
                         arrival time                           1.875
  -------------------------------------------------------------------
                         slack                                  0.002
```

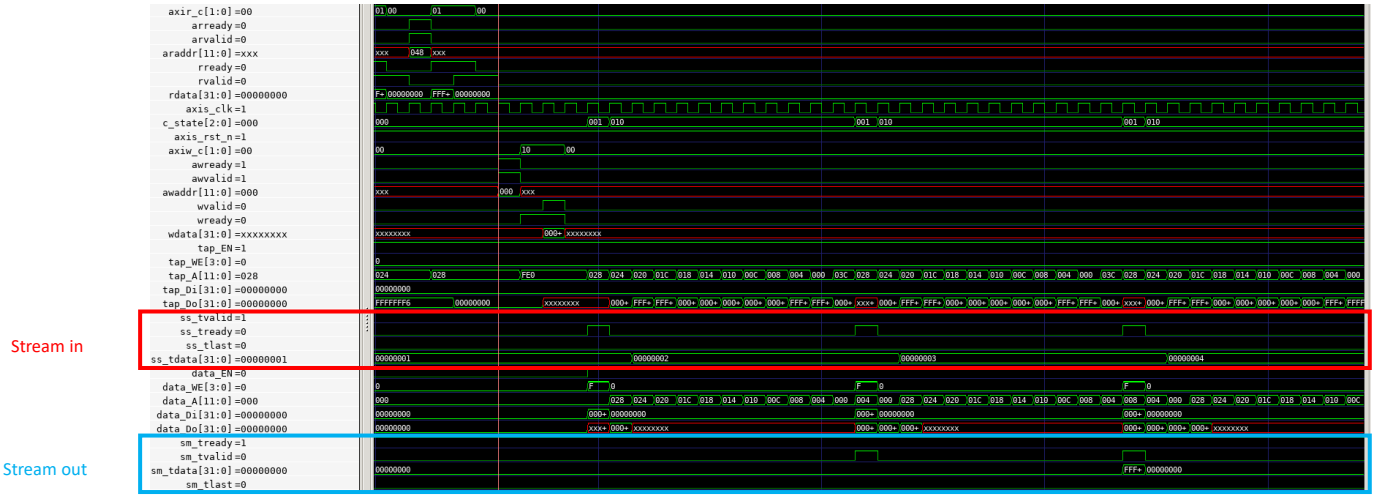
- Simulation Waveform：
  - Coefficient in，並將它存進 tap bram



  - Coefficient out，以及 tap bram 的訊號圖



  - ap_start sent into design，Start fir process



  - fir process complete、 next pattern comming