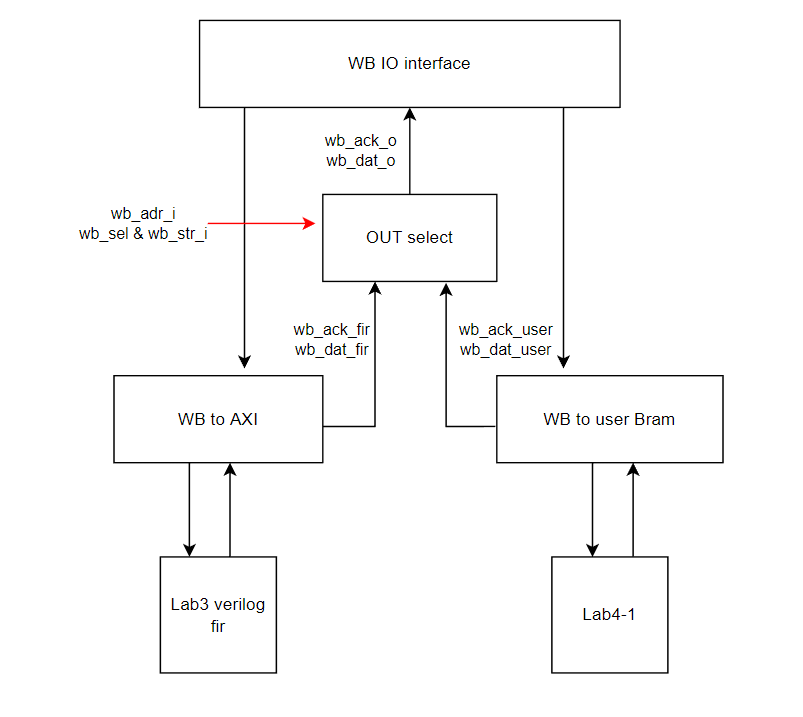
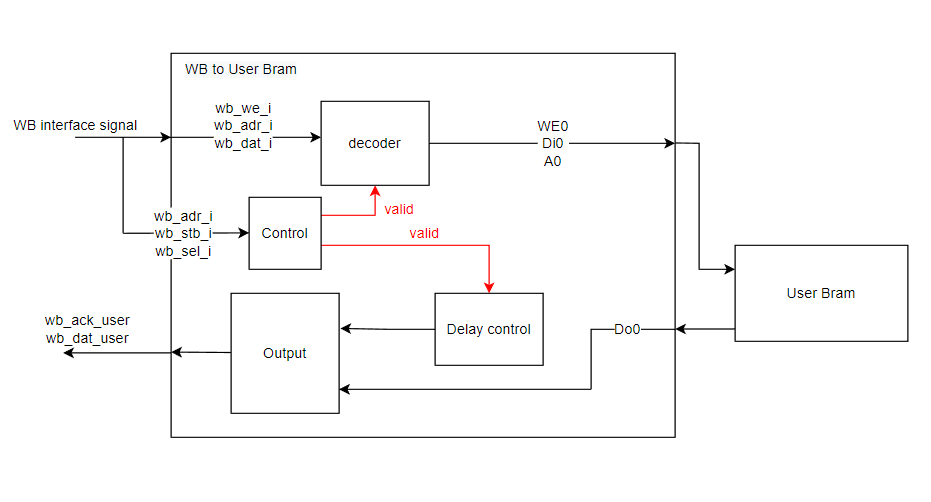
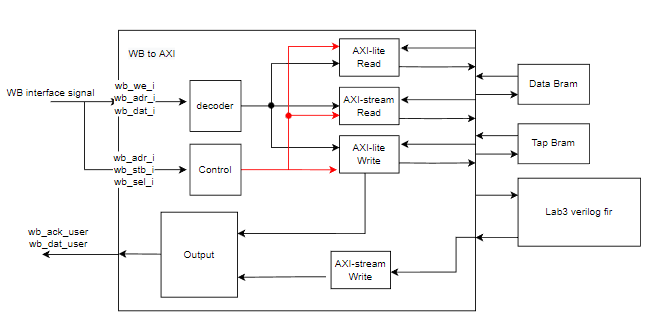
SOC Design Lab4-2 312510150 曹宗叡

* Design block diagram:datapath , control path：

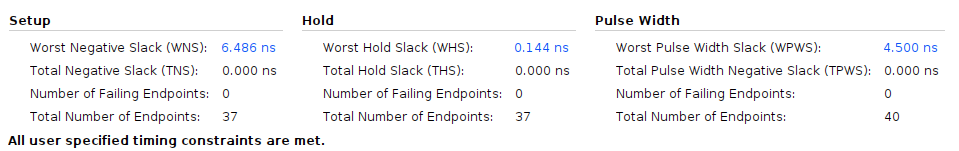




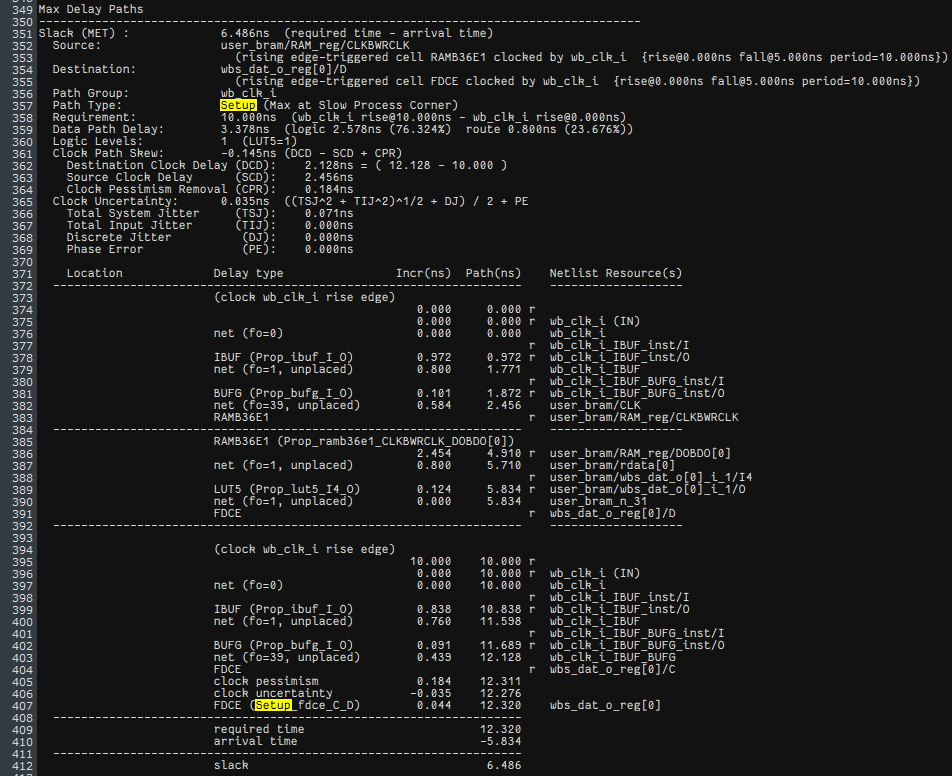


* The interface protocol between firmware, user project and testbench：
* Waveform and analysis of the hardware/software behavior.
* What is the FIR engine theoretical throughput, i.e. data rate? Actually measured throughput?
* What is latency for firmware to feed data?
* What techniques used to improve the throughput?
* Does bram12 give better performance, in what way?
* Can you suggest other method to improve the performance?
* Timing Report：

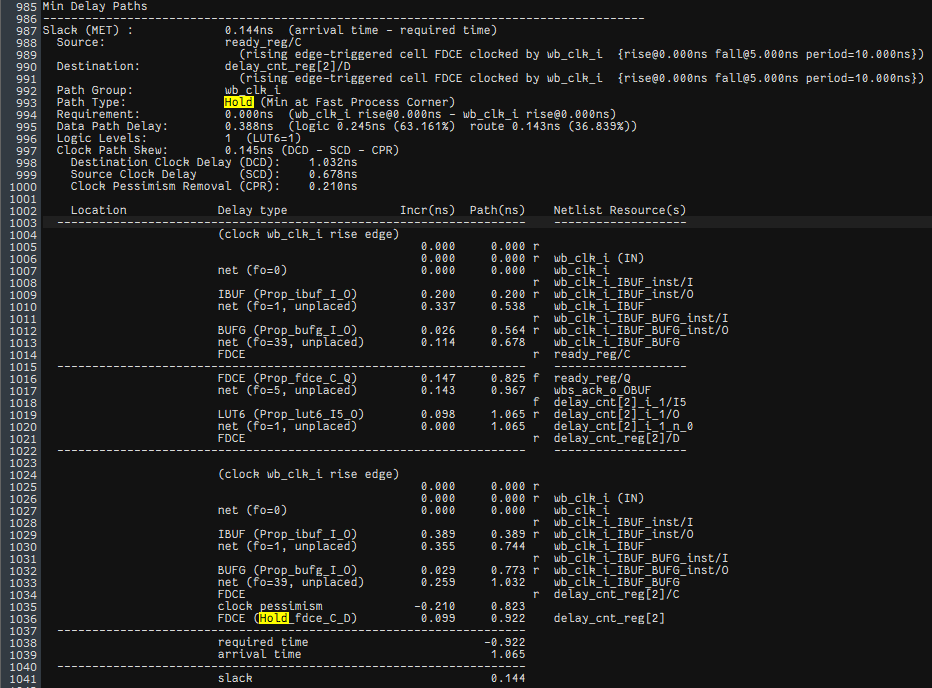
本次實驗合成clock time為10ns



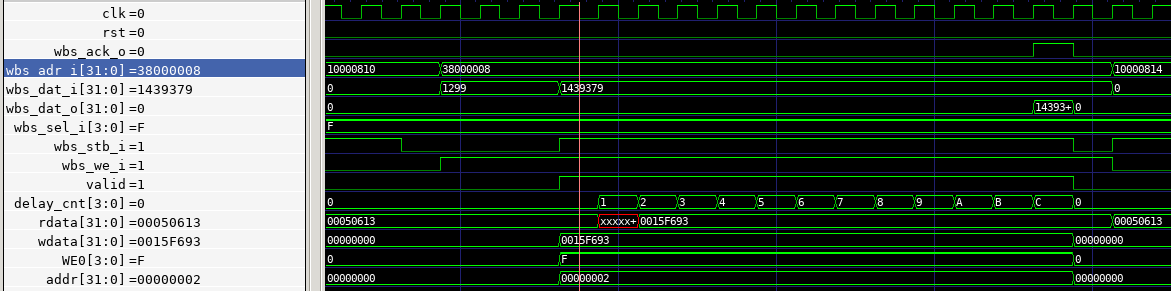
* + Setup longest timing path –6.486ns (require – arrival time) ：



* + Hold min timing path：



* Simulation Waveform：
  + Interface between BRAM and wishbone：

當stb\_i與sel\_i都為high時，才會開啟Bram與WB的通道，並由we\_i=1去決定是要寫入值到Bram，或是(=0)讀取Bram，那他會藉由WE0 signal傳至Bram，而Bram的addr則是將offset 0x38000000去掉，並右移2位，以word line形式儲存，並延遲DELAYS+2的cycle後再輸出wb\_ack\_0以模擬memory的低速下的workload。

* + FSM：

當stb\_i與sel\_i都為high，並且wb\_adr\_i是0x38開頭的Address，valid才會為一，並啟動delay\_cnt計數，直到計數至DELAYS+2後才將wb\_ack\_0拉為high已表示完成整個BRAM and wishbone的資料交換。