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CST331
Lab 5 – Basic I/O using EBI

1. Circuit diagram printout attached.

2. RTL net view printout attached.

3. FPGA design file printouts and Timequest data printouts attached.

4.

Formulas for write:

- tSU prv. min = tEBI-WP min – tEBIDO + tEBICO >= tSUext min (0ns)
- tH prv. min = tEBI-WR min + tEBIDO – tEBICO >= tHext min (3.4ns)

Formulas for read:

- tZX min = max of (min CS and min OE)
- tDV max = max of (max CS and max OE)
- tDV min = min of (min CS and min OE)
- tXZ max = min of (max CS and max OE)
- tSU prv. min = tEBI-RC min - tEBICO max – tDVmax >= tEBIDS min (5ns)
- tH prv. min = tEBICO min + tDV min >= tEBIDH min (3ns)

Part 6 write:

- tSU prv. min = 10ns – 5ns + 5ns >= 0ns, true
- tH prv. min = 10ns + 5ns – 5ns >= 3.4ns, true

Part 6 read:

- tSU prv. min = 20ns – 5ns – 23.97ns >= 5ns, false so RC must be >=2
- tH prv. min = 0ns + 5.173ns >= 3ns, true

Part 10 write:

- tSU prv. min = 10ns – 5ns + 5ns >= 0ns, true
- tH prv. min = 10ns + 5ns – 5ns >= 3.4ns, true

Part 10 read:

- tSU prv. min = 20ns – 5ns – 17.97ns >= 5ns, false so RC must be >=2
- tH prv. min = 0ns + 6.95ns >= 3ns, true

No changes required since tDV max only changed by around 6ns.

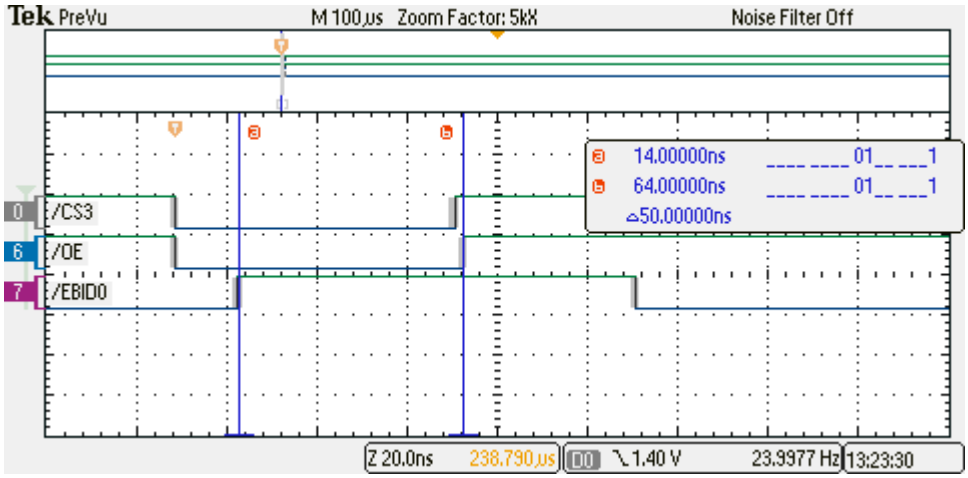
5. Construction and test steps:

- Decided which address bits to add to the Sidewinder by decoding the address range and looking for the bits that don't change.
- Simulated FPGA design in ModelSim with testbench.
- Wire wrapped and tested continuity.
- Timing analysis with Timing Analyzer in Quartus.
- Tested data pins with digital and analog signals on MSO, no contention observed. Initial C program testing went successfully.
- Wire wrapped data lines.
- Finished C program testing.
- Added invert functionality to Verilog files.

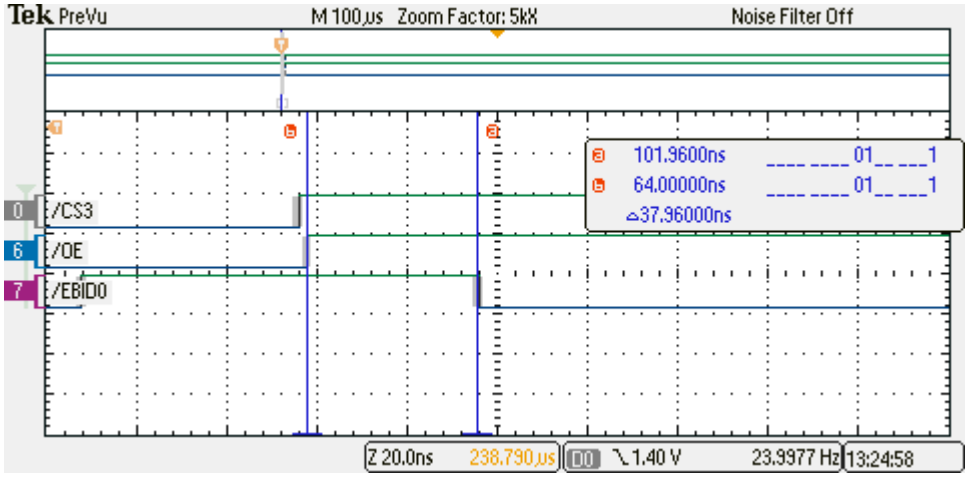
6. Commented code printout attached.

7. To measure setup, the data bus had to be sensitized and the parameter was read from the rising edge of OE or WE. Setup and hold is difficult to measure because we can't see the clock signal.

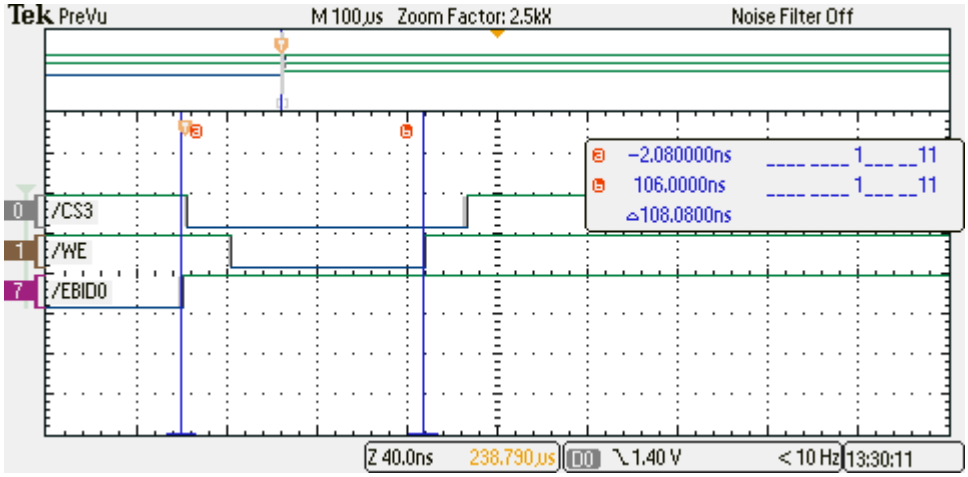
Provided setup during read: 50ns, the requirement is met because it is >5ns.



Provided hold during read: 37.96ns, the requirement is met because it is >3ns.



Provided setup during write: 108.08ns, the requirement is met because it is >0ns.



Provided hold during write: 16.08ns, the requirement is met because it is >3.4ns.