Figure 6:
TSSOP14 Pin Description for AS5048B

Pin	AS5048B	Type	Description
1	SDA	Digital I/O with open drain output	Data pin I^2C interface
2	SCL	Digital input with schmitt trigger	I^2C clock input
3	A2		I^2C address selection pin 3
4	A1		I^2C address selection pin 4
5	TEST	Analog I/O	Test pins. These pins should be grounded to GND.
6	TEST		
7	TEST		
8	TEST		
9	TEST		
10	TEST		
11	VDD5V	Supply pad	Positive Supply Voltage, 3.0 to 5.5 V
12	VDD3V		3.3V Regulator output; internally regulated from VDD. Connect to VDD for 3V supply voltage. 10µF capacitor to GND required in 5V operation mode
13	GND		Negative Supply Voltage (GND)
14	PWM	Digital output – push-pull	Pulse Width Modulation output