An Analysis of a CMOS Imager

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***Abstract*— A properly functioning 0.061-megapixel camera requires an active pixel sensor array with the ability to sequentially and reliably read voltages set by each sensor. Individual subcomponents, their connections, properties of photodiodes, and CMOS logic all play a role in successfully creating the circuitry for a CMOS Imager.**

***Keywords*— Cadence, Very Large Scale Integration (VLSI), Design Rules Check (DRC), Layout-Versus-Schematic (LVS), C2MOS, Transistor, Active Pixel Sensor (APS), Shift Register**

I. INTRODUCTION

The earliest cameras were very large, some the size of living rooms. Through innovation, cameras were able to decrease in many magnitudes of size notably with the miniaturization of semiconductors. The goal of this project was to create a grid of active pixel sensors to fit within a 2.5mm by 2.5mm rectangle, with the idea of eventually reading and sending off that data to a visual display.

In order to convert captured light to a current, we used photodiodes, which allow variable currents to be captured depending on light/photon intensity due to their reverse biasing property. To represent light intensities for the red, blue, and green spectra, we require three layers of active pixel sensor grids with each layer only accepting light after its respective color filter has been applied. In this way, representing each pixel's red, green, and blue intensity values becomes systematic, by simply sending over three voltages per pixel.

However, in order to address passive pixel sensor issues such as speed, scalability, power consumption, sensitivity, and cost, we created and used active pixel sensors (APS) to convert accumulated photons into current. Active pixel sensors are a crucial part of modern-day documentation and, when combined with a way to capture their data (as will be briefly touched on in the remainder of this introduction and more thoroughly explained in Section IV), they become the foundations of image capture.

For this project, we focus on the circuitry for only one layer of this active pixel grid. The most important aspect of this grid is being able to read out the voltage values and send them coherently to an output. This is done by creating shift registers, C2MOS connected in series, to sequentially loop through each column (left to right) of each row (top to bottom).

Through this project, we began by initially creating and testing an APS, C2MOS Latch, and shift registers individually, which are the main subsystems required. Once the behavior of each system was verified, we combined these subsystems into an imager, which was scaled up to the desired size of a 2.5mm by 2.5mm chip.

The software we used to implement this is Cadence Virtuoso. The sizing standard we decided upon was 0.18µm process size for the implementation of our imager to achieve the required goal size of 2.5mm by 2.5mm. To successfully design at this process size, we used transistor sizes of 720nm x 720nm, except for switching transistors of size 720nm x 180nm. Additionally, we used Cadence's built-in design functionality to verify our schematics and layouts such as Design Rules Check (DRC), Extracted, and Layout-Versus-Schematic (LVS).

II. SHIFT REGISTERS

A. C2MOS Latch

The C2MOS is a set of two inverters wired in series. This design is functionally a D-Latch made of eight transistors, four NMOS, and four PMOS. An initial schematic was made to create this transistor setup, with a corresponding symbol. The design once tested through a testing

schematic was then reconfigured to allow for cascading. Since these C2MOS would be used to create shift registers in the final schematic in Fig. 1. they were required to be created in a way that allowed their eventual 10-micron by 10-micron areas to flow into one another. Once designed using the schematic, a physical layout within the required parameters was created. This layout also featured the same requirements of allowing for vertical cascading of C2MOS shown in Fig. 1. Additionally, it was designed until both DRC and LVS were passed to confirm the functionality of the layout based on the tested schematic.

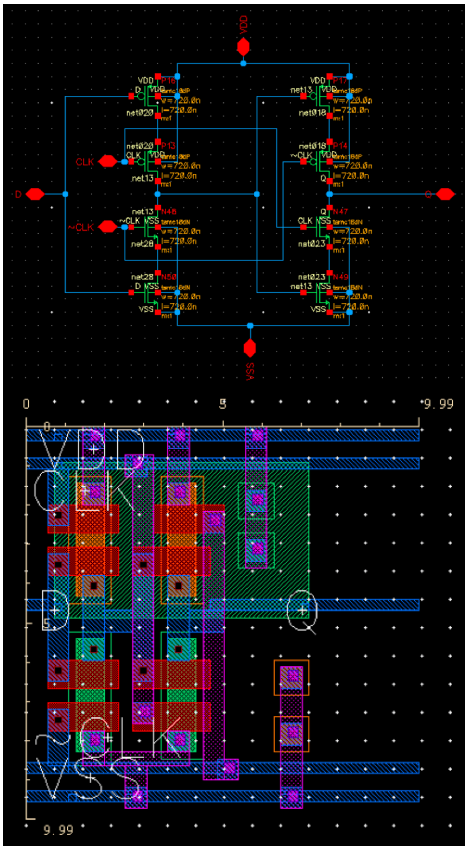

Fig. 1. C2MOS Schematic & Layout.

B. Shift Register

Shift registers are required in multiple parts of a CMOS Imager to correctly identify and send signals to each individual pixel. As described above each C2MOS is designed to be cascaded into each other. This allows the output of one C2MOS to be sent into the next C2MOS in the register, creating a cascading effect of signals that can be seen from each of the corresponding outputs. This is very useful in sending a signal to be carried out in an identical manner across a set of objects.

III. APS

A. Photodiode Design

To design the active APS it requires three NMOS transistors. A photodiode current is tied to the source of a row reset transistor and the gate of the second transistor, additionally, there is a third transistor for selection, shown below in Fig. 2.

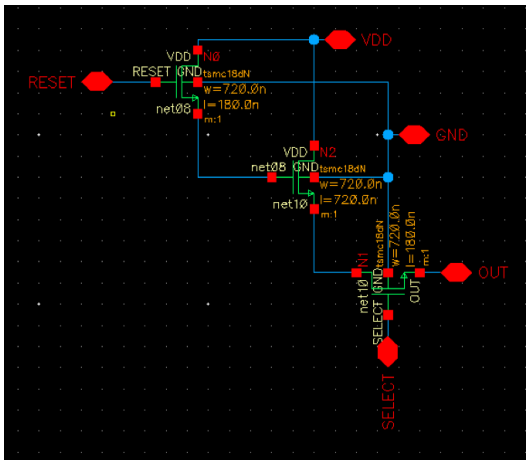

Fig. 2. APS Schematic.

B. Current Mirror

Due to Cadence having no photodiode instance included in its component libraries, a current mirror circuit is needed in its place to bias the current for testing. To create a current mirror, two NMOS transistors with their gates are tied together, as shown below in Fig. 3. Once created, to mimic a photocurrent, a current source is wired in parallel to a transistor through the current mirror.

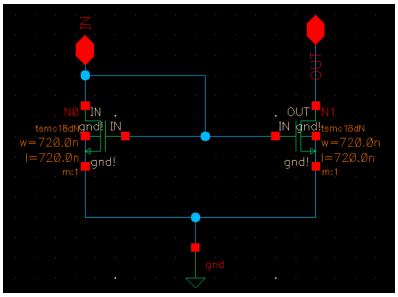

Fig. 3. Current Mirror Schematic.

C. Layout of APS

Once the schematic was fully tested the APS layout was created in Cadence which is shown below in Fig. 4. This cascadable layout maximizes the photodiode area, shown as the large green n-active area, which will accept light while still fitting the 3 required transistors in, while still meeting DRC checks and APS spacings, and fitting within a 10-micron by 10-micron area. The goal when designing this cascadable layout was to allow for the signals from each of the row shift registers, in addition to power and ground, to be cascaded across each row of APS. Additionally, the current outputs from each APS's photodiode are cascaded vertically, allowing the column shift register and additional NMOS to receive each specific APS output. This combination allows the currents from every APS in a grid to be outputted individually to maintain the location of the APS where the current output came from.

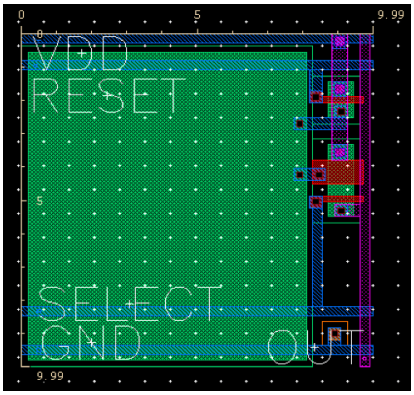

Fig. 4. APS Layout.

IV. 4X4 LAYOUT

A. 16 Pixel Layout Components

To create a 4 by 4 grid (16-pixel) imager, as touched on previously, three shift registers are required of four C2MOS each in series, shown in Fig. 5. These are used for three signals: row select, column select (including additional NMOS), and reset, which together allow for a traversal of all APS to be able to select, output, and reset. These were used on the 4 by 4 grid of APS that are cascaded against each other, which is also shown in Fig. 5.

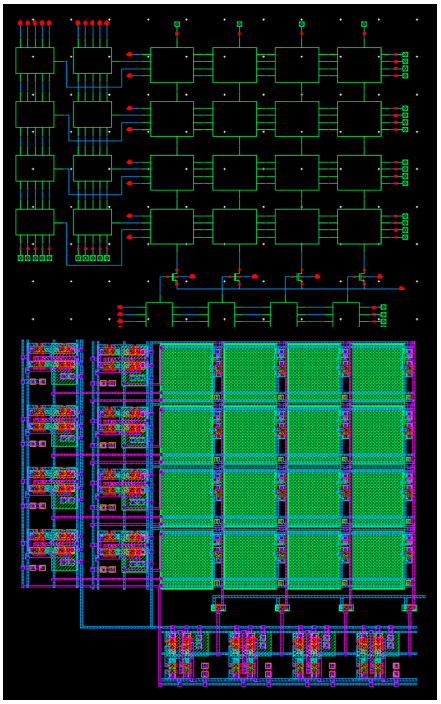

Fig. 5. 16 Pixel Schematic & Layout.

V. FINAL LAYOUT

A. Calculations

To find how many APS could be cascaded together with the respective shift registers, the calculations were done to find how many 10-micron squares fit in a 2.5mm by 2.5mm square which ended up being 62,500. Accounting for the fact that shift registers and select transistors took about 5 rows/columns, we arrived at 61,000 APS, a 0.061-megapixel camera sensor.

B. Scaling to 2.5mm by 2.5mm

Taking the 4 by 4 layout shown in Fig. 5. and scaling it to 2.5mm by 2.5mm was done through Cadence's Mosaic feature, which allows for efficient cascading. This final layout is not shown here as each APS is indistinguishable when zoomed as there are 61,000. The only interesting viewing of it is represented in Fig. 5. as the bottom left corner of this full CMOS Imager which extends up and right.

VI. TESTING AND LEARNINGS

Through the process of designing these components, we learned that testing is a critical aspect to verify our transistor logic, with the example below showing the functionality of the row select shift register working and 4 by 4 grid test shown in Fig. 6. Additionally, as we continued designing we learned more and more design techniques such as having Metal 1 and Metal 2 not run in parallel near each other to avoid contamination. With each discovery we went through and redesigned to optimize our layouts.

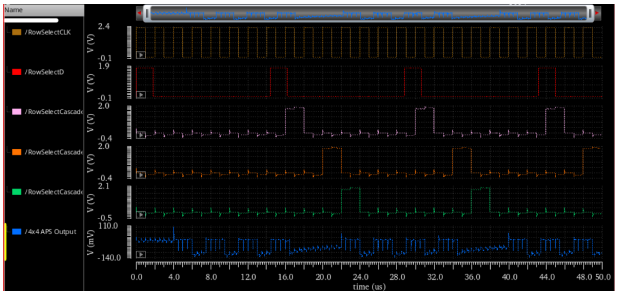

Fig. 6. Testing of Row Shift Register & 16 APS Output.

VII. Global Impacts of IC Design

With today's process sizes in the hundreds of nanometers and, as predicted by Moore's Law, the marginal cost of a transistor has been decreasing at a rapid rate. However, we are "nearing the end of our ability to continue shrinking existing silicon microchips" [2] and as the scale of components decreases, "they become harder to build and harder to make reliable" [2].

Each attempt to shrink chip size requires "increasingly complex new processes" [2], with the fabrication facilities spending billions of dollars on cutting edge processors. With these increasingly complex processes comes a drastic increase in resource consumption of e-waste and production processes.

Producing new wafers alone requires enormous amounts of secondary resources, including vast amounts of water that is purified on site to reduce as much contamination as possible, nearly all of which do not end up in the final product. With the average American household using 28 kWh per day, the energy consumption to produce just one square centimeter of wafer is 0.34 kWh, which is nearly one-fourth of the 1.5 kWh necessary for fabrication [3], alluding to the tremendous amounts of energy required for wafer production.

It is vital for major IC manufacturers to make their design processes less resource and energy intensive, and minimize and record the waste used in doing so. One way is by researching and applying more ways to reuse components in old devices. Currently, this responsibility is placed on "informal sectors that resort to crude dismantling and backyard recycling techniques", which is not at all sustainable for the expected 4%-5% annual increase of e-waste [4].

VIII. Engineering Ethics

While we worked on most parts of the project together, Zeyn focused more on schematic designs and testing, and Reid focused more on layouts, layout design considerations, and tiling.

During our process of creating, testing, and combining subcomponents to build the imager and meet the project requirements, we followed the IEEE Code of Ethics. As discussed in "Global Engineering Ethics: What? Why? How? and When?", we successfully worked through normative issues and descriptive claims during the process, and accepted criticisms and feedback from each other and academic faculty. Additionally, we made minimization of space and material in our layout designs a key factor.

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