CMOS Imager

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Introduction

An Active Pixel Sensor's (APS) ability to convert accumulated photons into current is a crucial part of modern-day documentation. When combined with a way to capture their data, they become the foundations of image capture, a CMOS imager. With almost infinite applications, this component is a crucial part of many types of electronics.

Objectives

In this project we explore the process to design and test a 2.5mm x 2.5mm CMOS Imager or 0.061-megapixel sensor. The initial goal is to create and test an APS, C2MOS Latch, and any subsystems required. Continuing, the end goal is to combine these subsystems into an imager, that will further be tested. This imager will be scaled to the desired size of 2.5mm x 2.5mm.

Research and Methods

For the implementation of this project, we are using Cadence Virtuoso. Additionally, we use a 0.18µm process size for the implementation of this sensor to achieve the required goal size. To successfully design at this process size, we are using transistor size of 720nm x 720nm except for switching transistors which are 720nm x 180nm. Also, Cadence has built-in testing to verify our layout (DRC) and verify our layout and schematic match (Extract & LVS), we will use throughout.

Results

Figure 1 — C2MOS Latch
The C2MOS Latch is used as a flip-flop, with output dependent on current input and past state. Made of 8 transistors, it takes in a signal every clock rising edge. When cascaded vertically and horizontally, they create a shift register which can select a single APS's data in a grid of APS's.

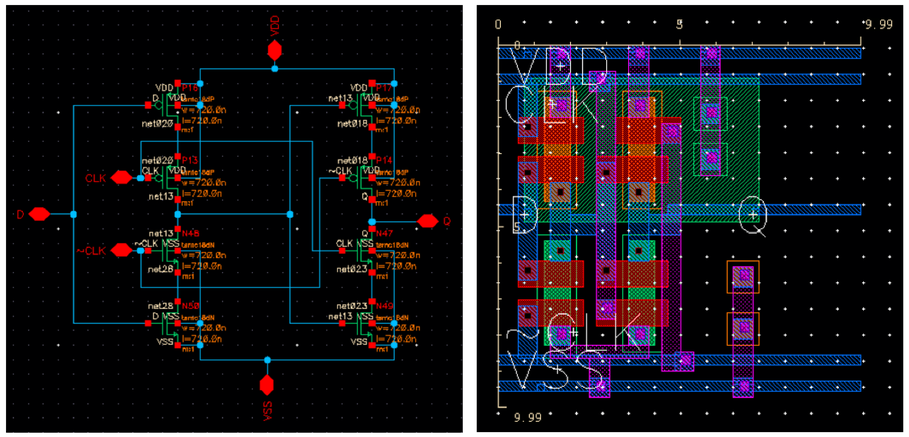


Figure 2 — Active Pixel Sensor (APS)
An individual APS is largely a photodiode, shown by green in the right layout image. It outputs current based on the inputs of two transistors implemented to receive a select signal and a reset signal.

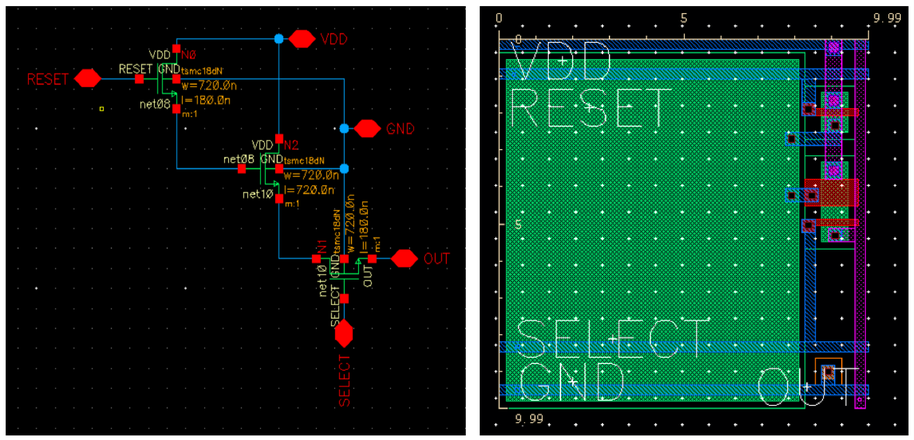
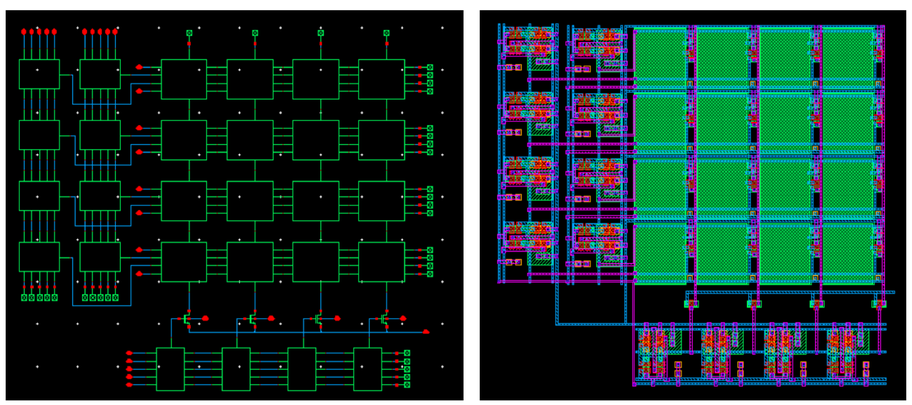


Figure 3 — Scaling APS & Shift Registers
The APS and C2MOS are designed to be gridded and scaled to achieve the goal size. The shift registers work to send/receive all signals from the APS grid and deliver an output stream of data with the use of additional transistors.



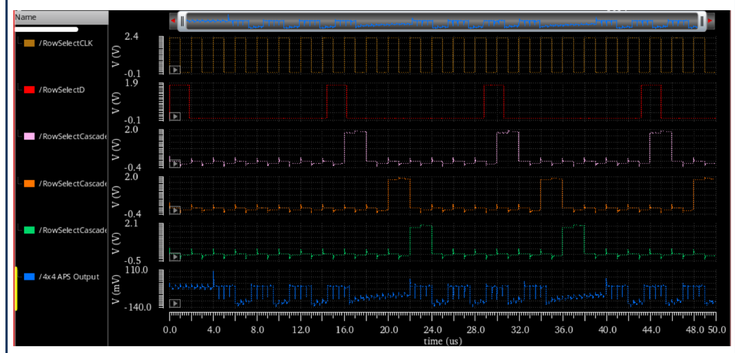


Figure 4 — Testing Implementation
Testing each sub-component and the overall design of the CMOS Imager was a detailed process. Each component required its own individual testing schematic to input simulated values for all required inputs. This then allowed us to plot the output from each component to debug and understand how it is affected by different values (e.g. current magnitudes, voltages, sine wave frequencies, etc.)
Above we chose an example plot of our first scaling, a 4 x 4 APS grid with the Row Select shift registers displayed, along with the final. Note there also also plots for Column shift registers and Row Reset shift registers not shown above, to prevent clutter on plot, both of which work similarly with their individual input signals to create APS output.

Conclusion

Through this processes we designed and tested all stages of the CMOS imager. While the schematic design process had a large learning curve through many iterations of each component it became easier by the end to implement. Similarly, the layout process took many attempts to understand how to create the transistors and design efficiently. By the end, all our layouts and schematics passed DRC, Extract, and LVS and were efficiently contained in 10um x 10um boxes for cascading. Additionally, we learned and implemented other good styling practices such as not running rails of metal 1 and metal 2 in parallel near each other. Overall, we were able to create a scalable design and achieve a CMOS imager.