China RISC-V Summit 2024

HVP: Hardware Accelerated RISC-V Android Emulator

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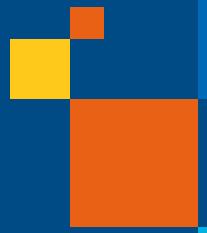

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 This document contains information on products and/or processes in development.

HVP: Intel **H**ypervized **V**irtual **P**latform

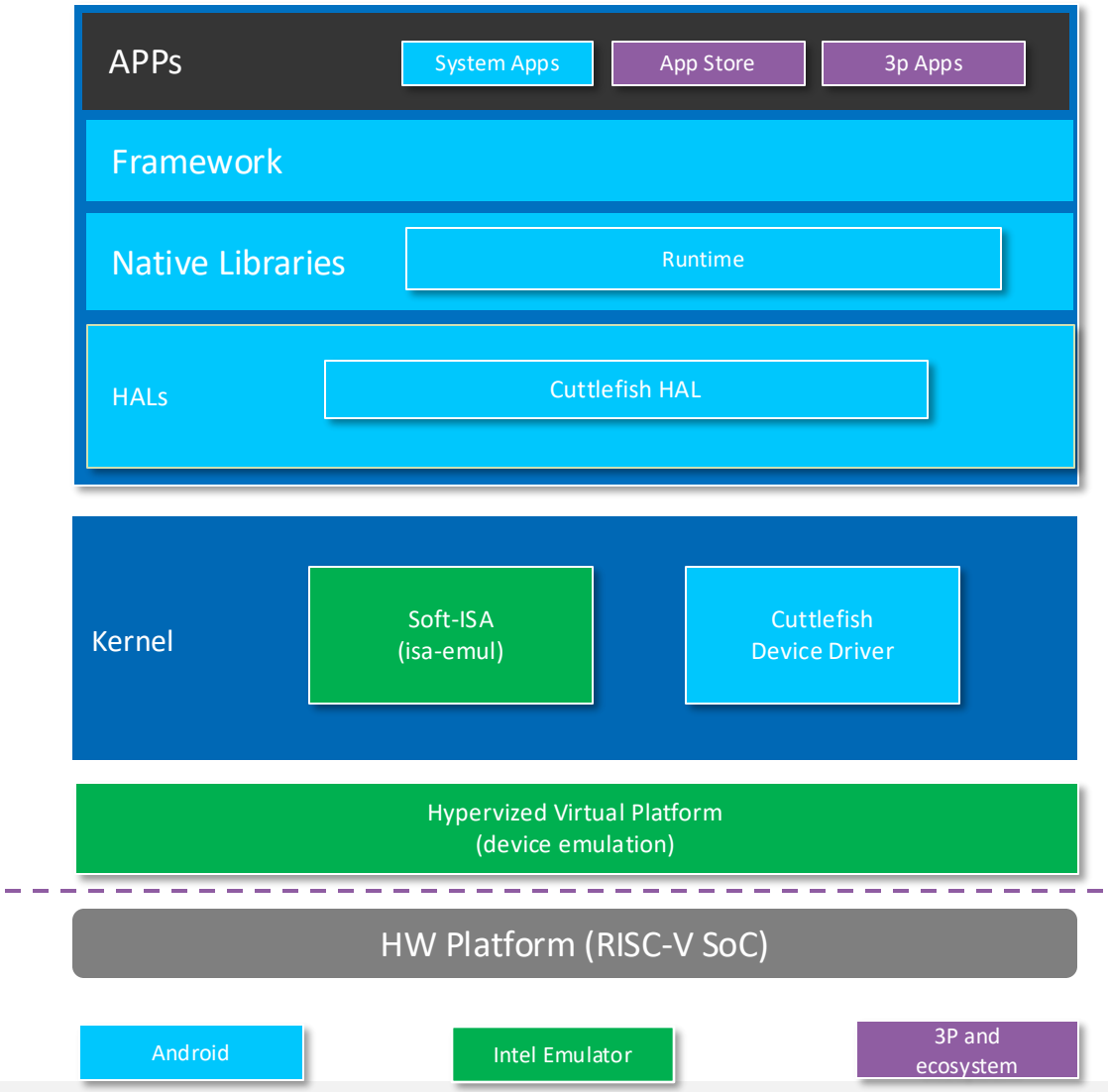
A RISC-V Android emulator accelerated with virtualization technology:

- Type-1 hypervisor (ACRN in M-mode (w/ PMP) or in HS-mode (w/ H-Ext))
- Device model (Android Cuttlefish QEMU DM)
- ISA emulation (Soft-ISA Technology)

Team Intro

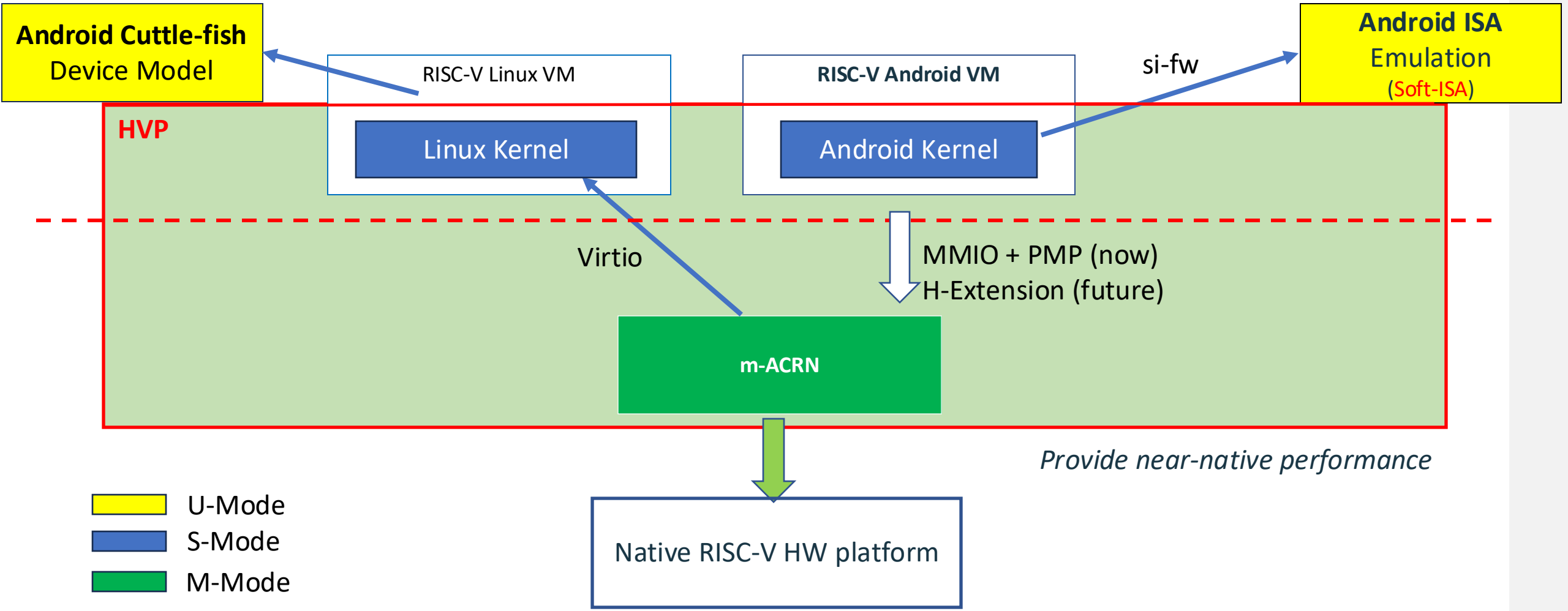
- Haicheng Li (Architect, Hypervisor & Soft-ISA)
- Qingshun Wang (QEMU Device Model, Linux HSM)
- Haibo Xu (IO Virtualization)
- Xiao Wang (Soft-ISA, AOSP Enabling)
- Victor Sun (ACRN Ecosystem)

Emulation: Shift-left Android Software Enabling

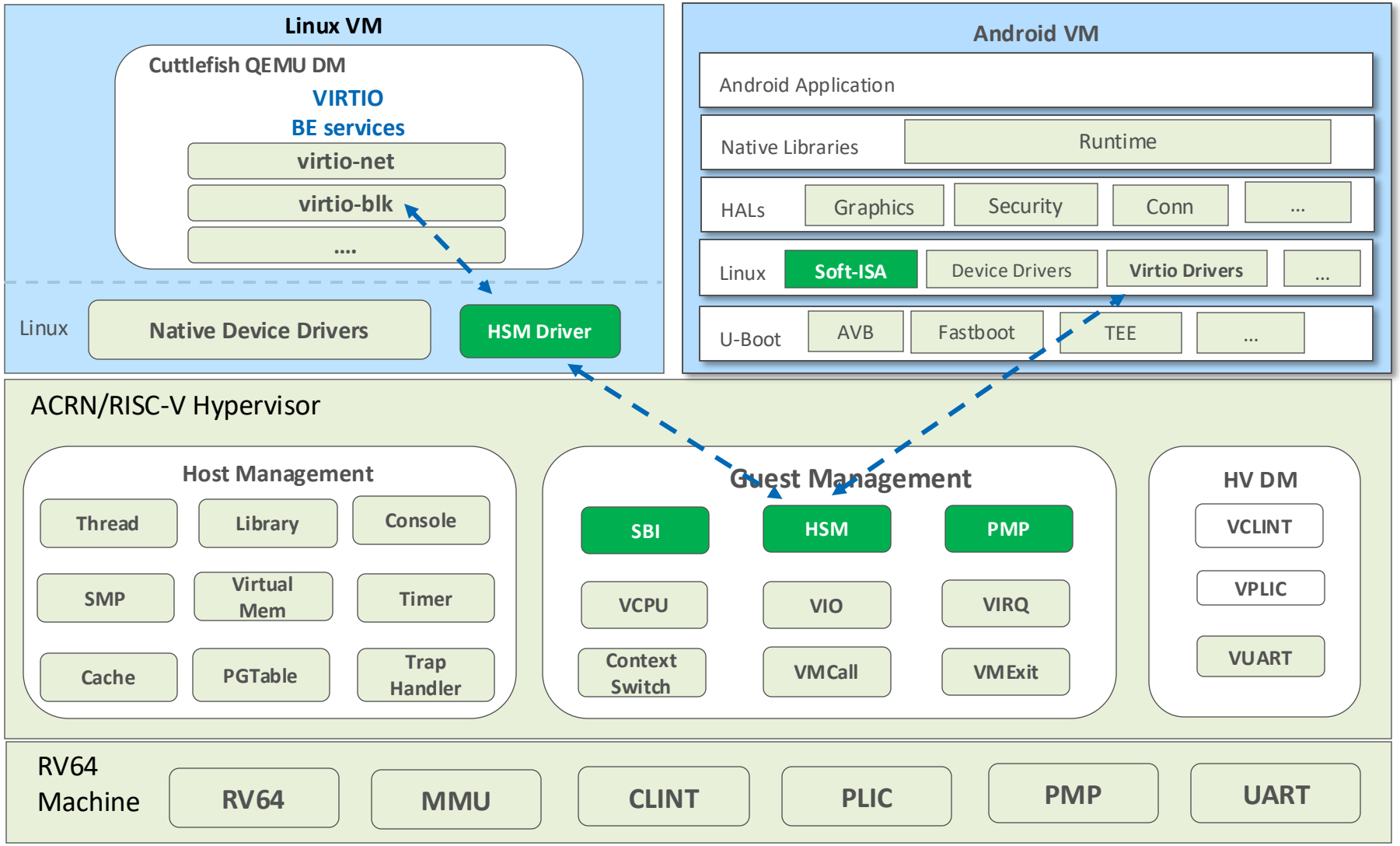


- Shift-left RISC-V Android software development and system optimization before hardware availability
- Accelerate RISC-V Android platform enabling and reduce product TTM

HVP Emulator Architecture



HVP High Level Design

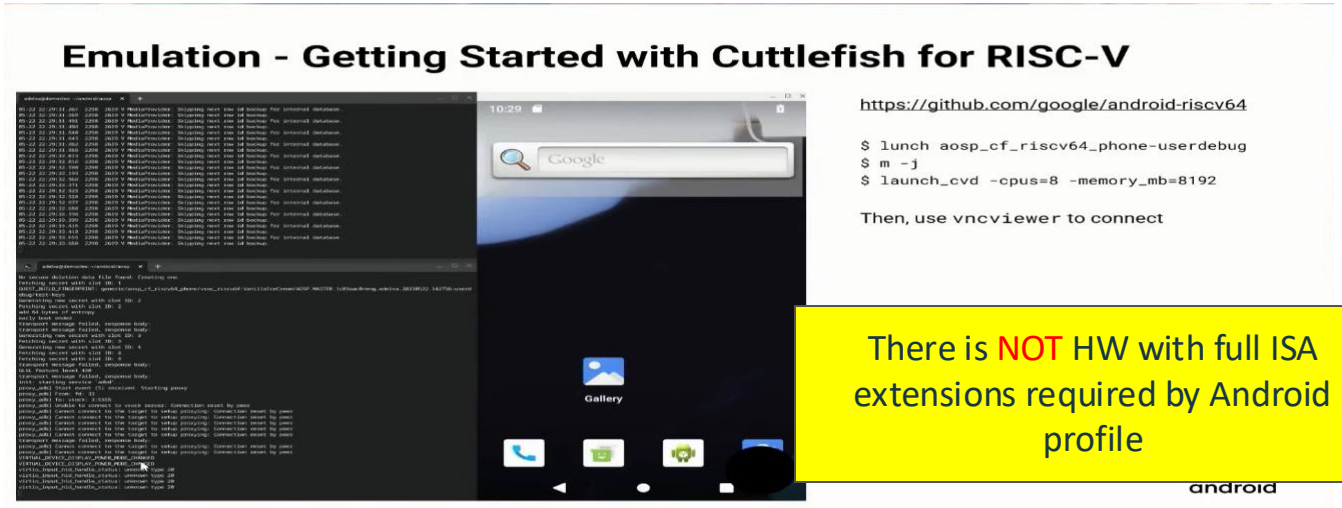


- **ACRN Hypervisor**
  - PMP Context Switch
  - HSM Support
  - RISC-V SBI support
- **SOS Linux VM**
  - Kernel HSM module
  - Cuttlefish QEMU DM
- **Android VM**
  - Virtio Devices
  - Soft-ISA

Virtio Data Flow

New Module Enabled in Existing Software Stack

Near-HW-Perf Android Emulator



There is NOT HW with full ISA extensions required by Android profile

AOSP

Android Runtime (ART) available

Cuttlefish emulator available

Prebuilt tools - compilers & system root libraries available

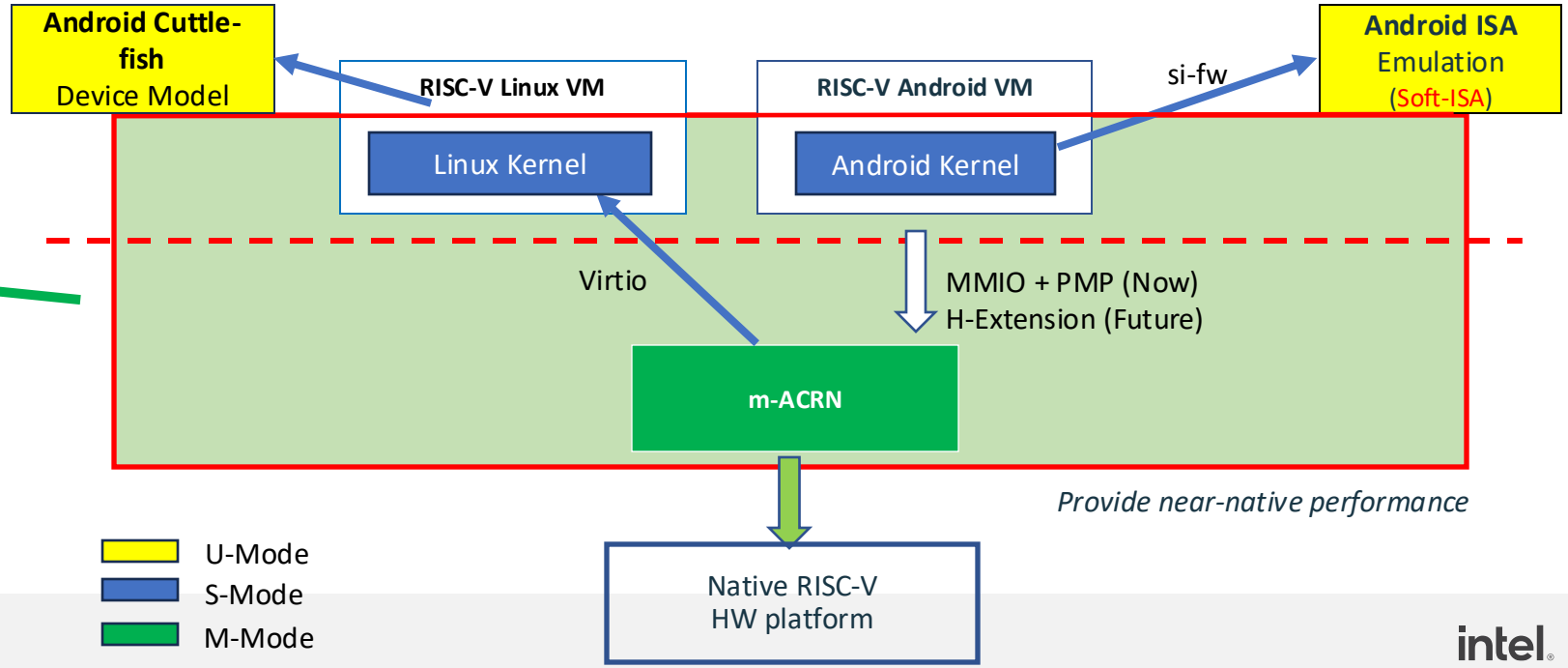
Initial support landing soon for extensions beyond RV64GC to optimize the platform

- Vector
- Bit-manipulation extension optimizations (Zba/b/s)

Profiling works (again, ~~prebuilts coming~~ soon)

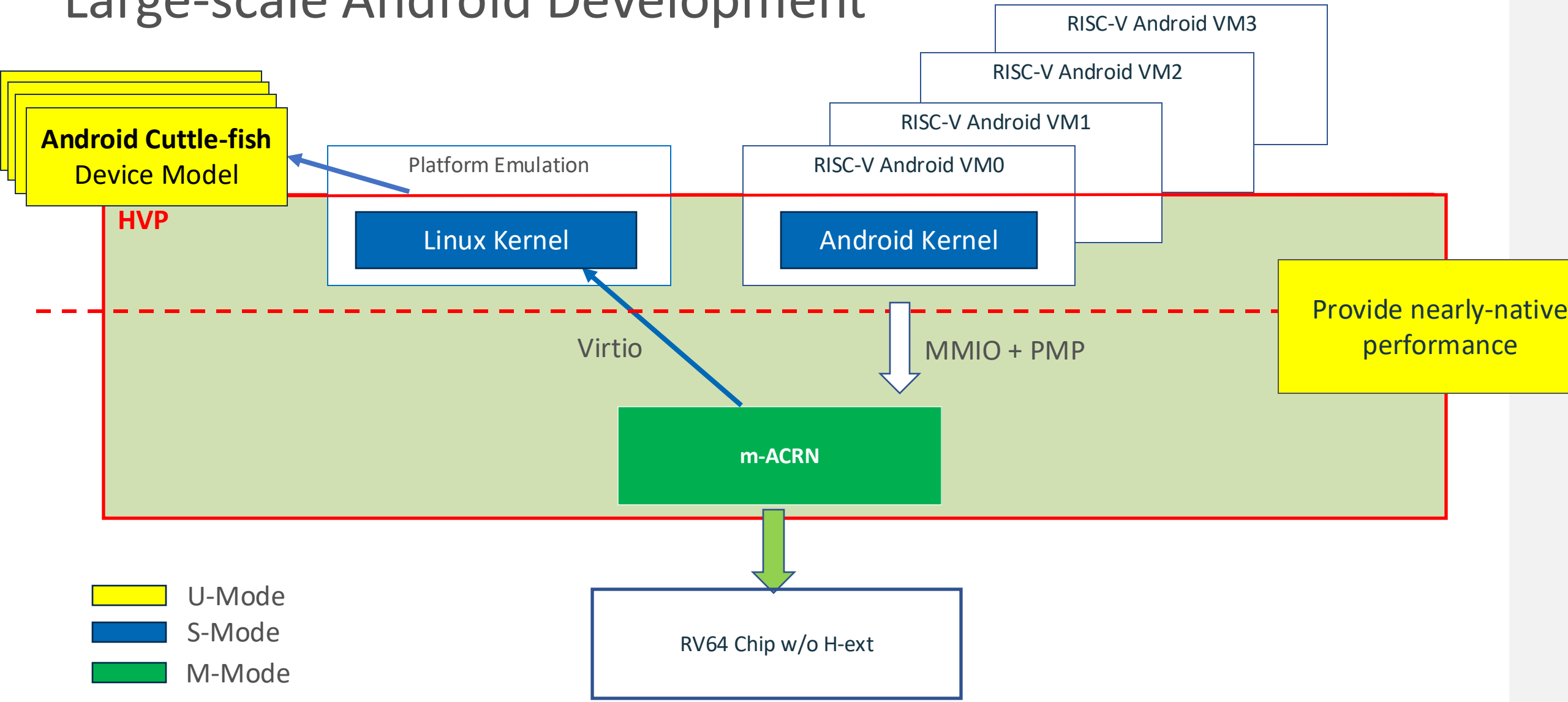
Performance comparison:

bootup **8min** vs. **30s**

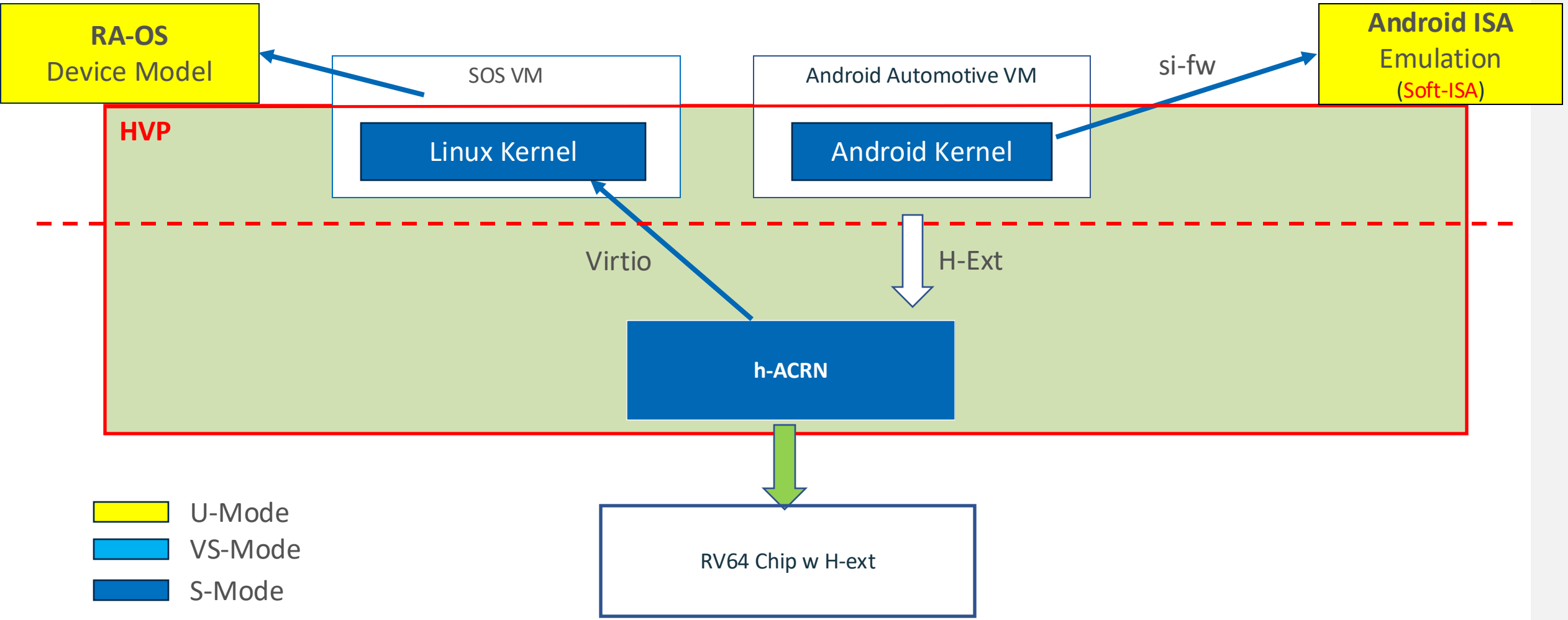


Provide near-native performance

Large-scale Android Development



HVP for RISC-V Automotive OS



Vision

- high performance Android & Automotive RISC-V platform emulation
- pre-configured, functionally accurate emulation of RISC-V platform profiles
- enable development of large portions of software ahead of hardware availability

Hypervized Virtual Platform as RISC-V Android Emulator

工欲善其事，必先利其器

- https://riseproject.dev

RISE is focused on positive and transparent collaborations with upstream projects to deliver commercial-ready software for various use cases

How: Align on highest priorities & avoid (accidental) duplication of work

Goal: Accelerate open source SW for RISC-V architecture

https://www.intel.com/content/www/us/en/developer/articles/community/rising-to-the-challenge-risc-v-software-readiness.html

Finding more interesting topics from Intel on RISC-V summit China 2024

Topic	When & Where
UXL 软件栈和 RISC-V 的初步探索	August 22 16:45 主会场A
LLVM 工具链 RISC-V 构建实现及其性能优化现状分析与未来展望	August 23 9:40 主会场A
GCC RVV 自动向量化及其应用	August 23 10:00 主会场A
Enhancing RISC-V Security with SBI Secure Service APIs	August 23 10:40 主会场B
Enabling Hardware Sampling Based PGO for RISC-V Platform	August 23 11:40 主会场A
利用 WASM 技术解决多种 ISA 的挑战	August 23 14:20 主会场B
HVP: Hardware Accelerated RISC-V Android Emulator	August 23 14:50 主会场A
Leverage BRS standard to improve RISC-V SW compatibility	August 23 17:30 主会场A
Soft-ISA: kernel built-in emulation engine to extend RISC-V silicon ISA capability	August 23 17:40 主会场A

Thanks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