SYNOPSYS。新思

Addressing Real-Time Workloads in Automotive Apps with ARC-V Processors

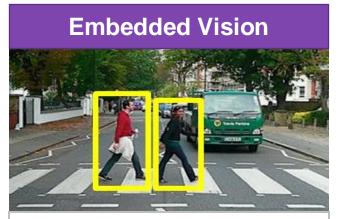
Yaqiang Pei – Sr. Processor Application Engineer August 2024

Agenda

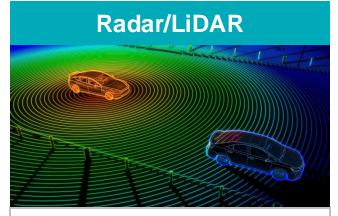
- Safety Critical Applications
- Evolution of automotive SoC architectures
- What is RT virtualization?
- Software Centralized Vehicle Processor Architecture
- ARC-V RHX Overview
- ARC-V RHX Real-time Virtualization Highlights
- Summary

Safety Critical Functions Require Real-time Determinism

Example Automotive Functional Safety Applications



- Analyzes camera data for safetyenhancement and autonomous driving
- Expert-level accuracy in classifying objects in fractions of a second
- Use Cases:
 - Lane departure detection
 - Parking assist / self-parking



- Key components of Level 3+ and autonomous vehicles
- Essential in night driving, conditions of rain and fog
- Use Cases:
 - Blind spot detection
 - Collision avoidance systems

Driver/Passenger Safety



- Critical real-time (predictable) performance for maintaining passenger safety
- Reduces the risk of injury, provides greater control and stability of the vehicle
- · Use Cases:
 - Anti-lock braking systems

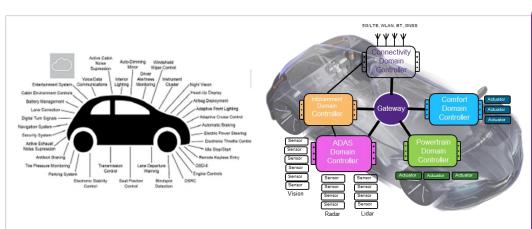
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Adaptive cruise control

Safety-critical systems require real-time determinism and processors which support this paradigm

Evolving Automotive Implementations

New Architectures. New Regulations. More Opportunities

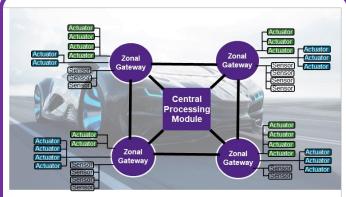


Yesterday 30 - 100+ ECUs in a car

Mainstream MCUs

Today **Domain Logical Architecture**

Consolidating of ECUs Integration of Functions



Tomorrow/Future

Zonal Physical Architecture

Multi-Applications Central Processing Multi-Chip & Higher Complexity/Performance SoCs

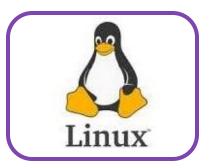
Many functions in the zonal architecture require deterministic (real-time) processing (e.g. sensor fusion, safety management)

Automotive SoCs increasing complexity

- Need system & SoC level security and functional safety
 - Transition to centralized Domain
 Compute Modules and zonal
 architectures
 - Growing number & types of sensors:
 Imaging, Lidar, Radar, Infrared require
 multi-core processing & interfaces
 - Increased compute processing performance
 - Connectivity OTA updates added to every sub-system & SoC
 - More entry points for attacks
- New UN regulations for cyber security to address increased risks
- New entrants developing SoCs (OEMs, Tier1s and start-ups)

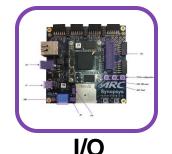
What is Real-time Virtualization?

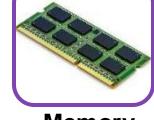
- Virtualization is the abstraction of Operating Systems (OSs) from hardware resources
 - Allows SoC resources to be "shared" by multiple OSs
 - Provides a more efficient implementation; reduces overall power and area for complex SoCs
- OSs "unaware" of virtualization; managed by a hypervisor
- Enables parallel development and incremental updates without re-testing / re-validating the entire system
- Supports concept of "mixed-criticality" safety-critical and non-safety applications co-exist on the same platform
- Next-gen automotive solutions will run non-RT OSs (e.g. Linux) for some workloads + traditional RT tasks based on AUTOSAR Classic / RTOS



Real-time Operating System (RTOS)

Hypervisor



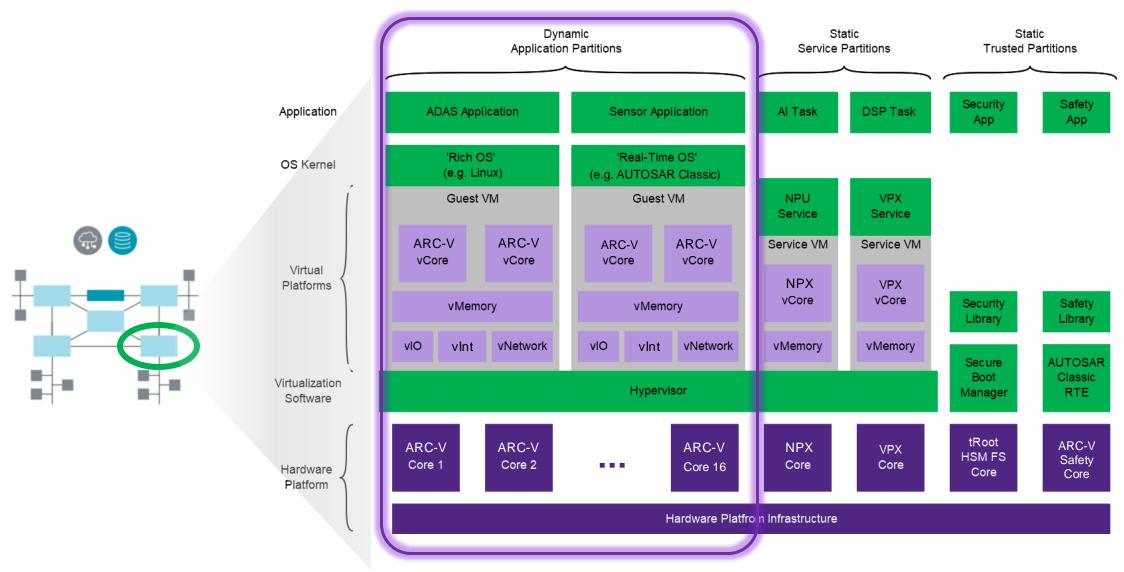




Memory

CPUs

Software Centralized Vehicle Processor Architecture

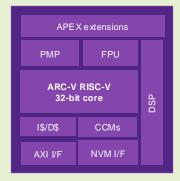


NEW! Synopsys ARC-V Processor IP

Extending the Synopsys Processor IP Portfolio to RISC-V

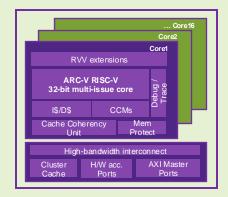
Common MetaWare Tool Chain

RMX Series



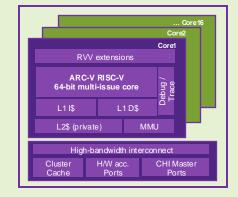
- 32-bit embedded processor, optimized for ultra-low power
- High efficiency 3- and 5-stage pipeline configurations
- Optional DSP extensions
- FuSa hybrid mode

RHX Series



- 32-bit processor, optimized for realtime applications
- Dual-issue 10-stage pipeline
- H/W virtualization support
- Up to 16x cores, H/W accelerators
- Optional RVV extensions

RPX Series



- 64-bit multi-core host processor supporting user/supervisor profiles
- 25% higher SPECint performance than ARC HS6x cores
- Multi-cluster cache coherency with AMBA-CHI interfaces



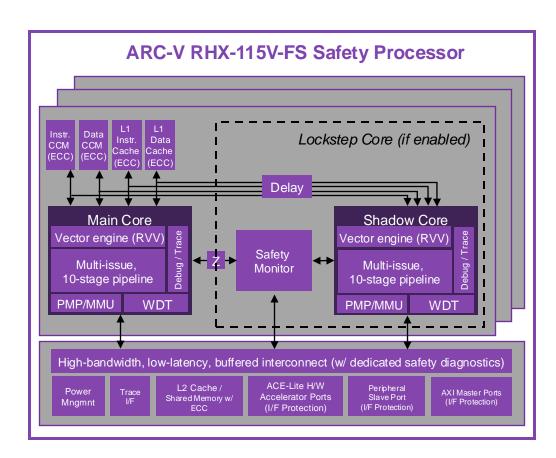
- Builds upon proven track record of processor IP success
 - 25+ years implementing extensible ISAs with leading PPA efficiency
 - Deep FuSa knowledge (industry's 1st Processor IP certified for full ASIL D)
- Unrivaled support for software development
 - Highly-optimized MetaWare toolkit + rapidly expanding RISC-V ecosystem
- Co-optimized Synopsys solutions accelerate SoC SW & HS dev't
 - Full-stack Al-driven EDA suite boosts engineering productivity and QoR
 - QuickStart Implementation Kits help SoC designers optimize ARC-V IP
 - Virtual prototyping solutions for early SW development & architectural exploration

SO 26262 Functional Safety + ISO 21434 Cybersecurity

ARC-V RHX-115-FS Safety Processor

32-bit Real-Time Safety Enabled Multi-core Processor





- 10-stage RISC-V 32-bit multi-core processor (1-16 cores)
 - RISC-V compliant profile support (RV32I + extensions)
 - Support for coherent HW accelerators, HW virtualization
 - Optional RVV extensions
- SP/DP/HP Floating Point support
- Configurable in lockstep or hybrid mode (RHX-11x-FS)
 - Up to 16x ASIL B or 8x DCLS (ASIL D) cores
- Security Features
 - Hypervisor support for mixed safety criticality & security
 - Standard RV crypto instructions
 - ISO21434 security compliance
- Software development with ASIL compliant MetaWare RISC-V C/C++ compiler and libraries

RT Virtualization Critical to Automotive

Synopsys' ARC-V RHX CPU architecture provides core, memory and interrupt virtualization that is:

Efficient



 Dedicated hardware avoids software overhead

Predictable



 Enables virtualized realtime applications

Composable



 Seamless integration with RHX security and safety features

Core virtualization

- Fully compliant implementation of the RISC-V H-extension
- Includes virtualized core-local peripherals (timers, interrupts, etc)
- ARC-V extensions minimize need for hypervisor emulation

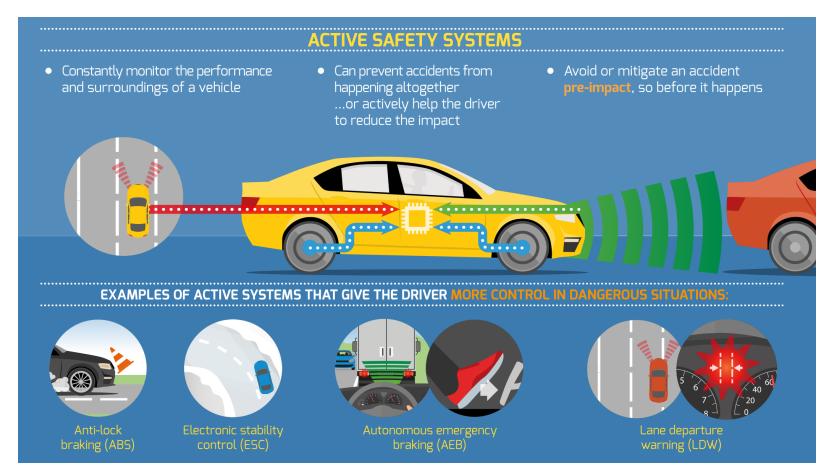
Memory virtualization

- Hypervisor Guest Physical Memory Protection (hgPMP)
- Virtual Supervisor Physical Memory Protection (vsPMP)

Interrupt virtualization

- Advanced Platform Level Interrupt Controller (APLIC)
- RHX core extensions to handle RT interrupts with bounded latency
 - Direct Message Signaling Interface extension delivers time critical MSIs
 - Support for nested vectored interrupts, including virtual & VM targeted interrupts
- H/W assisted stack pointer mngmnt for more predictable interrupt / trap latency

Summary



Source: roadsafetyfacts.eu

- Safety-critical automotive applications require processing workloads with minimum latency and real-time determinism
- System reliability and availability depend on the effectiveness of this real-time processing
- Real-time processors must provide safe, deterministic operation
- Synopsys' ARC-V RHX Processors provide excellent support for RT virtualization and predictability required by these applications

Thank You