# Accelerate RISC-V SOC SW/HW co-development with mixed Emulation platforms

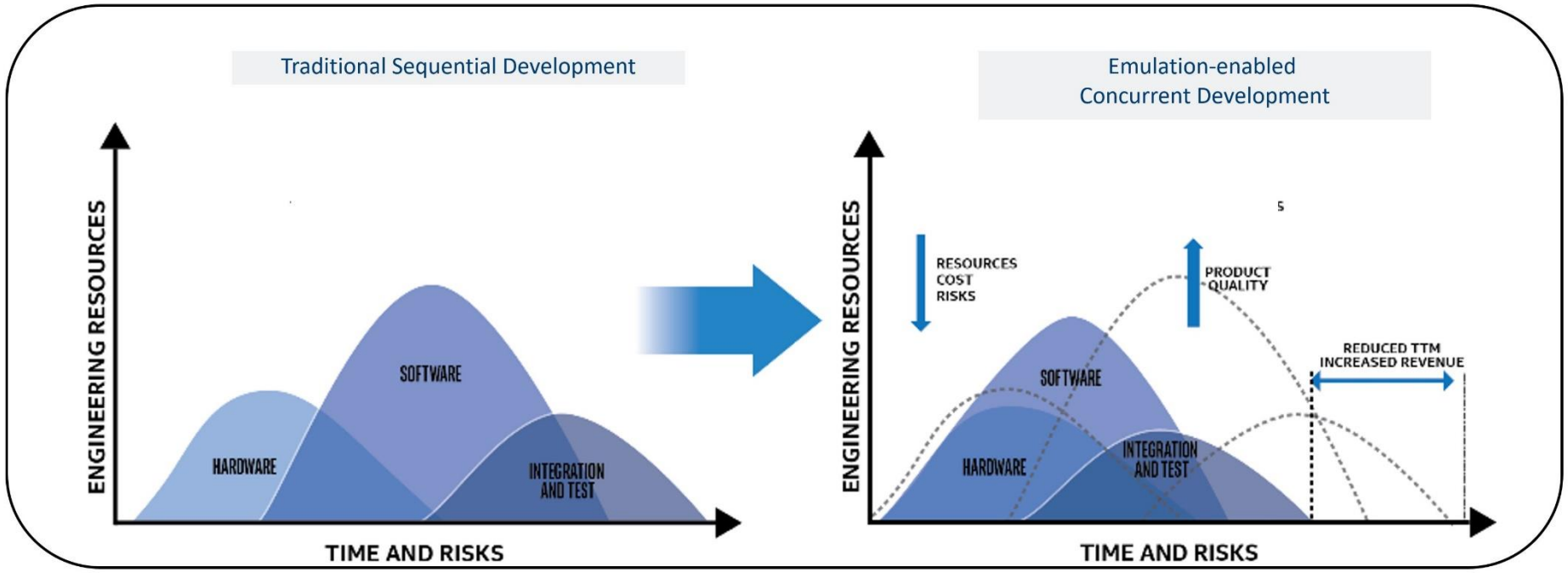
Zang Bo – Intel

# Pre-Si – “Shift Left!”

## Pre-Si Validation Shift-Left

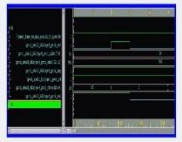
Big Challenges:

- RISC-V SOC becomes bigger and more complex.
- Hard to figure out all HW RTL bugs with only UVM verification.
- Huge software enabling efforts for RISC-V SOC power on stage.



# Pre-Si Platforms

## Pre-Silicon Prototyping Platforms



### RTL Simulation

### Emulation

### FPGA


### Virtual Platform

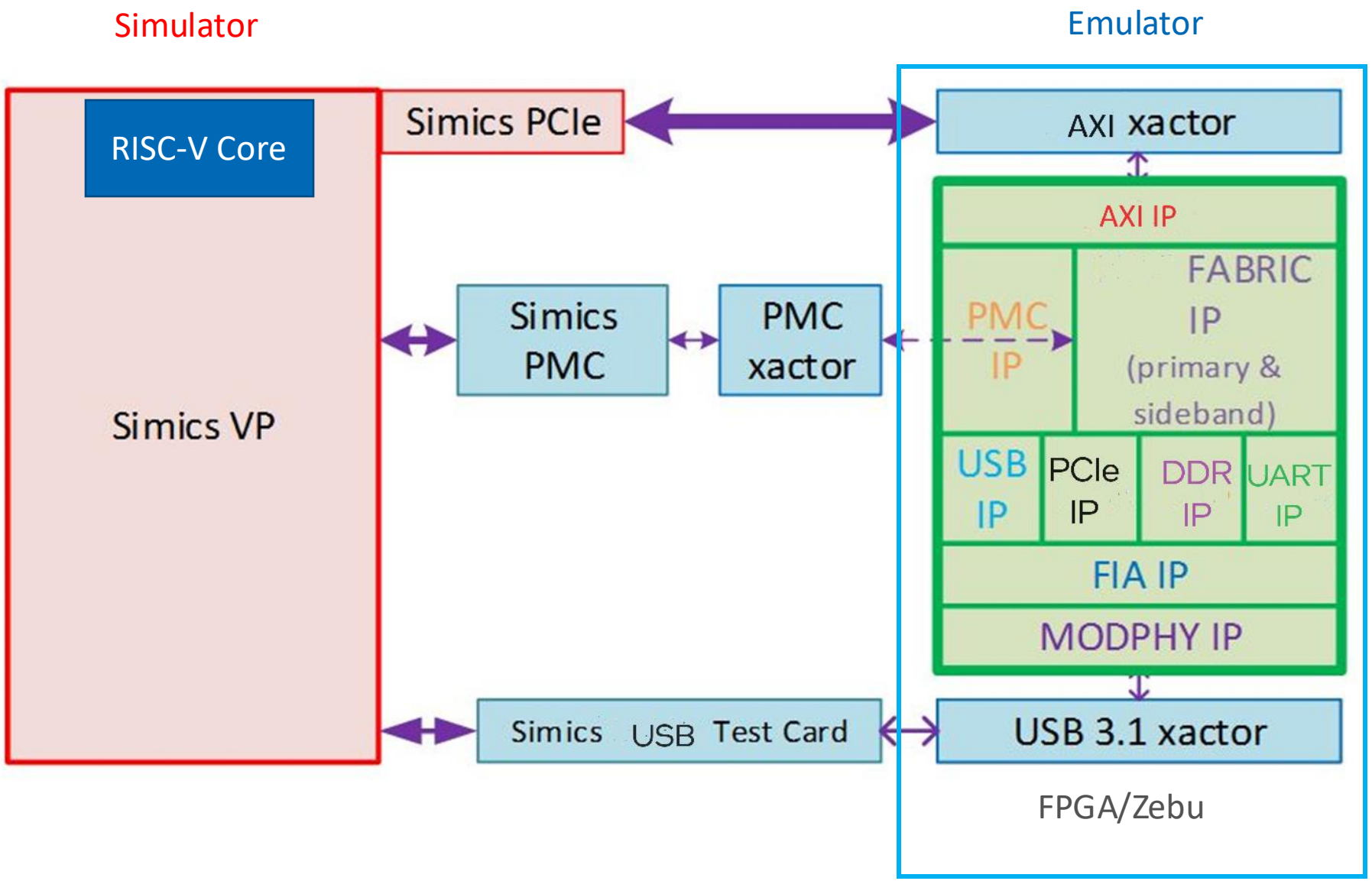
| | RTL Simulation | Emulation | FPGA | Virtual Platform |
|---|---|---|---|---|
| Application | Find logic bugs | System-level Bug hunting; PnP, Power-On Readiness | IP-level FW development and checkout | HW/FW/SW co-dev and integration |
| Accuracy | Switch/latch/gate | Gates | Abstracted Gates | Registers/Behavioral |
| Speed | ~10Hz | 1-2 MHz | 1-20 Mhz | 1-500+ Mhz |
| Cost | Licensing and Compute | ~$1M/Instance | ~$100k/Instance | Internal team or Licensing |
| Scale | IP-Full SoC | SoC Subset-Full SoC | IP-SoC Subset | IP-Full Platform |
| Vendors @ Intel | Synopsys VCS | Synopsys Zebu, Mentor Veloce, Cadence Palladium | Synopsys HAPS, Internal Design, ProDesign | Intel Simics, SNPS Virtualizer |

Emulator – HW (RTL)

Simulator- SW

Hybrid Sim/Emu

# Hybrid modeling type (simulator + emulator)



# RISC-V SW/HW co-develop based on mixed emulation platforms

**PCIe controller register program reference scripts**:
- PCIe link up
- PCIe speed change
- PCIe low power control
- Cfg/Mem access

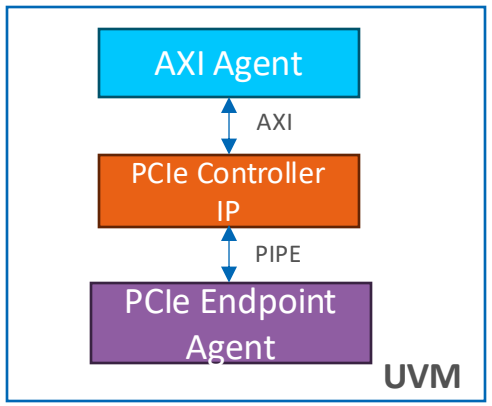
**PCIe controller driver.**

**PCIe device driver:**
- NVMe driver (PCIe SSD).
- Network stack (PCIe ethernet card)
- Graphics driver (PCIe graphics card)

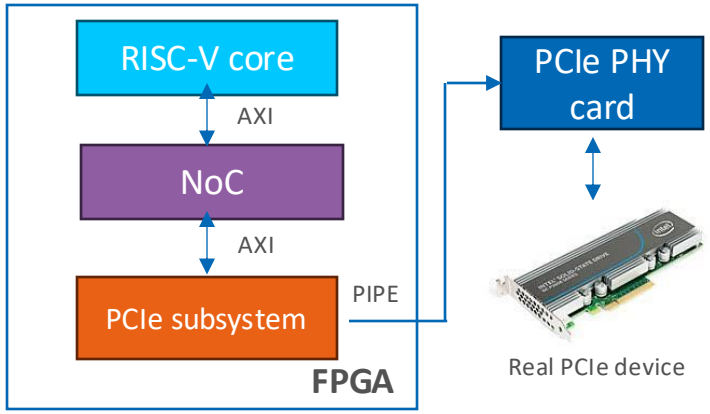
**Complex scenarios** :
- PCIe p-2-p transfer
- PCIe to DDR DMA
- Full SOC boot flow

SW

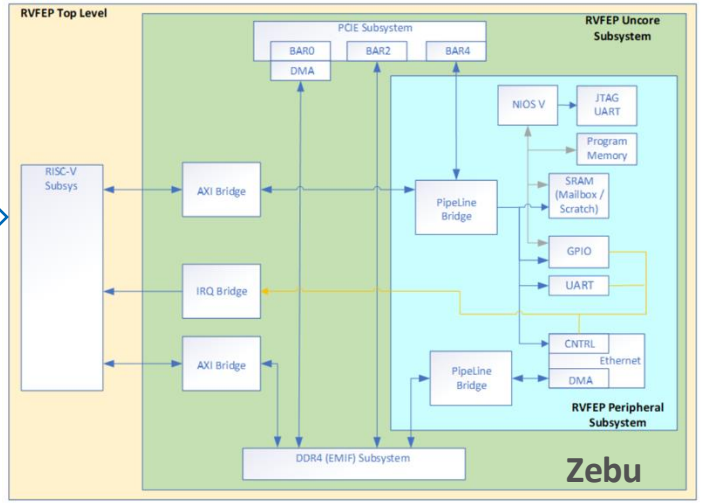
HW




PCIe standalone IP on UVM

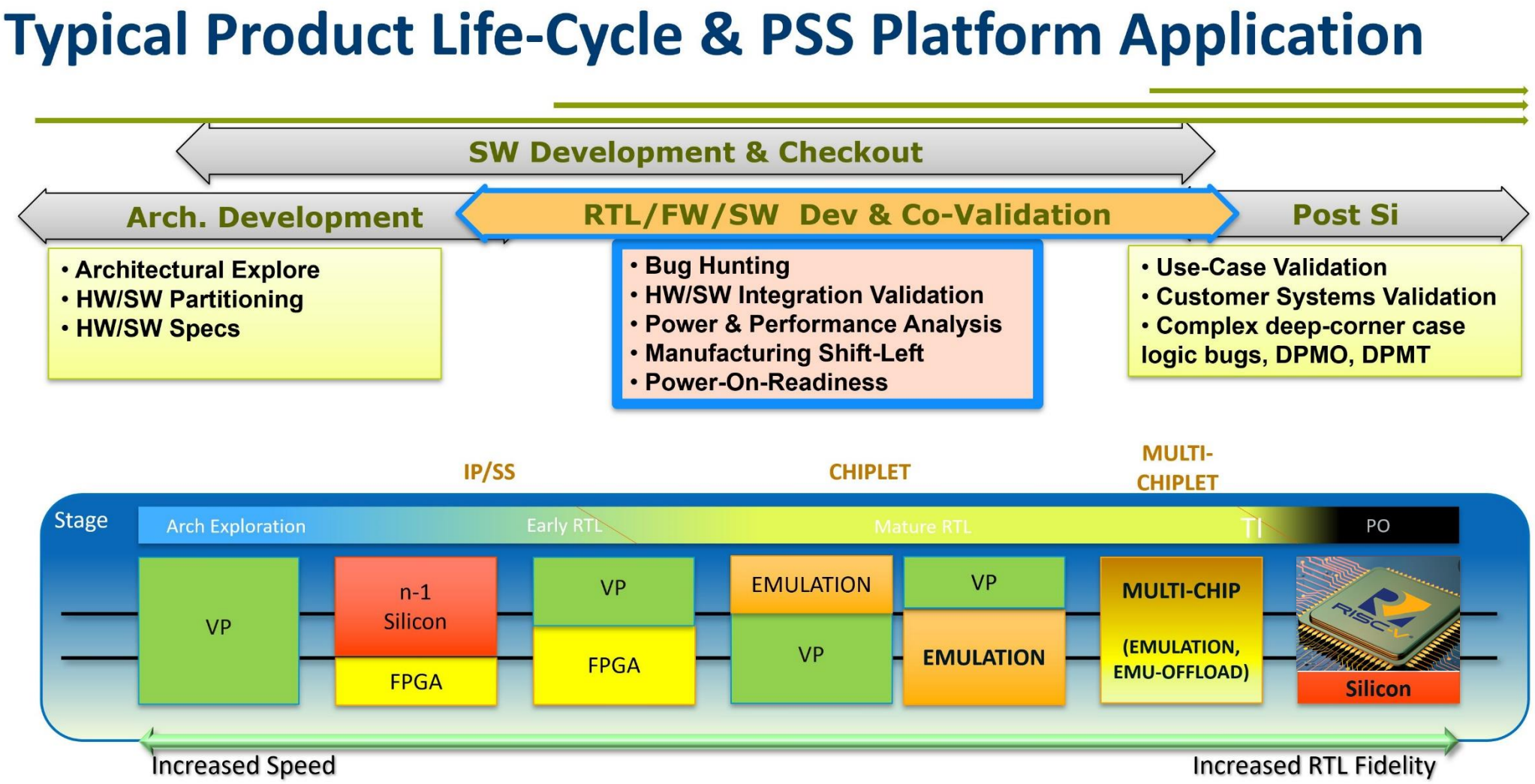



PCIe subsystem E-2-E on FPGA




Full RISC-V SoC on Zebu

# Mixed Pre-Si platforms in product life cycles



# Thanks!