SYNOPSYS® · 新思

RISC-V®

Accelerating SoC Innovation with Synopsys RISC-V Solutions

RISC-V Summit China 2024

James Ng, Executive Director

August 2024

37 Years of Advancing Chip Design

Leading electronic design automation tools and services

Broadest portfolio of interface, foundation, processor and security IP

Pioneer in electronics systems solutions and AI-powered EDA

#12 global software company by revenue

$5.79B*
Revenue (TTM)

~19K*
Employees

3,395
Patents

28%
R&D Investment

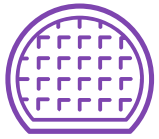
* Excluding SIG

Powering the Era of Pervasive Intelligence

Artificial intelligence

Exponential productivity and efficiency gains

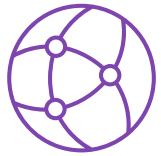
Overcoming energy and compute limits



Silicon proliferation

More silicon content everywhere

Addressing productivity and talent gaps



Software-defined systems

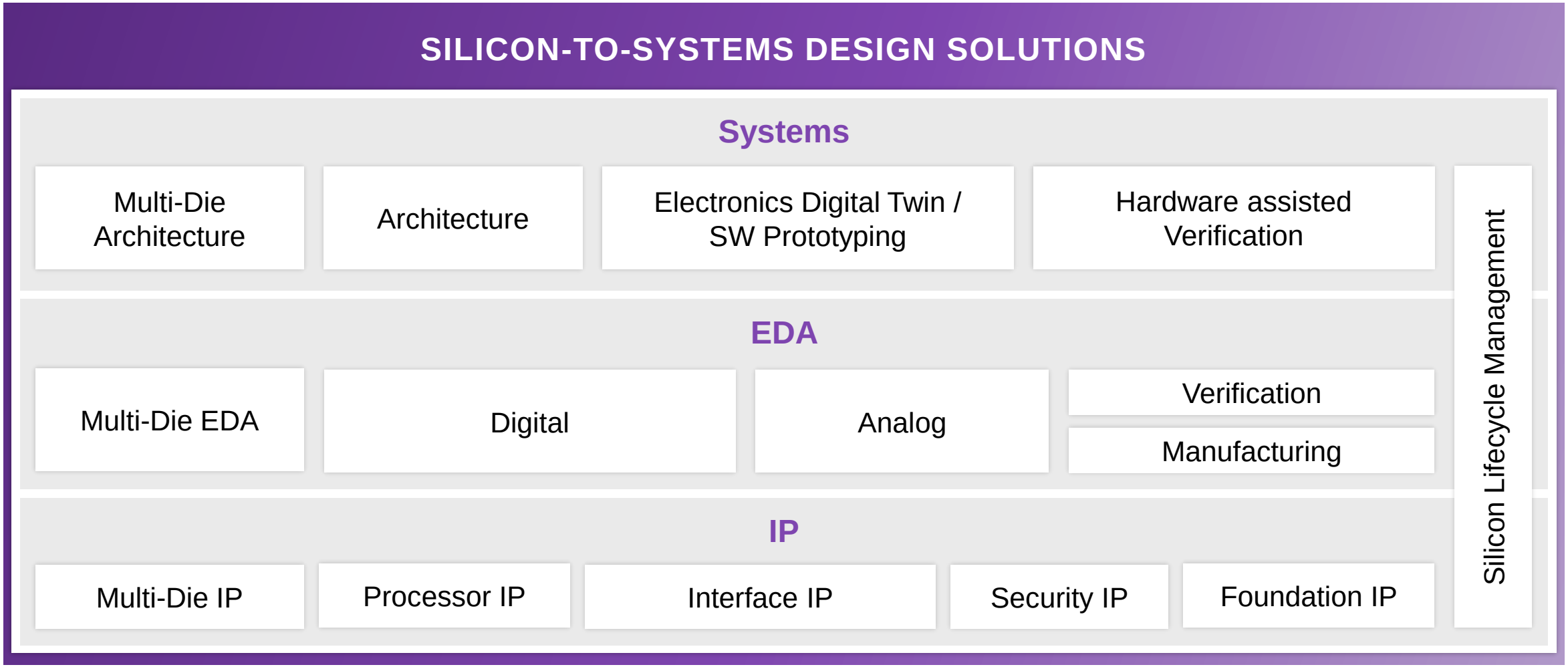
New applications, new methodologies

Enabling increased complexity, enablement of new developers

SILICON-TO-SYSTEMS DESIGN SOLUTIONS

New design paradigm; Solving challenges and addressing complexity

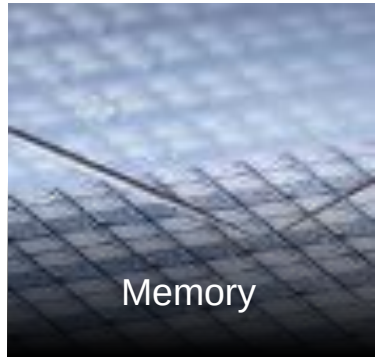
Synopsys Comprehensive Industry Solutions

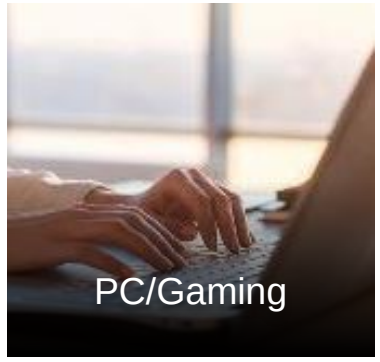


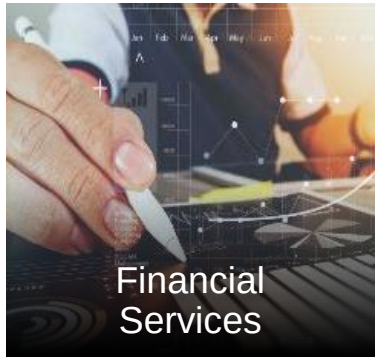
Addressing Needs of the RISC-V Design Community

Increased dependences in existing and emerging markets

>90% OF ADVANCED CHIPS USE SYNOPSYS TECHNOLOGY





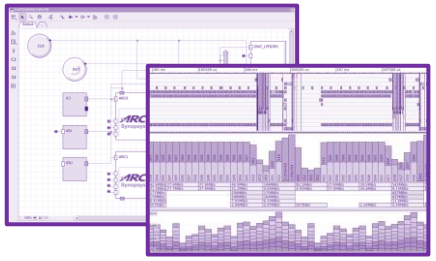


RISC-V Processor Design - Industry Challenges

Choice of IP Architecture Exploration	Designers experimenting with custom architectures for targeted application; limited resources to meet time to market deadlines
Superior Power, Performance, Area	Design complexity and expertise in achieving PPA for advanced process nodes
Verification Signoff	Custom instructions need proven & targeted verification methodologies to avoid silicon respins
Early Software Development	Scalable modeling to shift-left software development to catch bugs early; Need high-performance system validation prior to availability of the final SoC

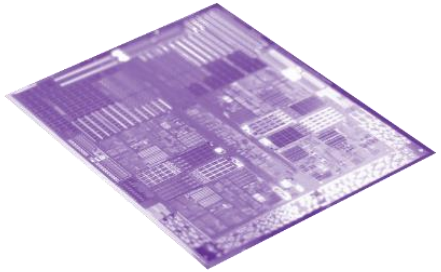
Synopsys Solutions for RISC-V

Custom Processor Design & Early SW Development



- Design and exploration of custom RISC-V processors with application-specific ISA extensions, using **ASIP Designer**
- Optimize HW/SW partitioning
- Flexible **virtual prototypes** for SW development

Optimize QoR, PPA and Productivity

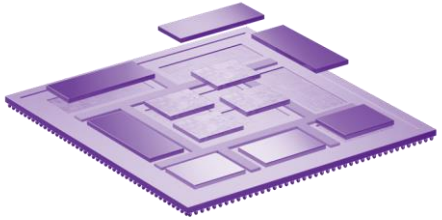


- Functional verification signoff with **ImperasDV & Valtrix STING**
- Fusion QuickStart Implementation Kit (QIK), & **reference flows for superior PPA**
- Synopsys **Cloud** offering

Accelerate SW Development w/HW

- Start SW development months before HW availability
- Avoid costly re-spins
- Actionable power profiling on full design & software workload

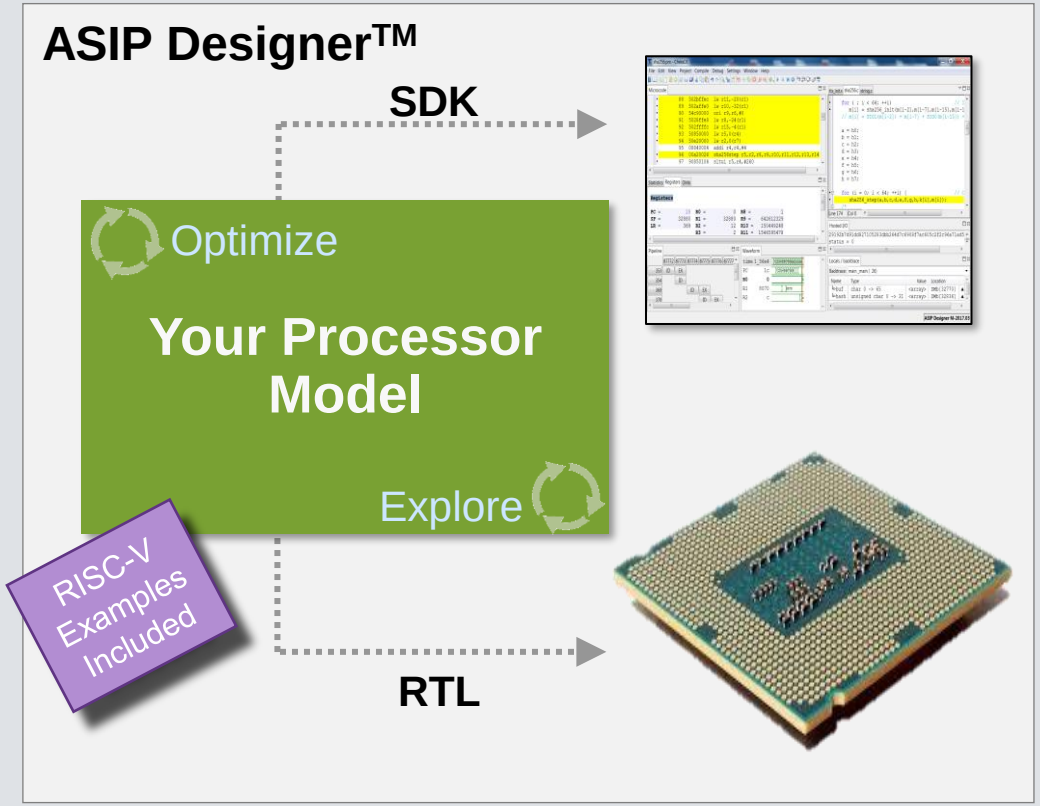
Broad Portfolio of IP



- **NEW ARC-V Processor IP** with robust SW dev toolkit
- Silicon-proven Interface IP minimizes risk
- High-speed, low-leakage & low-power Foundation IP optimizes PPA
- Efficient Security IP helps protect data

Synopsys ASIP Designer Automates Custom RISC-V Processor Design

Used by 7 of the Top 10 Semiconductor Developers



- Industry's leading tool for creating Application Specific Instruction set Processors (ASIPs)
  - Full architectural flexibility
  - Automatic generation of SDK, synthesizable RTL and debug infrastructure
  - Integrated with Synopsys' reference design flows
- 12 RISC-V example models included to accelerate productivity
  - 32-bit and 64-bit ISA models
  - Support for proprietary ISA extensions

Architectural Exploration through RTL Generation Enables PPA-Optimized Implementation

Synopsys Fusion QuickStart Implementation Kits (QIK) for RISC-V

Reference flows and guides to meet PPA targets faster

Synopsys Fusion QIKs

The fast path to best PPA

Flexible and complete implementation and static-verification flows

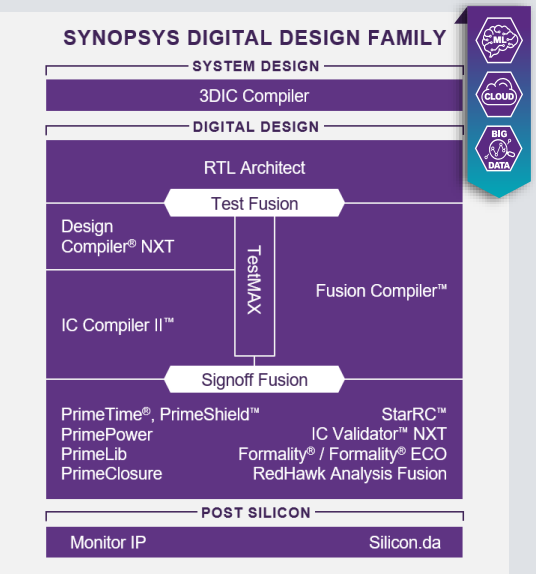
Available from Synopsys Solvnet

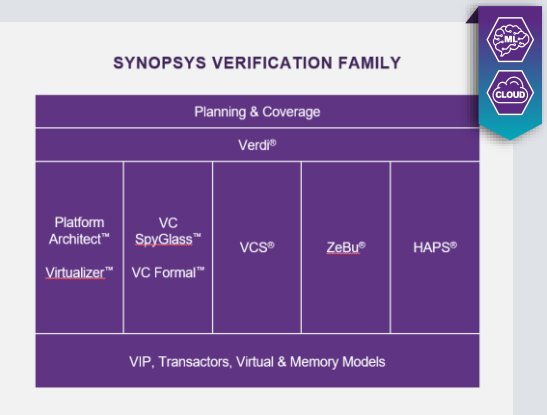
Delivers Native Out-of-the-Box PPA
Achieve PPA goals faster

Includes Recommended Flow and Scripts
Core configuration and constraints, RTL-to-GDSII implementation, ECO, signoff, formal verification

Easy to Customize
Core configuration, floorplan, technology library, PPA goals

Synopsys Implementation & Verification Solutions





- Co-development to achieve the **best Performance-per-Watt** with Fusion Compiler
- Focused on **differentiation** & **superior value** to RISC-V IP vendor & mutual customers
- Synopsys Fusion QuickStart Implementation Kit (QIK) to meet PPA targets using latest cores
- Best-in-class verification solutions and reference flows

Differentiated RISC-V Verification Solution

Formal Verification

VC Formal FPV + RISC-V ISA AIP
Functional Verification

VC Formal DPV
Verify computational correctness for RISC-V processors

VC Formal SEQ
Verify that custom instructions do not break the original core

VC Formal Apps Portfolio

Dynamic Verification

VC PS
Portable Stimulus

STING
RISC-V Test Generation

VSO.ai
Coverage Optimization

ImperasFPM
RISC-V Reference Model

ImperasFC
RISC-V ISA Functional Coverage

ImperasDV
Co-Simulation and Checking in Verification Environment

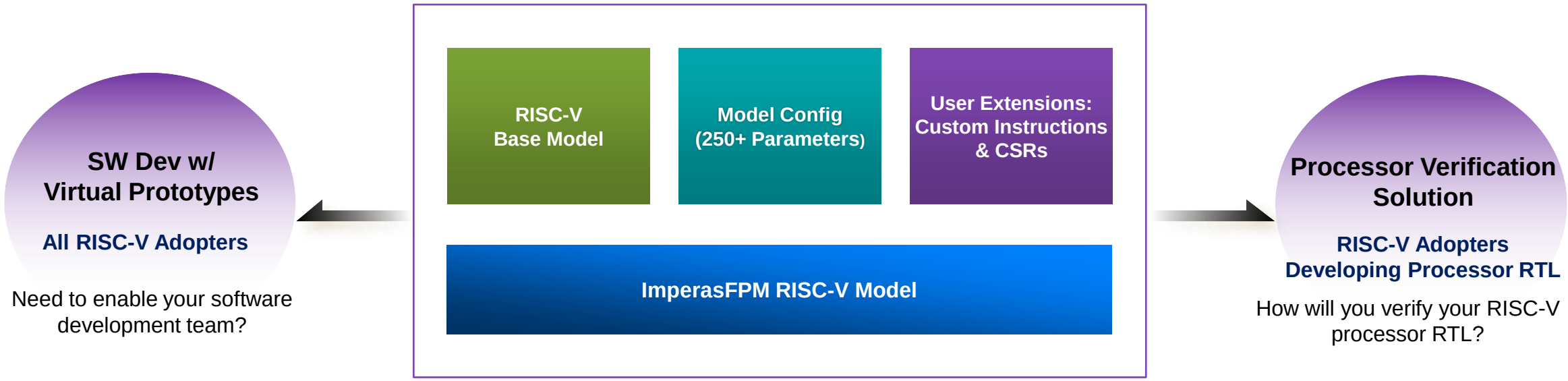
VCS & Verdi
Dynamic Sim, HW/SW Debug

ZeBu & HAPS
Hardware-assisted Verification

Verdi Verification Planning and Functional Coverage Platform

Fast Processor Models for RISC-V: ImperasFPMs

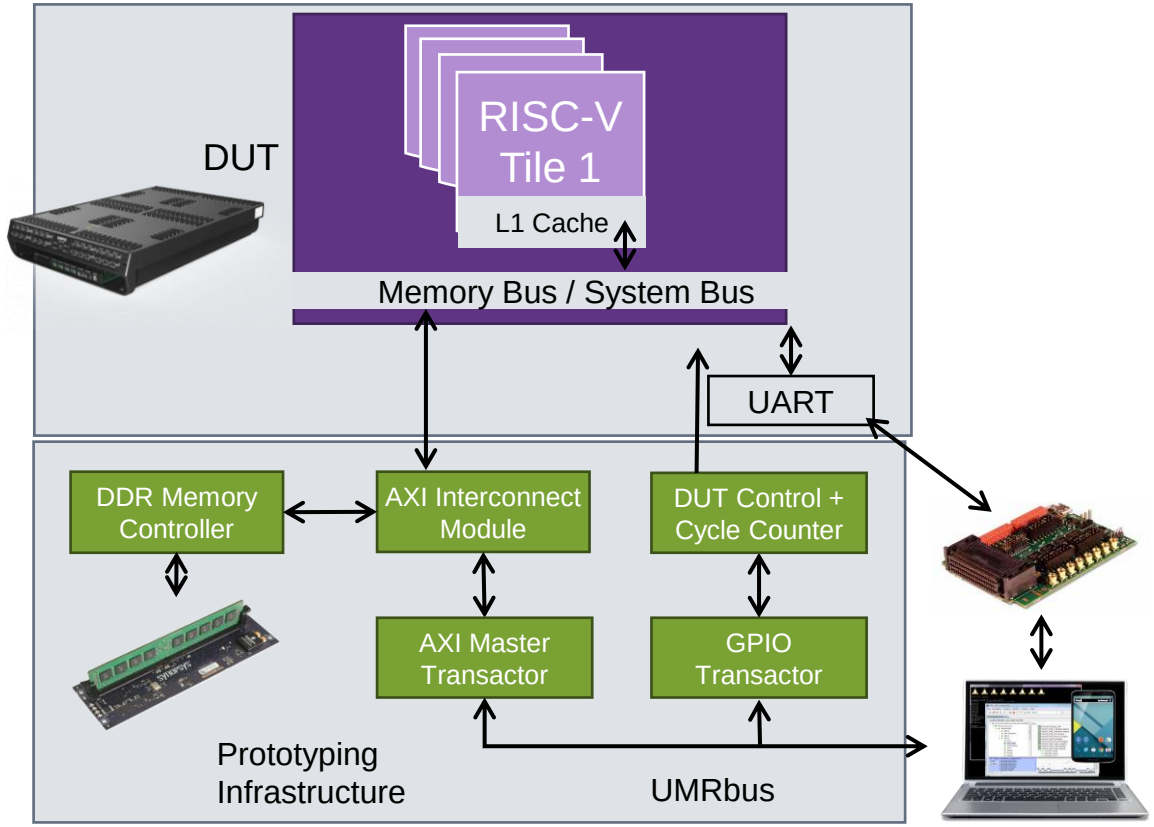
Use Cases: Software Development and RISC-V Processor Verification



Using the same model for both hardware and software verification enables significant reduction in SoC bring up time

Speeding Emulation and Prototyping for RISC-V Processors

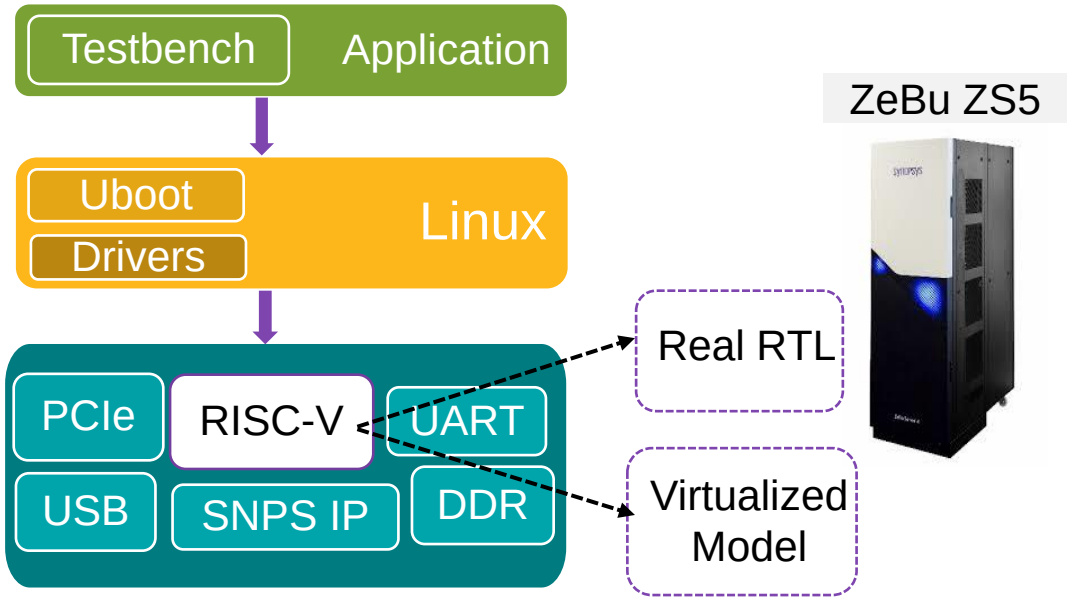
HAPS-100 Prototyping Solution



HW/SW debug with real ASIC | Unified RTL debug with Verdi |

4 RISC-V embedded cores running at 100MHz in one FPGA

ZeBu Emulation

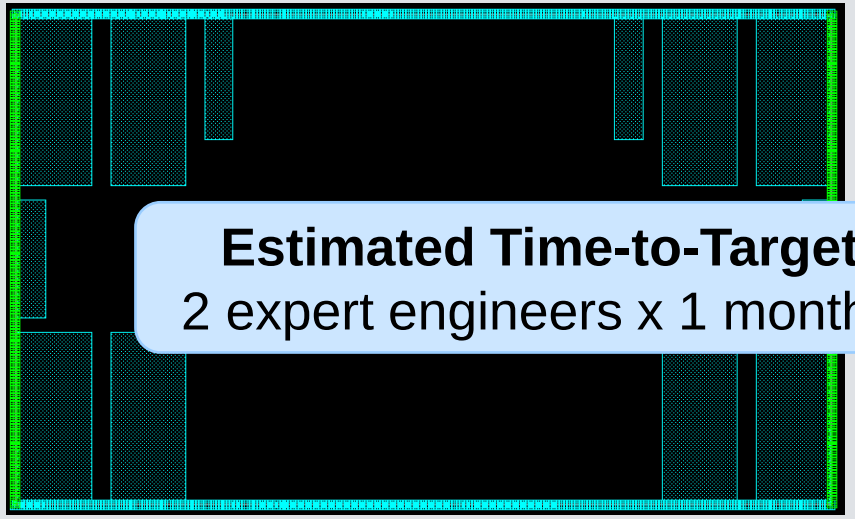


Emulation Bring-Up and Software Stack

Case Study: RISC-V High Performance CPU Core

AI-driven Optimization Results for Superior PPA

- RISC-V based “Big Core” targeted for data center applications
- Size: 426um x 255um (single core only)
- Technology process: 5nm

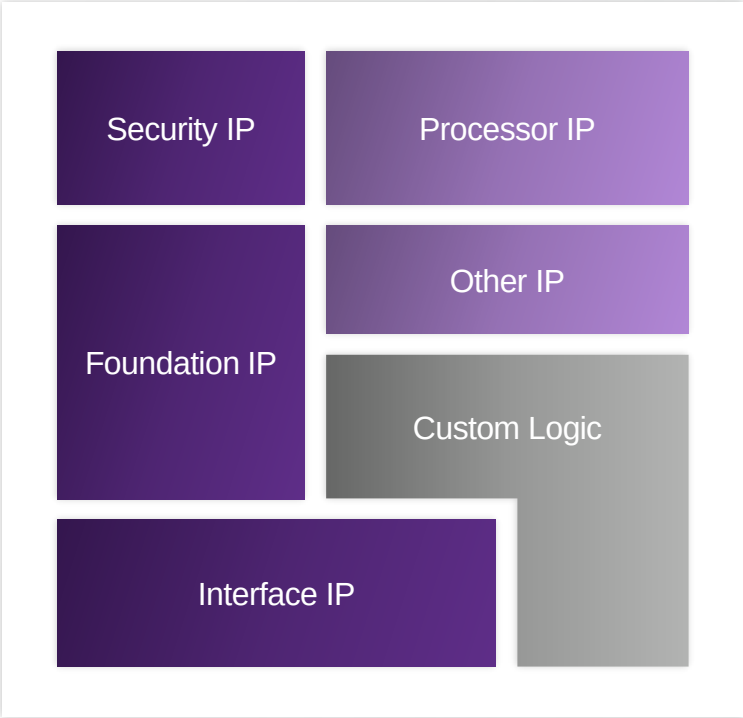


Estimated Time-to-Target
2 expert engineers x 1 months

	Perf.	Power	Area
Target User Expectation	1.95Ghz	30mW	MET
Baseline OOTB RISC-V Reference Flow	1.75Ghz	29.8mW	MET
DSO.ai AI-Driven RISC-V Reference Flow	**1.95Ghz**	**27.9mW**	**MET**

AI **2 days, 0 human!**

Broadest IP Portfolio



25 years of investment & commitment

#2 IP provider worldwide

Leader in Interface IP

Leader in Foundation IP

Growing Processor IP portfolio with ARC® -V

Reduce design risk and speed time-to-market with high-quality IP

Comprehensive End-to-End Design Solutions & Services

Spec-to-GDSII system solutions including MSP collaboration for GDSII-to-Parts

Synopsys

System Solutions Platform

Perf & Power Architecture

RTL & Verification

R2G Implement

Verify & Sign-off

Hardware / Software Co-design & Verification

IP & Subsystem Design

Virtual Prototyping & Emulation

Engineering Samples Silicon Bring-up

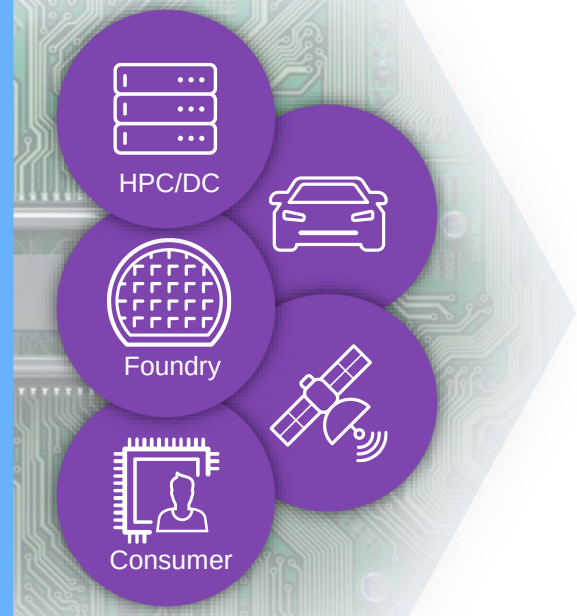
AI/ML (DSO.ai), Safety (FuSa), Reliability & Security (SLM)

Design Methodology & Flows

Supply Chain Ecosystem Partners

Silicon Manufacturing (Foundry)

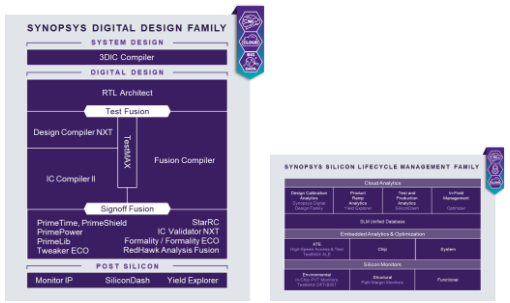
Package Design Analysis, Assembly & Test



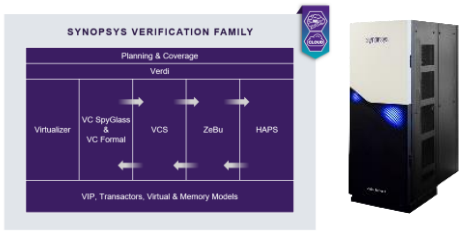
Program Management Office

Broad market verticals with segment specific needs

Synopsys Uniquely Positioned to Enable RISC-V Designs



Digital Families



High-Performance Verification

Silicon-proven I/F IP and ARC-V Processor IP

Co-optimized to drive next-level PPA & SLM

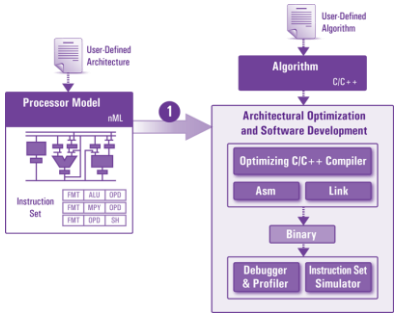
Custom core design & architectural exploration

SYNOPSYS®

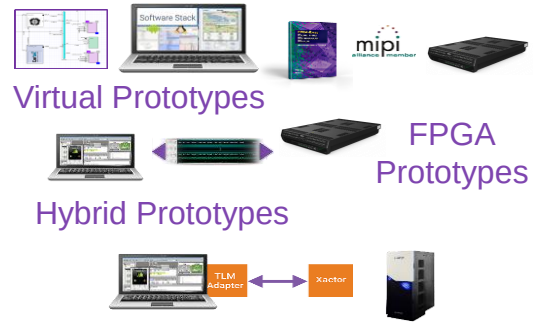
Simulation, debug & HW-assisted verification

Early software development, architecture design, SW/HW validation

Design Services



ASIP Designer



Virtual Prototypes

FPGA Prototypes

Hybrid Prototypes

Hybrid Emulation

Synopsys Sessions and Booth

Session: Creating Custom RISC-V Processors Using ASIP Design Tools: A Post-Quantum Cryptography Case Study

DATE: 08/22 11:20-11:40

Session: Addressing Real-Time Workloads in Automotive Applications with Efficient ARC-V Processors

DATE: 08/22 15:30-15:40

Session: 5 levels of RISC-V Processor Verification

DATE: 08/23 15:10-15:20

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Our Technology
Your Innovation