RISC-V Architectures for High-integrity Feature-Rich Automotive Applications

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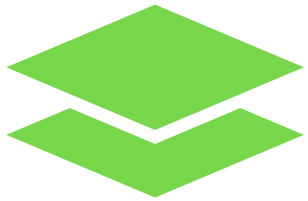
Agenda

RISC-V + PowerVR: The flexible, scalable, compute platform of choice for high-integrity feature-rich applications



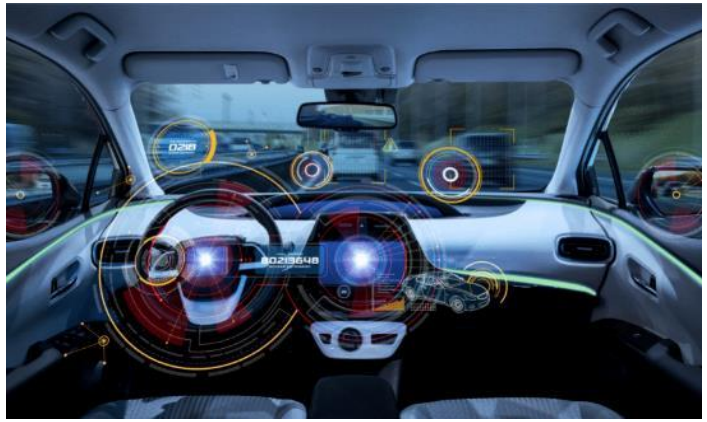
The Challenge

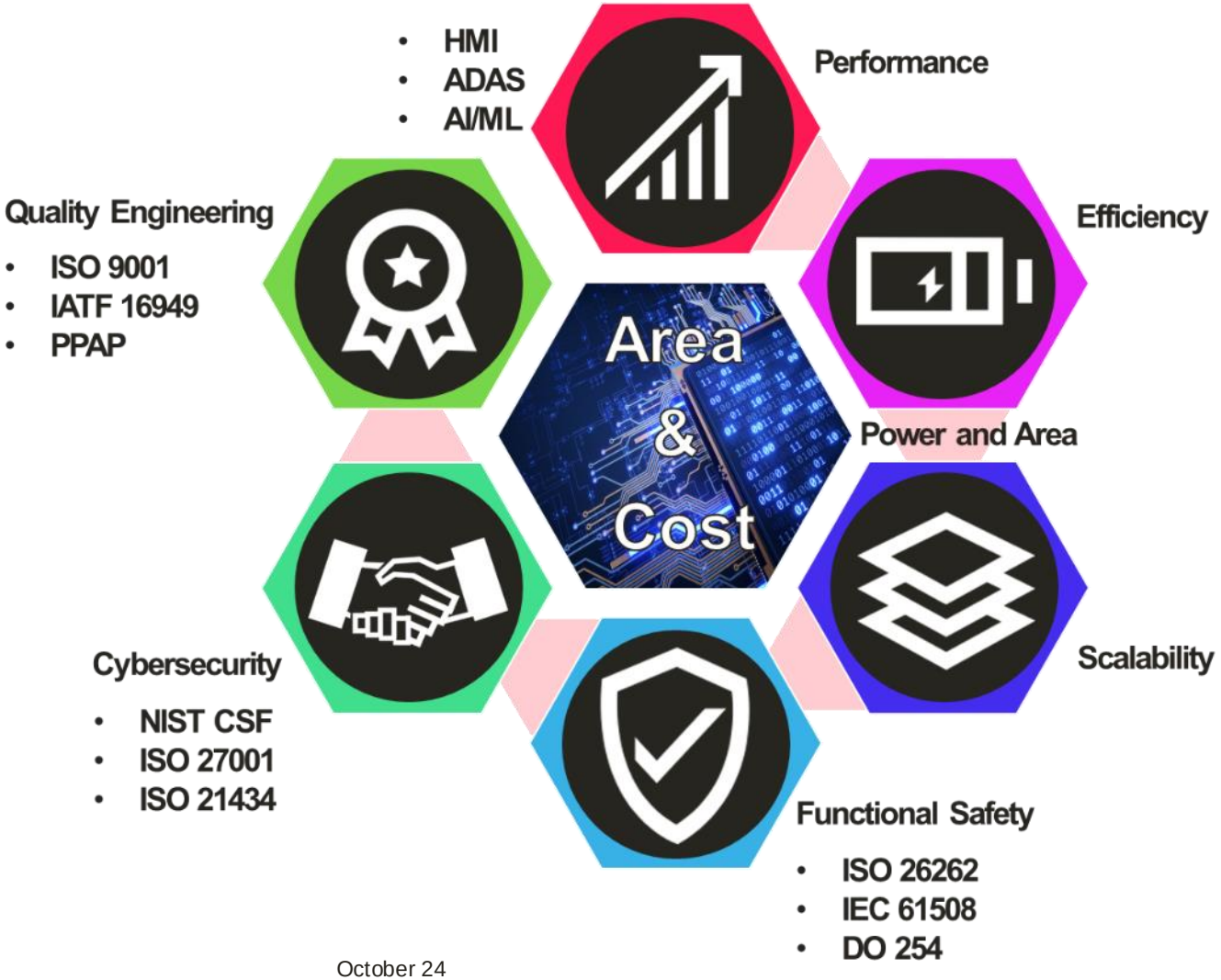
Finding the Right Balance

The Solution

The Challenge…

Complex Software Intensive Systems





Finding the Right Balance…

Quality by Design: World class semiconductor IP development lifecycle processes

✓ ISO 9001 ✓ IATF 16949 ✓ ISO 15288 ✓ ISO 26262 ✓ ISO 21434 ✓ Staged & Gated Dev Process ✓ V-Lifecycle

✓ Embedded a Systems Engineering approach to development and management of complexity

Strong heritage in CPU and GPU development including for Automotive applications

ISO 26262 *ASIL-D Systematic Development Process Certified*

Since 1995… | Series 8 | A series | C Series | …Future

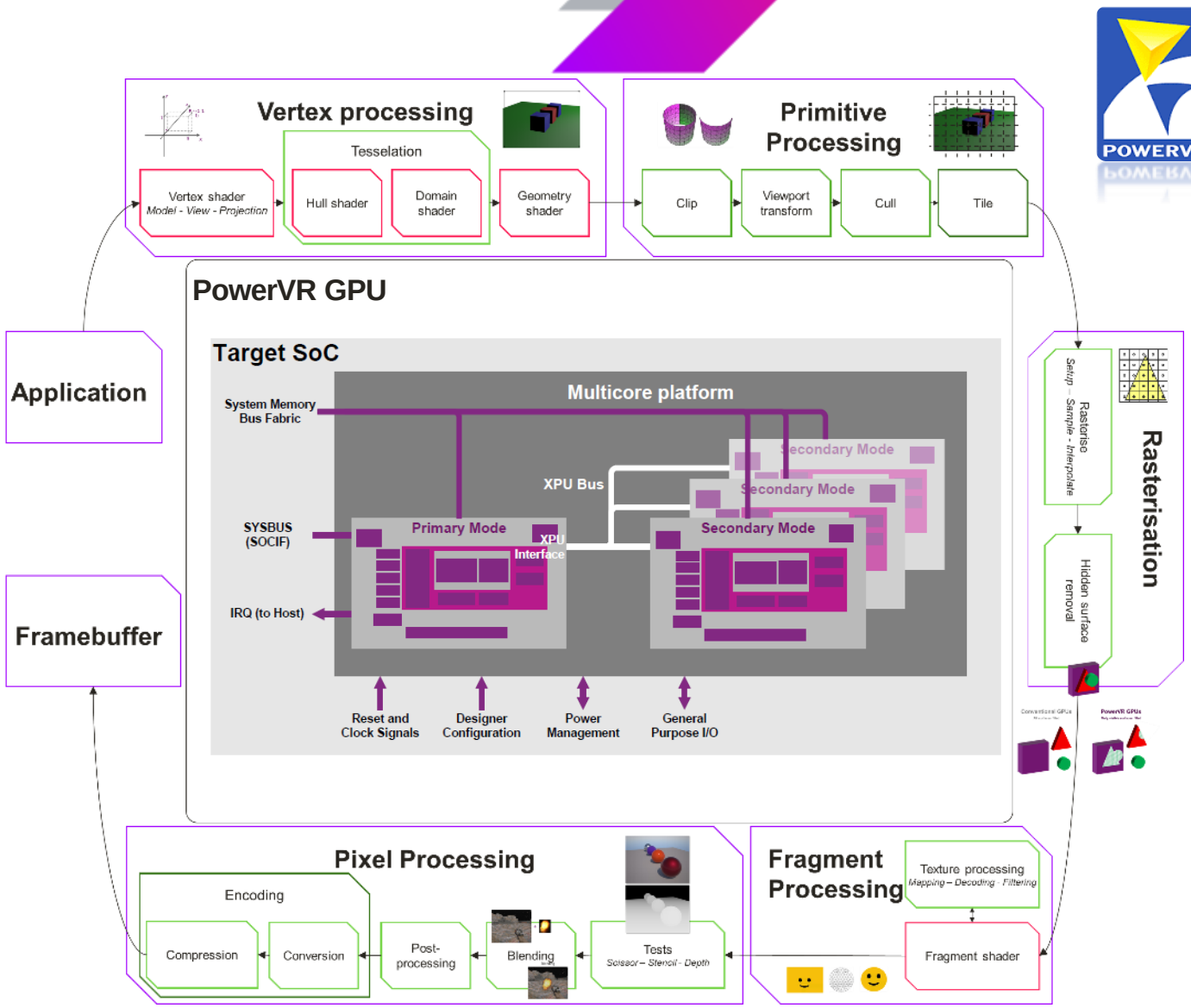
Series 7 | Series 9 | B Series *BXS* *ASIL-B HW* | D Series *DXS* *ASIL-B HW*

The Solution

Integrated Graphics & Compute Processing

- **High Performance**
- **Tile Based Rendering**

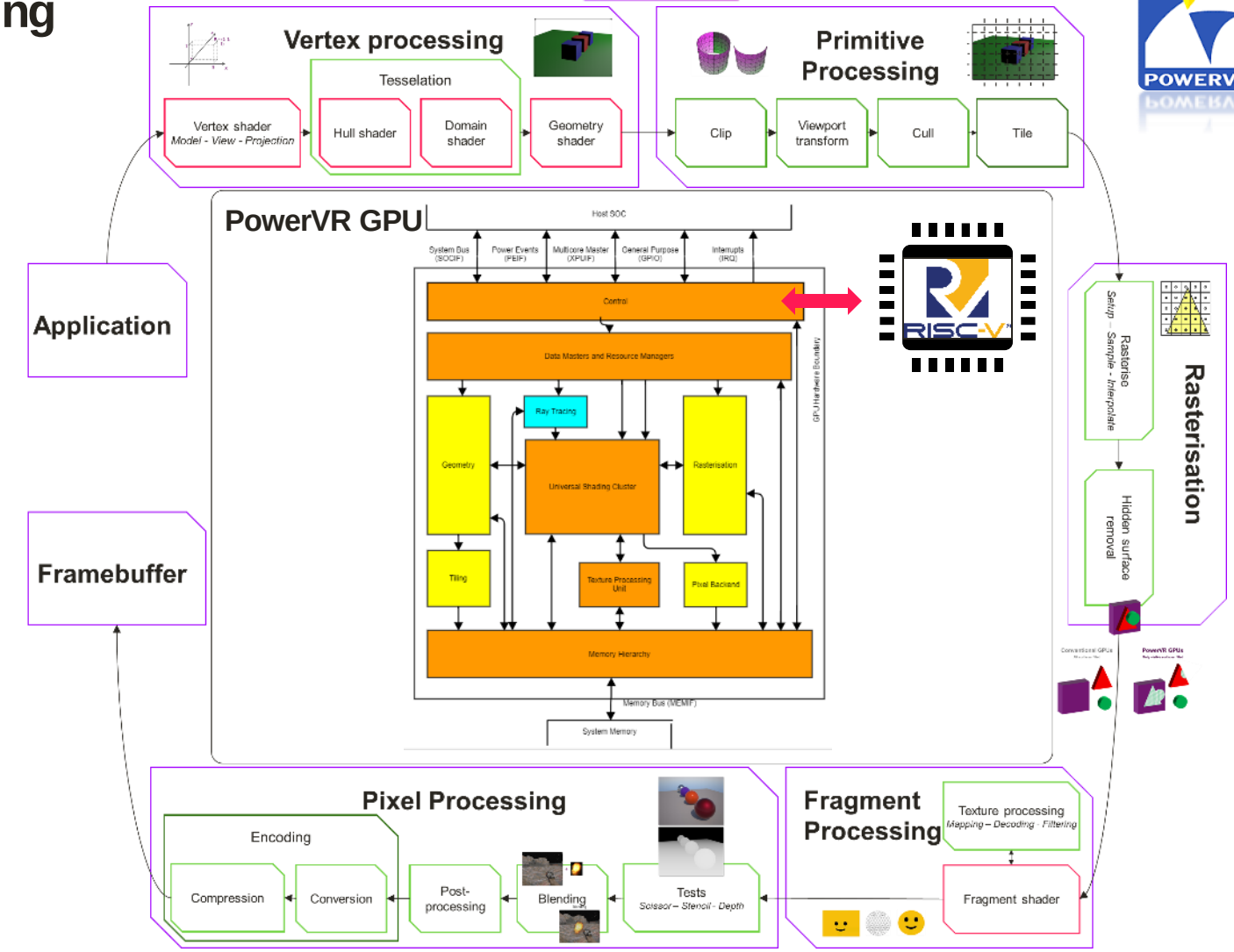
- **Hardware enabled Raytracing**
- **Efficient**
- **Scalable**
  - Core - Multicore Variants available (e.g. MC1-4)
  - SPU (Scalable Processing Unit)
  - Cluster



Integrated Graphics & Compute Processing

Simplified GPU Subsystem view

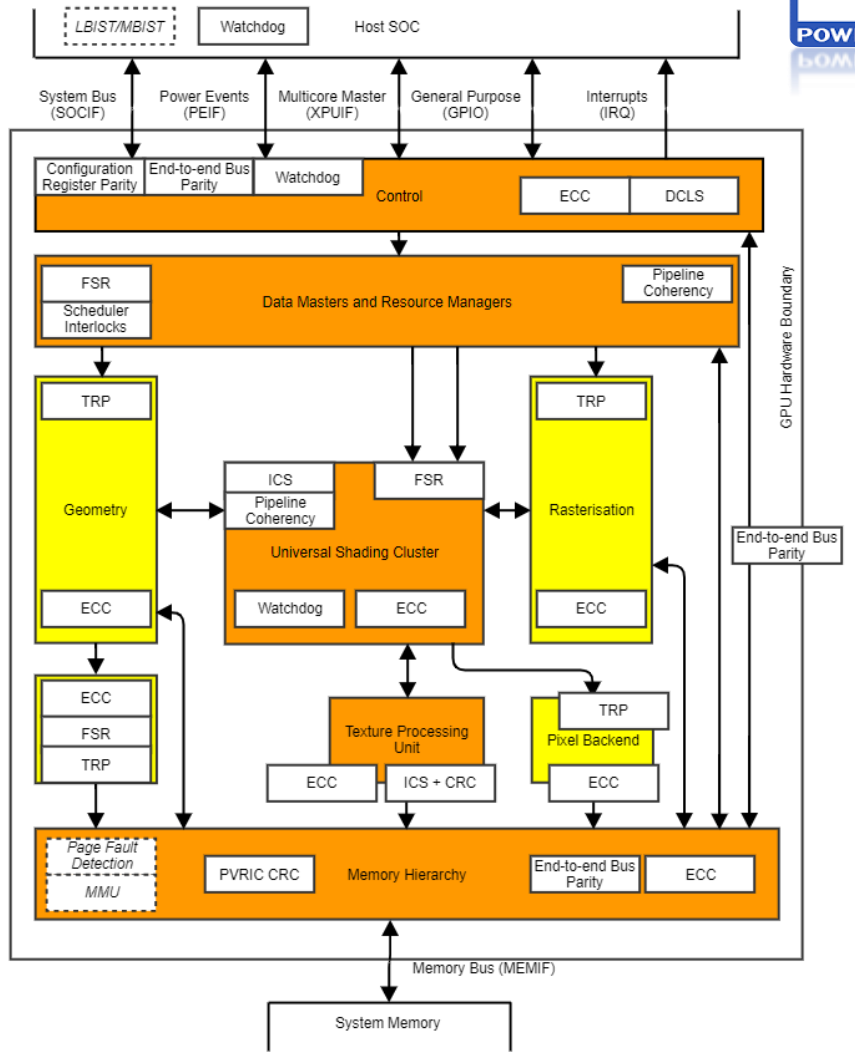
- **10 Subsystems in total**
  - Coupling and Binding
  - QFD
- **5x Subsystems support Compute & Graphics**
- **5x Graphics-only Subsystems**
- **Control Subsystem inclusive of RISC-V FW CPU**
- **'Compute-only' GPU variants are available**



Distributed Safety Architecture Summary

Requirements → Analysis → Design → Verification of Safety Performance

- **PHA**
  - Vehicle/Item level analysis to validate AoUs and target ASIL
- **FMEAs**
  - FMEAs across top-level/systems and all Subsystems
  - > 4000 failure modes analysed
- **FTA**
  - Fault tree construct from System, Subsystem, Module and Submodule, including Safety Mechanisms
- **DFA**
  - Cardinal DFIs considered across System, Subsystem, Structural (Multicore and Internal Core Hierarchy)
- **Fault Injection Campaign**
  - Safety Mechanisms inc verification of SM DC/performance
- **FMEDA**
  - ASIL-B achieved: DSMs only: > 90% SPFM, > 70% LFM.
  - ASIL-C achieved: DSMs + TRP/WGP: > 97 % SPFM, > 80% LFM.

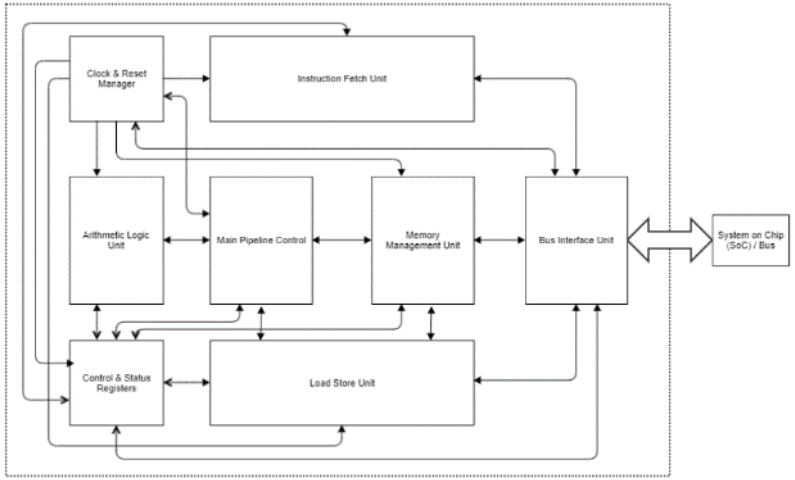


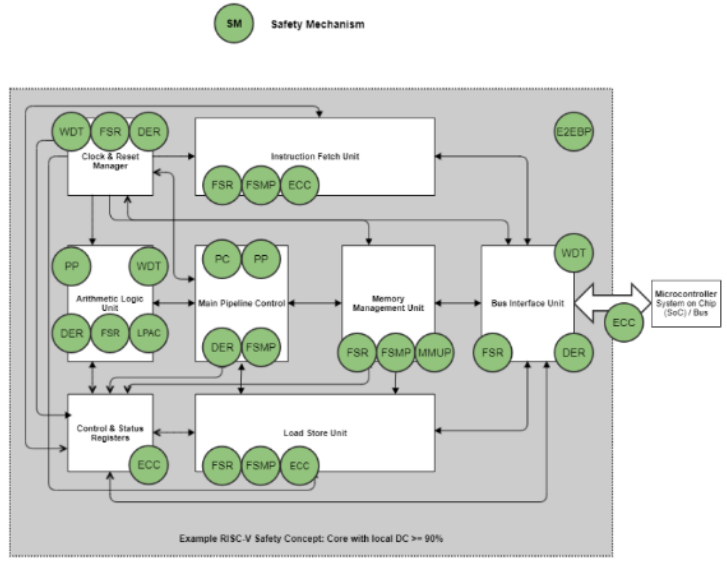
ASIL-B Distributed Safety with Defence-in-Depth Safety Mechanisms

Safety Architecture Summary (Firmware CPU)

Simplified Subsystem View

Same process applied at GPU level applied to CPU:





A generic Pipelined CPU architecture

ASIL-B Distributed Safety with Defence-in-Depth Safety Mechanisms

Results

IMG Distributed Safety Architecture (DSA) – Performance relative to a Non-safety equivalent IP (Generalised)

IP	Configuration	Area overhead	Performance delay	Power penalty	DC
RISC-V CPU	Non-safety	1	No delay	1	0 %
	DCLS	~1.75x	~1x	~1.75x	> 90 %
	IMG DSA	**~1.15x**	**~1.02x**	**~1.15x**	
PowerVR GPU	Non-safety	1	No delay	1	0 %
	DCLS	~1.75x	~1x	~1.75x	> 90 %
	IMG TRP/WGP MC1	~1.15x	~1.9x	~1.15x	
	IMG TRP/WGP MC2+	~1.8x	~1x	~1.8x	
	IMG DSA	**~1.20x**	**~1.02x**	**~1.20x**	

Summary & Conclusions

+

= A high performance Compute platform
= Gamechanger for AI and Graphics

+ Novel Safety Architecture = ASIL qualified

- PowerVR is a good match for RISC-V platforms – low in area and high in performance
  - 2x bus utilisation when used with IMG's own APXM-6600 Host CPU
  - Best-in-class performance density

- > ASIL-B metrics achieved per Core with IMG's Distributed Safety Architecture and novel safety mechanisms
  - Intrinsically Safe hardware – closely-coupled distributed safety mechanism approach with Defence-in-Depth: Scalable Safety
  - No complex or convoluted Software Test Libraries (STLs) needed
  - No performance hogging run-time LBIST needed (remains supported)

- All major APIs supported: Vulkan, Vulkan SC, and OpenGL and OpenCL
  - A safe and robust enabling AI/ML platform for advanced use-cases such as L3+ ADAS

Thank you

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