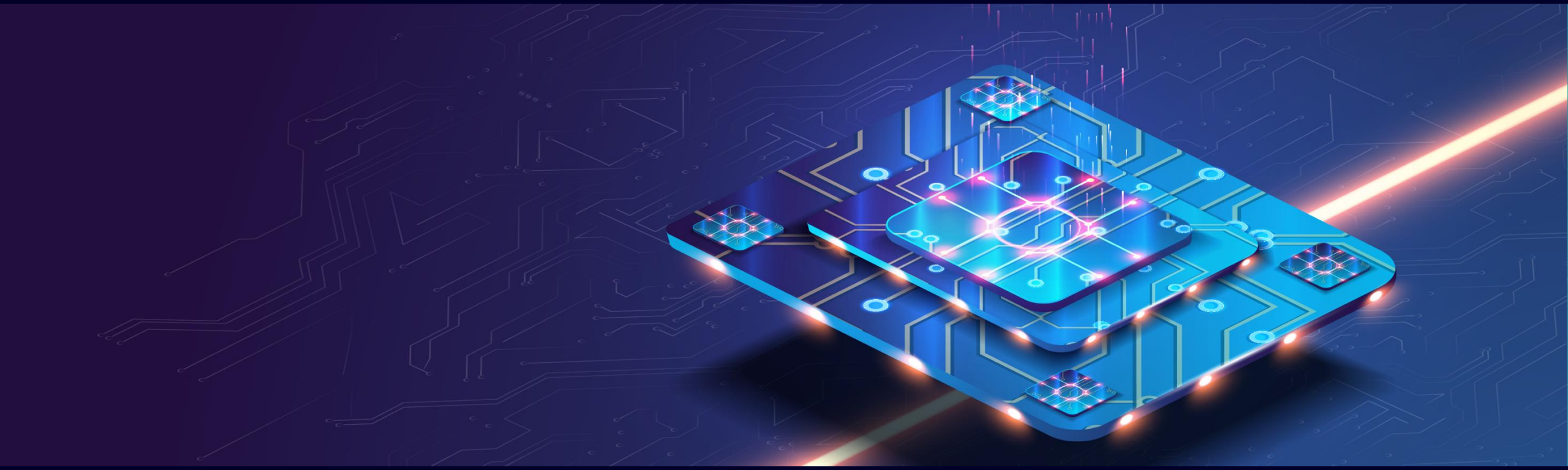

Leveraging the RISC-V Efficient Trace (E-Trace) Standard

Yifan Li, Account Technology Manager, Tessent Embedded Analytics & DFT

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Agenda

- Why Trace?
- Trace Basics
- E-Trace standard
- E-Trace IP by Siemens
- Summary

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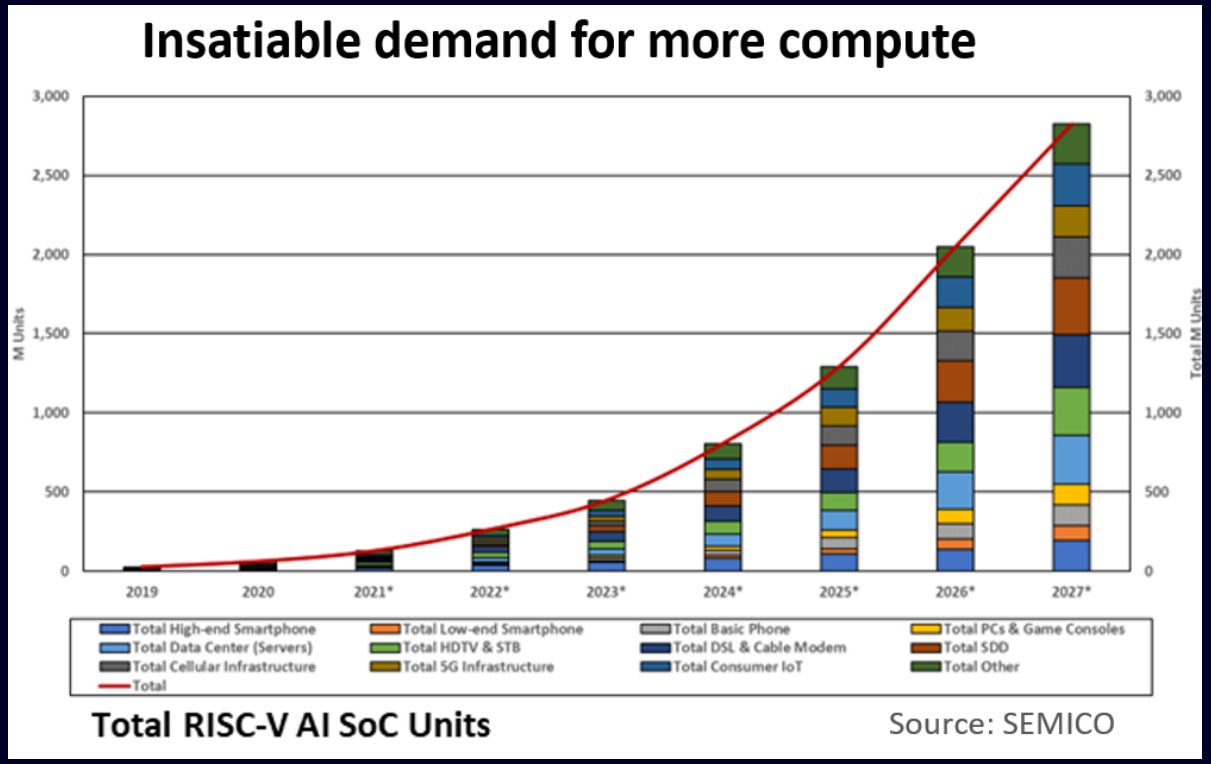
Insatiable demand for more compute



Total RISC-V AI SoC Units Source: SEMICO

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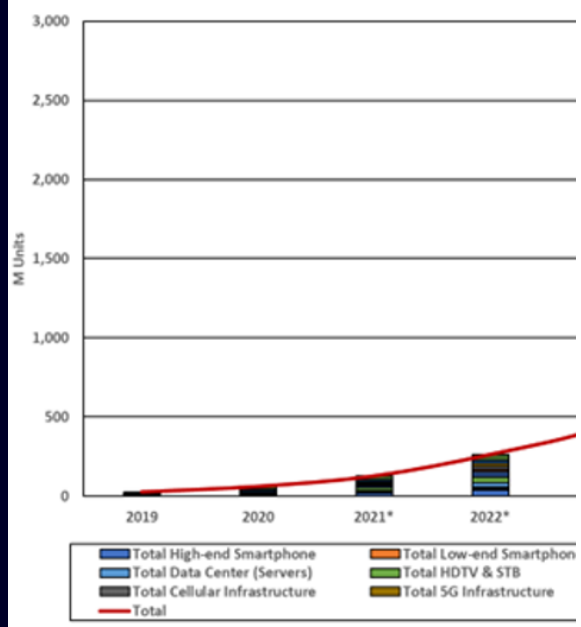
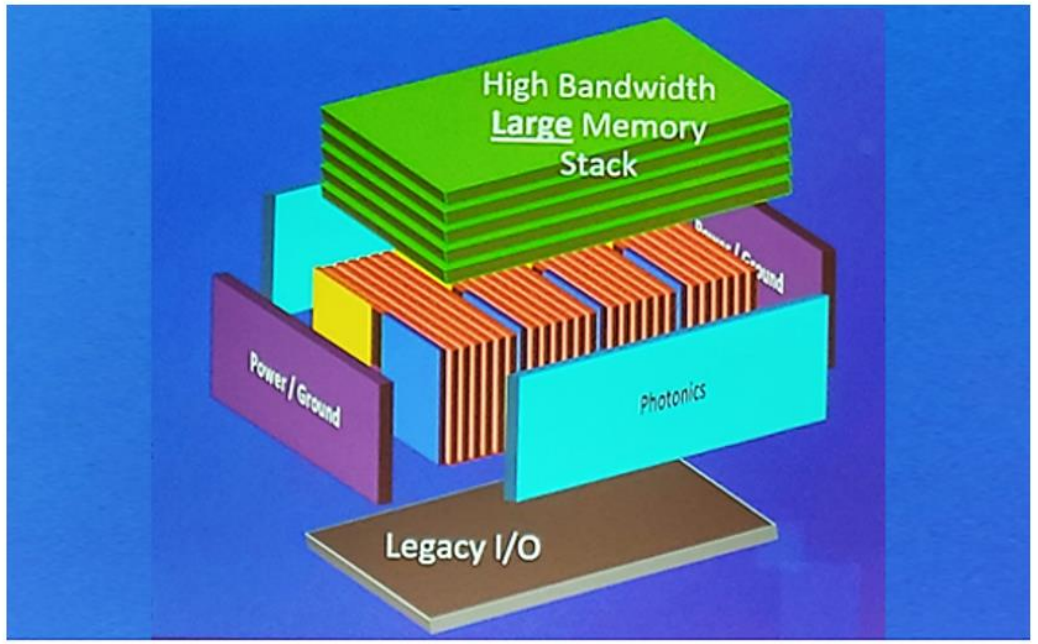
Insatiable demand for more compute



Total RISC-V AI SoC Units

Exponential increase in design complexities



Source: Joshua Fryman, Intel Fellow at ERI Summit 2023

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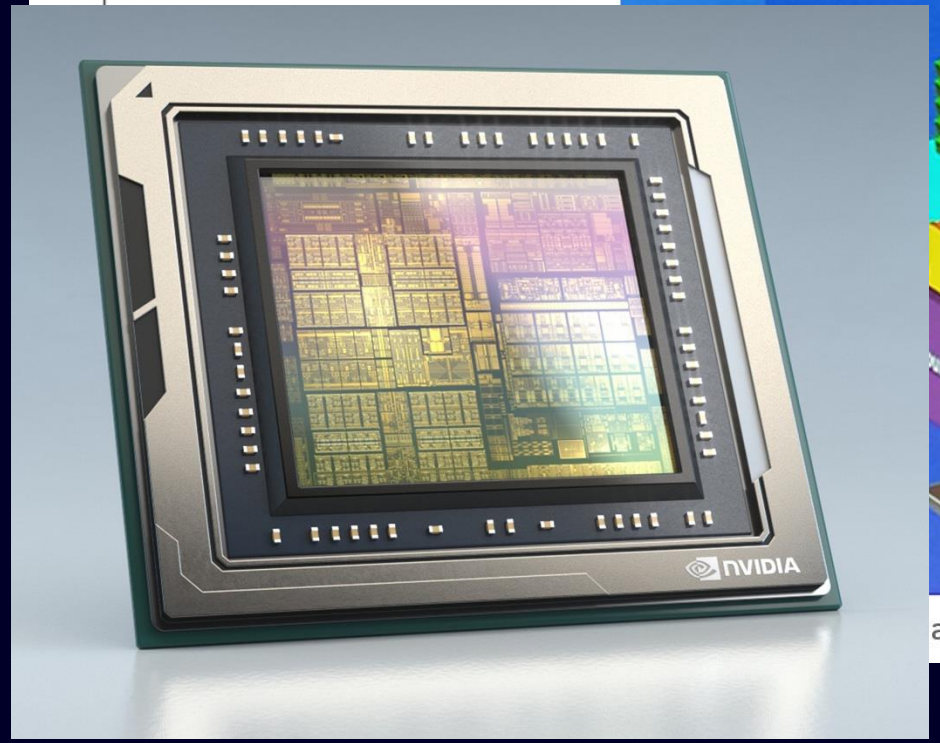
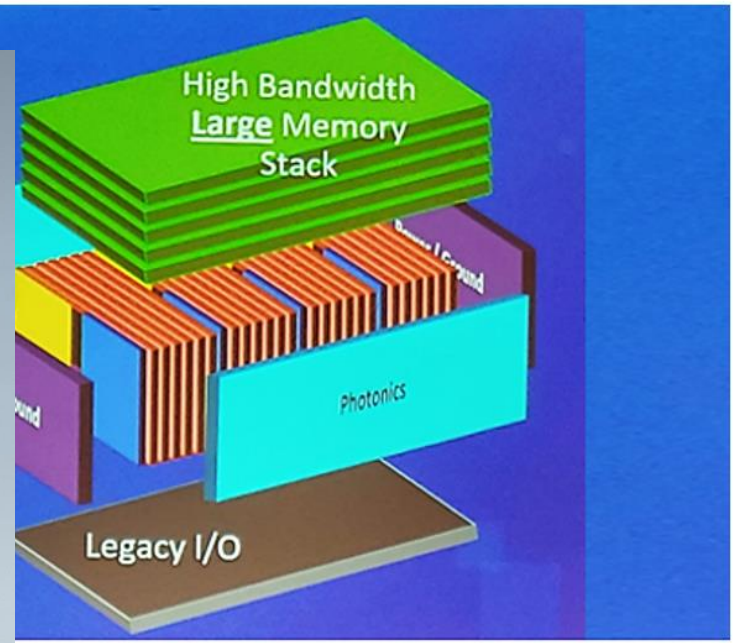
Insatiable demand for more compute

3,000

2,500

Exponential increase in design complexities





a Fryman, Intel Fellow at ERI Summit 2023

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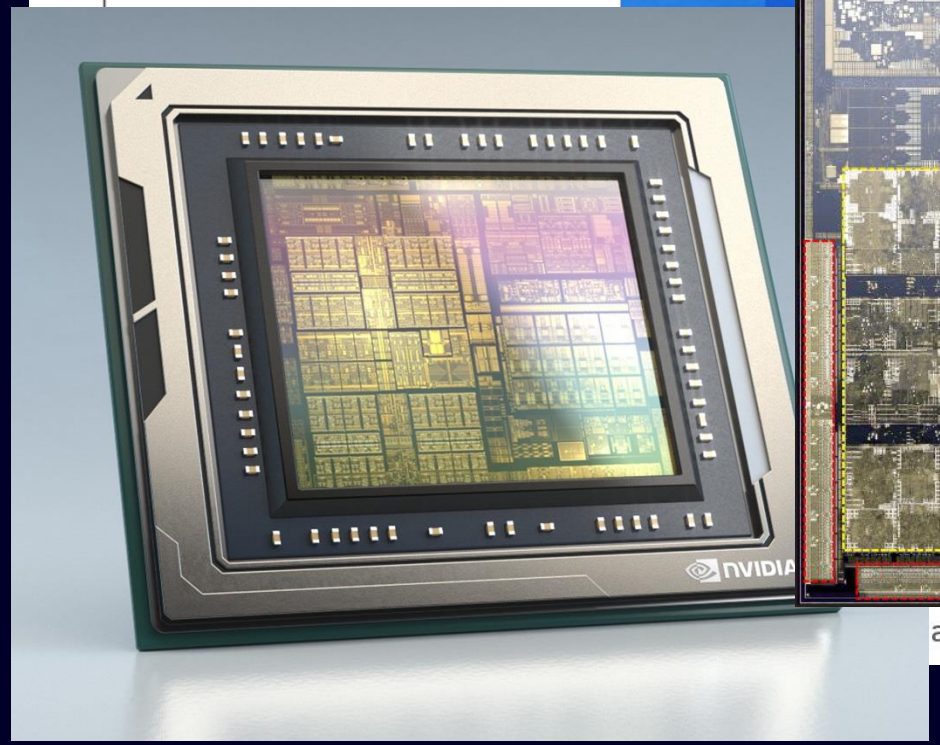
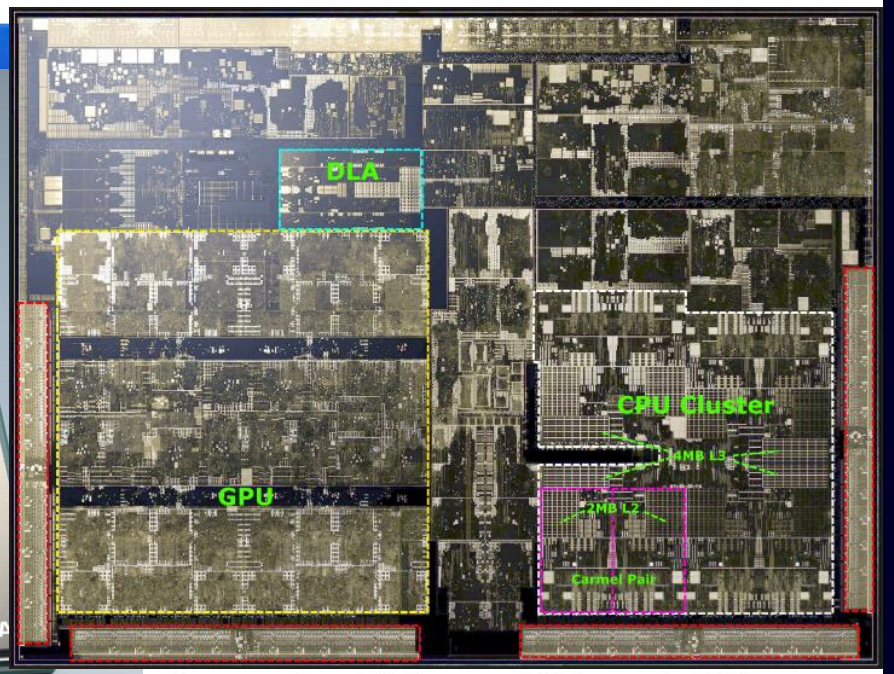
Insatiable demand for more compute

Exponential increase in design complexities





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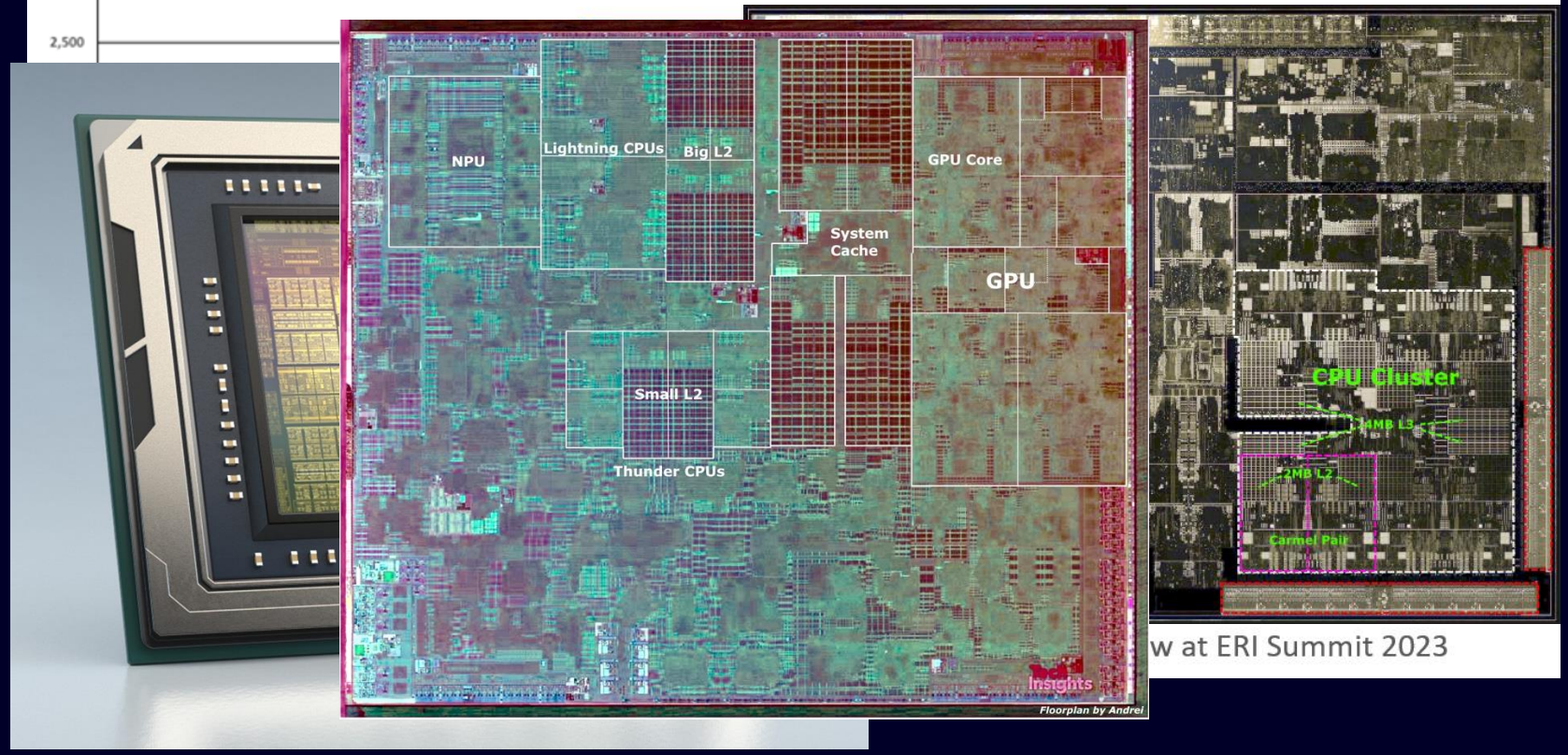

w at ERI Summit 2023

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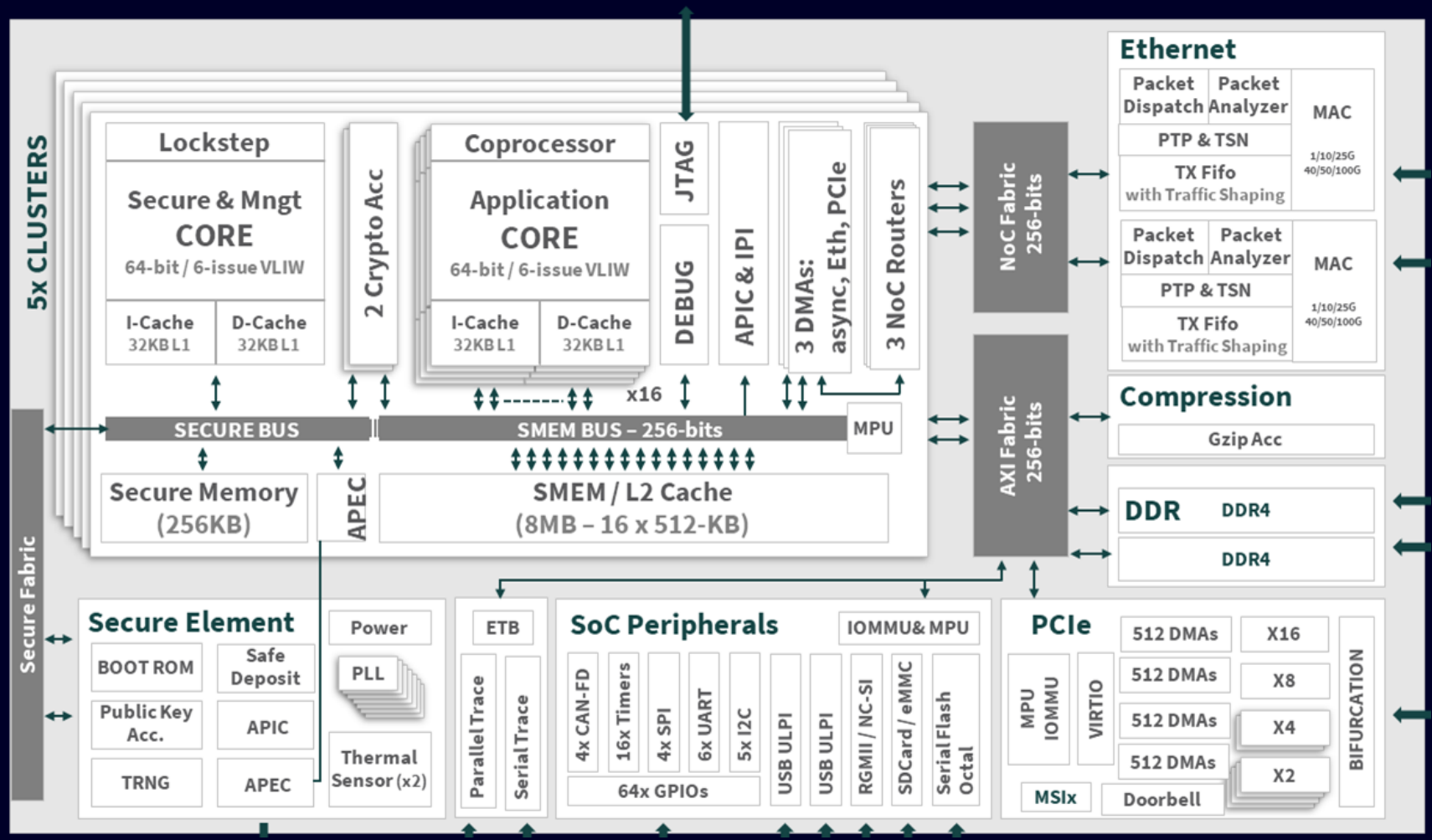
Why Trace?



complex designs **complex software** **real-time events** **CPU-CPU interactions**

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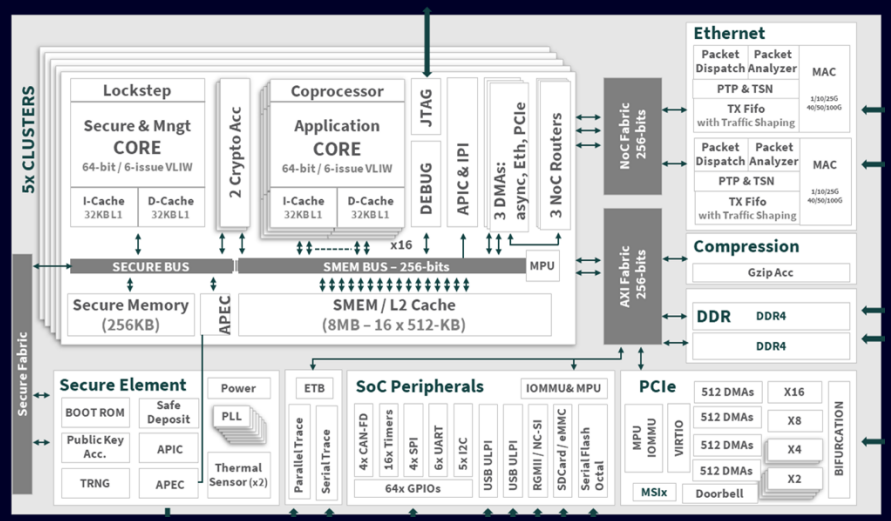
How is trace commonly implemented?

A debugging technique where executed instructions are compressed and transmitted to enable reconstruction of the exact program execution sequence



Forensic debugging **Code profiling** **Code coverage** **Heisenbugs** **Infrequent bugs**

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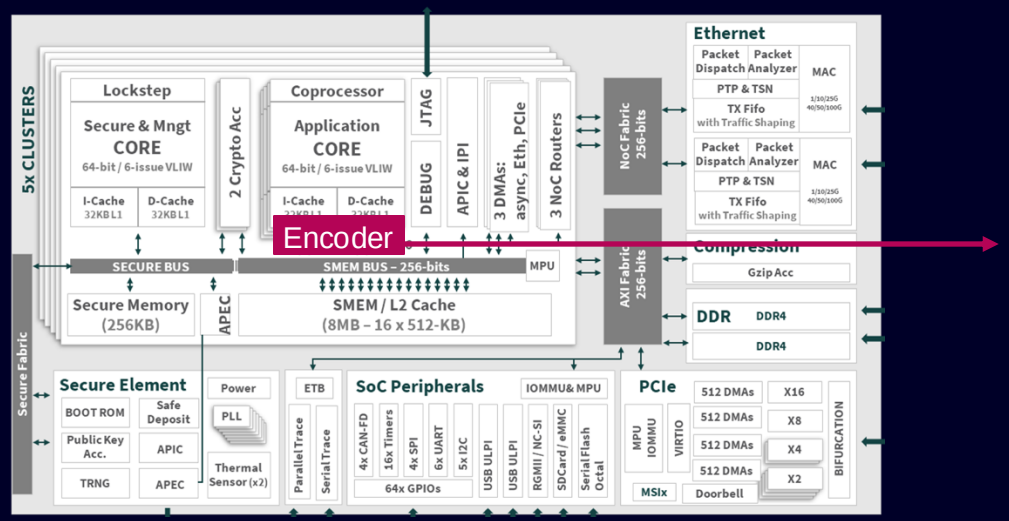

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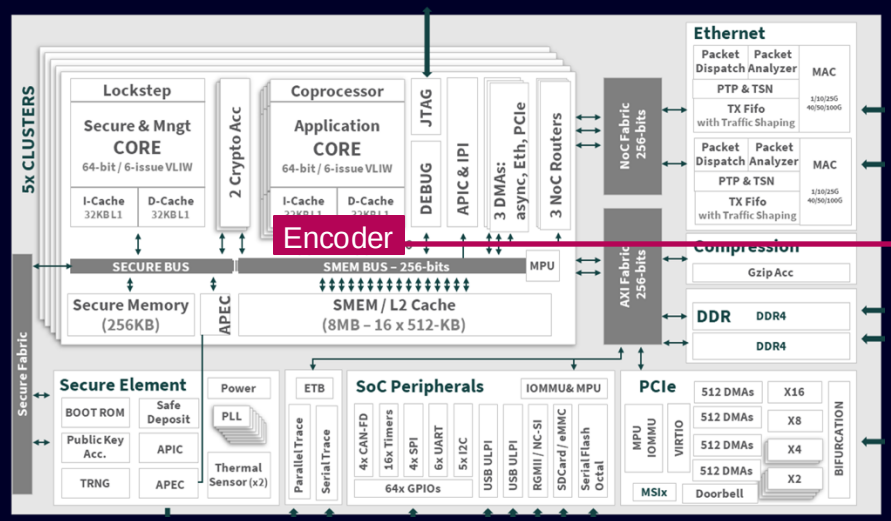
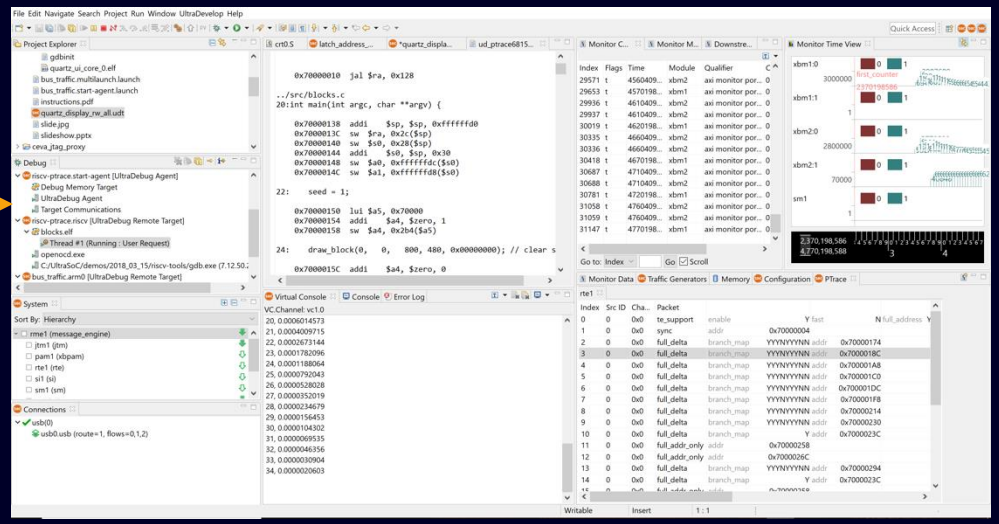


Host Software

Decoder



Forensic debugging **Code profiling** **Code coverage** **Heisenbugs** **Infrequent bugs**

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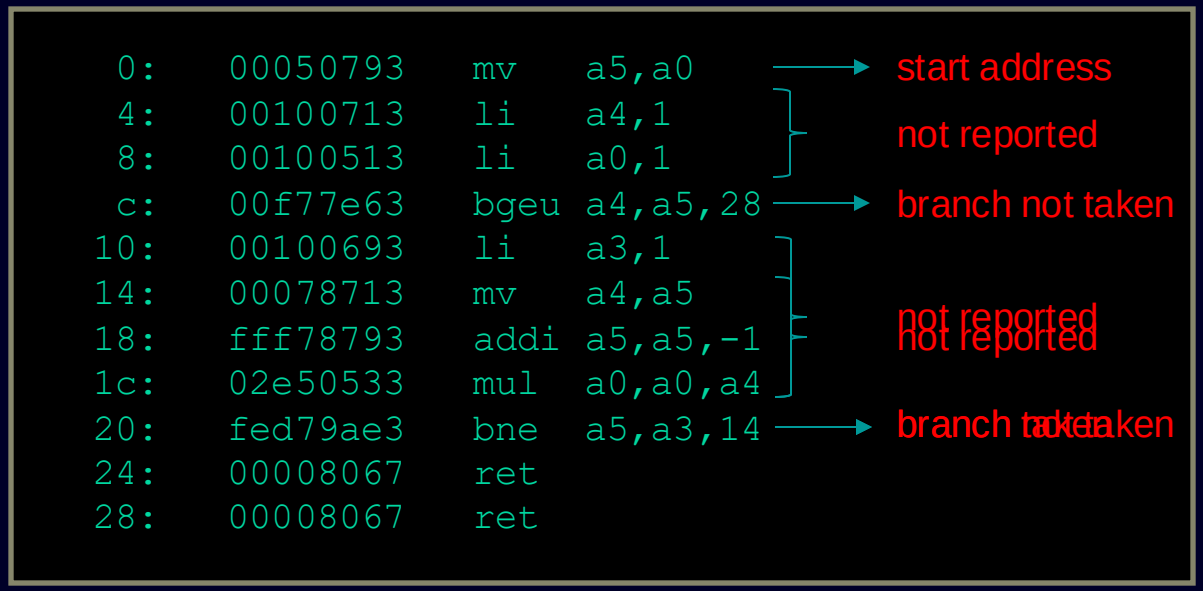
Processor Branch Trace

- Only branches are reported: jump, call, return, interrupt, exception
- Sequential Instructions are not reported
- Achieves very high compression → Trace more & avoid trace loss
  - Trace begins by reporting the start address
  - Indirect jumps, interrupts and exceptions
    - or “Un-inferable program counter discontinuities”
    - The destination address must be reported
    - Interrupts must also report PC at time of interrupt
- E-Trace defines additional optional instruction trace modes
  - even higher compression
  - debugging aids for software decoder developers
- Data Trace
  - Where data (and address) of load and store operations are reported



Branch Trace Log

1. start address
2. branch not taken
3. branch taken
4. branch not taken

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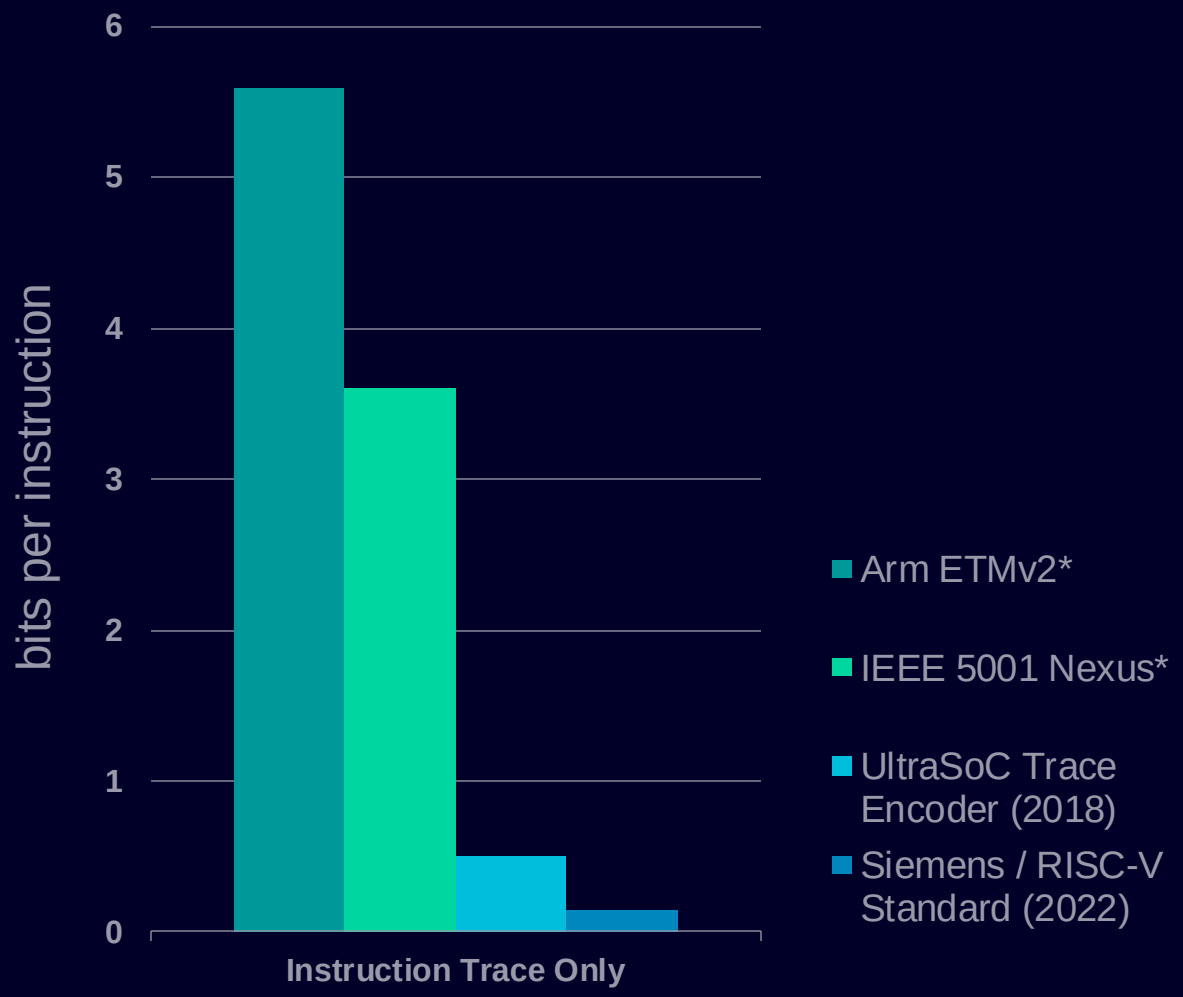
How does the RISC-V Efficient Trace standard compare?



- Higher compression enables
  - Trace longer
  - Trace faster
  - Trace more
  - Less bandwidth

*data taken from https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=4291979

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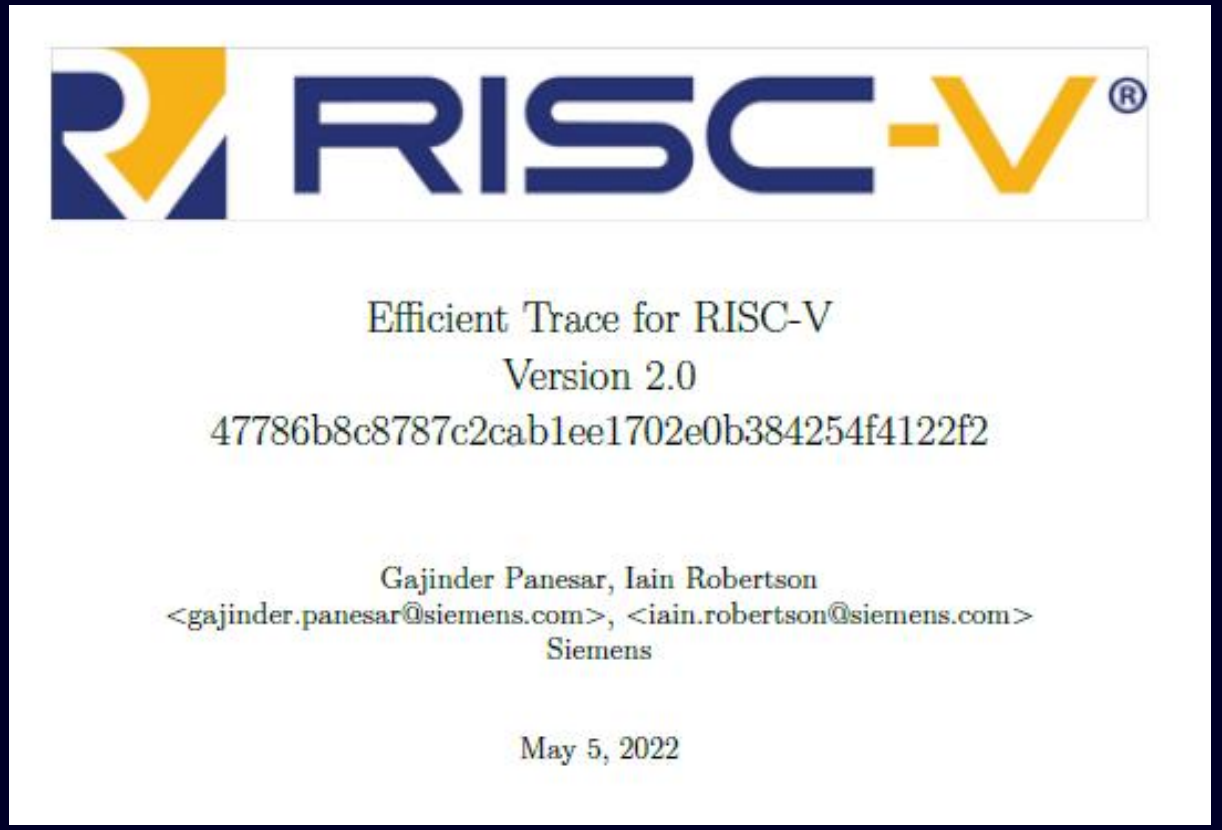
RISC-V E-Trace Standard

- A successful debug and trace ecosystem requires partners working together on a common set of standards
- ***The Efficient Trace for RISC-V*** standard covers encoding of instruction and data trace, as well as a standard CPU core to trace encoder hardware interface
- Originally donated by Siemens, the specification was refined by the community and ratified by RISC-V International
- https://github.com/riscv-non-isa/riscv-trace-spec



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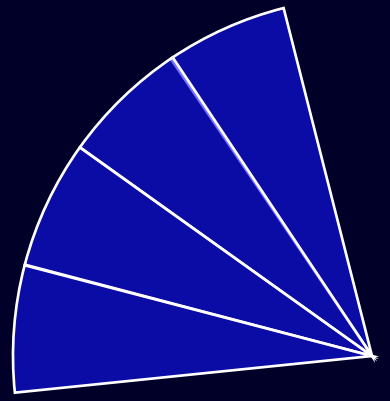
E-Trace Features – Standard and Beyond

RISC-V Trace mandatory features

- Instruction trace
- Hart (CPU) to encoder interface
- ‘Delta Address’ trace mode
- Efficient packet format



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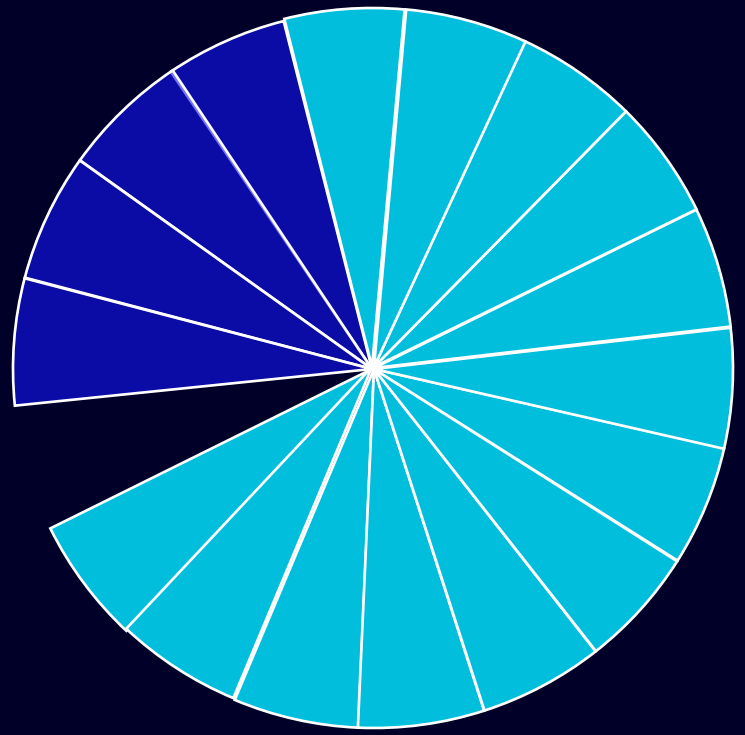

RISC-V Trace optional features

- Multiple instruction retirement
- Data Trace
- Implicit exception mode
- Sequentially inferable jump mode
- Implicit return mode
- Branch Prediction mode
- Jump Target Cache mode
- Full Address mode
- Sign-based compression
- XOR data trace compression
- Differential data trace compression
- Filtering
- Timestamps

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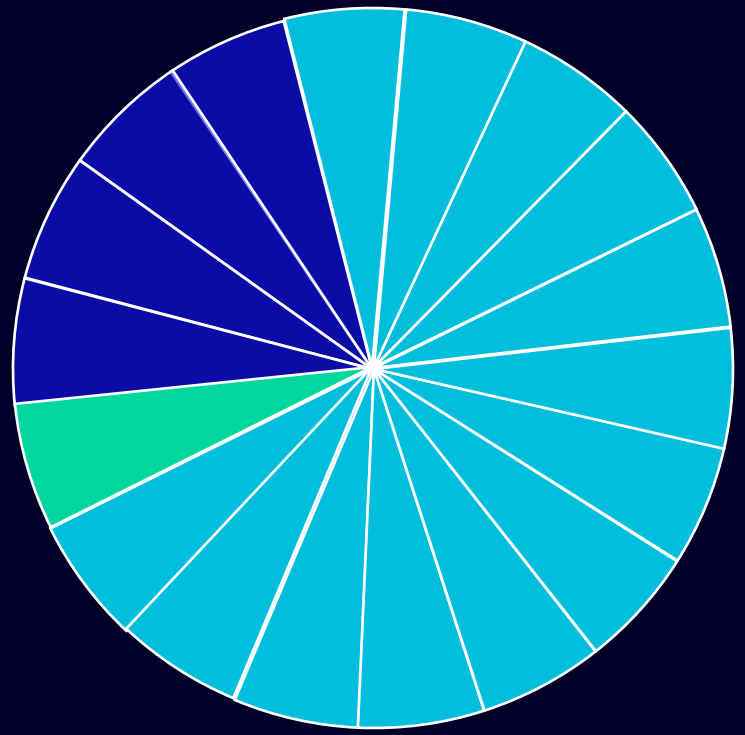
E-Trace Features – Standard and Beyond

RISC-V Trace mandatory features

- Instruction trace
- Hart (CPU) to encoder interface
- ‘Delta Address’ trace mode
- Efficient packet format

Siemens extra capability

- Cycle accurate trace



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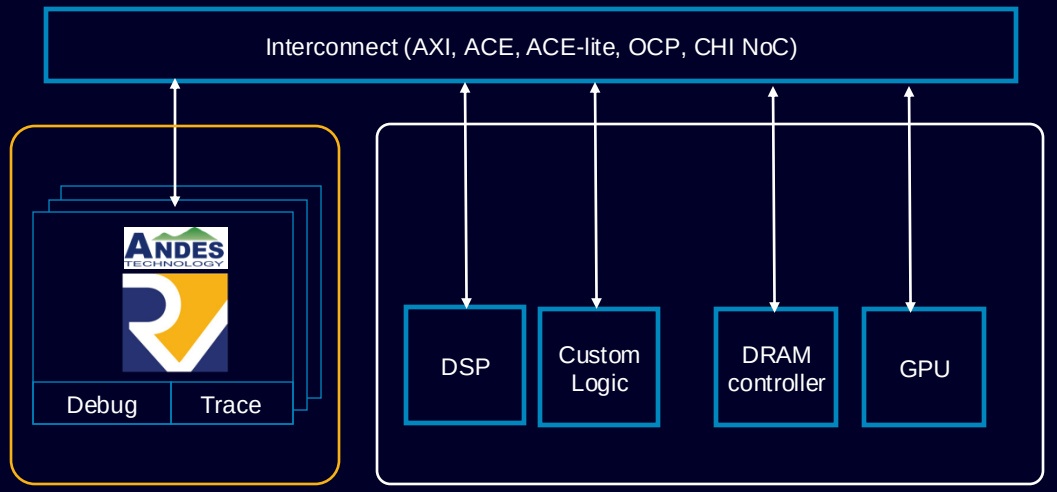
System-Level Visibility of Entire SoC including other CPU Custers



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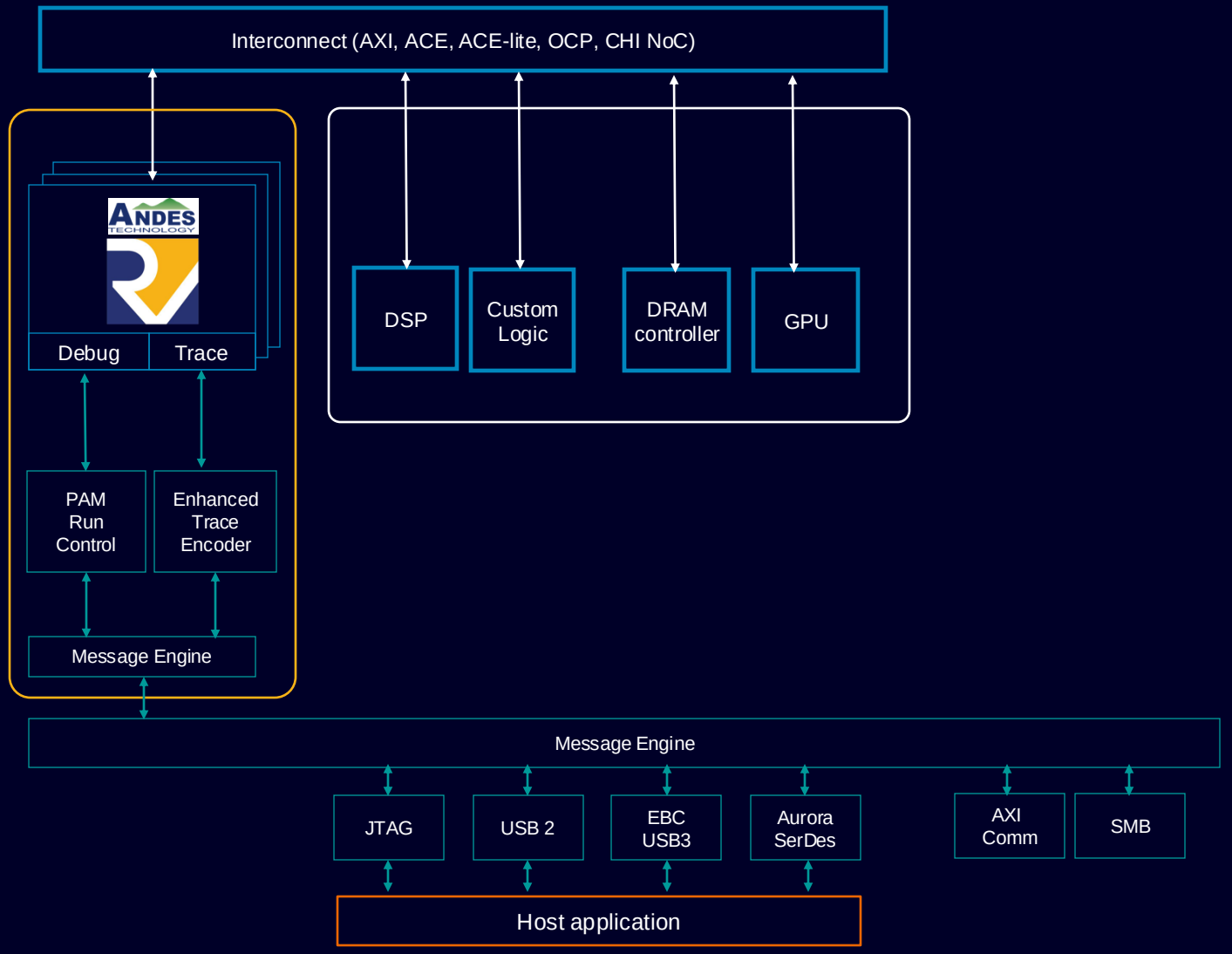

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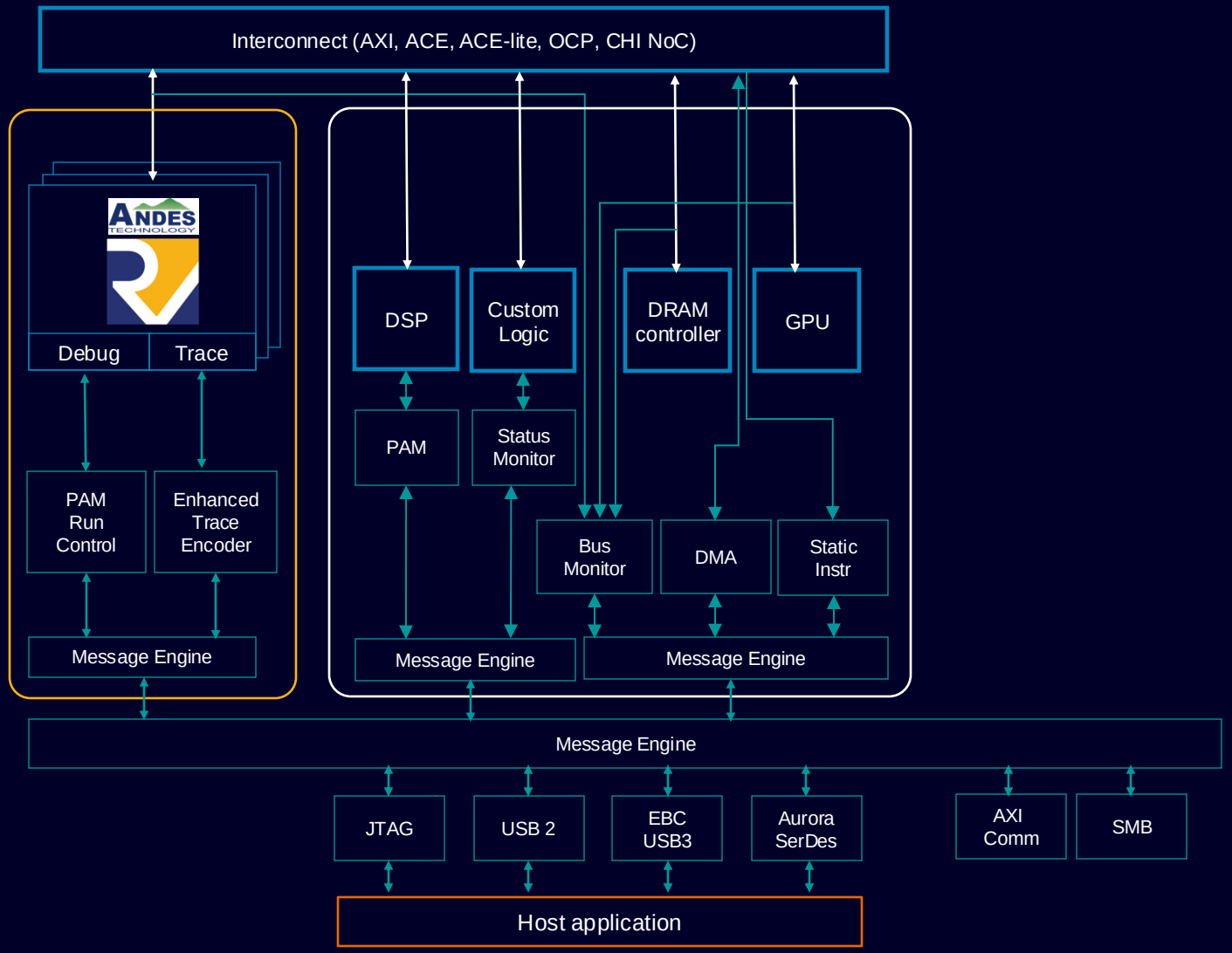

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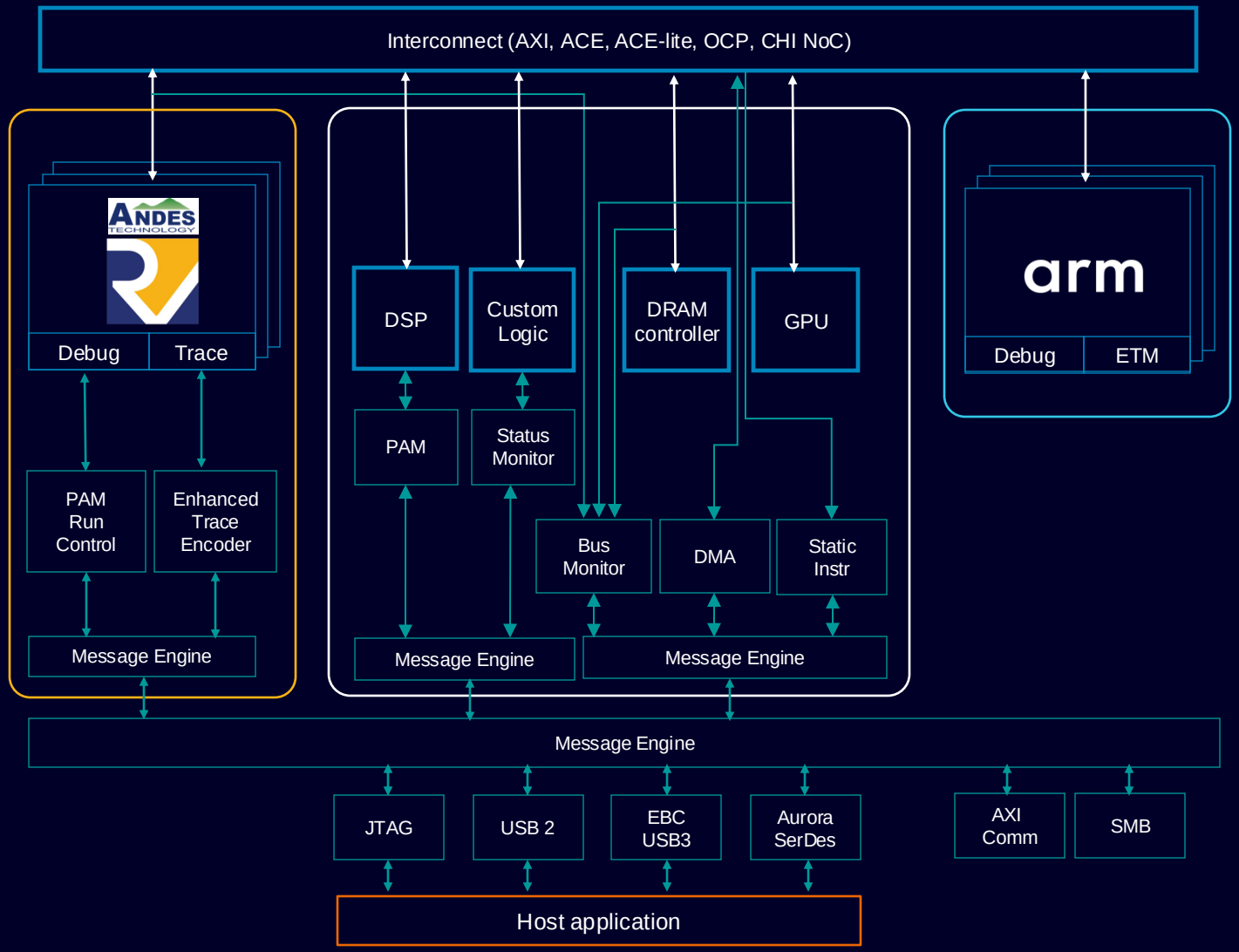

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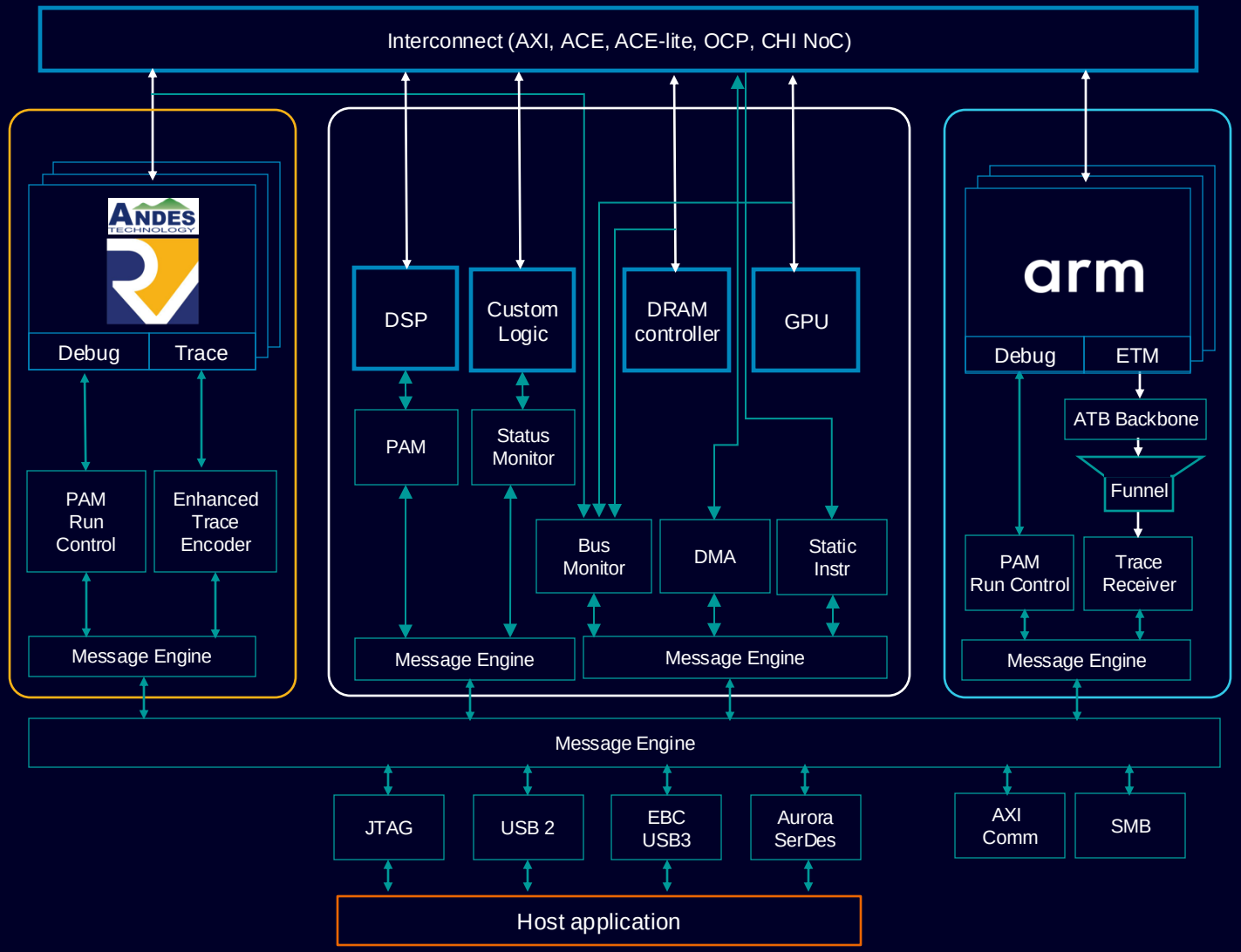

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Summary

- Understanding program behavior in complex systems is challenging
- Non-intrusive, full-speed observation of program behavior is required
  - Efficient Trace for RISC-V addresses the problem
  - Optional encoding modes offer significant benefit

- Siemens offers a Trace Encoder fully compliant with RISC-V standard
- Tessent Embedded Analytics is a complete platform for system level visibility
  - Optimize system software
  - Slash design validation costs
  - Accelerate in-lab system bring-up
  - Extend in-field diagnostics after system deployment

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Thank you

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