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5 Levels of RISC-V Processor Verification

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20 August 2024

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- The RISC-V Verification Disconnect
- 5 levels of processor verification
- Asynchronous lockstep continuous compare
- Summary

The RISC-V Verification Disconnect

RISC-V Core **User**:

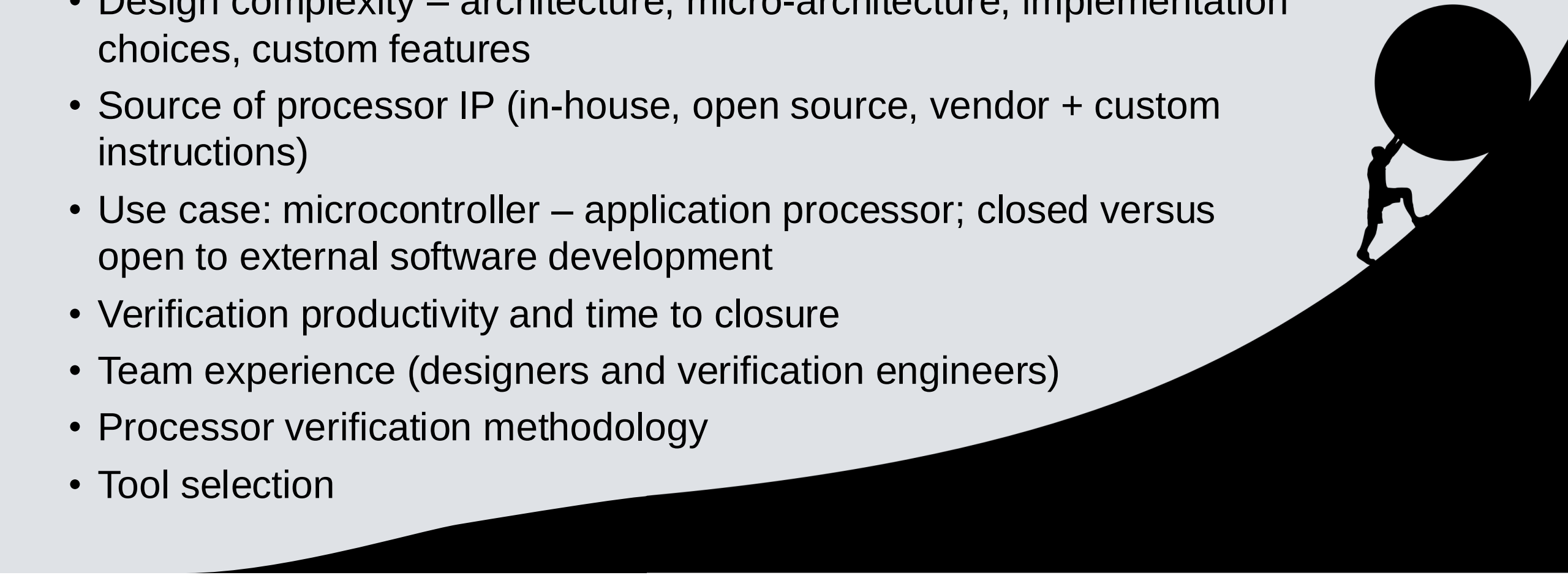
- Expects core quality to be the same as ARM
- 10^{15} verification cycles =10^{4} RTL simulators running 24/7!

RISC-V Core **Developer**:

- Needs to deliver high-quality core
- Potential issues with necessary expertise, methodologies, technologies, resources

Challenges in RISC-V Processor Verification

- Design complexity – architecture, micro-architecture, implementation choices, custom features
- Source of processor IP (in-house, open source, vendor + custom instructions)
- Use case: microcontroller – application processor; closed versus open to external software development
- Verification productivity and time to closure
- Team experience (designers and verification engineers)
- Processor verification methodology
- Tool selection



5 Levels of RISC-V Processor DV Methodology

CPU Quality

1) Asynchronous lockstep continuous compare
2) Synchronous step-and-compare
3) Post-simulation trace log file compare
4) Self-checking tests
5) “Hello World”, Linux boot, …

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3) **Post-simulation trace log file compare**
4) Self-checking tests
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Post-sim Trace Compare (entry level DV): Pros and Cons

- Pros:
  - Simple to set up and use
- Cons:
  - Must run RTL simulation to the end
  - Cannot debug live
  - Incompatible trace formats (between RTL, ISS, …)
  - Easy to skip instructions, and only compare selected few
  - Difficult to verify asynchronous events (e.g. interrupts, debug requests)
  - Not a comprehensive DV strategy
- Key requirement: high-quality model of the RISC-V processor
  - ImperasFPM is the high quality commercially supported model
  - Companies/engineers often think they can “easily” build their own model and Instruction Set Simulator (ISS) or use open source as a starting point
    - In our experience, building/maintaining an ISS is not nearly so easy

- Post-sim trace compare is widely used
- Most effective as a complementary methodology to asynchronous continuous compare

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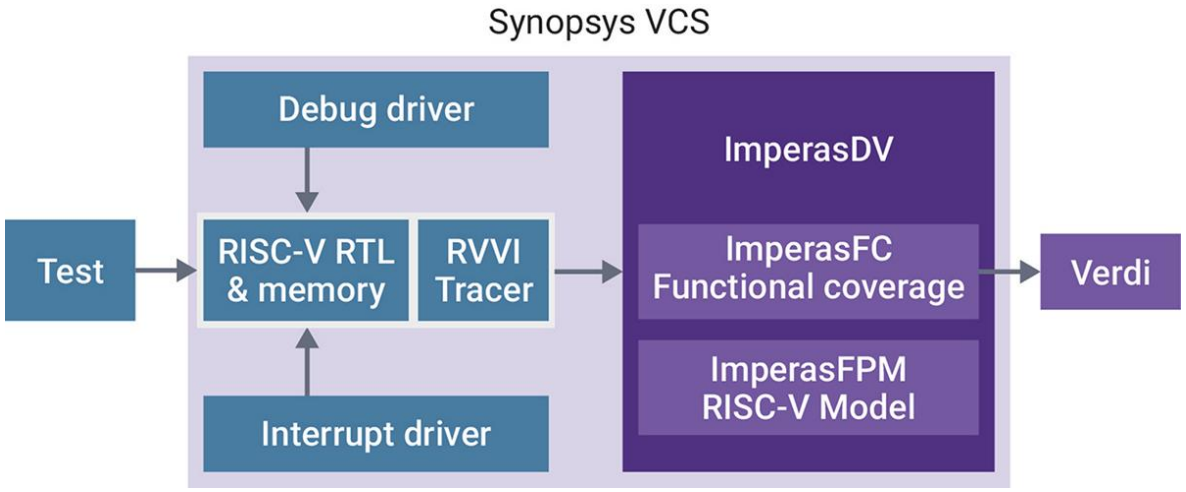
Asynchronous Lockstep Continuous Compare Methodology (highest quality processor DV)

- RTL and reference model are run in “lock-step” in the same simulation (co-simulation)
- Asynchronous events are driven into the DUT
- Tracer informs reference model about async events
- ImperasDV handles async events, scoreboarding, comparison, pass/fail
- Test source can be directed test suites for complex features, architecture validation tests, instruction stream generator or other constrained random generator
- Asynchronous events include interrupts, Debug mode, multi-hart processors, multi-issue and Out-of-Order pipeline, …



Asynchronous Lockstep Continuous Compare: Pros and Cons

- Pros:
  - Immediate comparison; immediate reporting of bugs
    - Allows for debug introspection at point of failure – very powerful
    - Does not waste execution cycles after failure
  - Most comprehensive DV methodology
    - Enables DV of complex features e.g. interrupts, Debug mode, privilege modes, virtual memory, multi-hart, multi-issue and OoO pipelines
    - Upon instruction retirement, full internal state of the processor is compared to the reference model
- Cons:
  - Users need to develop the RTL RVVI Tracer module, for communication between the DUT and reference model
    - For an engineer familiar with the processor RTL, this is typically 1-2 weeks
- Key requirements: high quality model of the RISC-V processor, co-simulation verification environment
  - ImperasFPM is the high quality commercially supported model
  - Building the verification environment is typically a make versus buy decision
    - ImperasDV provides a commercially supported, easy to use, asynchronous lockstep continuous compare processor verification environment, including functional coverage modules

- Asynchronous lockstep continuous compare methodology is used by the leading process IP vendors and companies building their own RISC-V processors
- ImperasDV and ImperasFPMs have been used for DV of processors in > 30 SoC tapeouts

How to close the RISC-V Verification Disconnect?

- Use the best processor verification methodology
- Use the best reference model
- Carefully calculate the tradeoffs and return on investment in the make versus buy decisions
- When possible, use silicon-proven processor verification tools, models, and methodologies

Thank You