RISC-V Summit 2024

利用WebAssembly技术解决 多种ISA的挑战

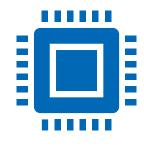
Chen Yolanda (yolanda.chen@intel.com), Huang Wenyong



Agenda







多种ISA的新挑战

WebAssembly技术及其 特性 对 Risc-V的应用和实践

多种ISA的挑战



随着RISC-V等新的ISA标准的兴起。未来会是一个多种ISA的世界。



不同硬件平台上, 新兴的编程语言也层出不穷。



如何提供更好的软件开发工具来帮助开发者开发跨平台的解决方案是一个重要的问题。



WebAssembly(缩写WASM)于2019年正式成为W3C的推荐标准,其定义了一种低级字节码,具有可移植性、可以安全且快速地跨平台运行。它实现了对现代硬件的抽象,并且独立于语言、硬件和平台,为Web应用而生但又不仅限于Web平台。



目前在Chrome V8 引擎, Wasm Micro Runtime (WAMR)中都已实现WASM 对 RISC-V平台的支持。

What is WebAssembly

WebAssembly is a type of code that can be run in modern web browsers — it is a low-level assembly-like language with a compact binary format that runs with nearnative performance and provides languages such as C/C++, C# and Rust with a compilation target so that they can run on the web. It is also designed to run alongside JavaScript, allowing both to work together.[1]

```
#include <stdio.h>

int fib(int x) {
   if (x < 2) {
     return 1;
   } else {
     return fib(x - 1) + fib(x - 2);
   }
}

int main() {
   int result = fib(45);
   printf("%d\n", result);
   return 1;
}</pre>
```

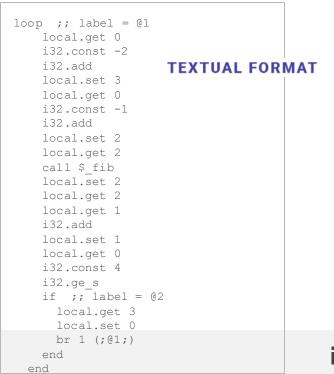
```
emcc -03 -g -o fib.js fib.c

BINARY FORMAT

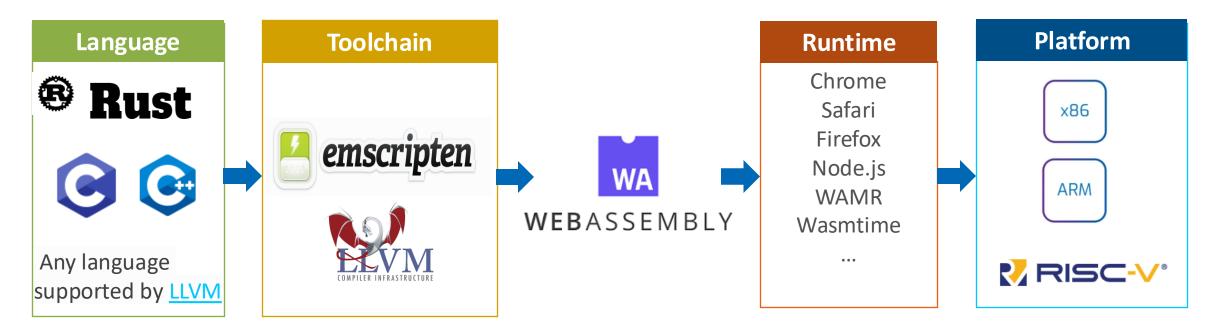
00 61 73 6d 01 00 00 00 01 87 80 80 80 00 01 60
02 7f 7f 01 7f 03 82 80 80 80 00 01 00 04 84 80
80 80 00 01 70 00 00 05 83 80 80 00 01 00 01
06 81 80 80 80 00 00 07 90 80 80 80 00 02 06 6d
65 6d 6f 72 79 02 00 03 61 64 64 00 00 08 8d 80
80 80 00 01 87 80 80 80 00 00 20 01 20 32 68 0b

fib.wasm

2 ./wasm2wat fib.wasm > fib.wat
```



用法和特点



Portable

- Write once, run everywhere.
- Language-, hardwareand platformindependent.

Fast

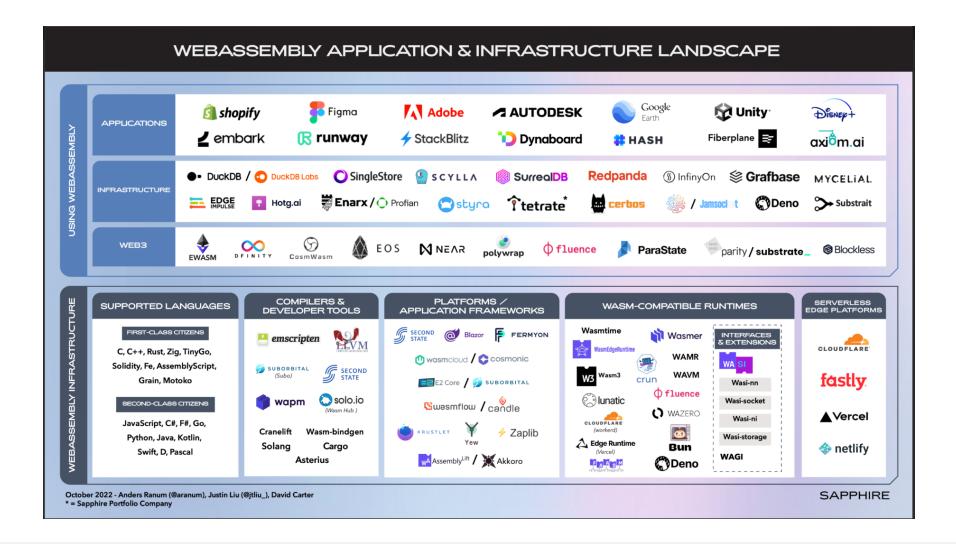
- Low-level code emitted by a C/C++ compiler is typically optimized ahead-of-time.
- Support hand-written intrinsics.

Safe

- Every memory access can be guaranteed safe with a single dynamic bounds check.
- Managed runtime and sandboxed execution.
- Efficient Representation

- Compact binary format.
- Easy to decode, validate and compile.
- Streamable and parallelizable. [2]

WebAssembly 应用和框架



[3]

Wasm-Micro-Runtime (WAMR)

A lightweight standalone wasm runtime under BytecodeAlliance, adopted in many commercial products and maintained by Intel, Xiaomi, Amazon, Sony, Siemens, etc.

- Rich running modes
 - AOT, JIT, Fast Interpreter, Classic Interpreter
- Support multiple architectures and platforms
 - x86, riscv, aarch64, arm, thumb, xtensa, etc.
 - Linux, Windows, MacOS, Android, Zephyr, etc.
- Near native performance with AOT/JIT
 - <u>Siemens report</u>, <u>Frank Denis's report</u>
- Rich features
 - Source debugging, lib-pthread, wasi-threads, multi-module
 - GC, wasi-nn, socket, XIP, SIMD128, memory64
 - C/Python/Go/Rust language bindings

Active contributors







Siemens



Sony Semiconductor Solutions



WAMR home: https://github.com/bytecodealliance/wasm-micro-runtime

Wasm2native compiler

A compiler to compile WebAssembly into native binary

Remove AOT runtime dependency

No standalone wasm runtime required

Support multiple architectures

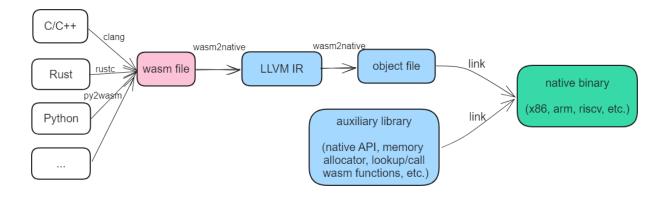
- x86-86, x86-32, riscv64, riscv32
- aarch64, arm, thumb, xtensa, etc.

Support two compilation modes

- sandbox mode: wasm sandbox is kept
- no-sandbox mode: wasm sandbox is discarded but allows sharing pointers between wasm and native

Good performance

- Good performance in sandbox mode
- Near native performance in no-sandbox mode



wasm2native home: https://github.com/web-devkits/wasm2native (open-sourcing is WIP)



- https://riseproject.dev

RISE is focused on positive and transparent collaborations with upstream projects to deliver commercial-ready software for various use cases

How: Align on highest priorities & avoid (accidental) duplication of work

Goal: Accelerate open source SW for RISC-V architecture

https://www.intel.com/content/www/us/en/developer/articles/community/rising-to-the-challenge-risc-v-software-readiness.html

Finding more interesting topics from Intel on RISC-V summit China 2024

Торіс	When & Where
UXL 软件栈和 RISC-V 的初步探索	August 22 16:45 主会场A
LLVM 工具链 RISC-V 构建实现及其性能优化现状分析与未来展望	August 23 9:40 主会场A
GCC RVV 自动向量化及其应用	August 23 10:00 主会场A
Enhancing RISC-V Security with SBI Secure Service APIs	August 23 10:40 主会场B
Enabling Hardware Sampling Based PGO for RISC-V Platform	August 23 11:40 主会场A
利用 WASM 技术解决多种 ISA 的挑战	August 23 14:20 主会场B
HVP: Hardware Accelerated RISC-V Android Emulator	August 23 14:50 主会场A
Leverage BRS standard to improve RISC-V SW compatibility	August 23 17:30 主会场A
Soft-ISA: kernel built-in emulation engine to extend RISC-V silicon ISA capability	August 23 17:40 主会场A

intel

References

- 1. WebAssembly in MDN: https://developer.mozilla.org/en-us/docs/WebAssembly
- 2. Bringing the web up to speed with WebAssembly
- 3. What's Up With WebAssembly: Compute's Next Paradigm Shift

Legal Notices and Disclaimers

Statements in this document that refer to future plans or expectations are forward-looking statements. These statements are based on current expectations and involve many risks and uncertainties that could cause actual results to differ materially from those expressed or implied in such statements. For more information on the factors that could cause actual results to differ materially, see our most recent earnings release and SEC filings at www.intc.com.

All product plans and roadmaps are subject to change without notice. Any forecasts of goods and services needed for Intel's operations are provided for discussion purposes only. Intel will have no liability to make any purchase in connection with forecasts published in this document. Code names are often used by Intel to identify products, technologies, or services that are in development and usage may change over time. No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document.

© Intel Corporation. Intel, the Intel logo, and other Intel marks are trademarks of Intel Corporation or its subsidiaries. Other names and brands may be claimed as the property of others. This document contains information on products and/or processes in development.

#