BREKER™

Advanced RISC-V Core and SoC Verification Towards the Anticipated Certification Requirements

RISC-V Summit China 2024

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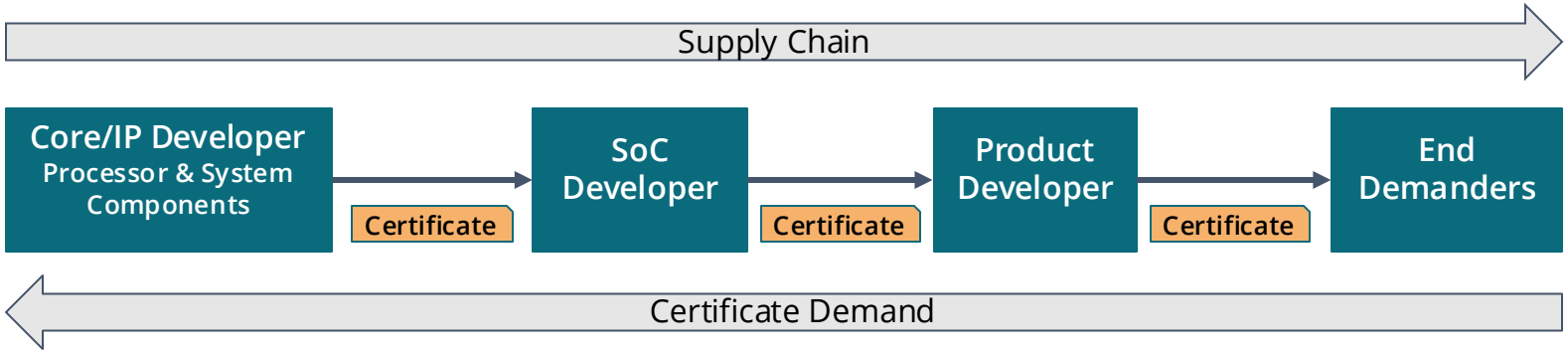
RISC-V 中国峰会

A Look At RISC-V

- Open Instruction Set Architecture (ISA) gaining significant traction in multiple applications
- Significant verification challenges
  - Arm spends $150M per year on 10^{15} verification cycles per core
  - Hard for RISC-V development group to achieve this same quality
  - Lots of applications expands verification requirements
  - Requires automation, reuse and new thinking
- RISC-V International developing certification program to provide an assurance metric for RISC-V devices

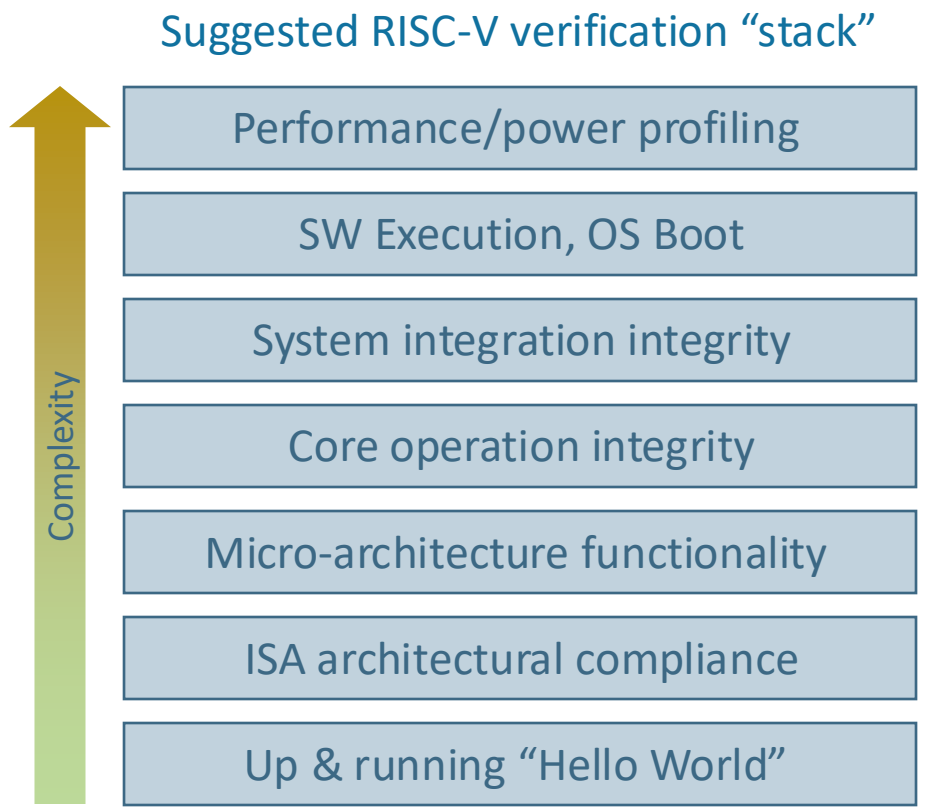
RISC-V International Certification



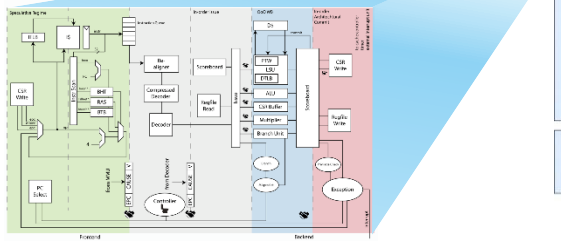
- RVI Certification Steering Committee (CSC) recently formed with the intent of increasing industry confidence in certified RISC-V cores and IP
  - Considered important as RISC-V gains in popularity
- CSC now working on test sources, process plans, etc.
  - May look to commercial entities to provide rigorous certification tests
- Breker involved as our SystemVIPs are aligned with potential CSC tests

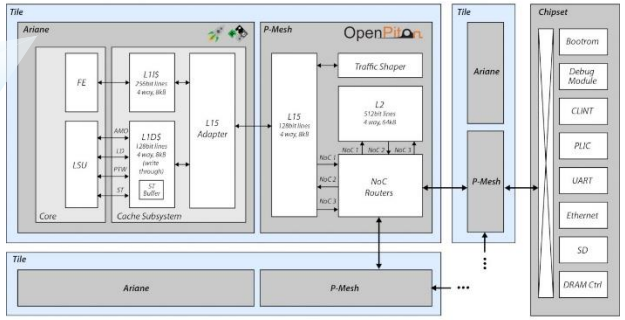
Meeting RISC-V Verification Challenges

- Reuse & automation to meet quality expectation
  - Automated test generation key
- RISC-V special requirements
  - Custom instruction verification
  - Compliance assurance
  - Broad range of architectures
- Different processors have different needs
  - Embedded cores
  - Processor clusters
  - Application processors



Different Challenges for Core vs SoC Verification





RISC-V Core Verification Challenges

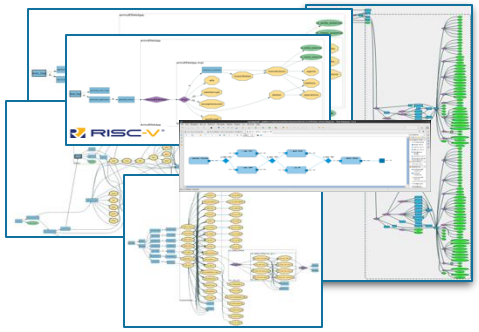
Random Instructions	Do instructions yield correct results
Register/Register Hazards	Pipeline perturbations dues to register conflicts
Load/Store Integrity	Memory conflict patterns
Conditionals and Branches	Pipeline perturbations from synchronous PC change
Exceptions	Jumping to and returning from ISR
Asynchronous Interrupts	Pipeline perturbations from asynchronous PC change
Privilege Level Switching	Context switching
Core Security	Register and Memory protection by privilege level
Core Paging/MMU	Memory virtualization and TLB operation
Sleep/Wakeup	State retention across WFI
Voltage/Freq Scaling	Operation at different clock ratios
Core Coherency	Caches, evictions and snoops

RISC-V SoC Verification Challenges

System Coherency	Cover all cache transitions, evictions, snoops
System Paging/IOMMU	System memory virtualization
System Security	Register and Memory protection across system
Power Management	System wide sleep/wakeup and voltage/freq scaling
Packet Generation	Generating networking packets for I/O testing
Interface Testing	Analyzing coherent interfaces including CXL & UCIe
Random Memory Tests	Test Cores/Fabrics/Memory controllers across DDR, OCRAM, FLASH etc
Random Register Tests	Read/write test to all uncore registers
System Interrupts	Randomized interrupts through CLINT
Multi-core Execution	Concurrent operations on fabric and memory
Memory Ordering	For weakly order memory protocols
Atomic Operation	Across all memory types

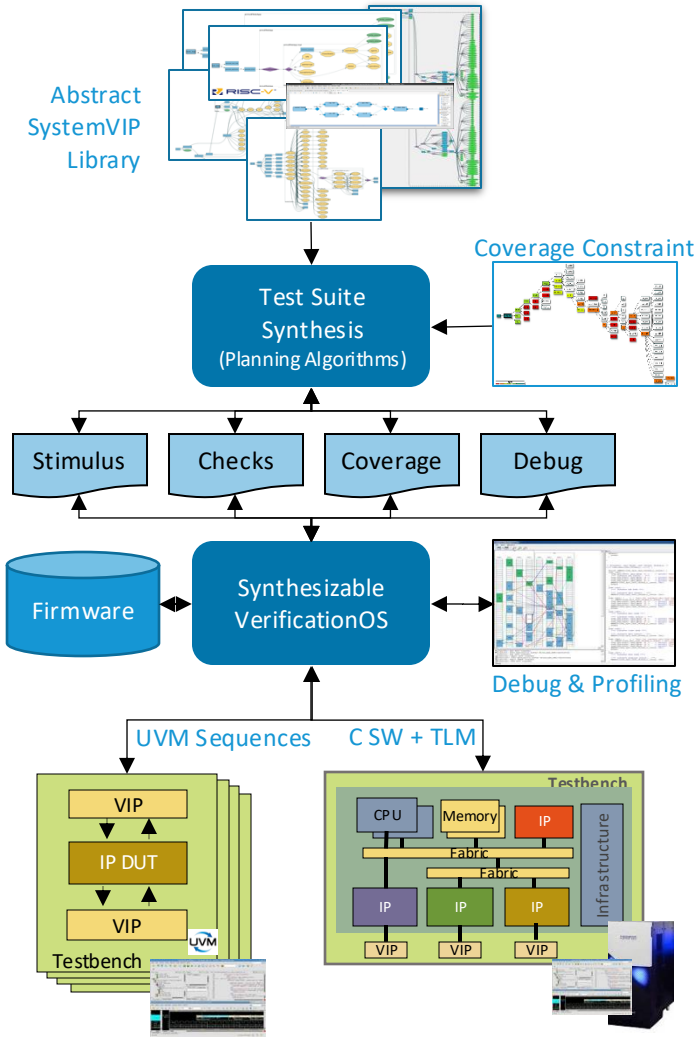
Breker Background:
Test Suite Synthesis for RISC-V Cores & SoCs

- Breker is a key, longstanding part of the verification ecosystem for processors and SoCs based on x86 and Arm architectures
- Breker has become part of the verification ecosystem for processors and SoCs based on RISC-V architectures
  - Working with multiple RISC-V developers and users/integrators
- RISC-V has room to grow if we solve the verification barrier
  - We are experienced in x86 and Arm verification, now are sharing this experience with RISC-V teams through automated tests



The Breker SystemVIP Library

- *Core Integrity FastApps*
- *RISC-V System Integrity TrekApp*
- *ARM System Integrity TrekApp*
- *Cache Coherency TrekApp 2.0*
- *Firmware-First TrekApp*
- *Power Management TrekApp*
- *Security TrekApp*
- *Networking TrekApp*

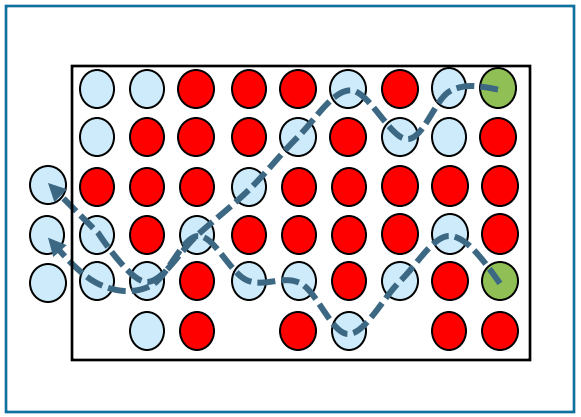


Breker Technology Significantly Differentiates SystemVIP

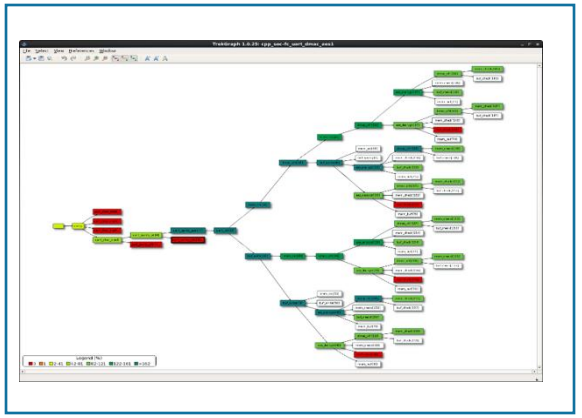
- Targets operational scenarios rather than functional components
- Common model easily configured for varied system architectures
- Vertical/horizontal verification portability
  - Virtual C, UVM sim, emulation, prototyping/post silicon
  - UVM, C & TLM for SoCs, Virtual C code, Silicon diagnostics

- Deep scenario, bug-hunting coverage
- Concurrency for system stress testing
- Self-checking tests with included debug, and coverage capability
- Extensibility for custom functionality, test methods
- Functional AND performance bugs found

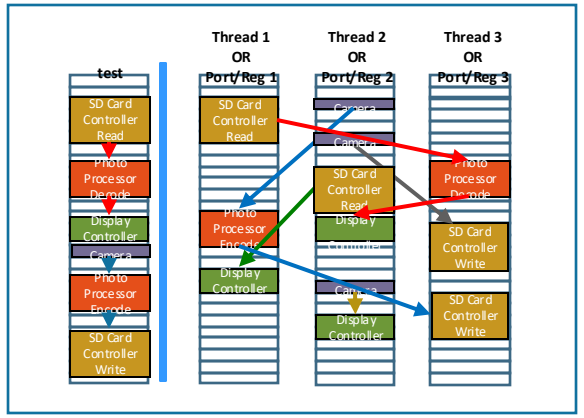
Examples of Breker's Test Suite Synthesis Technology Enhancing SystemVIP



AI Planning Algorithms



Cross-Test Coverage Generation



Concurrent Stress Test Scheduling

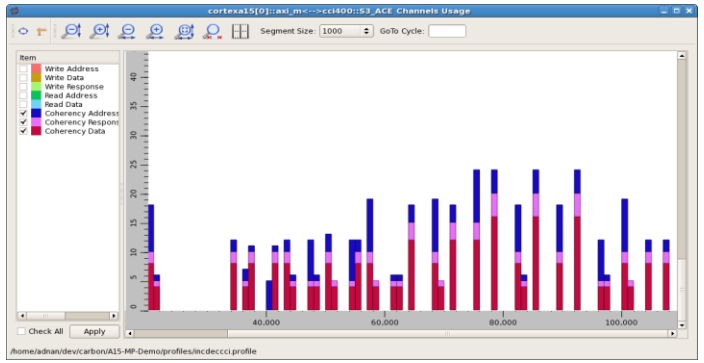
High Coverage and Bug Hunting

Recent examples of bugs discovered in real designs

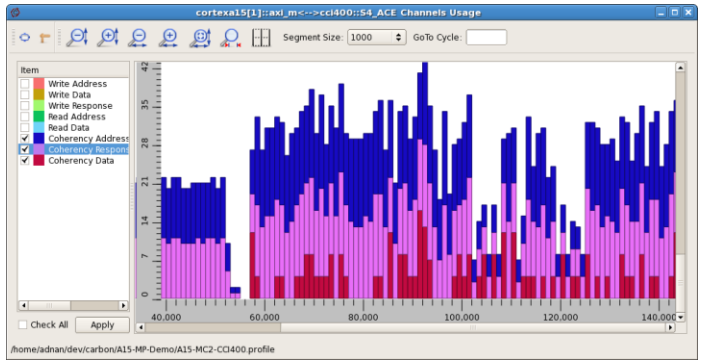
- RISC-V spec misunderstanding between core vendor and user
- Coherent Mesh Network (CMN) programming issues
- Misconfigured ARM CMN pin to enable coherent traffic
- DDR model unable to handle AXI "wrap" transactions.
- Common cache line access reveals deadlock
- Custom instruction bugs discovered by stress tests
- Results mismatch with ultrawide address strides
- Incorrect exception for guest virtual address[63:38] = 0x1ffffff
- Bad mcause value for guest physical address[63:31] != 0x0

SystemVIP Test Suite Synthesis Coverage Comparison

Typical directed coherency coverage



... vs. Breker automated coherency tests



Core-Integrity Challenges

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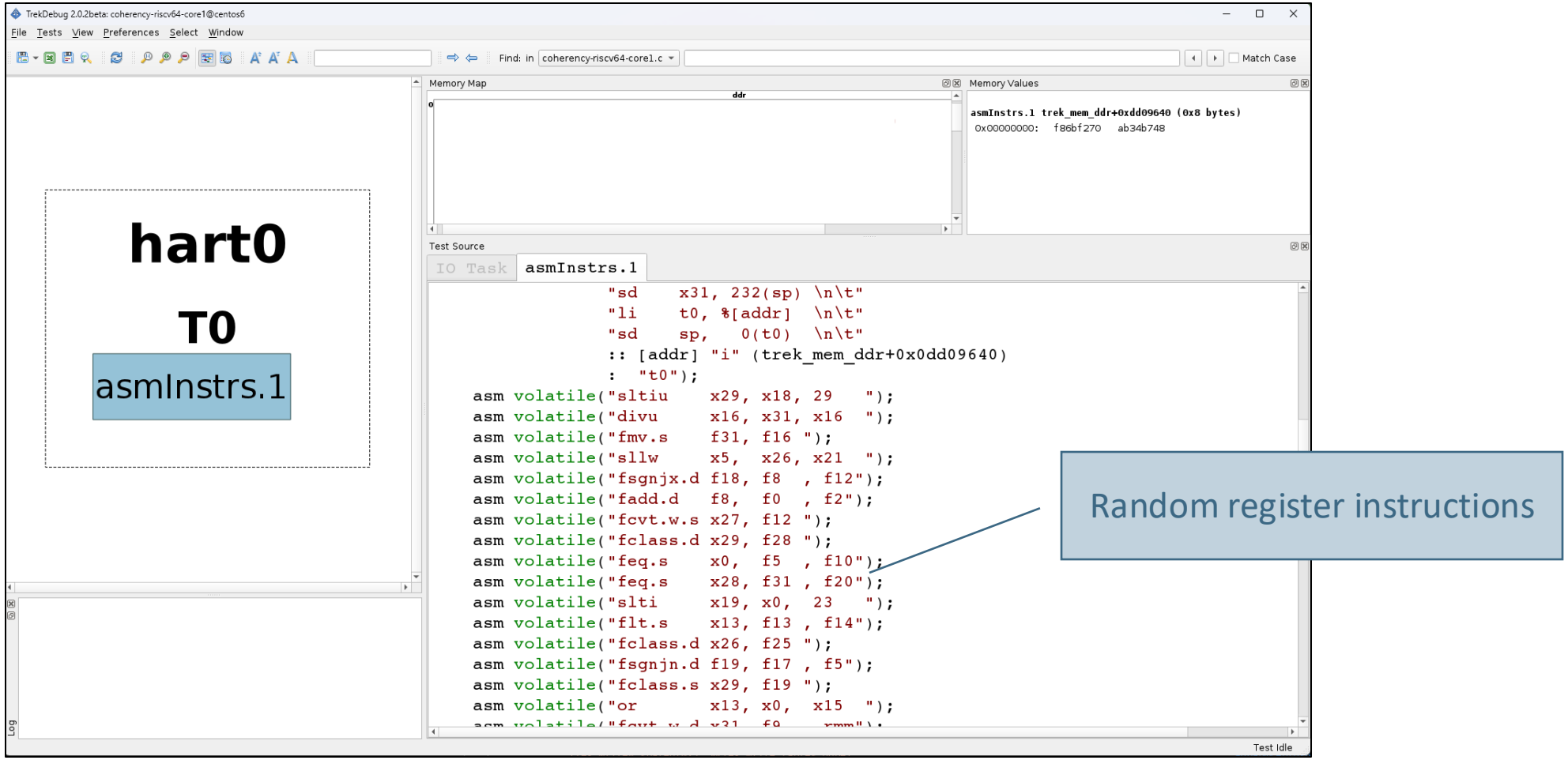
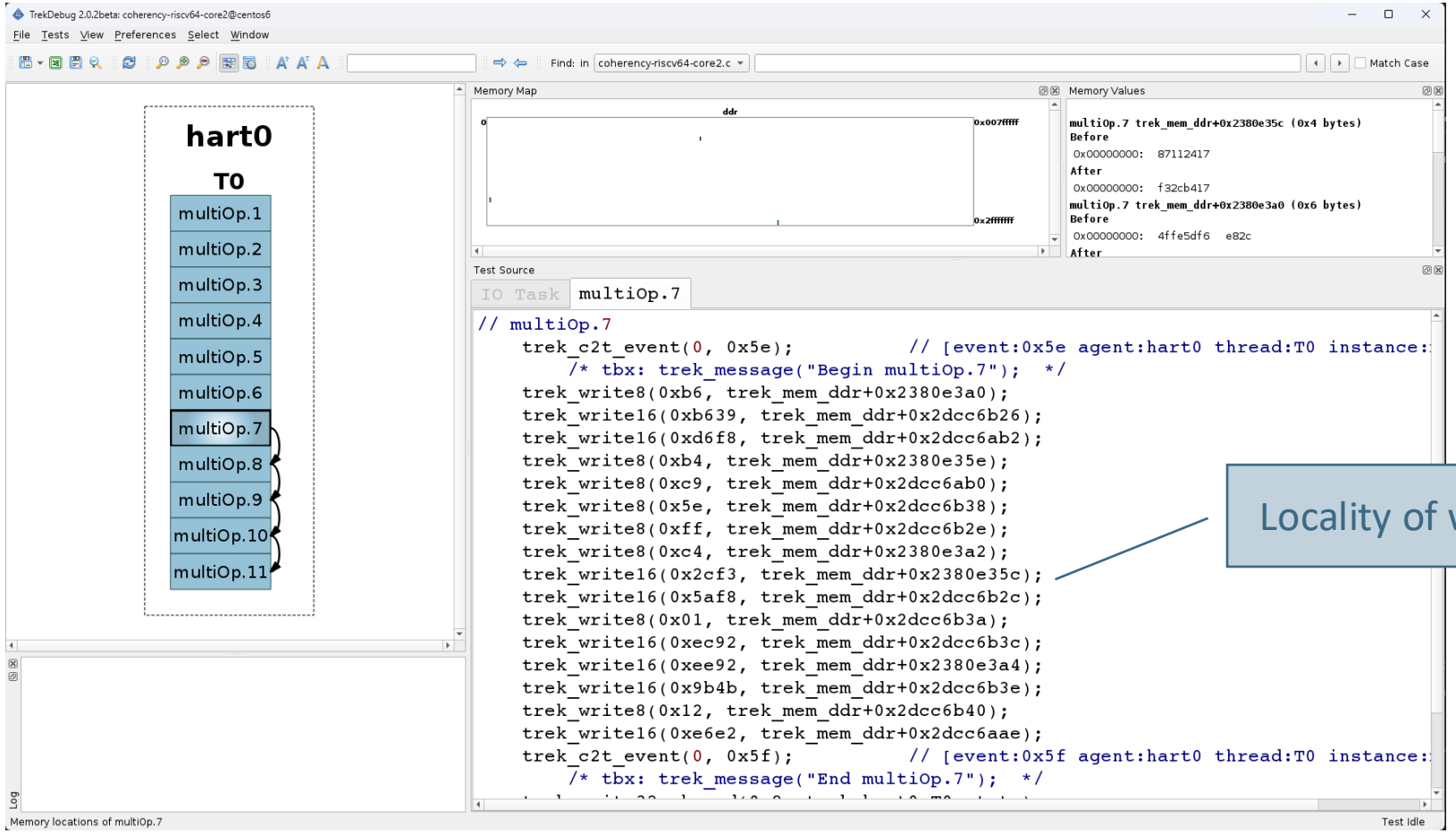
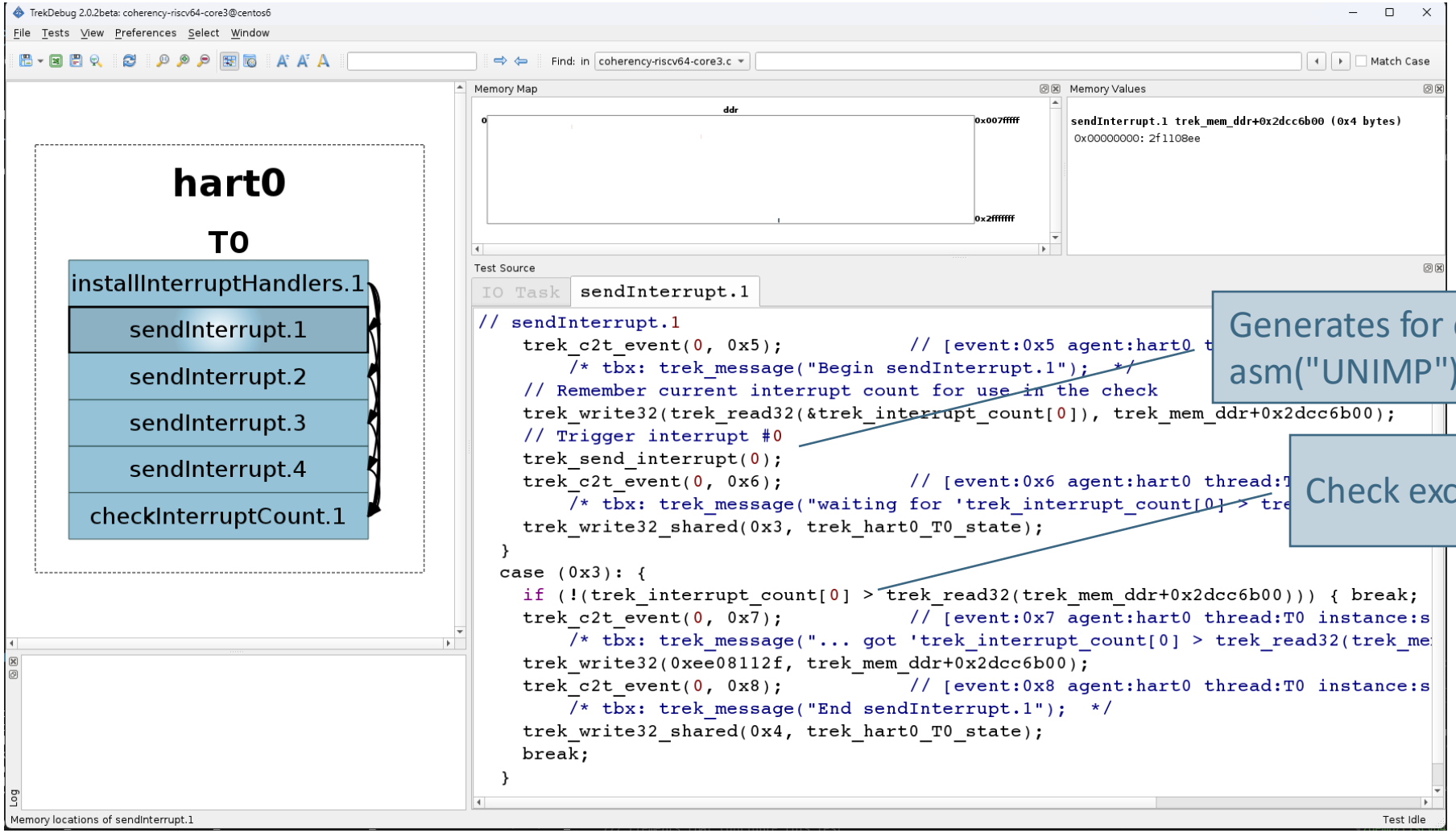
RV64 Core Instruction Generation



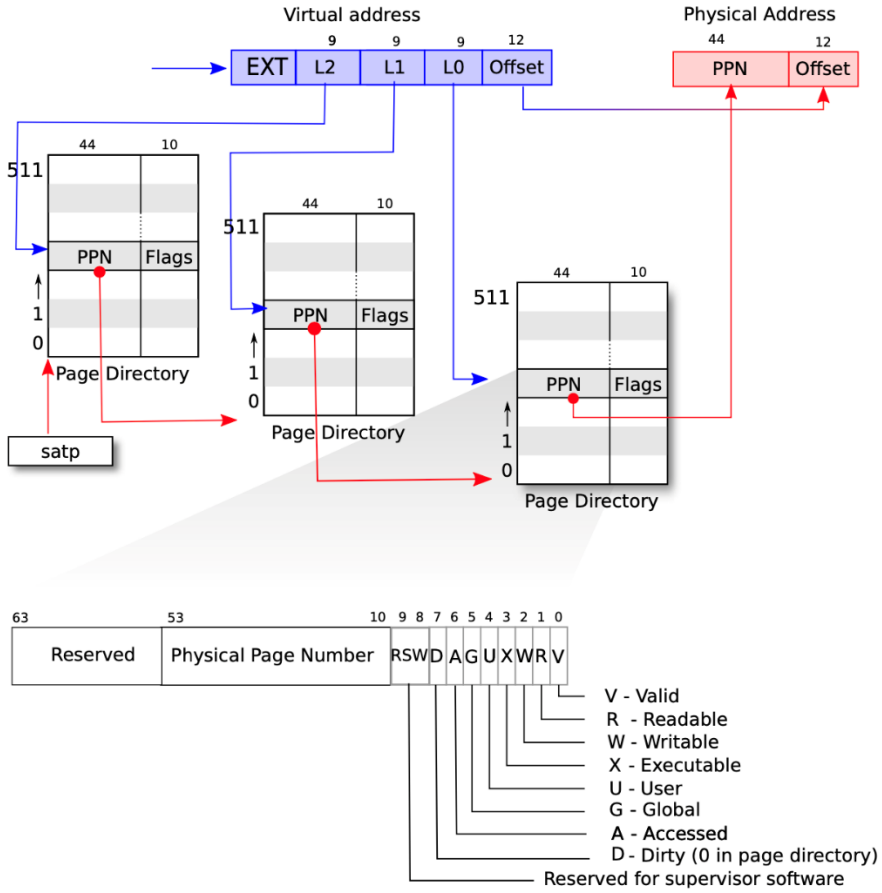
RV64 Core Load/Store



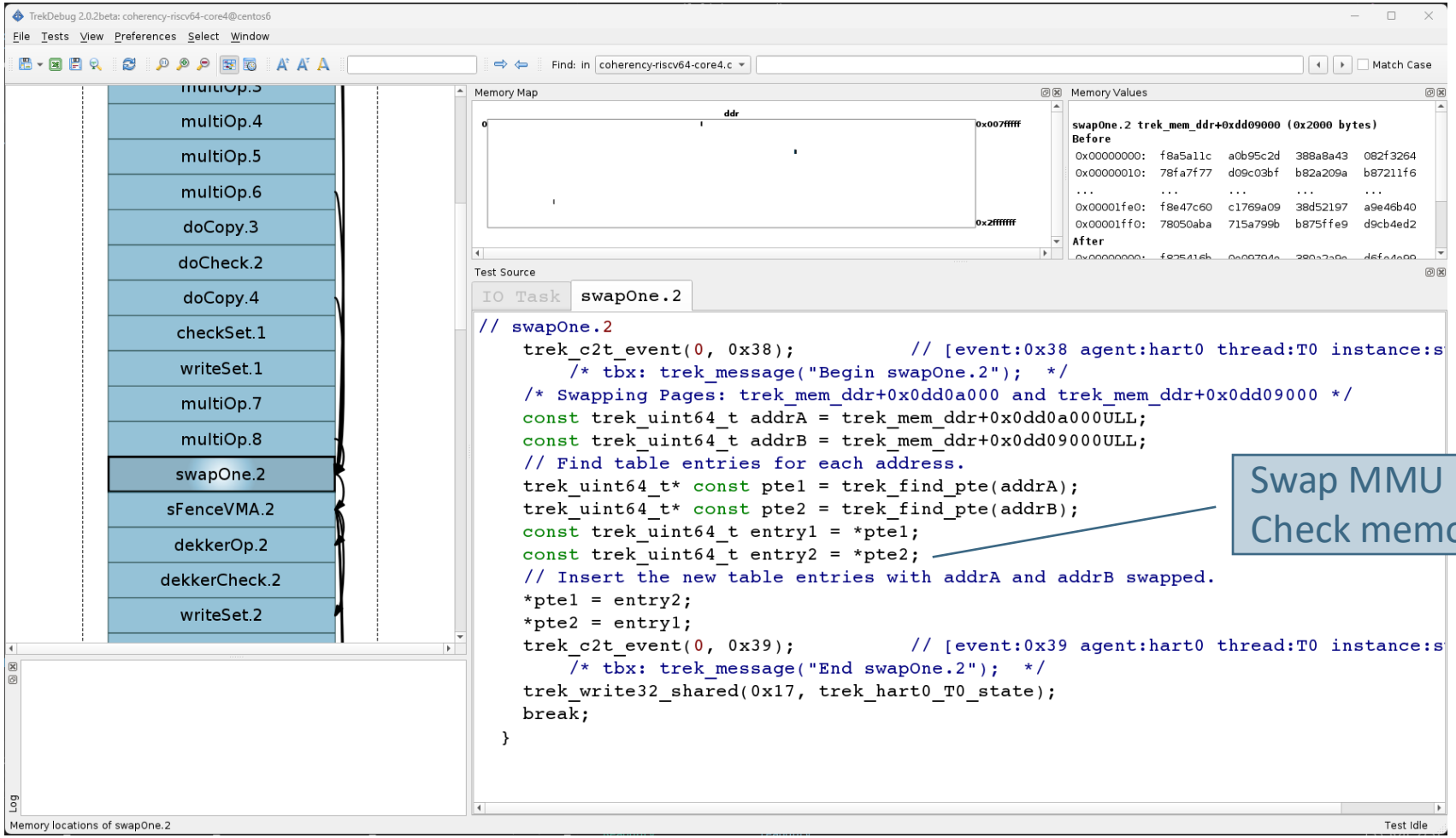
RV64 Core Exception Testing



Page Based Virtual Memory Tests



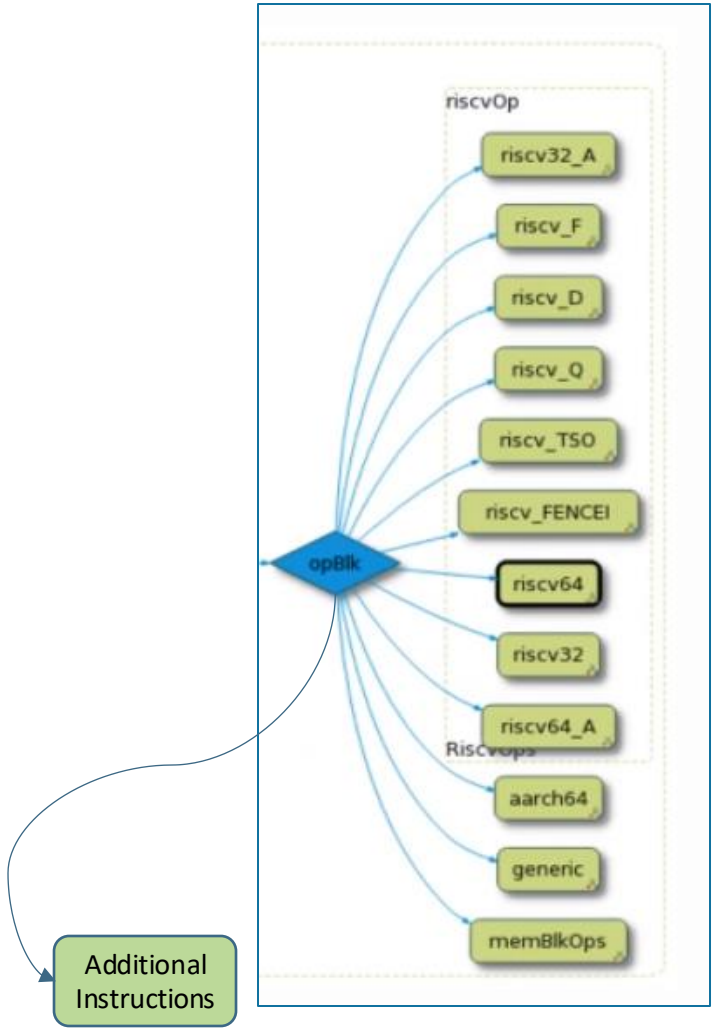
RV64 Core Page Based MMU Tests



Swap MMU PTE's and Check memory access

Testing a Custom Instruction

- RISC-V ISA custom instructions pose a particularly difficult verification challenge
- Custom instructions need to be tested with the processor tests, not as an afterthought
- Breker solution allows custom instruction tests to be easily added into test graph
- Breker synthesis combines these tests with the app to ensure full custom processor testing



SoC-Integrity Challenges

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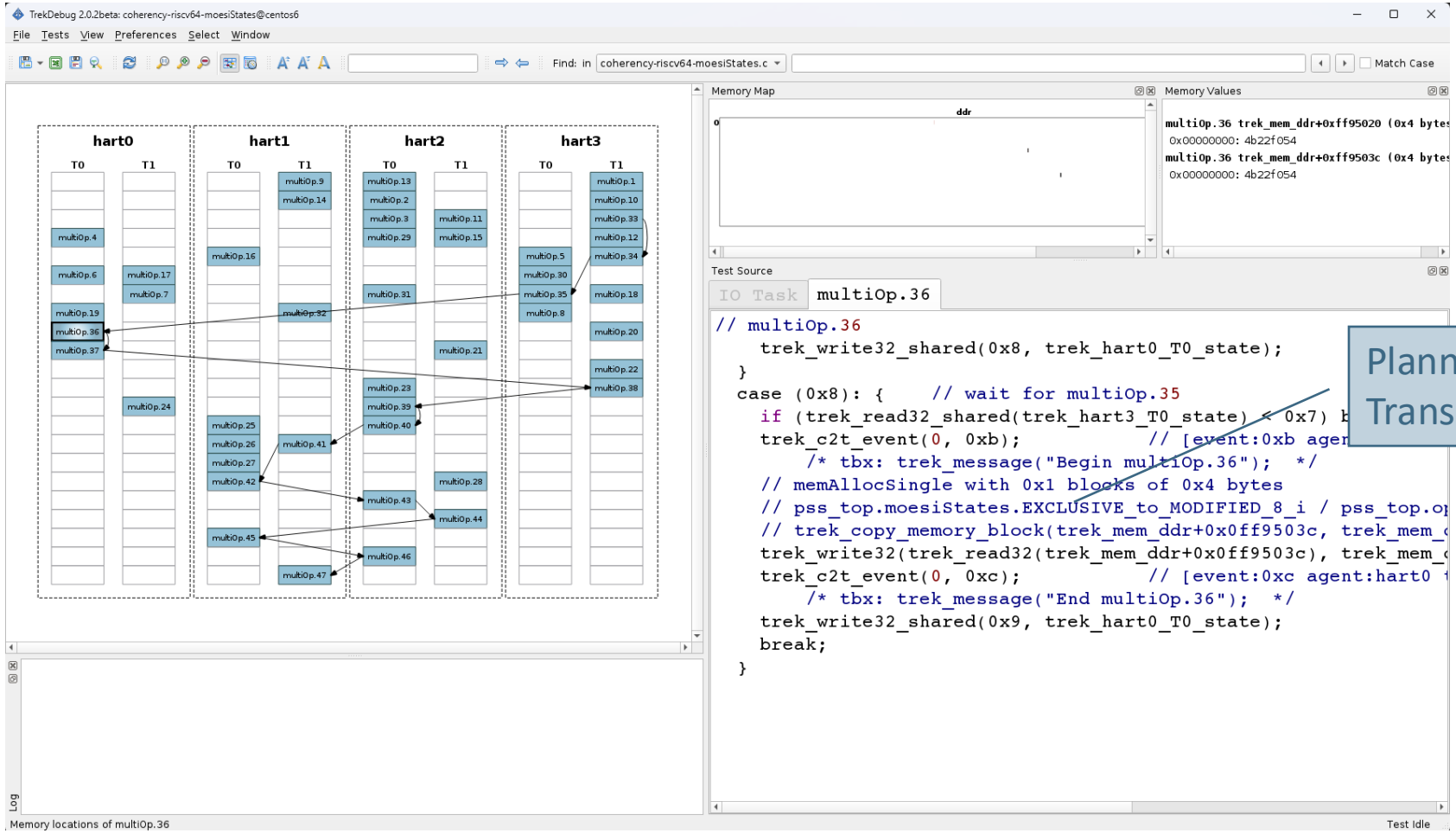
System Security	Register and Memory protection across system
Power Management	System wide sleep/wakeup and voltage/freq scaling

Breker
RISC-V SoC-Integrity
SystemVIP

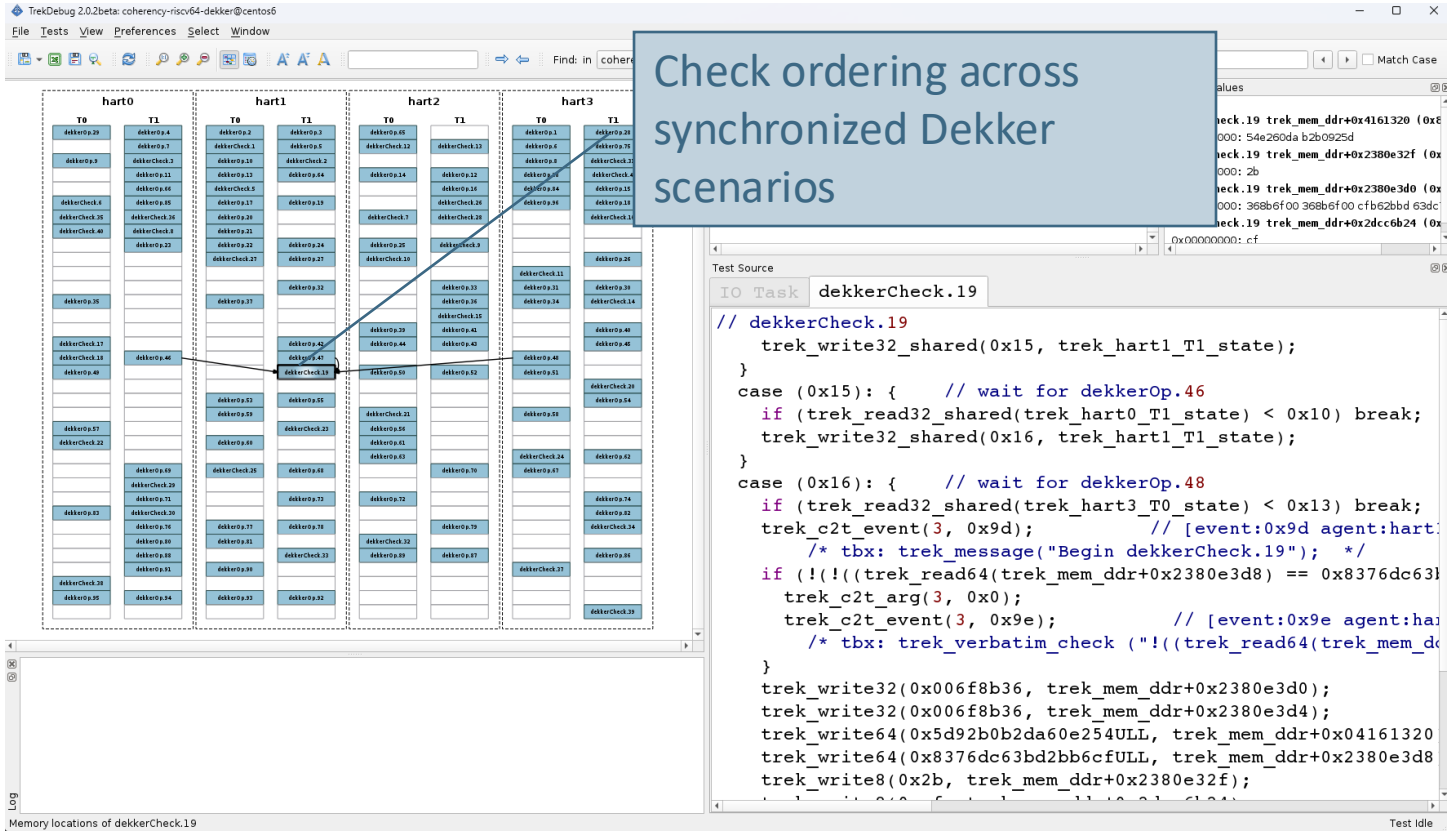
- **End-to-End use cases**
- **Early Firmware Testing**
- **Performance-Power Profiling**

RV64 MultiCore MoesiStates

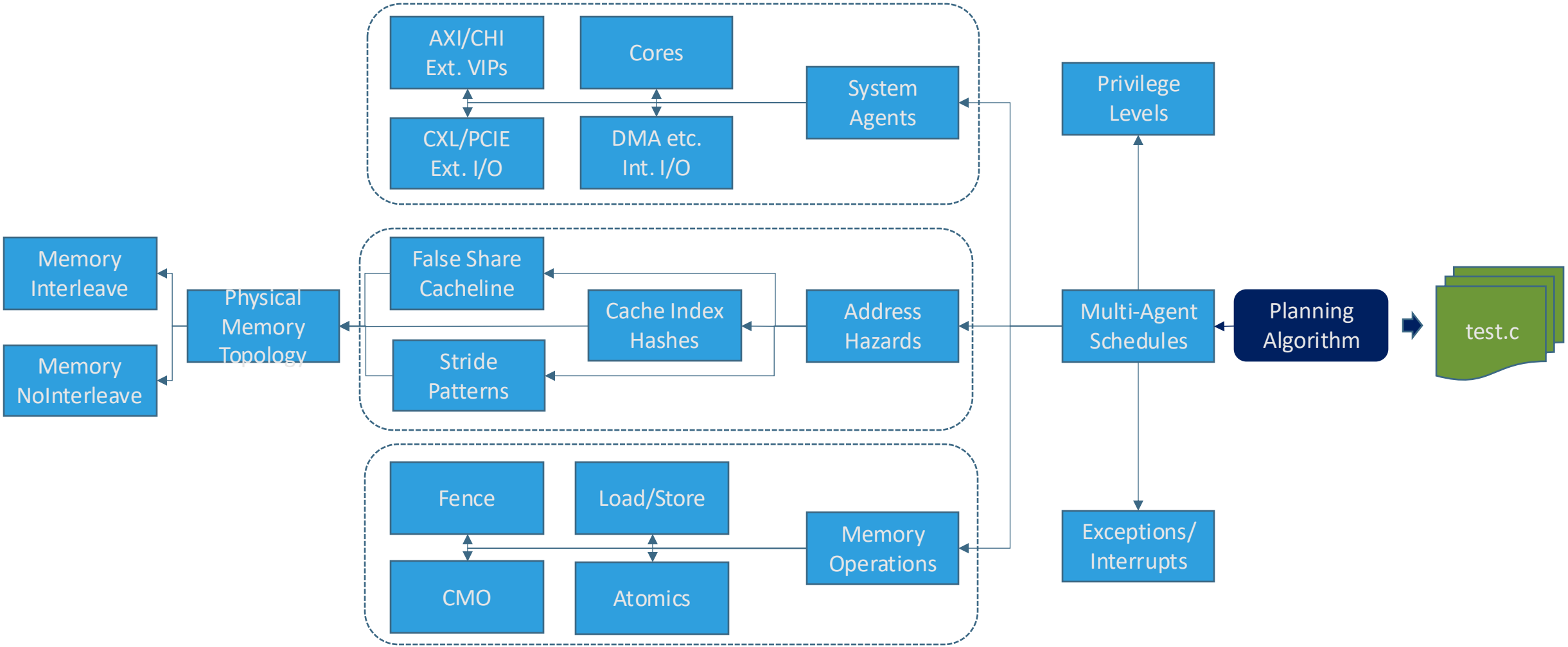


Planned Cache State Transitions

Dekker Memory Ordering



RISC-V SoC Integrity TrekApp



Summary

- RVI is creating a certification program that requires rigorous testing
  - Probably will be an important part of RISC-V development in the future
- Breker is now providing state-of-the-art test solutions that accelerate and amplify RISC-V core and SoC test quality
- RVI certification is likely to borrow heavily from commercial verification solutions such as Breker SystemVIP and Test Suite Synthesis

Thanks for Listening!
Any Questions?