Optimizing Interconnect Architectures for High-performance and Complex RISC-V SoCs

基于 RISC-V 复杂高性能 SoC 的互联架构优化

RISC-V Summit China 2024

https://www.arteris.cn/solutions/risc-v/

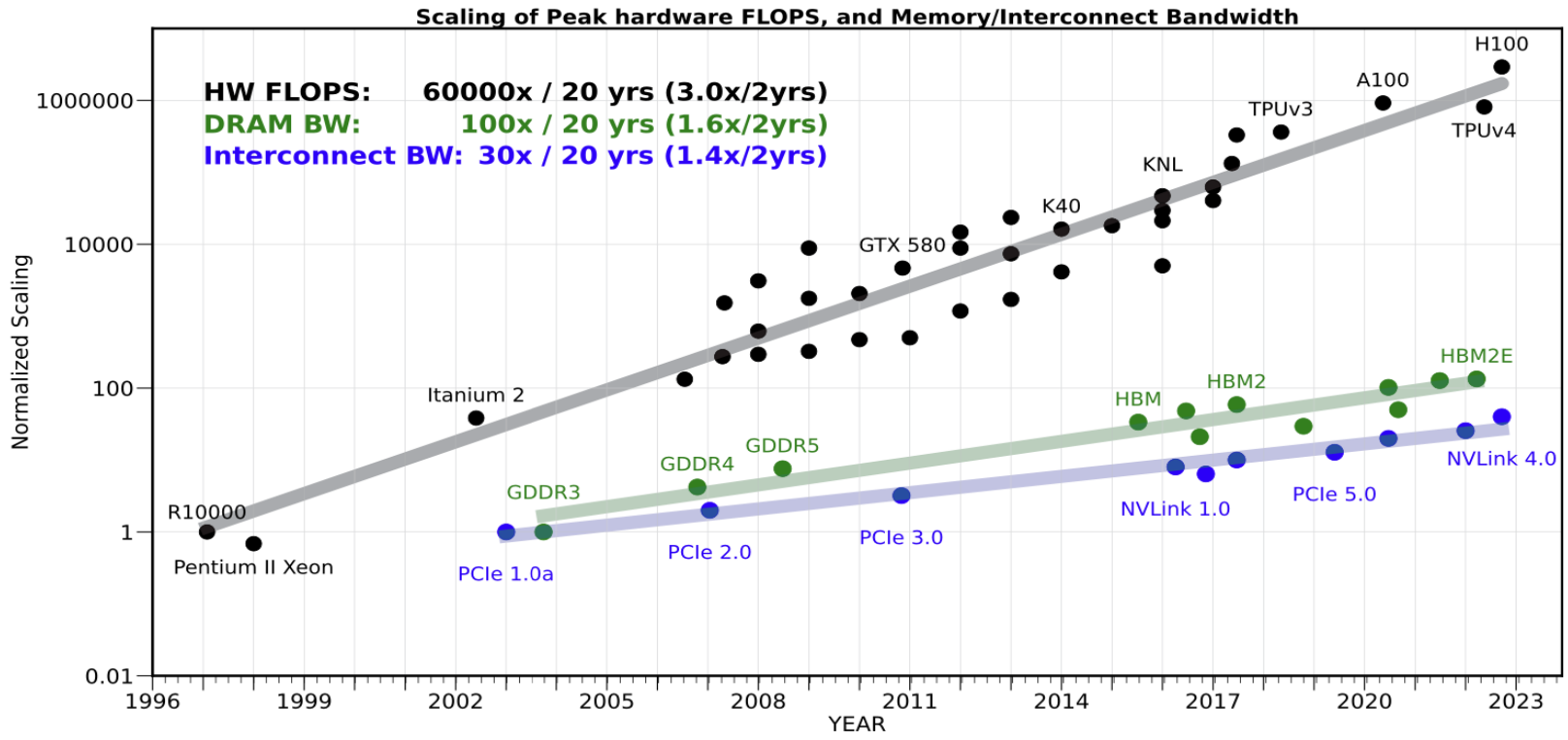
Hao Luan
Chief Architect

August 2024

ARTERIS IP

The Opportunities and Challenges

Interconnect is the Enabler for High Performance & Complex SoCs



However, the peak compute of server-grade AI hardware has increased over 60,000x over the past 20 years, as opposed to 100x for DRAM or 30x for the interconnect bandwidth

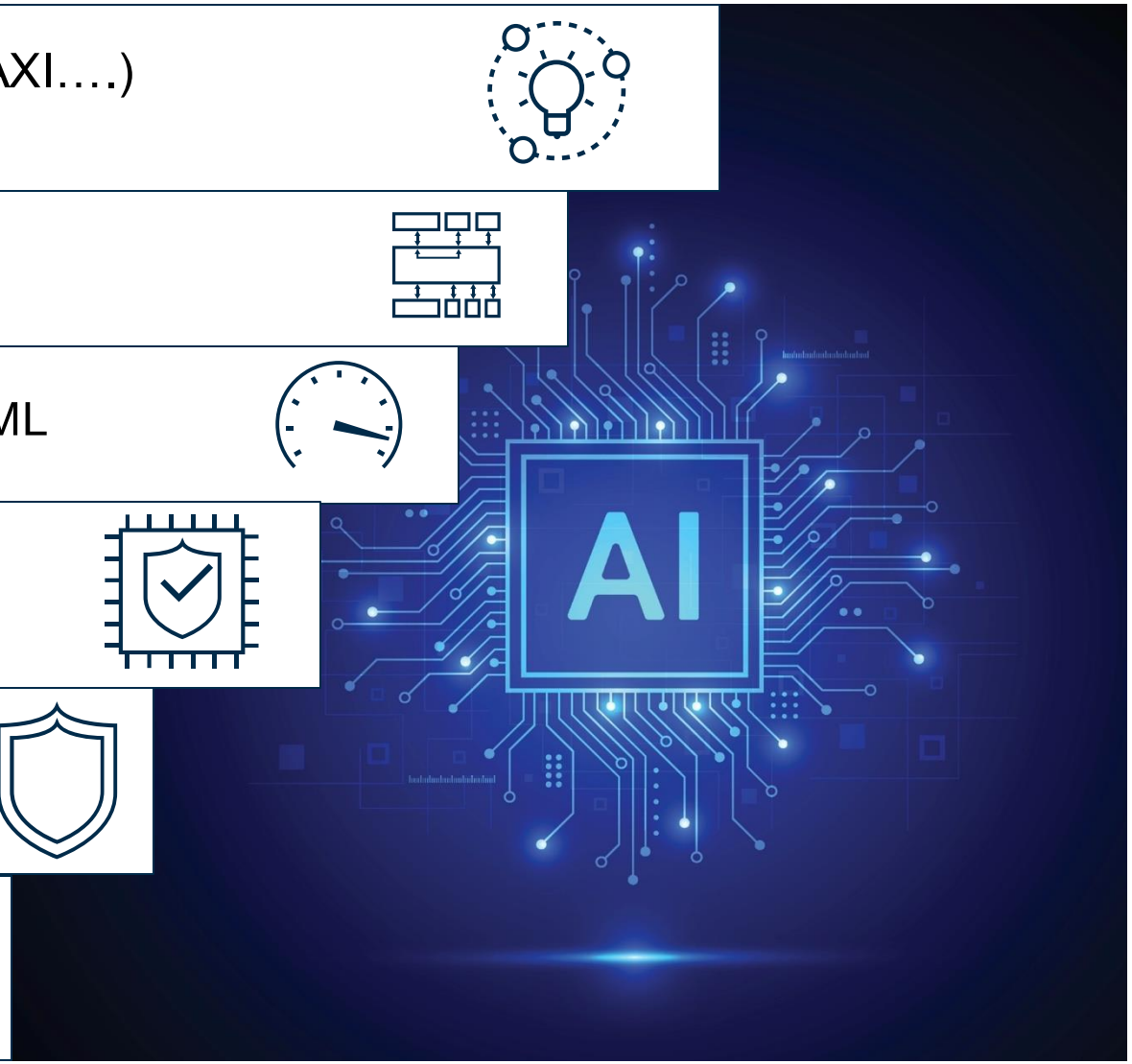
- Dr. John L. Hennessy and David A. Patterson predicted a few years ago that we are right in a new golden age for computer architecture with a few trends below:
  - Open Instruction Sets
  - Domain Specific Architecture
  - Agile Chip Development

John L. Hennessy and David A. Patterson. 2019. A new golden age for computer architecture. Commun. ACM 62, 2 (February 2019), 48–60. https://doi.org/10.1145/3282307

A. Gholami, Z. Yao, S. Kim, C. Hooper, M. W. Mahoney and K. Keutzer, "AI and Memory Wall," in IEEE Micro, vol. 44, no. 3, pp. 33-39, May-June 2024, doi: 10.1109/MM.2024.3373763

Challenges of RISC-V SoCs – Interconnect is the Problem to Address

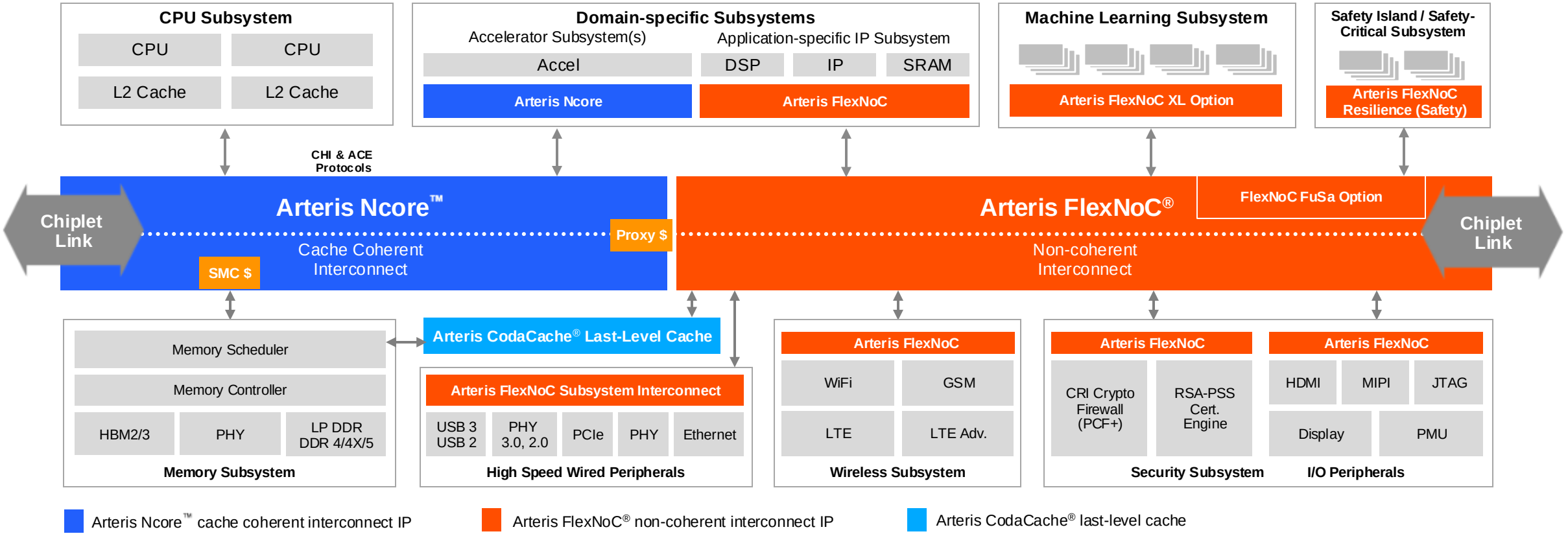
- Diverse interface protocols (ACE, CHI, ACE-Lite, AXI….)
- Varying coherency models (MESI, MOESI)
- ‘Memory wall’ - Massive memory bandwidth of AI/ML
- Safety standards for automotive functional safety
- Verification / Performance models / FPGAs
- Physical implementation (PD)



System IP and Network-on-Chip (NoC) SoC Interconnect IPs

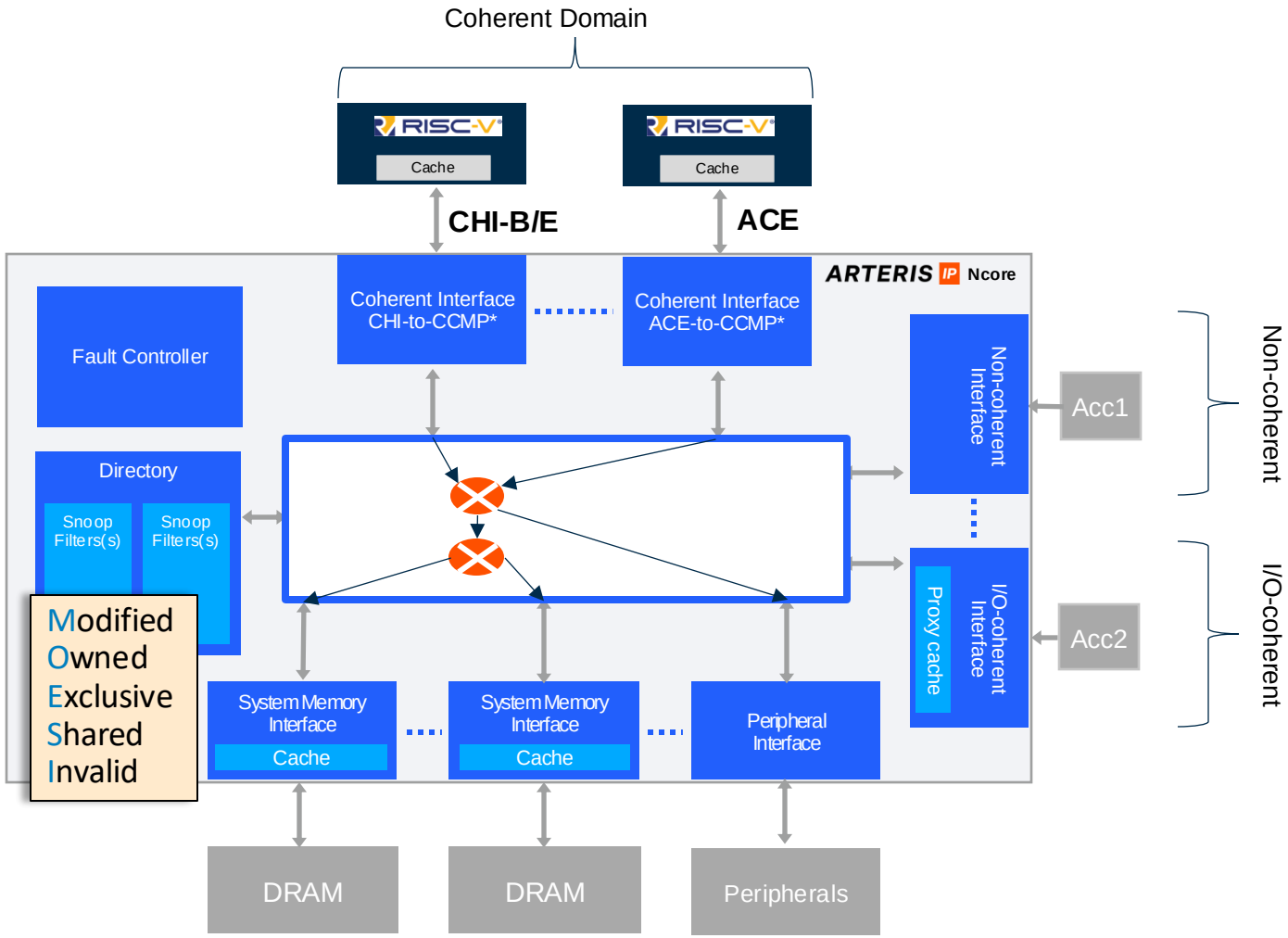
Networking techniques for improved on-chip communication & data flow

Smaller Die Area | Lower Power Consumption | Faster Frequency Lower Latency | Shorter, Predictable Schedules | Rapid Timing Closure Estimation | Automated Verification | Easy Configuration



Arteris Ncore Configurable Coherent Interconnect

Multi-protocol coherent interconnect

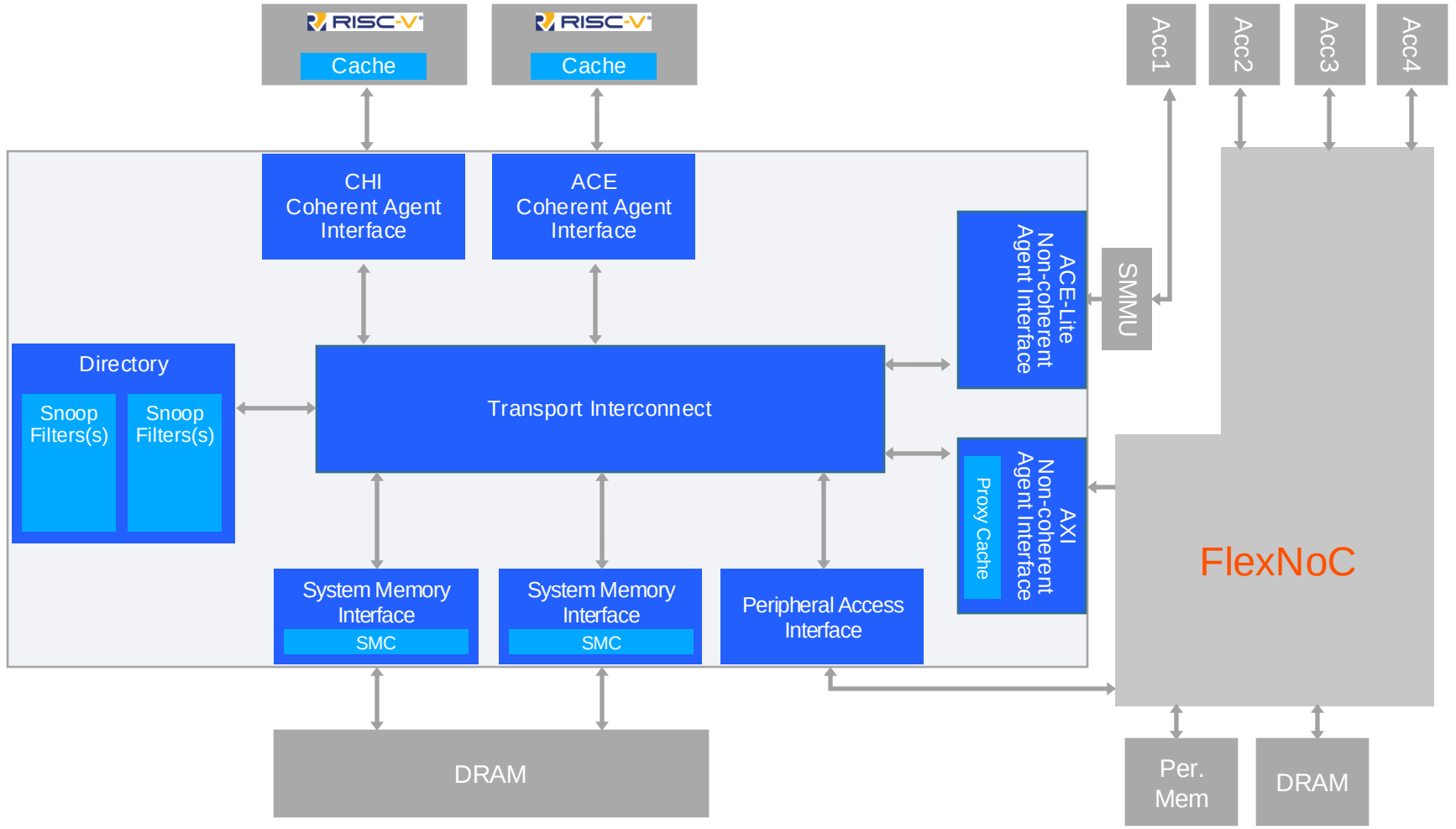


**CCMP: Concerto Coherent Messaging Protocol*

- AMBA protocols converted to internal Arteris CCMP protocol
  - Coherent Interfaces: CHI-B, CHI-E or ACE, **interoperable**
  - Arteris internal protocol supports MESI and MOESI coherency models
- I/O Interfaces:
  - ACE-Lite, AXI
  - Optional Proxy Cache participates in coherency domain as fully coherent cache
- Memory interface with optional system memory cache
- Peripheral Interface for I/O targets
- Directory with snoop filters
- Fault controller for functional safety option
- Transport created from switches

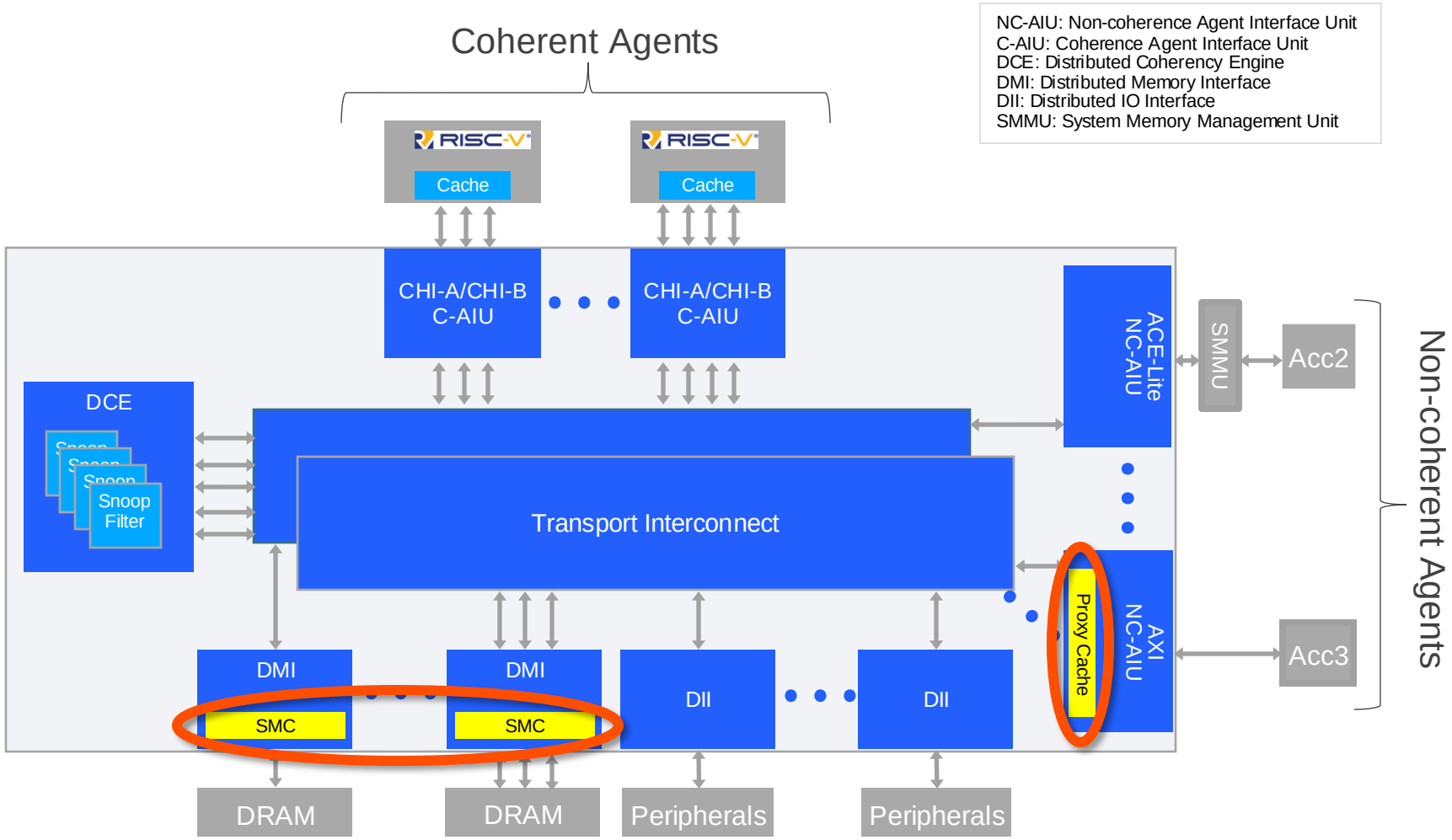
Why Use AMBA CHI and ACE in the Same System?

Adapt to RISC-V dynamic ecosystem



- RISC-V is a diverse and evolving ecosystem
- Mixed ACE/CHI can ease integration of new and legacy processors
  - Mix latest high-performance RISC-V clusters using CHI with older RISC-V CPUs using ACE
  - Leverage investment in ACE IP
- Proxy caches ease integration of non-coherent accelerators into the coherent domain
- Provide PCIe connectivity for storage and data center applications

Proxy Cache & System Memory Cache (SMC)



Proxy cache

- Configurable up to 8MB, 1-16 ways
- Cache for non-coherent or I/O coherent accelerators
- Fully coherent with caches and memories in the system
- Reduces accelerator traffic into coherency system
- Smooths accelerator traffic with varying bursts into 64B coherency granules
- Enables Domain Specific Architecture with flexible and efficient heterogeneous SoCs

SMC

- System Memory Cache per distributed memory interface
- Configurable up to 8MB, 1-16 ways per DMI
- Scratchpad, partitioning, atomics
- Cache Maintenance Operations

Both can be configured with parity or ECC for FuSa systems

Efficient and Performant AI/ML Data Transport Architecture

Optimal solutions combine coherent and non-coherent NoCs

- Coherent NoCs required for data shared with cached CPUs
  - Coherent systems work on 64B coherency granules (512b cache line)
- Extreme bandwidths in AI/ML devices
  - Local memories may reduce traffic to external memory
  - Separate shared and non-shared memory traffic
- Provide a fast and wide path to memory for non-shared traffic
- Combine coherent and I/O-coherent NoCs for optimal performance
  - Coherent hub close to the cached CPUs with narrower buses
  - Wide NoC connects the rest of the SoC including AI core array
  - Mesh topology can be appropriate for AI applications

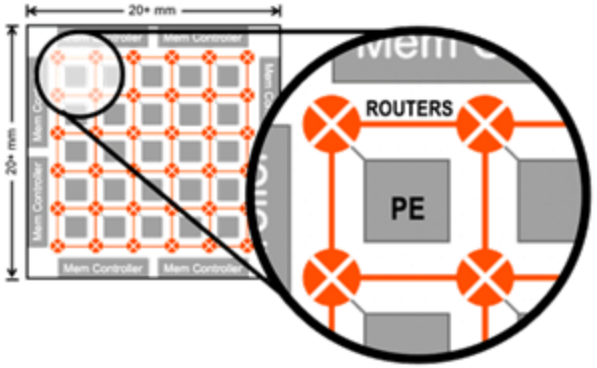
Ncore 3 coherent interconnect provides the coherent hub

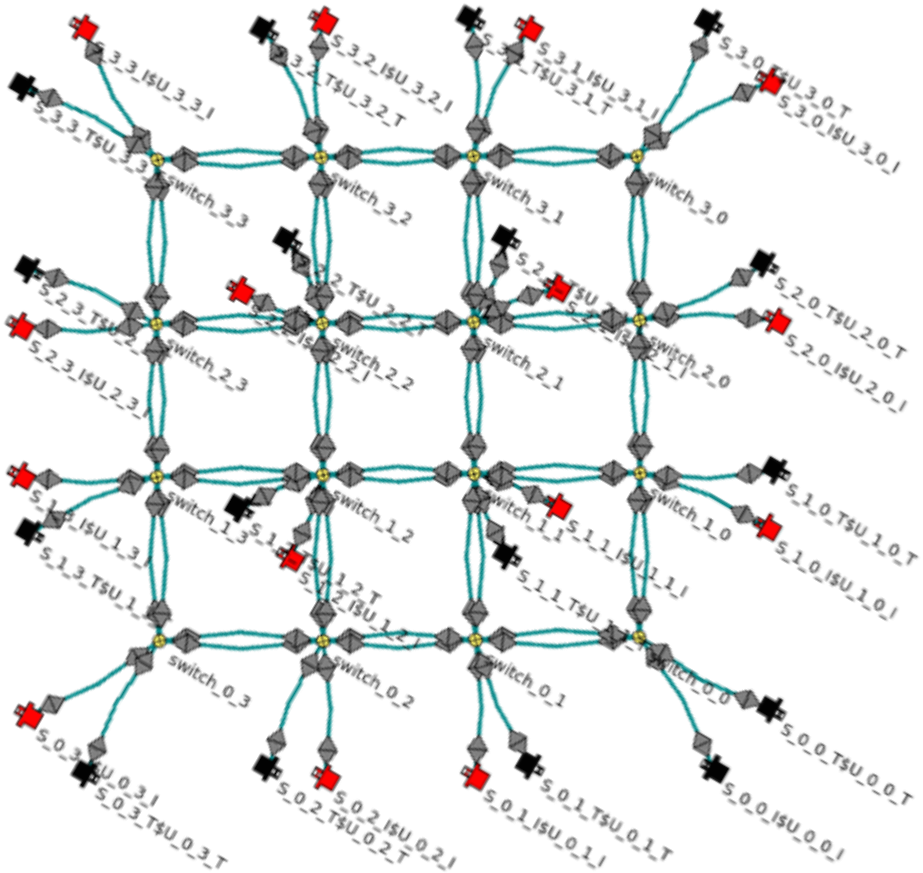
FlexNoC 5 connects the AI core accelerator units

AI/ML Accelerator SoC

AI Bandwidth Demands Met with FlexNoC 5 XL

- FlexNoC ® 5 XL addresses non-coherent bandwidth requirements of AI/ML systems
  - Large capacity mesh generator
  - Up to 1024-bit wide connections
  - Up to 200 Network Interface Units (NIUs)
  - Up to 512 Pending transactions
- Quality of Service ensured by virtual channels
- Multi-Cast/Broadcast Stations
  - Broadcast to multiple units to reduce bandwidth



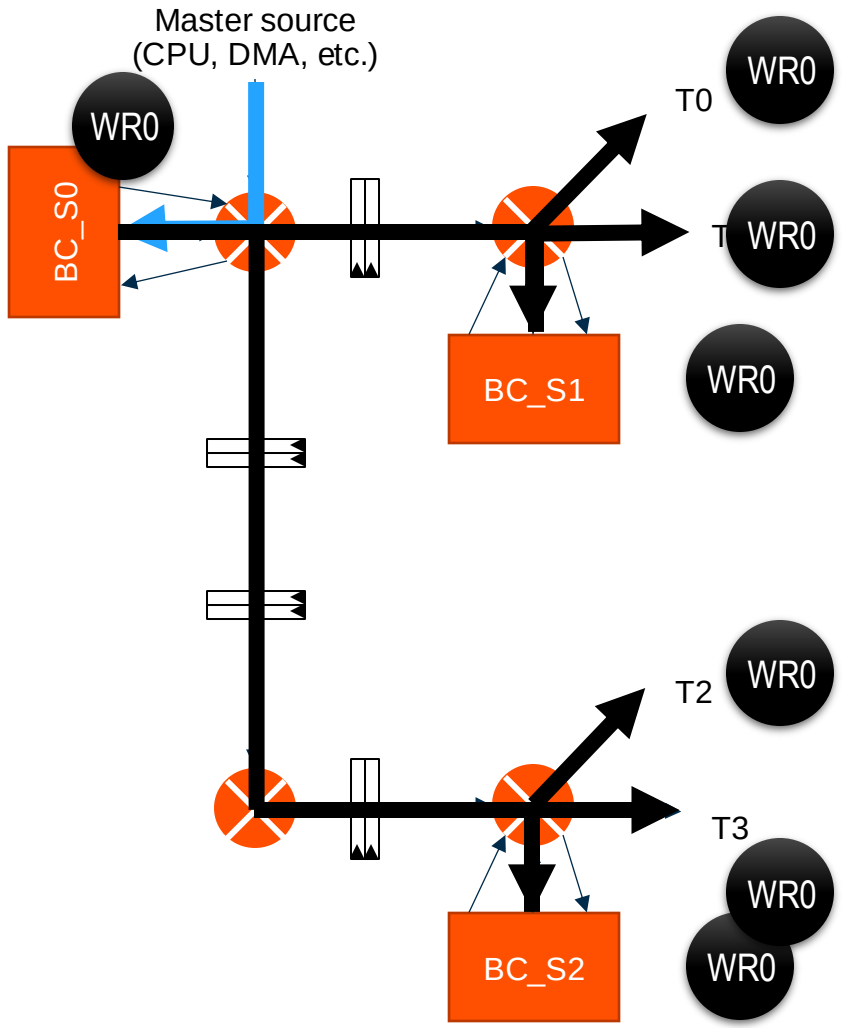


ARTERIS IP

FlexNoC Intelligent Multicast Write

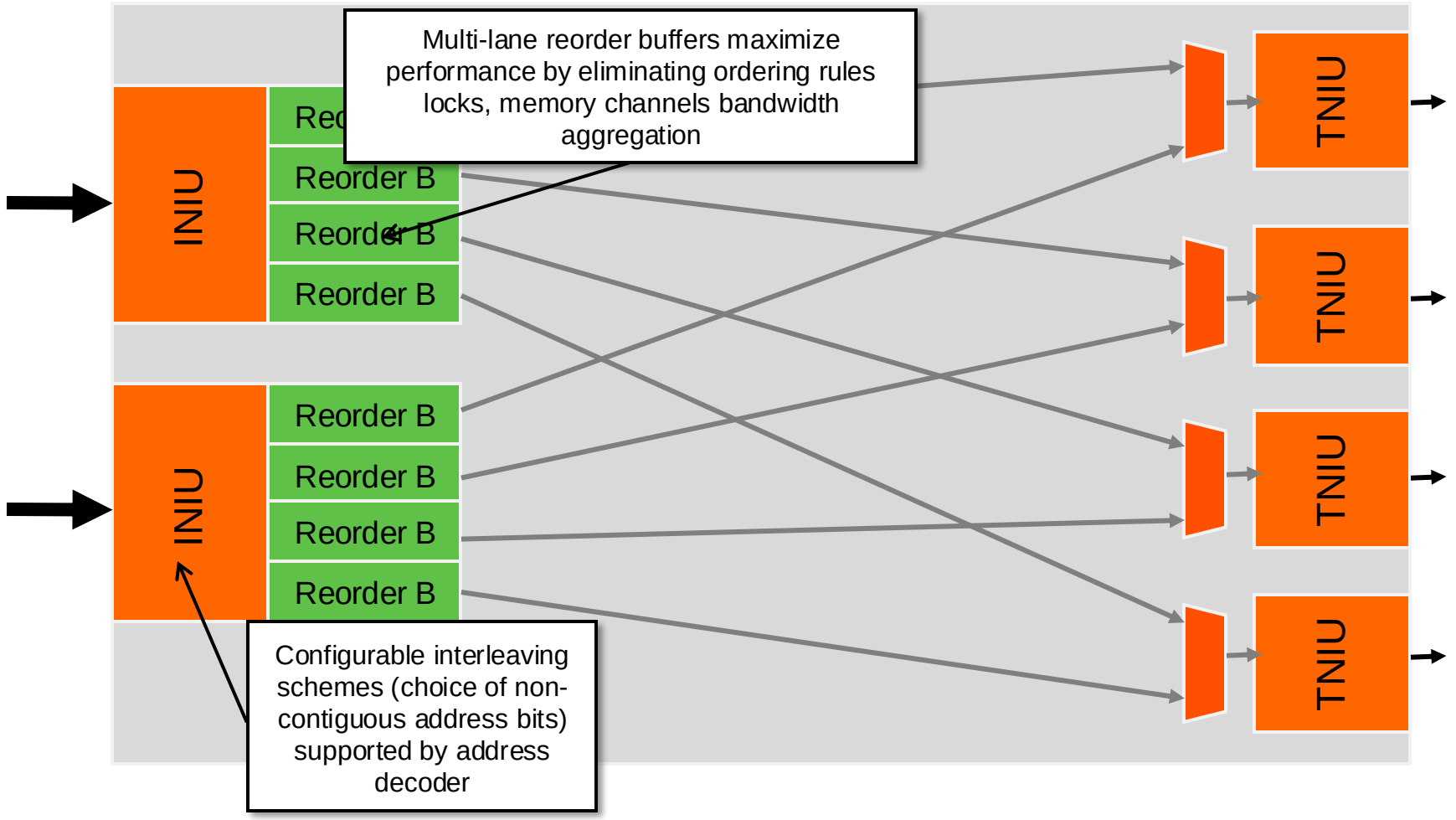
Efficient multicast – bandwidth saving

- Broadcast station optimizes use of NoC bandwidth
  - Broadcasts performed as close as possible to the destination
  - Any number of broadcast stations in a FlexNoC
- Writing to broadcast station will cause it to send posted writes to multiple destinations
- Used in AI for DNN weight and image map updates



High Memory Bandwidth from Interleaving Channels

- Up to 8 or 16 channels interleave
- Read-reorder buffers
- Traffic aggregation / data width conversions
- Up to 1024 bits wide connections



ARTERIS IP

Improved Productivity & Configurability

Save time and resources with library reuse and automation

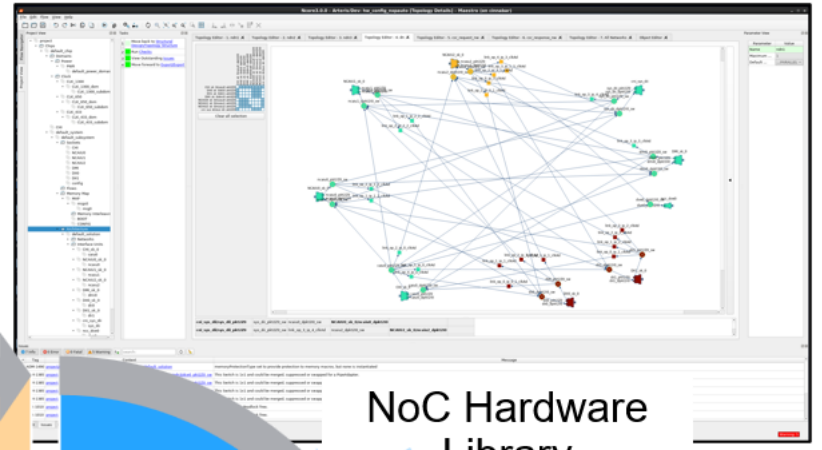
Manual "from scratch" development

Quick estimates, simplified assumptions:
Area, performance, timing closure, power

Manually-created topologies

Change requests:
- Add/remove interfaces
- User bits, QoS, address map, safety, buffering, service, probes, interrupts, modules, etc.
- **… cause significant changes to RTL**

Floorplan & timing closure issues:
- Add/remove interfaces
- Interface location, blockages, fences
- Iterations for timing
- **… causing even more changes**



NoC Hardware Library

Chip Specification
- Power/clock domains
- Floorplan
- Subsystems
- Memory Maps

Inputs

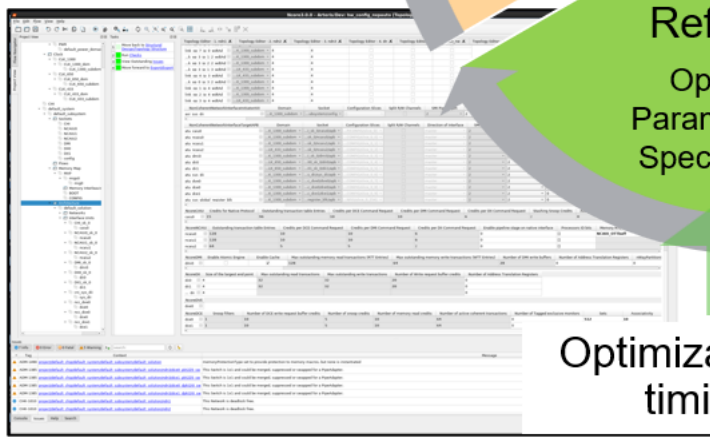
Architecture
Topology
Routing
Architectural Choices

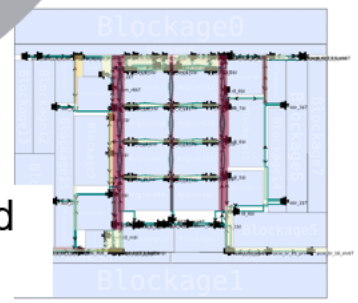
Mapping
Automatic choice of library elements

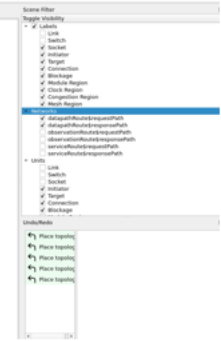
Refinement
Optimization
Parameter Tuning
Special Features

Outputs

RTL
Scripts
Docs
Collateral

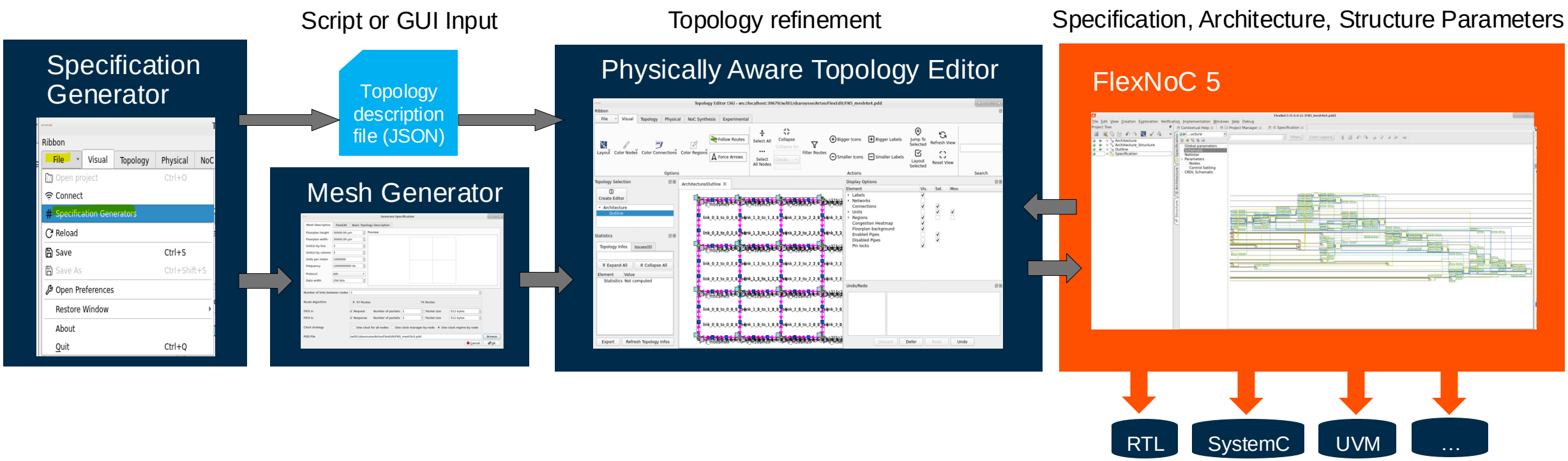






Optimization goals and timing closure

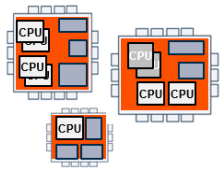
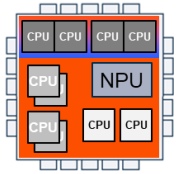
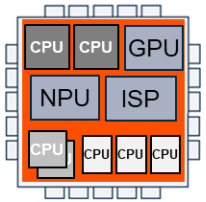
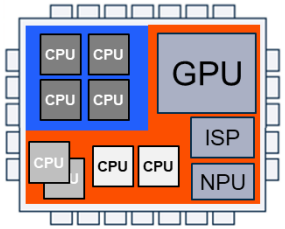
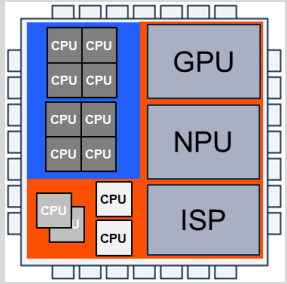
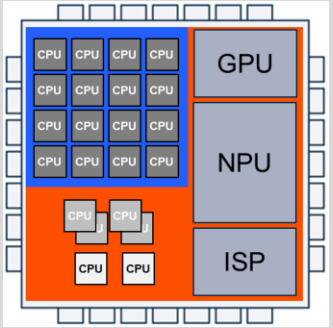
FlexNoC Physically-Aware Mesh Topology Generator Flow



SystemC and UVM models enable system level simulation

Automotive Domains and Their Complexity

Cache coherency is required in safety-critical systems

Auto MCU	Zonal Controller	Vision	Cockpit	L2+ ADAS	Autonomous
					
Non-coherent	Coherent or non-coherent	Mostly non-coherent	Mix of coherent and non-coherent	Mix of coherent and non-coherent, some with large coherent meshes	Mix of coherent and non-coherent, large coherent meshes
					
Monolithic	Monolithic	Maybe chiplet (Sensors!)	Monolithic or maybe chiplet	Monolithic, trending towards chiplet	Likely mostly chiplet in the future

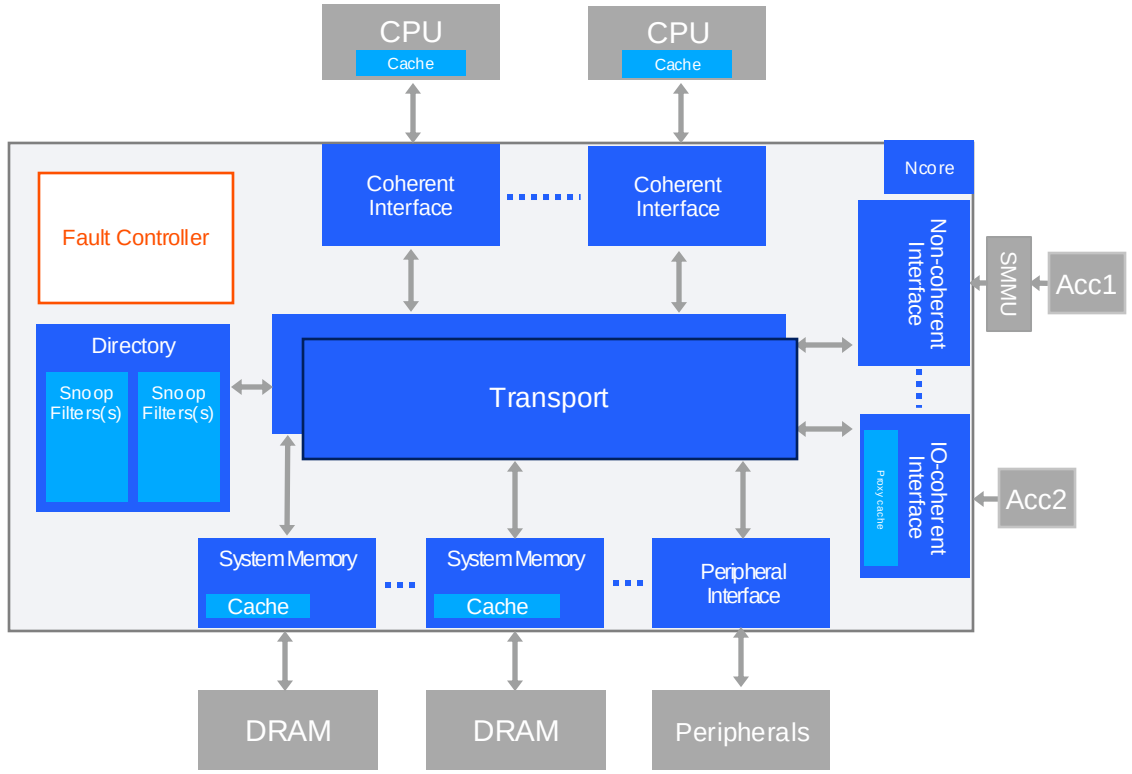
Chiplets increasingly important in future

CPU Application CPU Real Time CPU Microcontroller Cache coherent NoC Non-coherent NoCs

ARTERIS IP

Challenge of Safety-certification for Coherent Systems

Automotive ADAS/autonomous driving is a key application of AI/ML



- The complexity of coherent systems makes safety certification especially challenging
- Ncore 3 safety/resilience capabilities:
  - External ECC or parity
  - Interface ECC or parity
  - Interface duplication
  - Cache/SF ECC or parity
  - Transport link ECC or parity
  - Directory duplication
  - Fault controller/signaling


Certificate / Certificat
Zertifikat / 合格証

Arteris 21/05-038 C001

exida hereby confirms that the:

Arteris Ncore 3.4

Arteris, Inc.
Campbell (CA), USA

Has been assessed per the relevant requirements of:

ISO 26262 : 2018 Parts 2, 4, 5, 7, 8 and 9

and meets the requirements providing a level of integrity to:

Systematic Capability: ASIL D

Revision 1.0 October 30, 2023
Surveillance Audit Due
November 1, 2026

Safety related function:
The Arteris Ncore 3.4 IP is a configurable cache coherent interconnect that was developed as a Hardware Safety Element out of Context (SEooC) with the following assumed top-level safety requirements:

- Data coherency shall be ensured
- The integrity of transactions between agents shall be ensured
- The integrity of memory data shall be ensured
- The integrity of the Ncore configuration shall be ensured
- Faults shall be signaled via a fault reporting unit

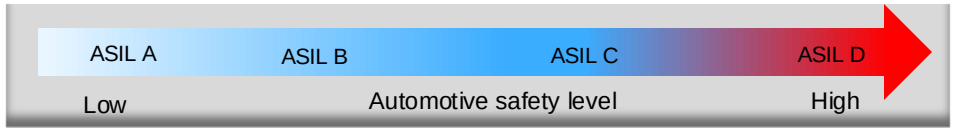
Application restrictions:
The Ncore 3.4 shall be used according to the requirements described in the Arteris Safety Manual.

Evaluating Assessor

Certifying Assessor

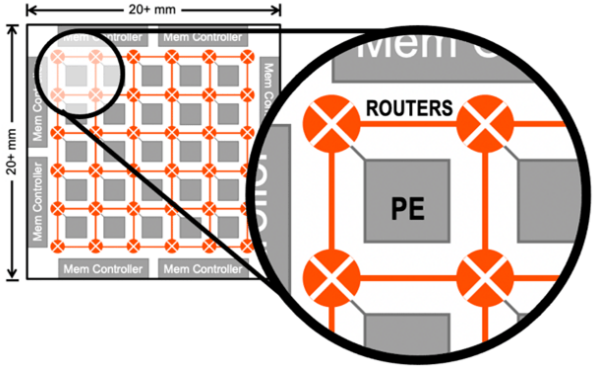
Page 1 of 2

Ncore 3.4 is ISO 26262 ASIL D certified



Summary

- Separate shared coherent traffic from high-bandwidth traffic where possible
- FlexNoC 5 Network-on-Chip XL option is suited to many complex SoCs
  - Mesh topology for large regular structures that align with physical layout
  - Wide buses for massive AI bandwidths
  - Broadcast writes for simultaneous updates of weights, map updates, and commands to heterogenous functional units
- Tooling environments speed design iterations compared with point solutions
- Ncore is ISO 26262 certified to ASIL D and FlexNoC 5 is available with a safety package enabling safety for AI-enabled automotive
- Chiplets offer an additional optimization opportunity enabling modularity, scaling of systems, and cost reductions due to yield improvement from disaggregation across dies and packages




exida

Certificate / Certificat

Zertifikat / 合格証

Arteris 21/05-038 C001

exida hereby confirms that the:

Arteris Ncore 3.4

Arteris, Inc.
Campbell (CA), USA

The manufacturer may use the mark:

exida CERTIFIED ISO 26262 ASIL D

Has been assessed per the relevant requirements of:

ISO 26262 : 2018 Parts 2, 4, 5, 7, 8 and 9

and meets the requirements providing a level of integrity to:

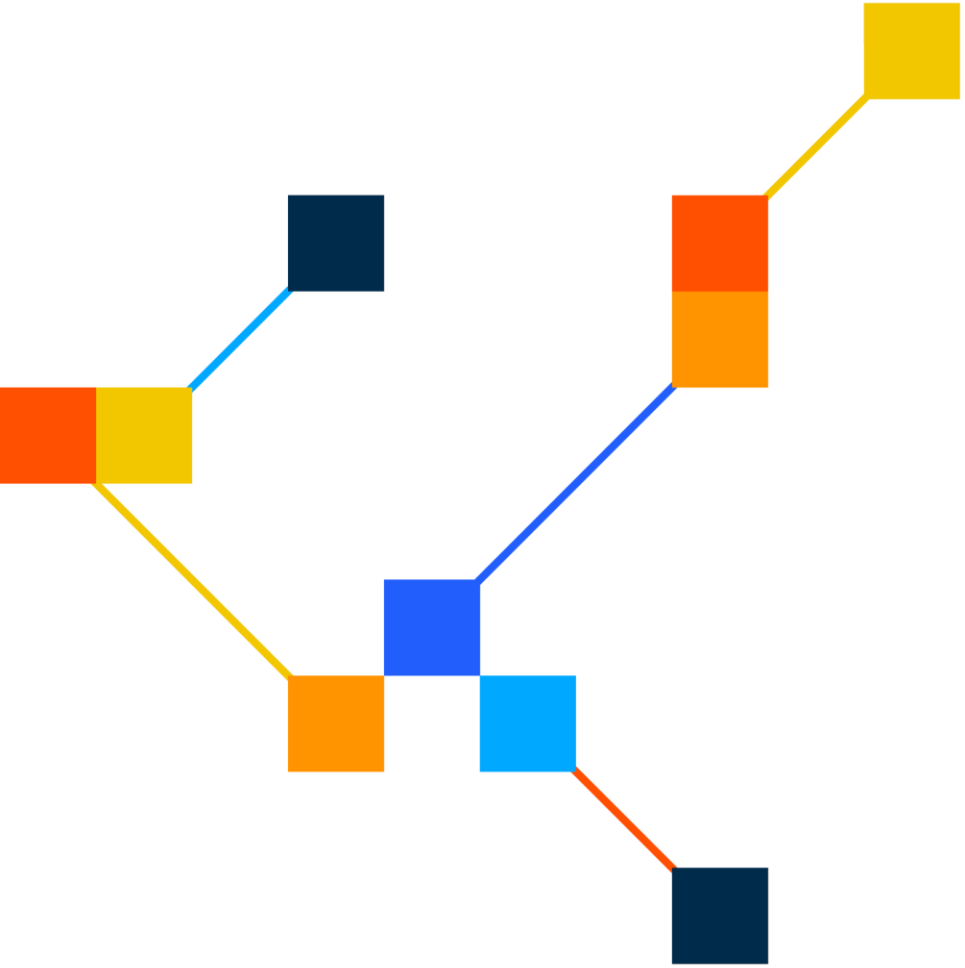
Systematic Capability: ASIL D

Revision 1.0 October 30, 2023
Surveillance Audit Due
November 1, 2026

Safety related function:
The Arteris Ncore 3.4 IP is a configurable cache coherent interconnect that was developed as a Hardware Safety Element out of Context (SEooC) with the following assumed top-level safety requirements:

- Data coherency shall be ensured
- The integrity of transactions between agents shall be ensured
- The integrity of memory data shall be ensured
- The integrity of the Ncore configuration shall be ensured
- Faults shall be signaled via a fault reporting unit

ARTERIS IP



ARTERIS IP

Thank you