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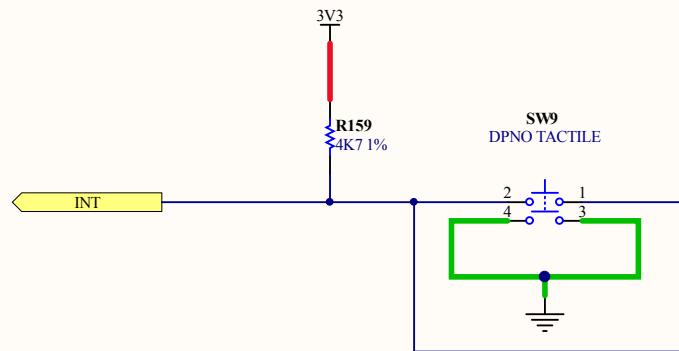
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Sheet Title ***Push Button SPNO Switch***

Project Title ***NanoBoard NB2DSK01***

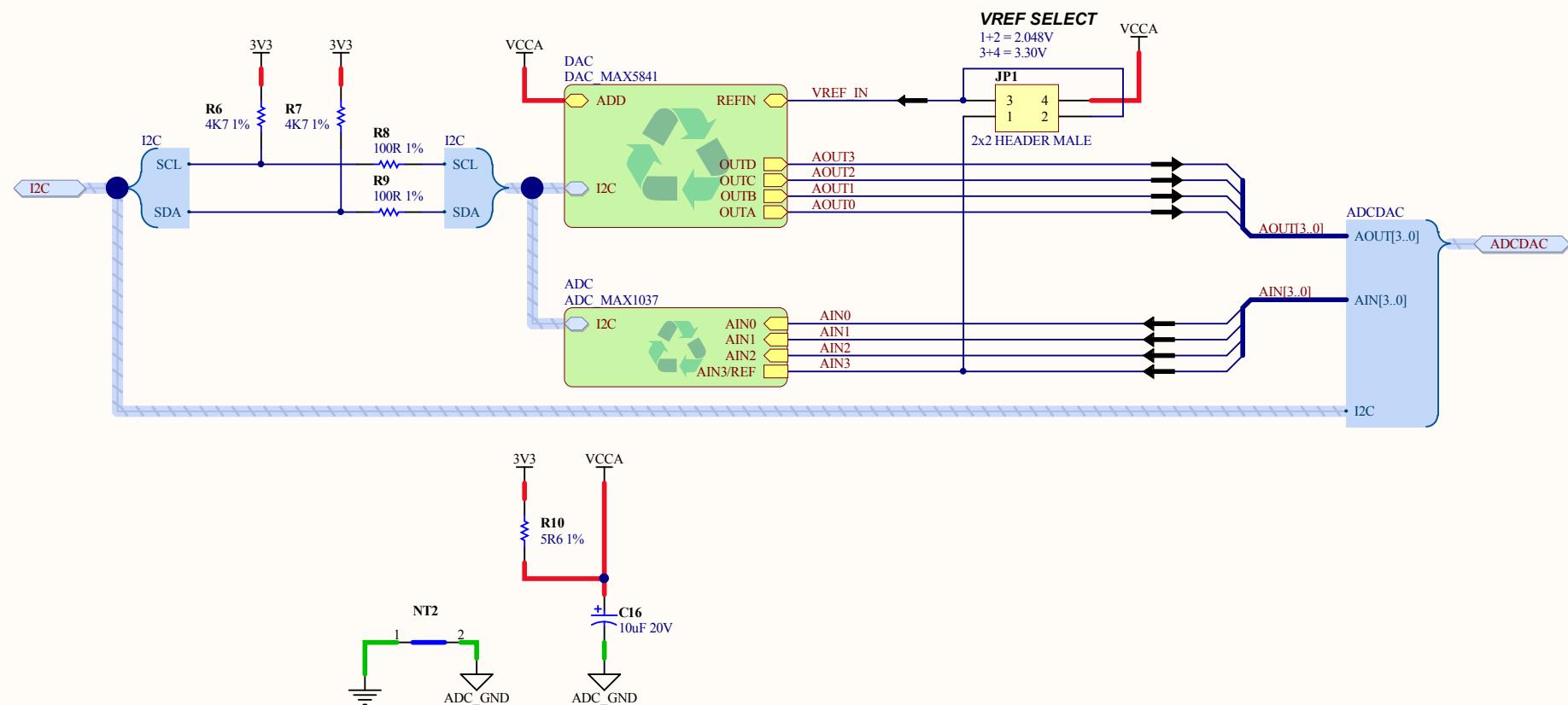
Size: **A4** Assy: **D-810-0007** Revision: **08**

Date: **2/17/2011** Time: **5:49:52 PM** Sheet **2** of **64**

File: **HOST_RESET_SPNO.SCHDOC**

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Sheet Title **4-Ch I₂C 10-Bit DAC & 8-Bit ADC**Project Title **NanoBoard NB2DSK01**Size: **A4** Assy: **D-810-0007** Revision: **08**Date: **2/17/2011** Time: **5:49:52 PM** Sheet **39** of **64**File: **DAC+ADC_MAX5841+MAX1037.SchDoc**

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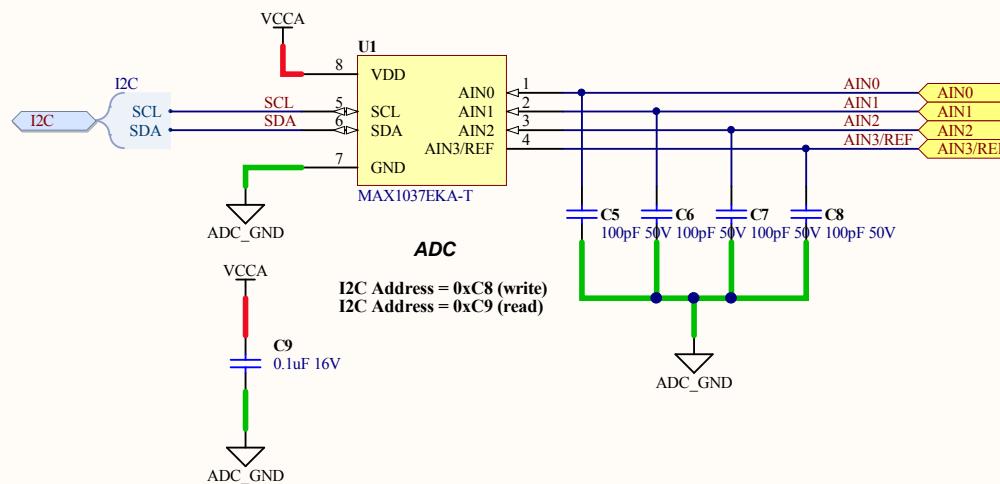
B

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Sheet Title	MAX1037 ADC	
Project Title	NanoBoard NB2DSK01	
Size:	A4	Assy: D-810-0007
Date:	2/17/2011	Time: 5:49:52 PM
File:	ADC_MAX1037.SchDoc	
Revision:	08	Sheet 40 of 64

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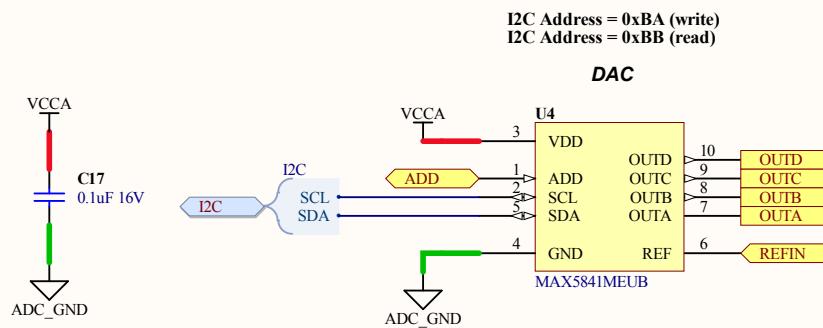
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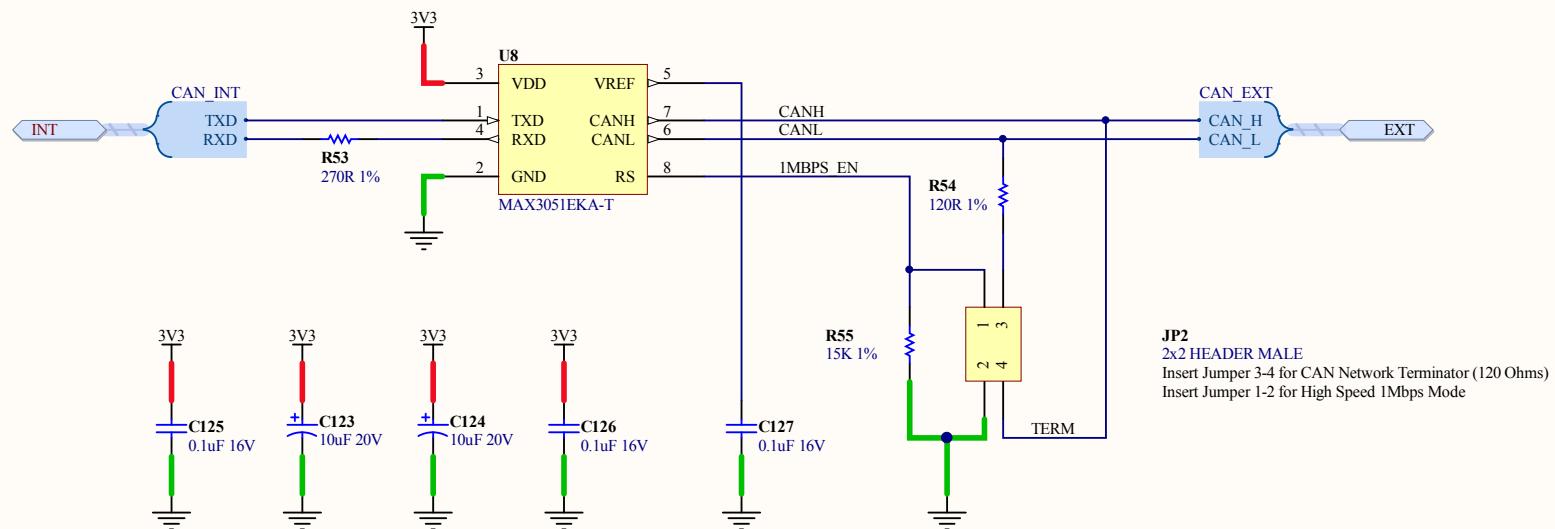
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Sheet Title MAX5841 DAC		
Project Title NanoBoard NB2DSK01		
Size: A4	Assy: D-810-0007	Revision: 08
Date: 2/17/2011	Time: 5:49:53 PM	Sheet 41 of 64
File: DAC_MAX5841.SchDoc		

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Sheet Title **CAN Transceiver MAX3051**Project Title **NanoBoard NB2DSK01**Size: **A4** Assy: **D-810-0007** Revision: **08**Date: **2/17/2011** Time: **5:49:53 PM** Sheet **58** of **64**File: **CAN_MAX3051.SchDoc**

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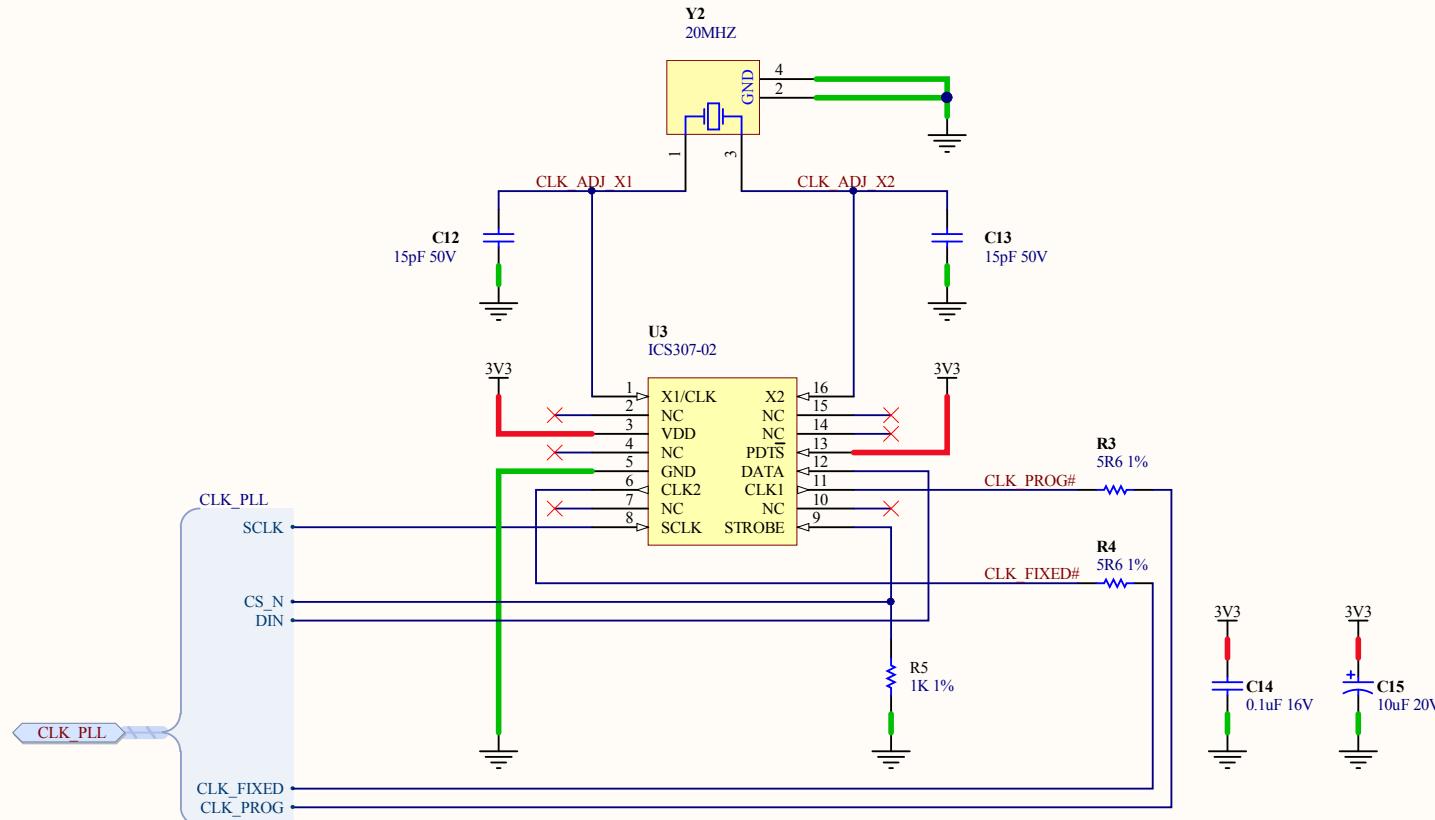
B

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Sheet Title **Programmable SPI Clock**Project Title **NanoBoard NB2DSK01**Size: **A4** Assy: **D-810-0007** Revision: **08**Date: **2/17/2011** Time: **5:49:53 PM** Sheet **11** of **64**File: **CLK_IKS307-02_PLL.SchDoc**

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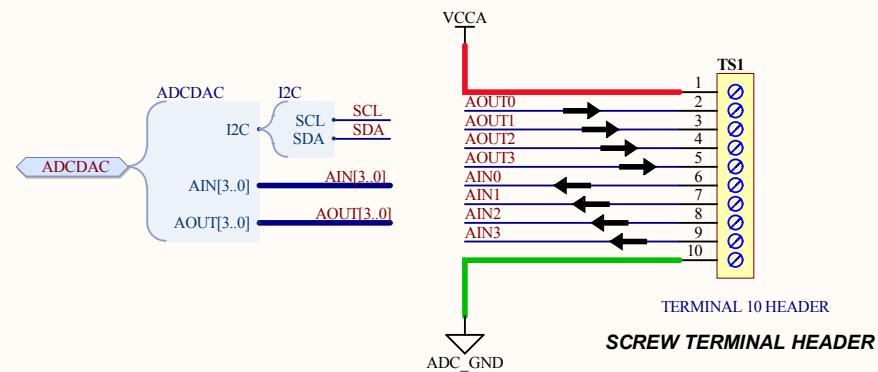
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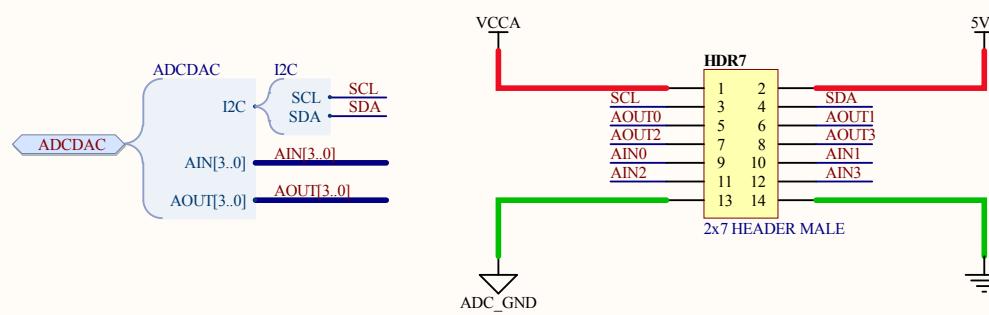
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Sheet Title ***ADC / DAC Screw Header***Project Title ***NanoBoard NB2DSK01***Size: **A4** Assy: **D-810-0007** Revision: **08**Date: **2/17/2011** Time: **5:49:53 PM** Sheet **55** of **64**File: **CON_ADCDAC_SCRSTR10F.SchDoc**

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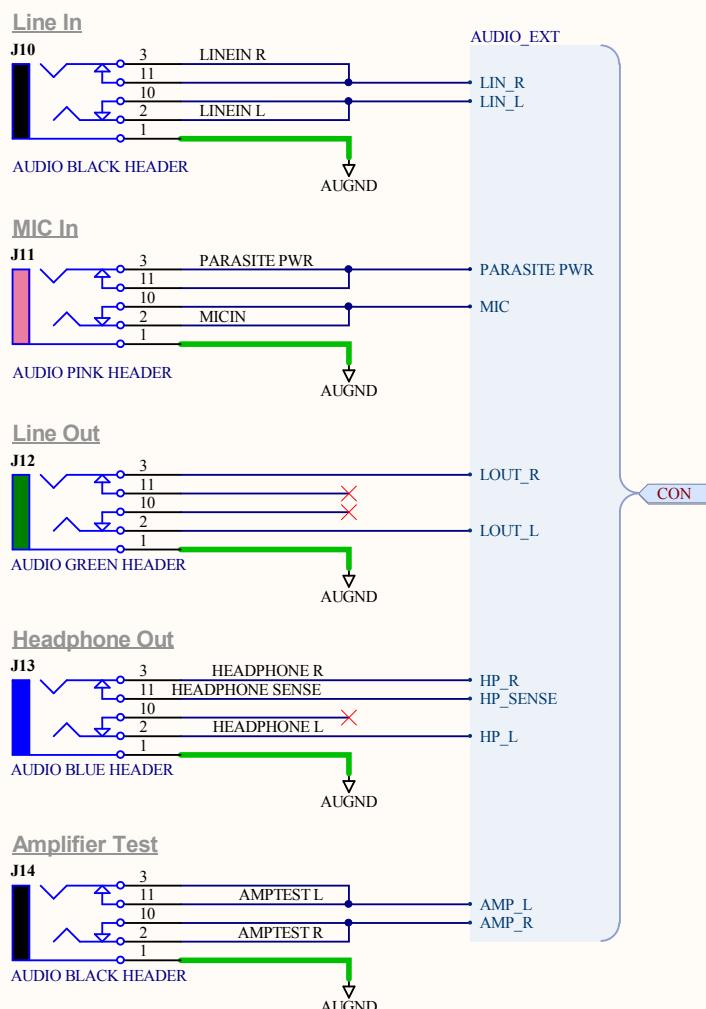


Sheet Title ADC / DAC Header		
Project Title NanoBoard NB2DSK01		
Size: A4	Assy: D-810-0007	Revision: 08
Date: 2/17/2011	Time: 5:49:53 PM	Sheet 52 of 64
File: CON_ADCDAC_HDR14M.SchDoc		

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Sheet Title **AUDIO AC99 Interface**Project Title **NanoBoard NB2DSK01**Size: **A4** Assy: **D-810-0007** Revision: **08**Date: **2/17/2011** Time: **5:49:53 PM** Sheet **54** of **64**File: **CON_AUDIO_AC99.SchDoc**

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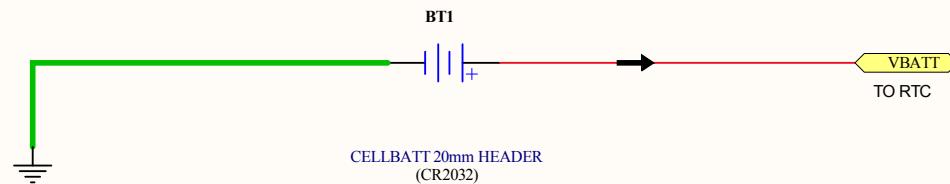
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Sheet Title Lithium Batter Holder - CR2032		
Project Title NanoBoard NB2DSK01		
Size: A4	Assy: D-810-0007	Revision: 08
Date: 2/17/2011	Time: 5:49:53 PM	Sheet 49 of 64
File: CON_BATT_COIN.SchDoc		

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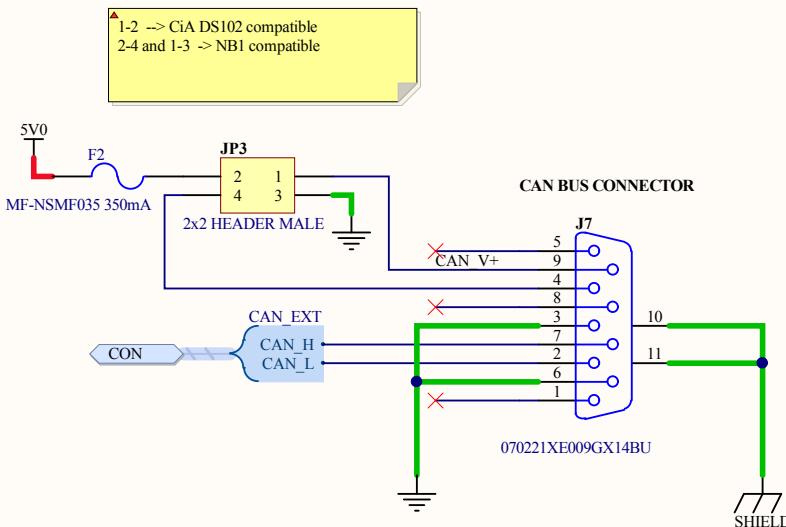
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Sheet Title **CAN Connector DB9 Male**

Project Title **NanoBoard NB2DSK01**

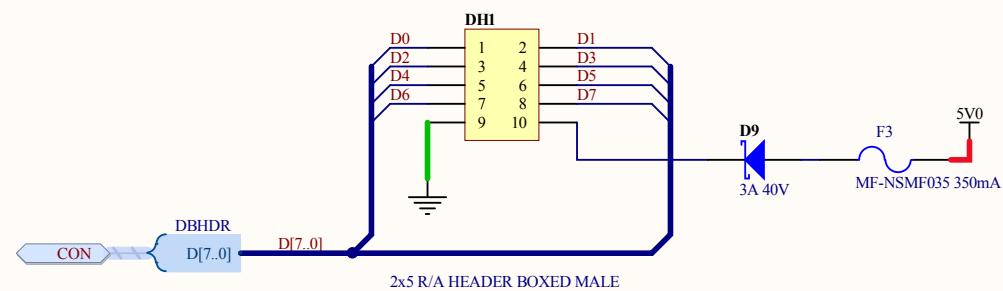
Size: **A4** Assy: **D-810-0007** Revision: **08**

Date: **2/17/2011** Time: **5:49:53 PM** Sheet **51** of **64**

File: **CON CAN DB9M.SchDoc**

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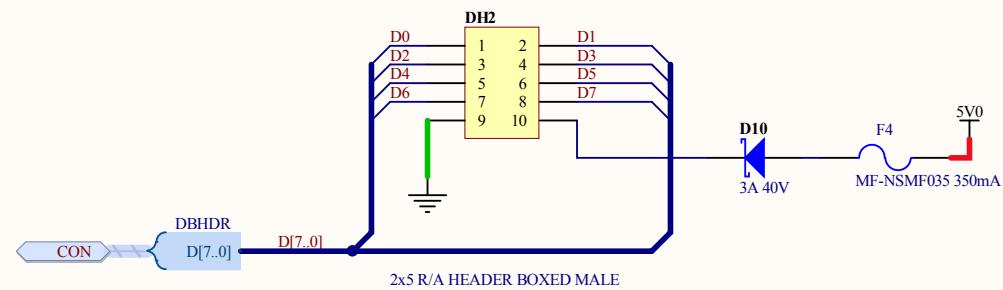




Sheet Title	8-Way Debug Header		
Project Title	NanoBoard NB2DSK01		
Size:	A4	Assy:	D-810-0007
Date:	2/17/2011	Time:	5:49:53 PM
File:	CON DEBUG 10WBOXHDRAM.SchDoc	Revision:	08
Sheet	43	of	64

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Sheet Title	8-Way Debug Header
Project Title	NanoBoard NB2DSK01
Size:	A4
Assy:	D-810-0007
Revision:	08
Date:	2/17/2011
Time:	5:49:53 PM
Sheet	43 of 64
File:	CON DEBUG 10WBOXHDRAM.SchDoc

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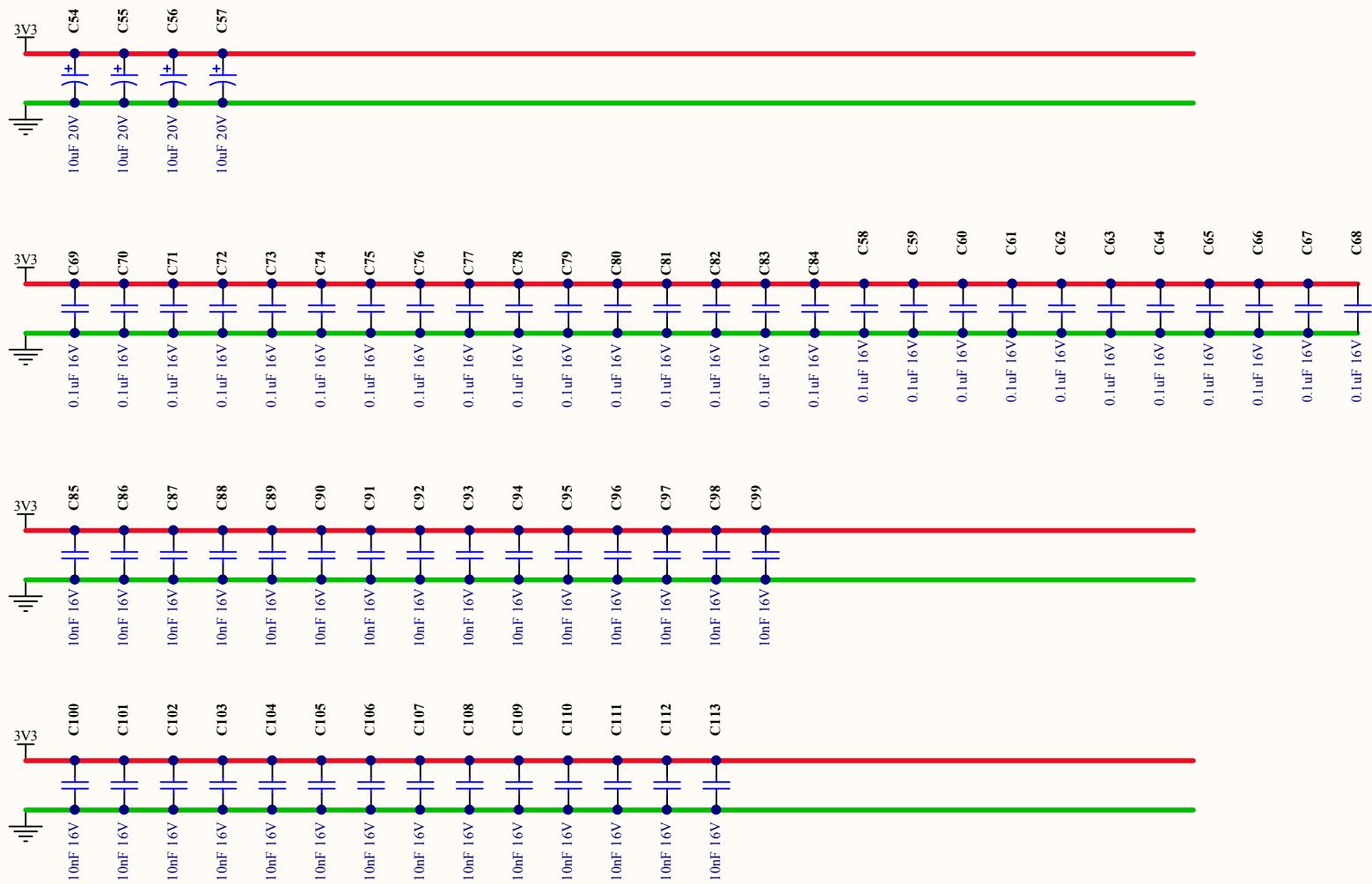
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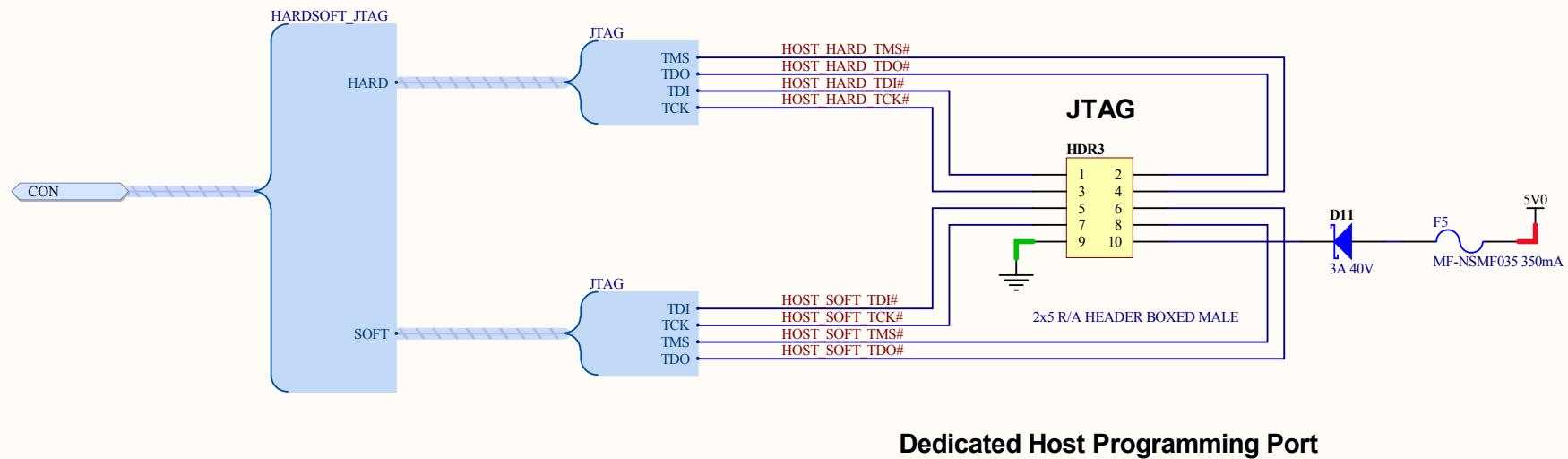


► The FPGA bypass capacitors are physically grouped as 10nF and 100nF pairs on all major accessible power pins on the FPGA.

Sheet Title	FPGA Bypass 3V3	
Project Title	NanoBoard NB2DSK01	
Size:	A4	Assy: D-810-0007
Date:	2/17/2011	Time: 5:49:53 PM
File:	FPGA_Bypass_3V3.SCHDOC	
Revision:	08	
Sheet	15	of 64

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Sheet Title	Host JTAG Header	
Project Title	NanoBoard NB2DSK01	
Size:	A4	Assy: D-810-0007
Date:	2/17/2011	Time: 5:49:54 PM
File:	CON_HOSTJTAG_10WBOXHDRAM.SchDoc	
Revision:	08	
Sheet	42	of 64

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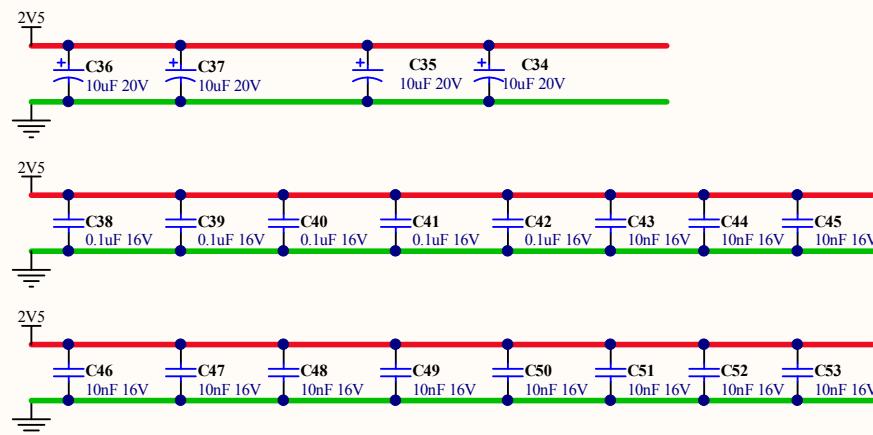
B

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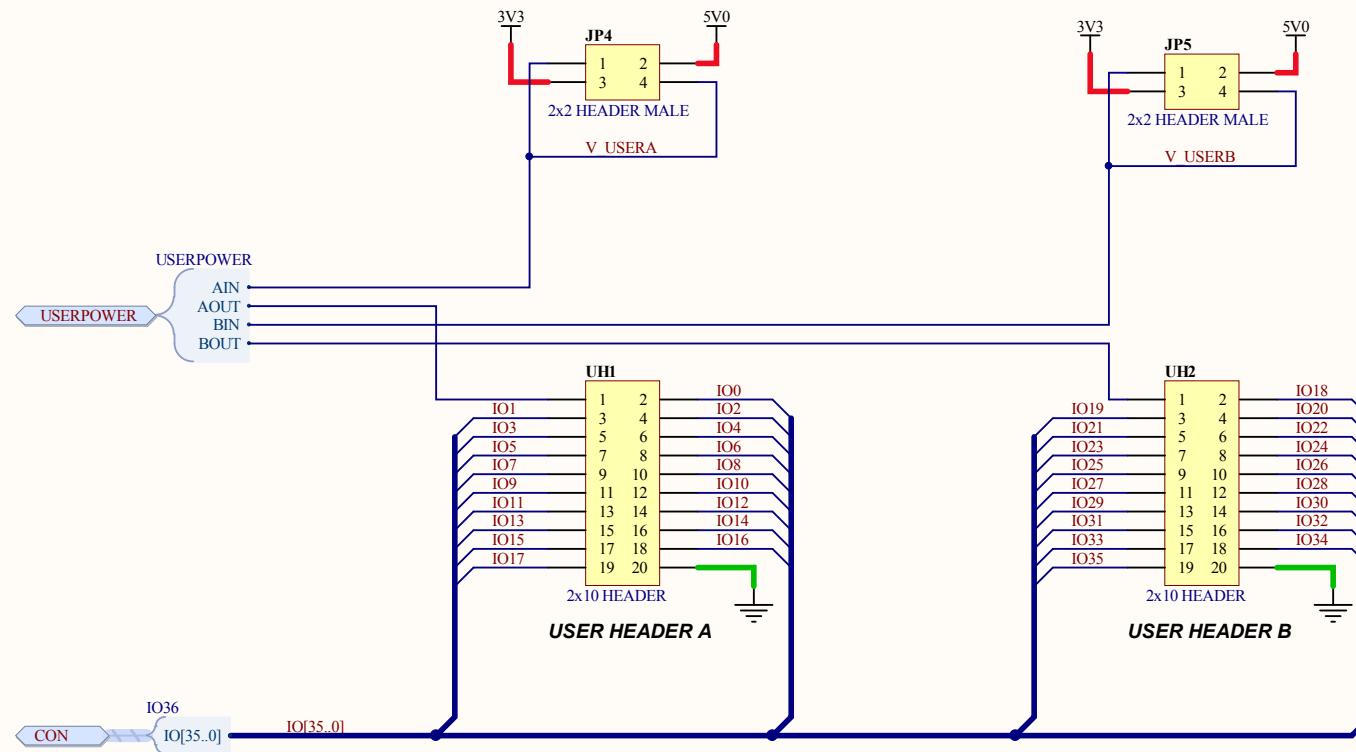


Sheet Title	FPGA Bypass 2V5
Project Title	NanoBoard NB2DSK01
Size:	A4
Assy:	D-810-0007
Revision:	08
Date:	2/17/2011
Time:	5:49:54 PM
Sheet	16 of 64
File:	FPGA_Bypass_2V5.SCHDOC

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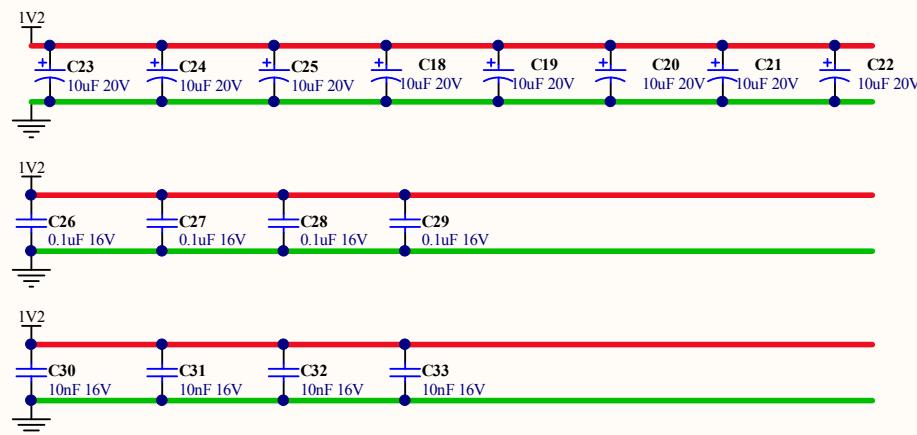


A

Sheet Title **36-Way User I/O Headers**Project Title **NanoBoard NB2DSK01**Size: **A4** Assy: **D-810-0007** Revision: **08**Date: **2/17/2011** Time: **5:49:54 PM** Sheet **46** of **64**File: **CON_USER_20WBOXHDRAMx2.SCHDOC**

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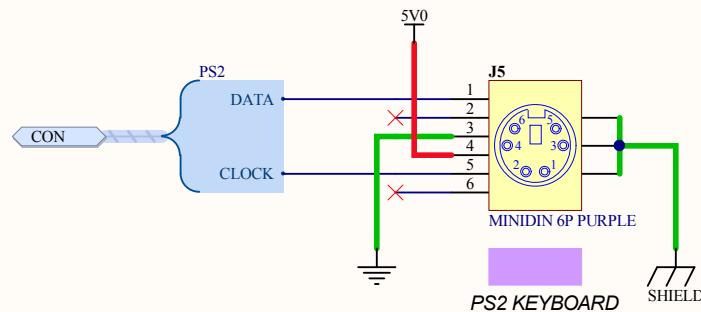




Sheet Title	FPGA Bypass 1V2	
Project Title	NanoBoard NB2DSK01	
Size:	A4	Assy: D-810-0007
Date:	2/17/2011	Time: 5:49:54 PM
File:	FPGA_Bypass_1V2.SCHDOC	Sheet 17 of 64
Revision:	08	

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Sheet Title ***PS2 Keyboard Connector***

Project Title ***NanoBoard NB2DSK01***

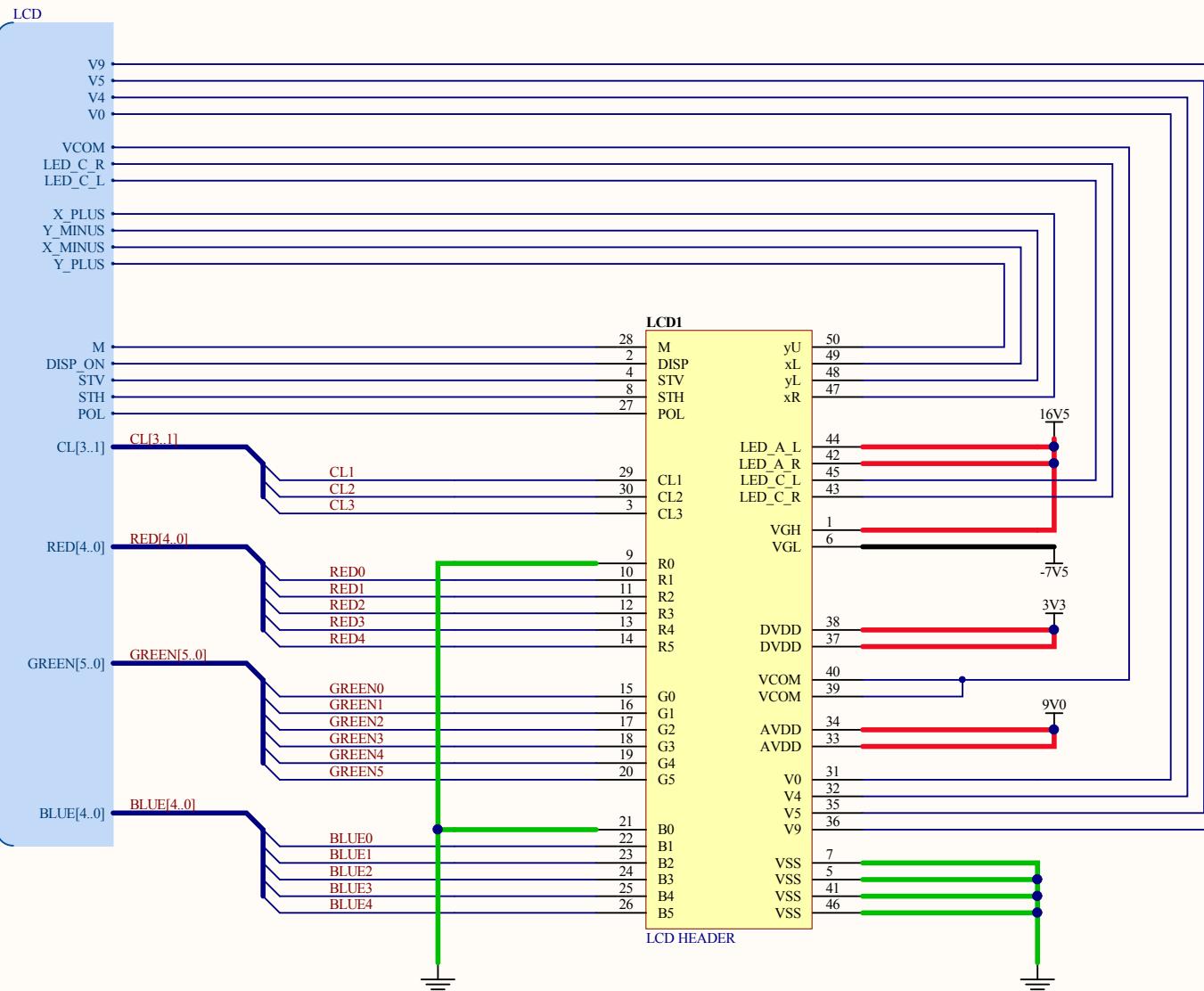
Size: **A4** Assy: **D-810-0007** Revision: **08**

Date: **2/17/2011** Time: **5:49:54 PM** Sheet **53** of **64**

File: **CON_PS2KEYBOARD_MINIDIN6.SchDoc**

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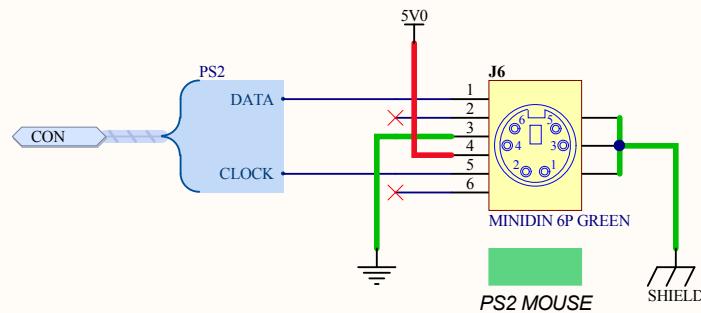
Touch-Screen Connector



Sheet Title	TFT LCD Header	
Project Title	NanoBoard NB2DSK01	
Size:	A4	Assy: D-810-0007
Date:	2/17/2011	Time: 5:49:54 PM
File:	CON_LCD_TX09D50VMICAA.SchDoc	
Revision:	08	
Sheet	48	of 64

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Sheet Title ***PS2 Mouse Connector***

Project Title ***NanoBoard NB2DSK01***

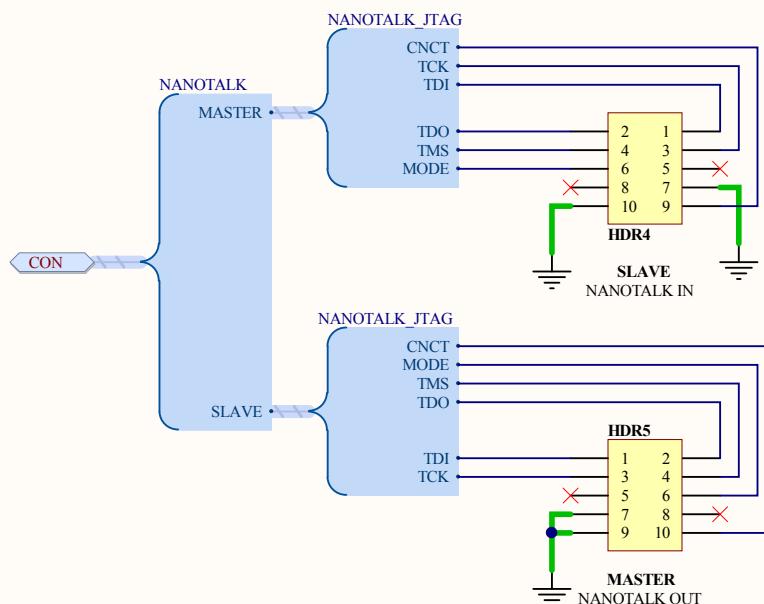
Size: **A4** Assy: **D-810-0007** Revision: **08**

Date: **2/17/2011** Time: **5:49:54 PM** Sheet **20** of **64**

File: **CON_PS2MOUSE_MINIDIN6F.SchDoc**

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Sheet Title ***NanoTalk JTAG Headers***

Project Title ***NanoBoard NB2DSK01***

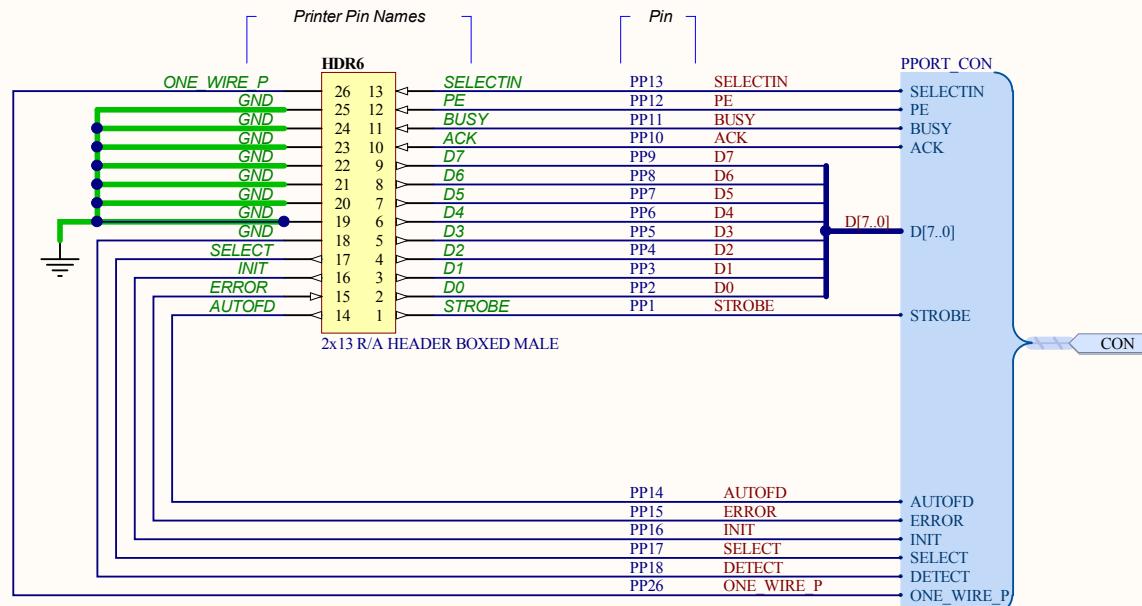
Size: **A4** Assy: **D-810-0007** Revision: **08**

Date: **2/17/2011** Time: **5:49:54 PM** Sheet **45** of **64**

File: **CON_NANOTALK_10WHDRAMx2.SchDoc**

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Sheet Title **PC Parallel Port + 1-Wire**Project Title **NanoBoard NB2DSK01**

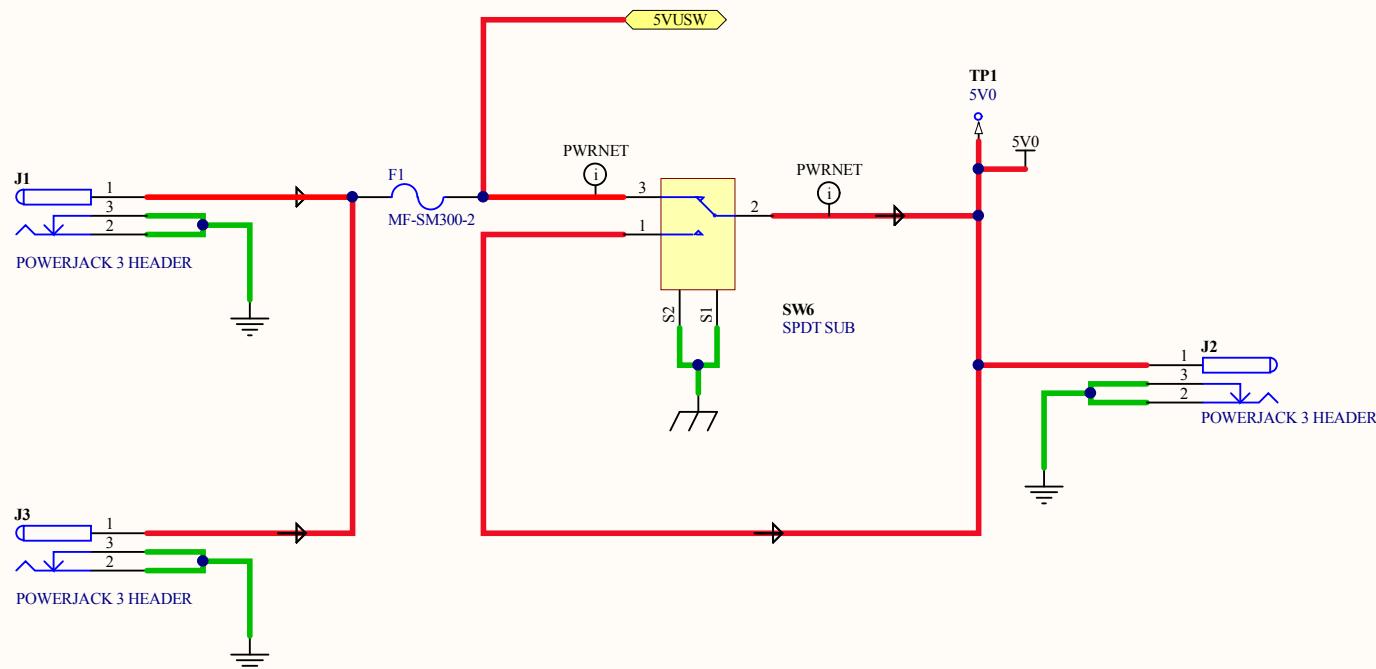
Size: A4 Assy: D-810-0007 Revision: 08

Date: 2/17/2011 Time: 5:49:54 PM Sheet 47 of 64

File: CON_PCP.PORT_26WBOXHDRAM.SchDoc

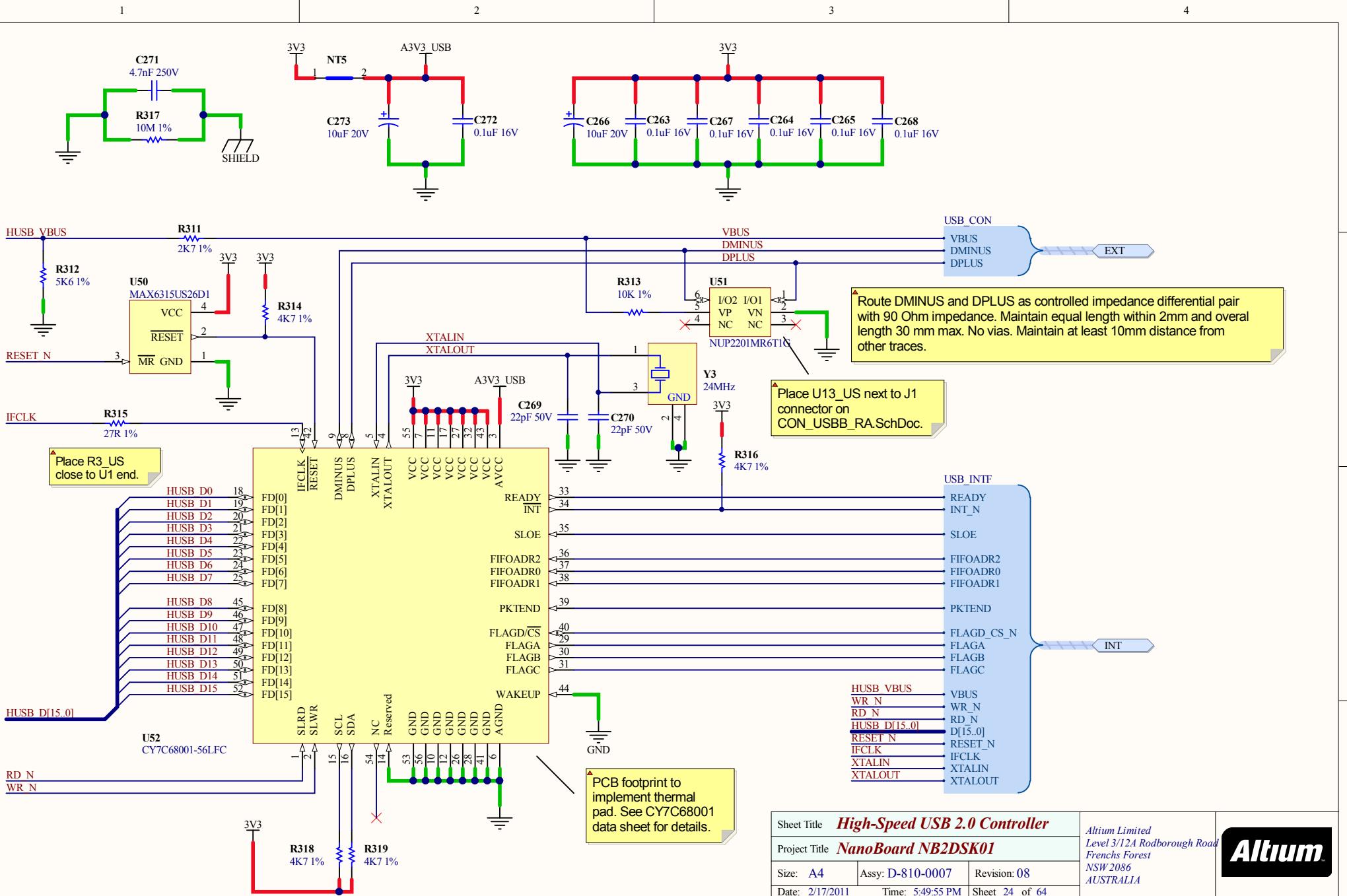
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Sheet Title **Power Jack & Switch**Project Title **NanoBoard NB2DSK01**Size: **A4** Assy: **D-810-0007** Revision: **08**Date: **2/17/2011** Time: **5:49:54 PM** Sheet **62** of **64**File: **PWJACK+SWITCH.SchDoc**

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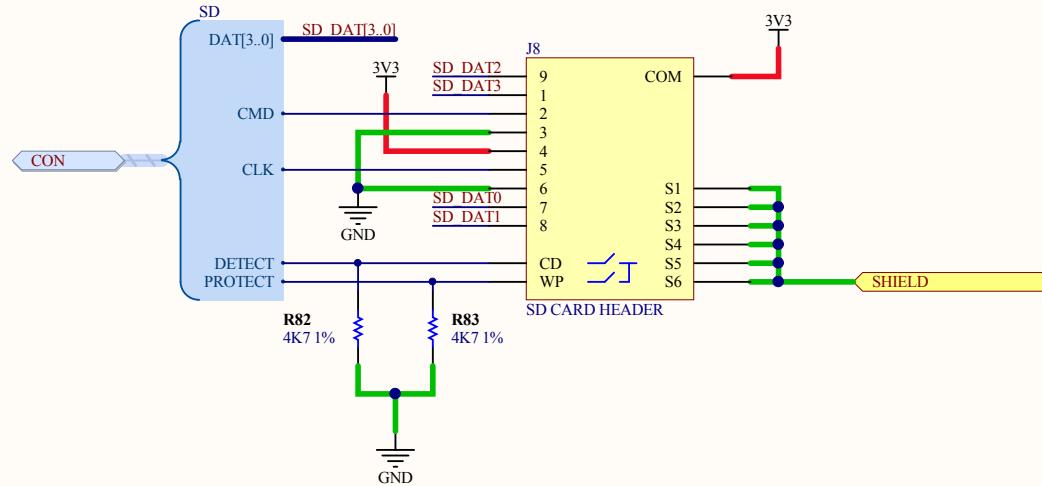


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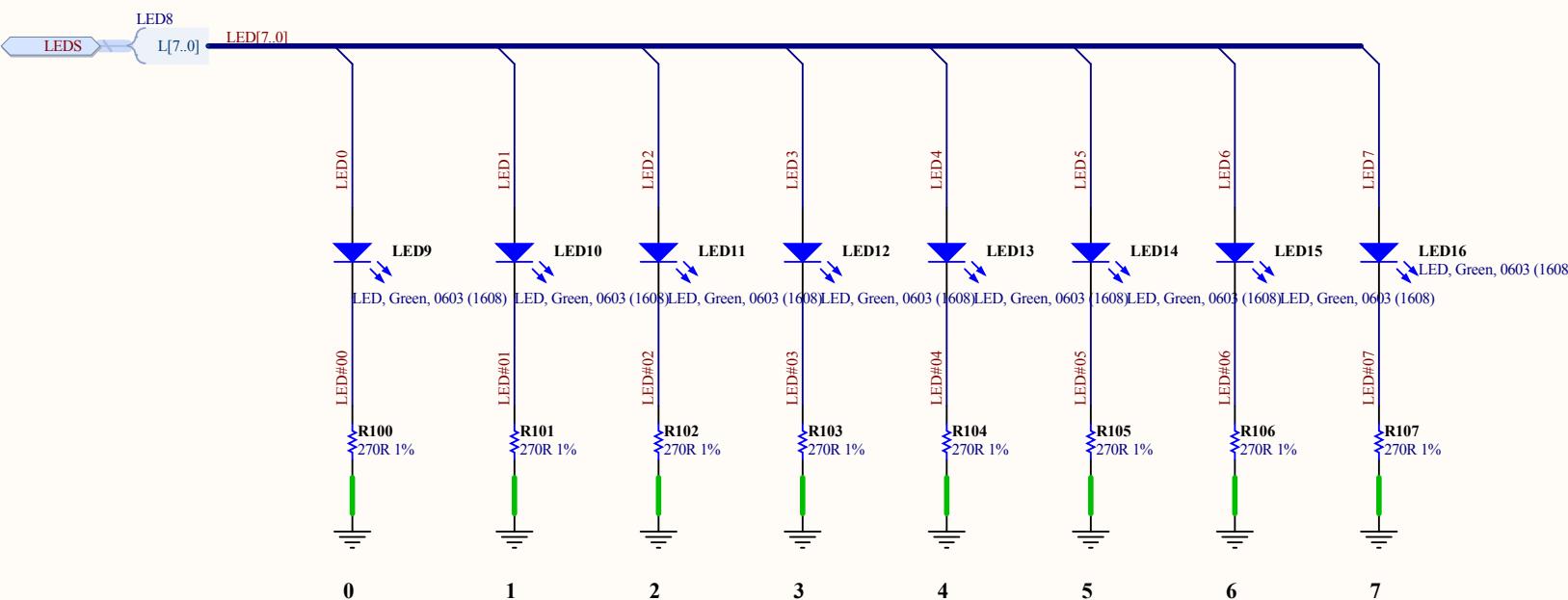
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Sheet Title	SD-CARD HIROSE 609_0003_5		<i>Altium Limited Level 3/12A Rodborough Road Frenchs Forest NSW 2086 AUSTRALIA</i>	
Project Title	NanoBoard NB2DSK01			
Size:	A4	Assy: D-810-0007	Revision: 08	
Date:	2/17/2011	Time: 5:49:55 PM	Sheet 56 of 64	
File:	CON SD HIROSE 609_0003_5.SchDoc			

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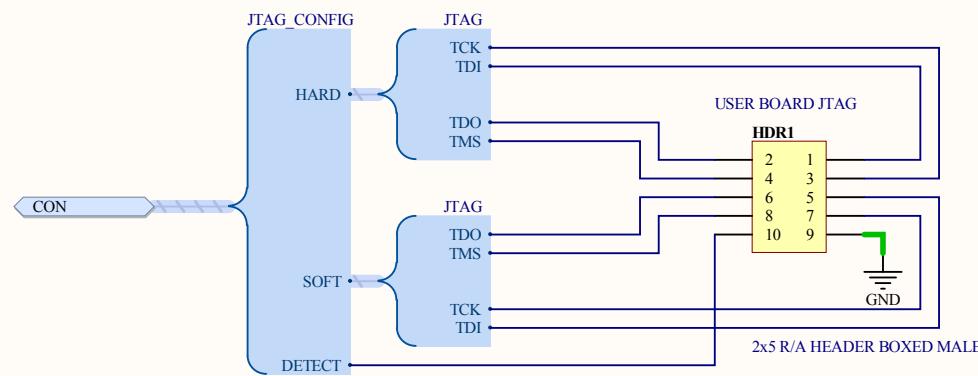
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Sheet Title **8-Way 0603 Green LED Array**Project Title **NanoBoard NB2DSK01**Size: **A4** Assy: **D-810-0007** Revision: **08**Date: **2/17/2011** Time: **5:49:55 PM** Sheet **25** of **64**File: **LED_GREEN_0603x8.SCHDOC**

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Sheet Title **User-Board JTAG Header**

Project Title **NanoBoard NB2DSK01**

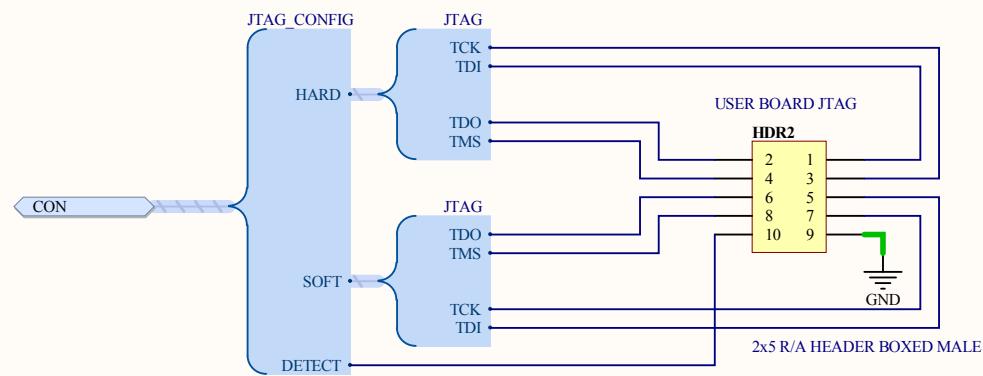
Size: **A4** Assy: **D-810-0007** Revision: **08**

Date: **2/17/2011** Time: **5:49:55 PM** Sheet **44** of **64**

File: **CON_USERITAG_10WBOXHDRRAM.SchDoc**

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Sheet Title **User-Board JTAG Header**

Project Title **NanoBoard NB2DSK01**

Size: **A4** Assy: **D-810-0007** Revision: **08**

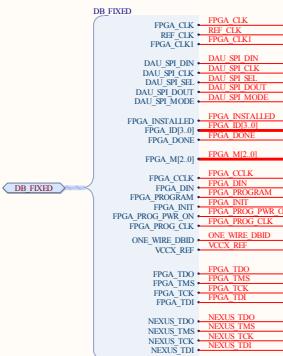
Date: **2/17/2011** Time: **5:49:55 PM** Sheet **44** of **64**

File: **CON_USERITAG_10WBOXHDRRAM.SchDoc**

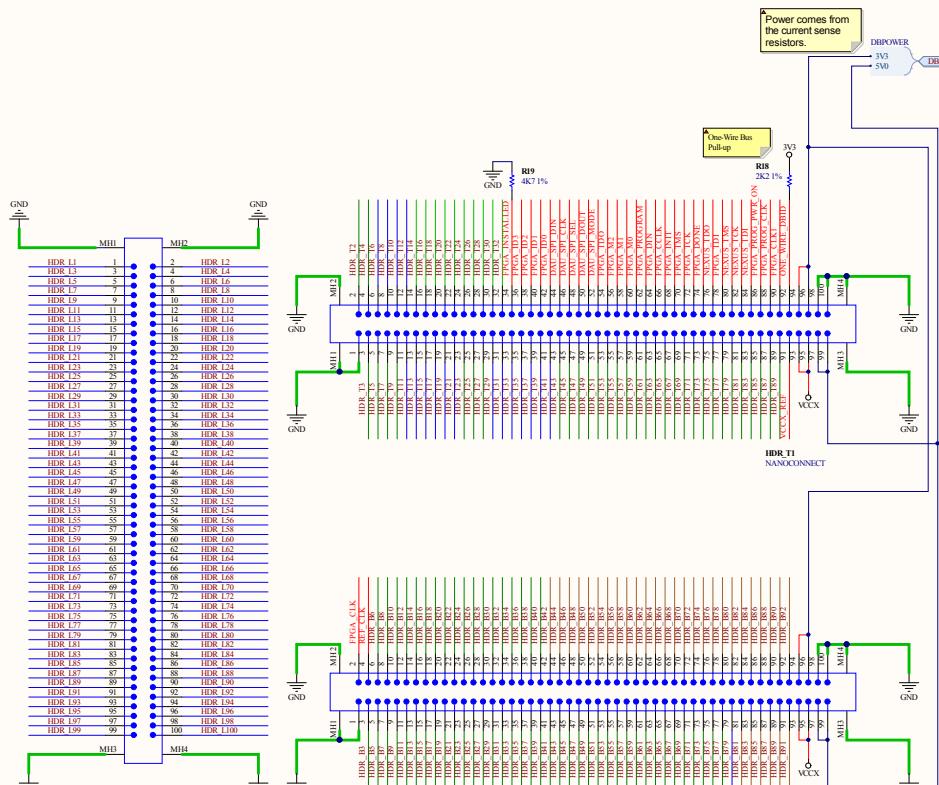
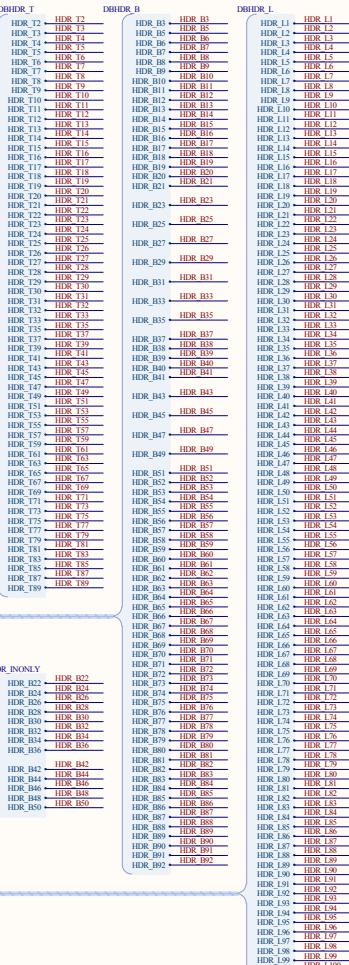
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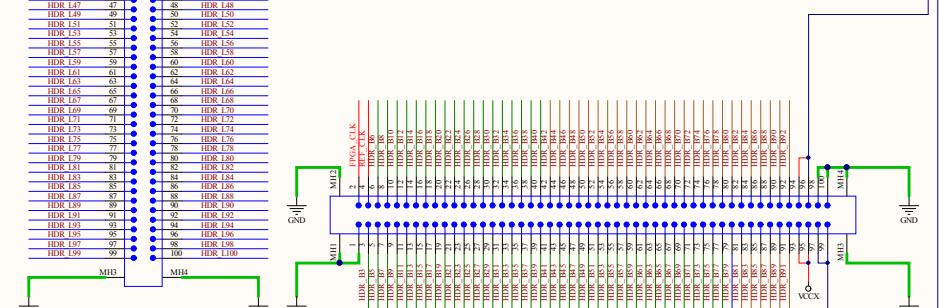
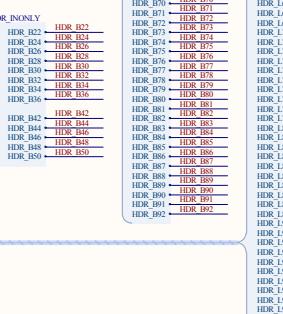
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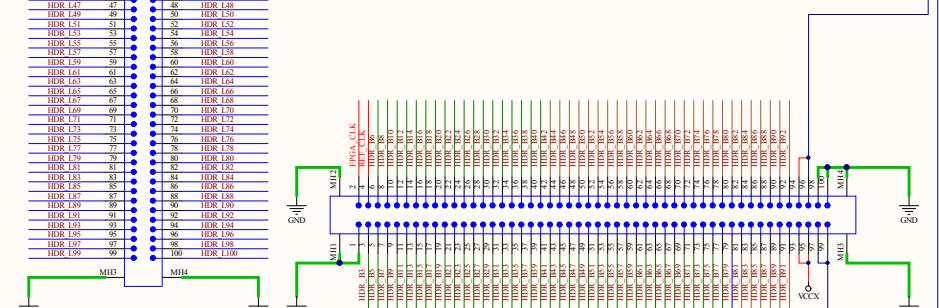
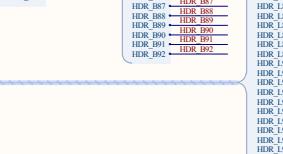
B



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Sheet Title	3-Way Daughter-Board Socket	Altium Limited
Project Title	NanoBoard NB2DSK01	Leyton House Road French Forest NSW 2089 Australia
Size	A3	Assembly: D-S10-0007 Revision: 08
Date	2/17/2011	Time: 5:49:55 PM Sheet: 27 of 64



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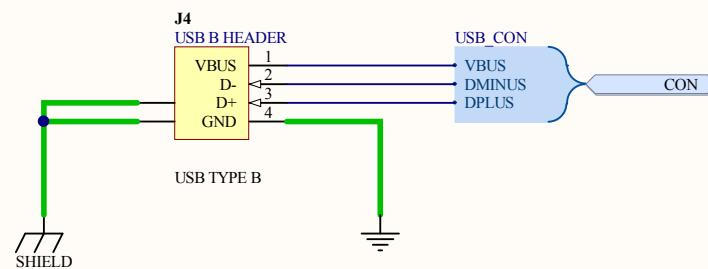
B

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Sheet Title ***USB 2.0 Type B Connector***

Project Title ***NanoBoard NB2DSK01***

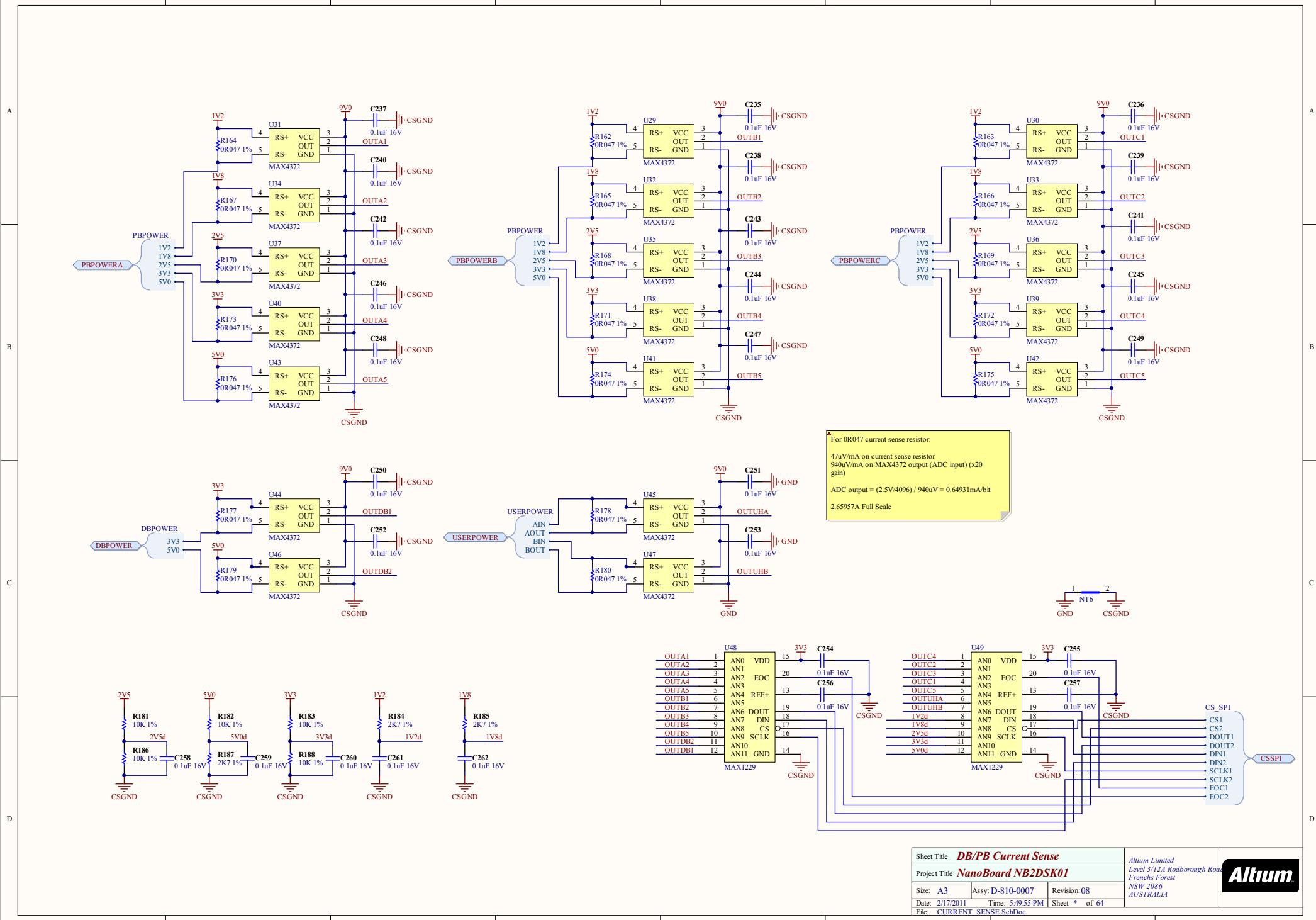
Size: **A4** Assy: **D-810-0007** Revision: **08**

Date: **2/17/2011** Time: **5:49:55 PM** Sheet **57** of **64**

File: **CON_USBB_RA.SchDoc**

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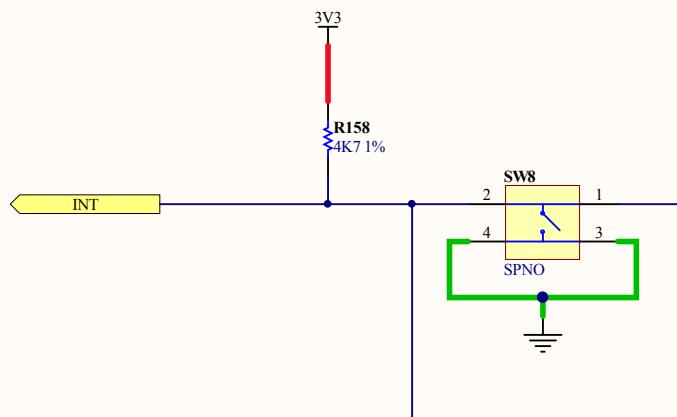


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Sheet Title ***Push Button SPNO Switch***

Project Title ***NanoBoard NB2DSK01***

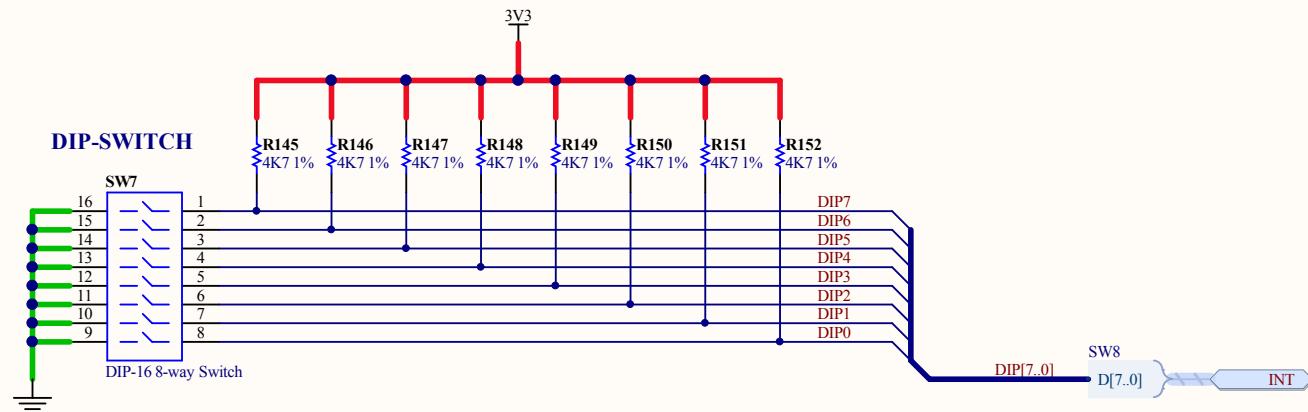
Size: **A4** Assy: **D-810-0007** Revision: **08**

Date: **2/17/2011** Time: **5:49:56 PM** Sheet **2** of **64**

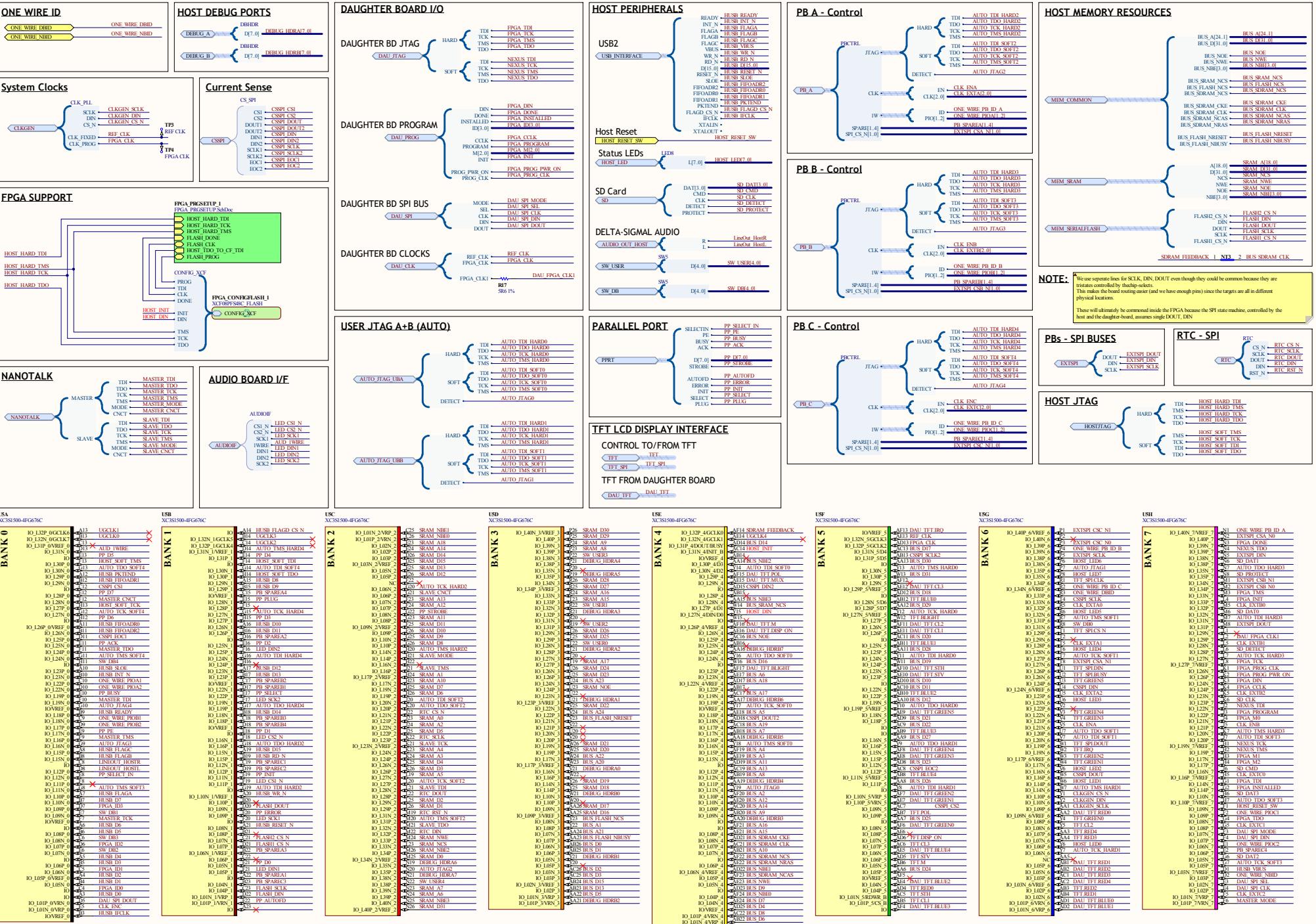
File: **SW RESET SPNO.SCHDOC**

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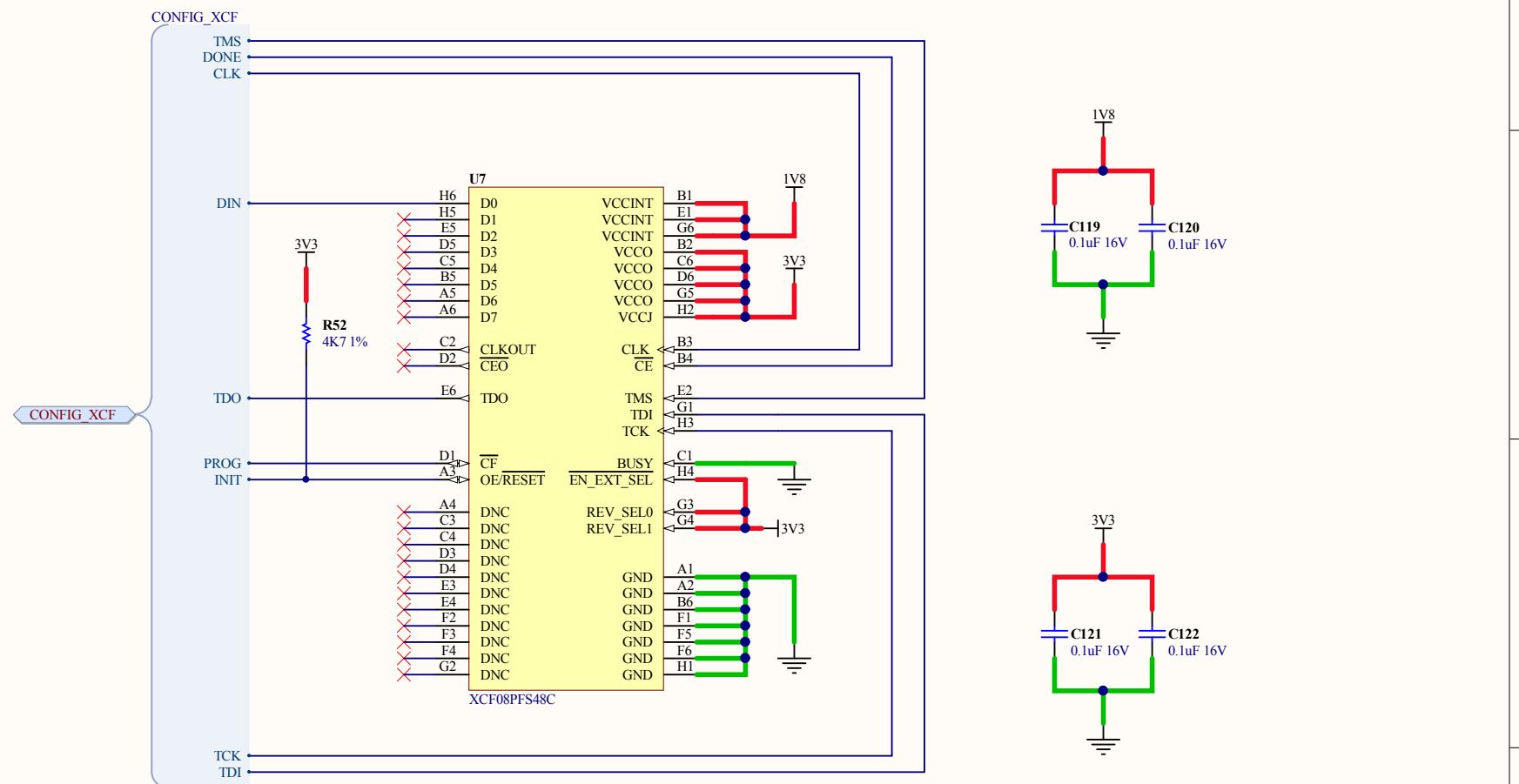




Sheet Title	8-Way DIP Switch	
Project Title	NanoBoard NB2DSK01	
Size:	A4	Assy: D-810-0007
Date:	2/17/2011	Time: 5:49:56 PM
File:	SW_DIP8.SchDoc	Revision: 08
Altium Limited Level 3/12A Rodborough Road Frenchs Forest NSW 2086 AUSTRALIA		Altium



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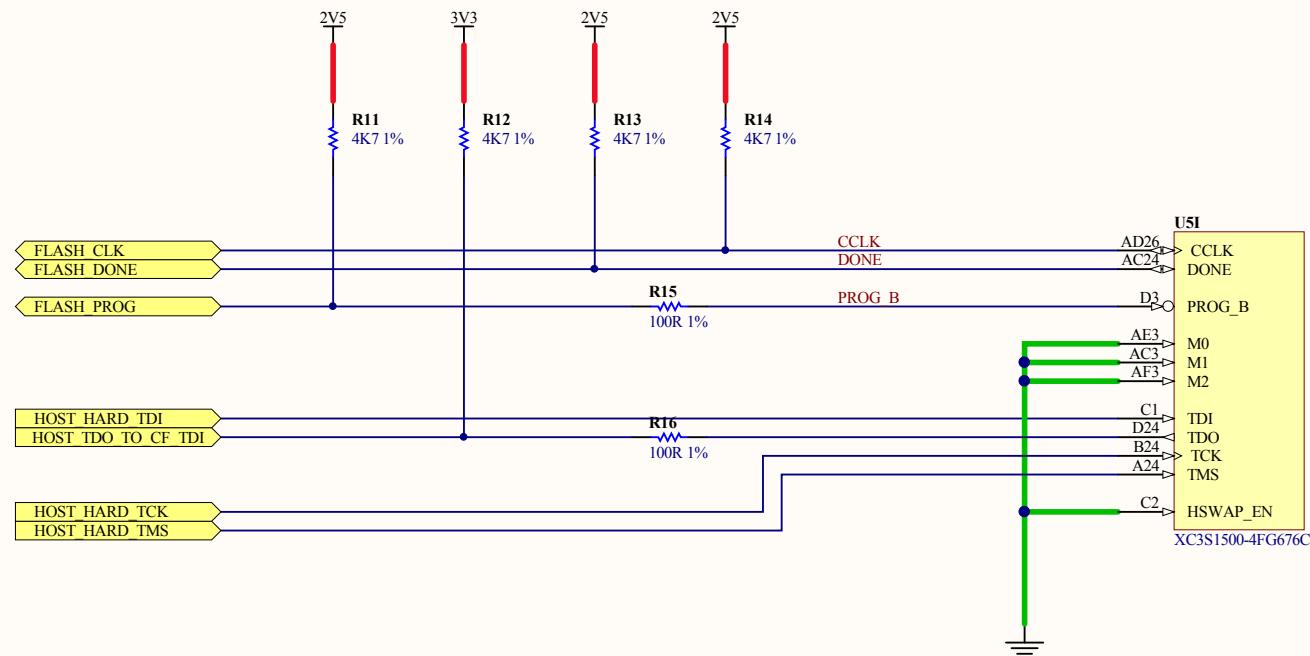
Sheet Title **FPGA Config XCF08PFS48C**Project Title **NanoBoard NB2DSK01**Size: **A4** Assy: **D-810-0007** Revision: **08**Date: **2/17/2011** Time: **5:49:56 PM** Sheet **18** of **64**File: **XCF08PFS48C_FLASH.SchDoc**

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XC3S1500-4FG676C_CONFIGPWR_1
XC3S1500-4FG676C_PWRSETUP.SchDoc



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Sheet Title XC3S1500-4FG676C Configuration		
Project Title NanoBoard NB2DSK01		
Size: A4	Assy: D-810-0007	Revision: 08
Date: 2/17/2011	Time: 5:49:56 PM	Sheet 13 of 64
File: FPGA_PRGSETUP.SchDoc		

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1V2

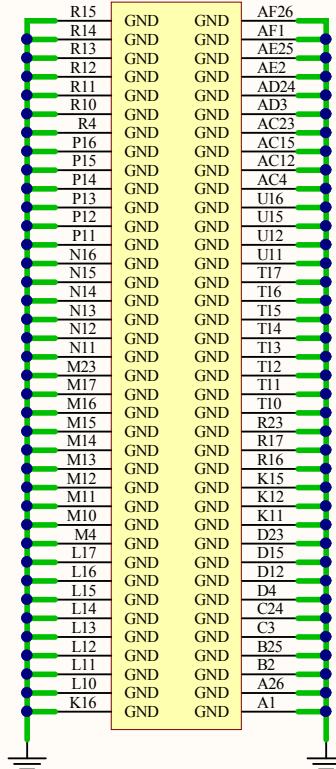
2V5

3V3

DECOUPLING_CAPS_1V2_1



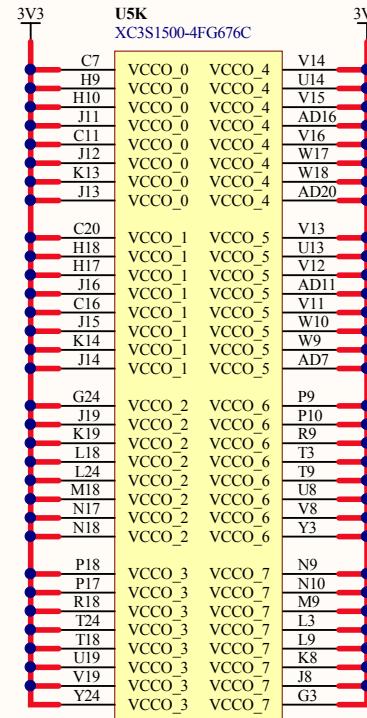
U5J
XC3S1500-4FG676C



DECOUPLING_CAPS_2V5_
FPGA Bypass 2V5



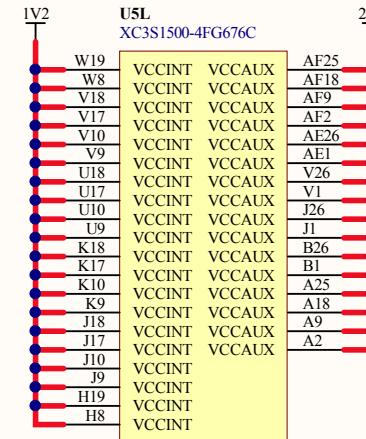
U5K
XC3S1500-4FG6



DECOUPLING_CAPS_3V3_FPGA Bypass 3V3



U5L
XC3S1500-4FG67C

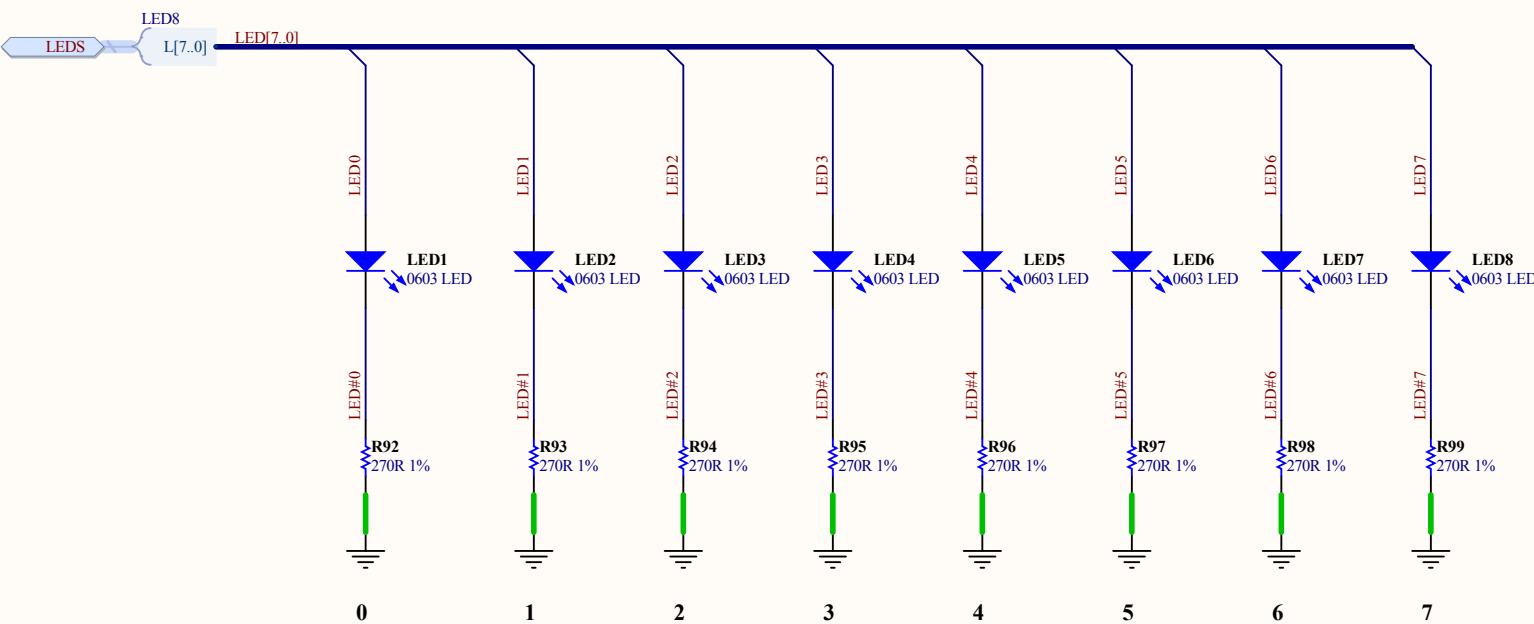


Sheet Title ***XC3S1500-4FG676C POWER***
Project Title ***NanoBoard NB2DSK01***
Size: **A4** Assy: **D-810-0007** Revision: **08**
Date: **2/17/2011** Time: **5:49:57 PM** Sheet **14** of **6**
File: **XC3S1500-4FG676C_PWRSETUP.SchDoc**

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A



A

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Sheet Title **8-Way 0603 Red LED Array**

Project Title **NanoBoard NB2DSK01**

Size: **A4** Assy: **D-810-0007** Revision: **08**

Date: **2/17/2011** Time: **5:49:57 PM** Sheet **25** of **64**

File: **LED_RED_0603x8.SCHDOC**

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A

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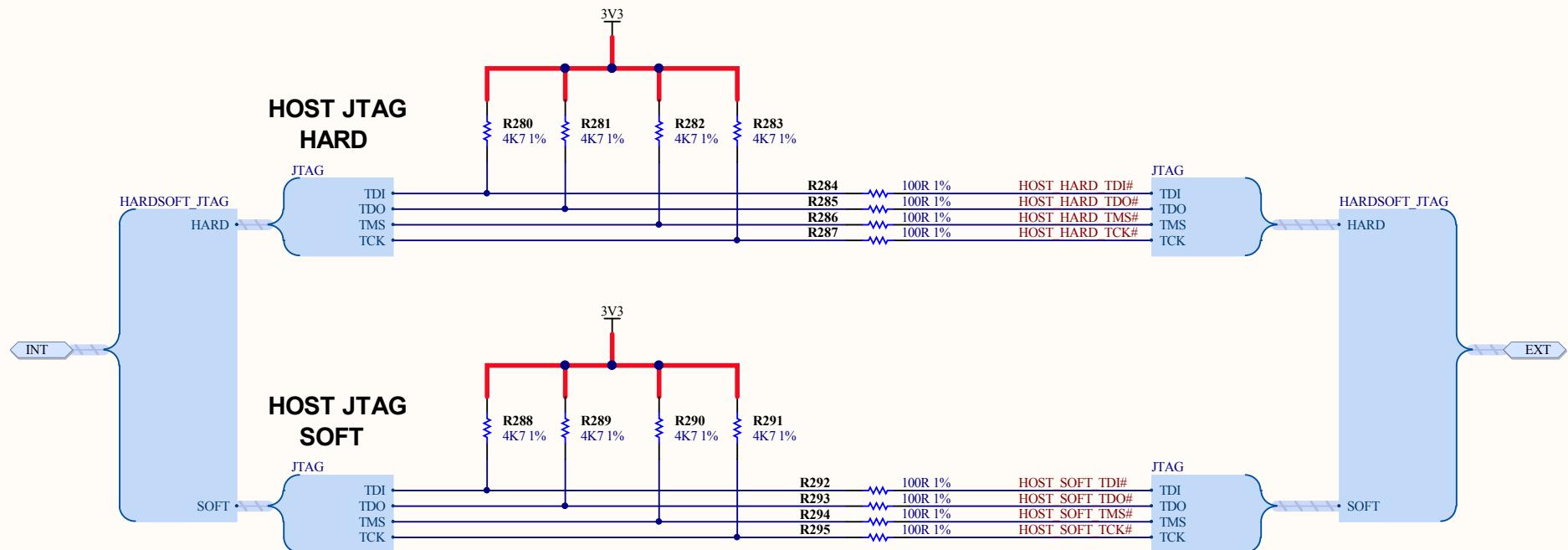
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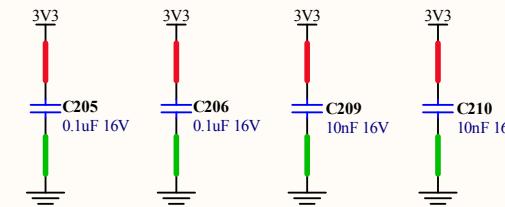
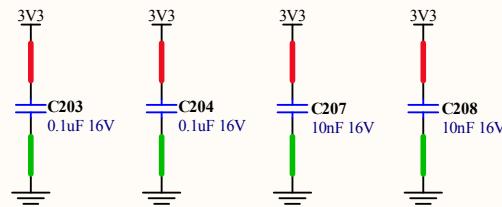
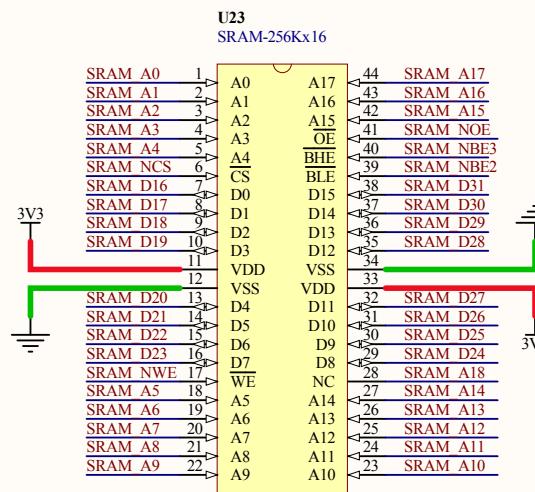
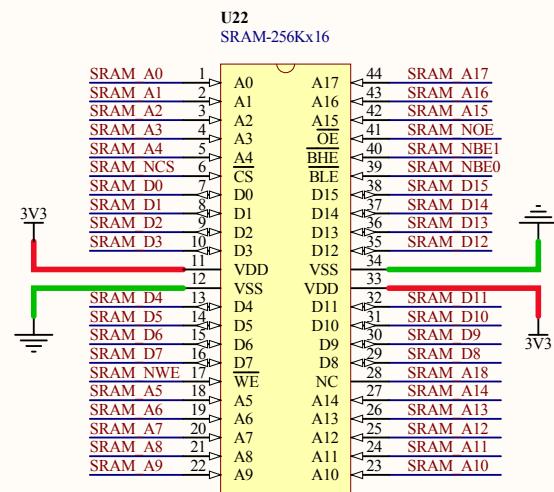
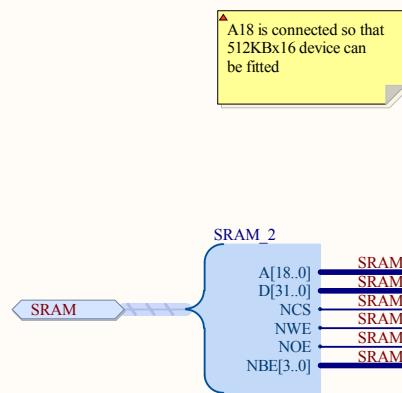
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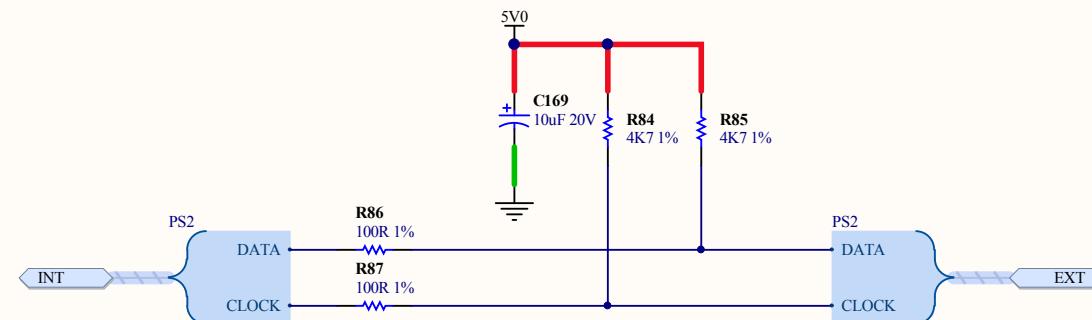
Sheet Title	<i>Host JTAG Header</i>		<i>Altium Limited Level 3/124 Rodborough Road Frenchs Forest NSW 2086 AUSTRALIA</i>	
Project Title	<i>NanoBoard NB2DSK01</i>			
Size:	A4	Number:	Revision: 08	
Date:	2/17/2011	Time:	5:49:57 PM	Sheet 19 of 64
File:	JTAG ALTIUM HOST.SchDoc			



Sheet Title 256K x 32 SRAM - TSOP44 x 2		
Project Title NanoBoard NB2DSK01		
Size: A4	Assy: D-810-0007	Revision: 08
Date: 2/17/2011	Time: 5:49:57 PM	Sheet 9 of 64
File: SRAM_256Kx32_TSOP44_2.SchDoc		

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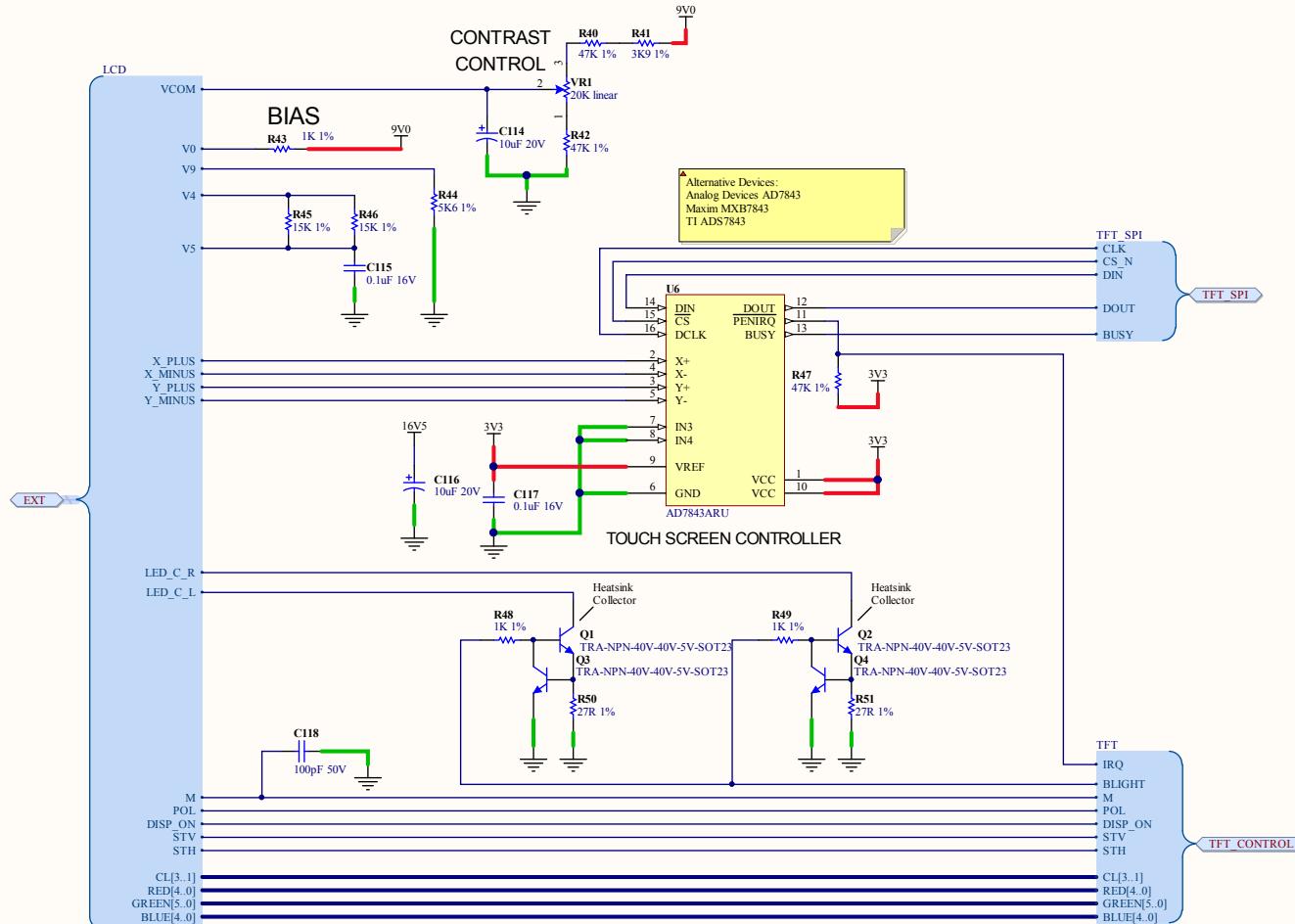


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Project Title	NanoBoard NB2DSK01		
Size:	A4	Assy:	D-810-0007
Date:	2/17/2011	Time:	5:49:57 PM
File:	PC_PS2.SchDoc	Revision:	08
Sheet:	59	of	64

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A



B

A

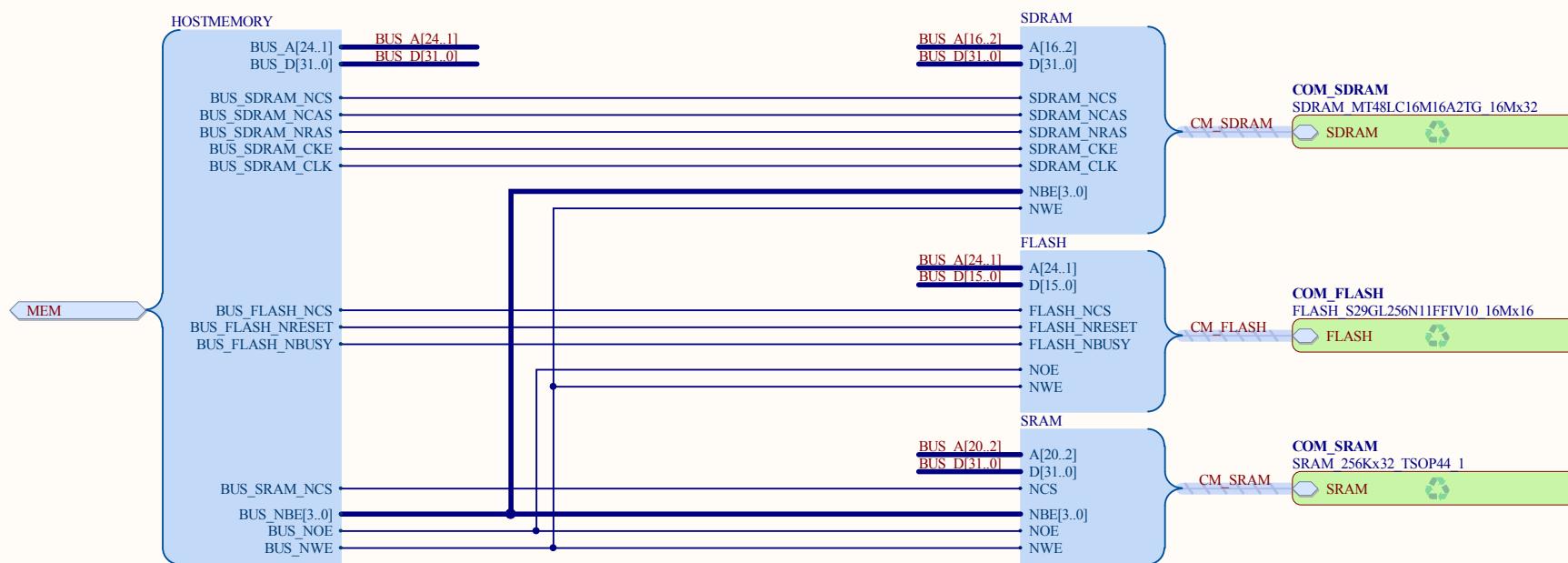
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Sheet Title TFT Touchscreen Interface	Altium Limited
Project Title NanoBoard NB2DSK01	Level 3/12A Rodborough Road Frenchs Forest NSW 2086 AUSTRALIA
Size: A3	Assy: D-810-0007
Date: 2/17/2011	Revision: 08
Time: 5:49:57 PM	Sheet 26 of 64
File: TSC_AD7843.SchDoc	

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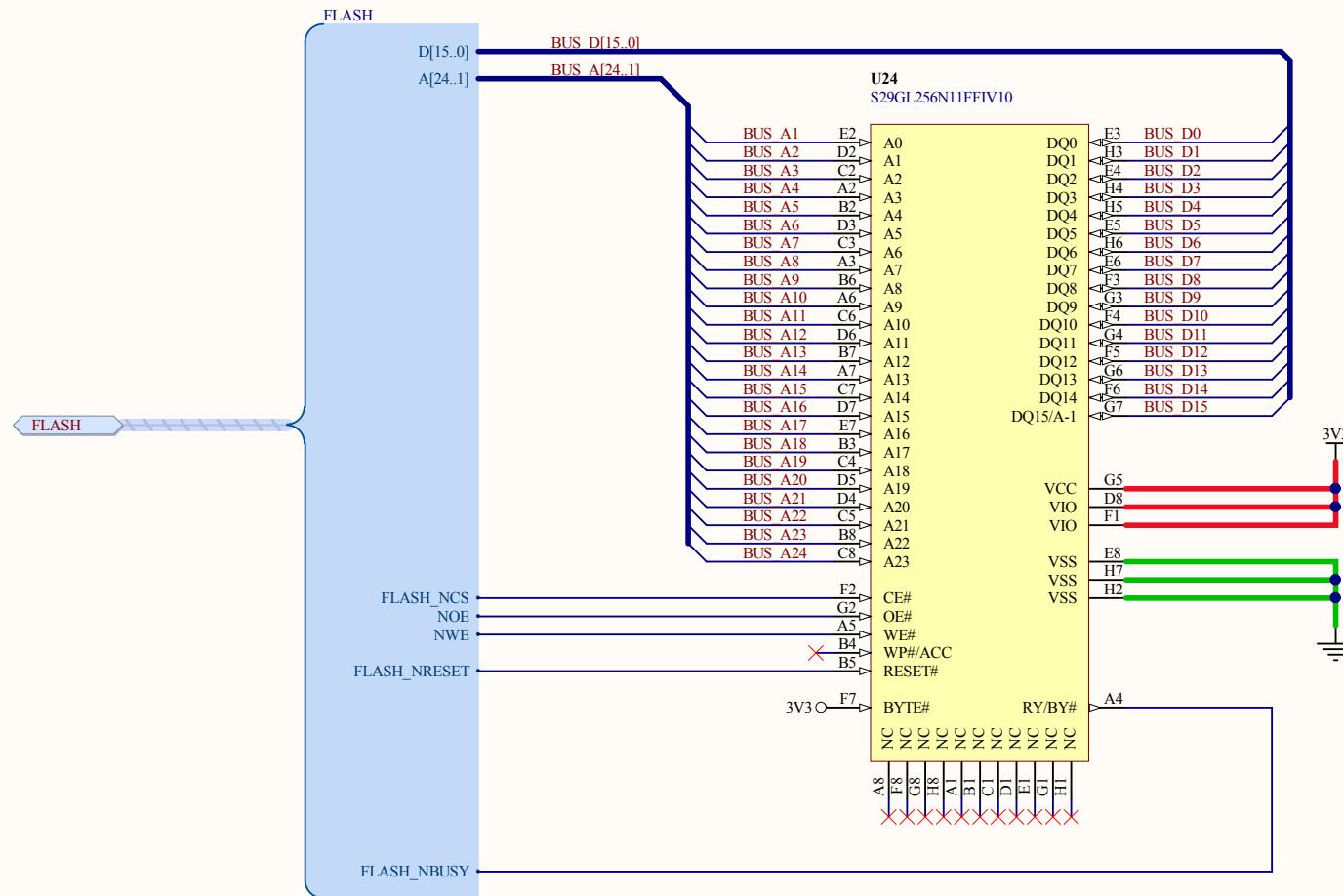
C

D

Common-Bus Memory Block

**256K x 32-bit SRAM (1 MByte)
16M x 32-Bit SDRAM (64 MByte)
16M x 16-Bit Flash (32 MByte)**

Sheet Title	Common-Bus Memory Block	
Project Title	NanoBoard NB2DSK01	
Size:	A4	Assy: D-810-0007
Date:	2/17/2011	Time: 5:49:57 PM
File:	Sheet 4 of 64 NB2_CommonMemory.SchDoc	
Altium Limited Level 3/12A Rodborough Road Frenchs Forest NSW 2086 AUSTRALIA	Altium	

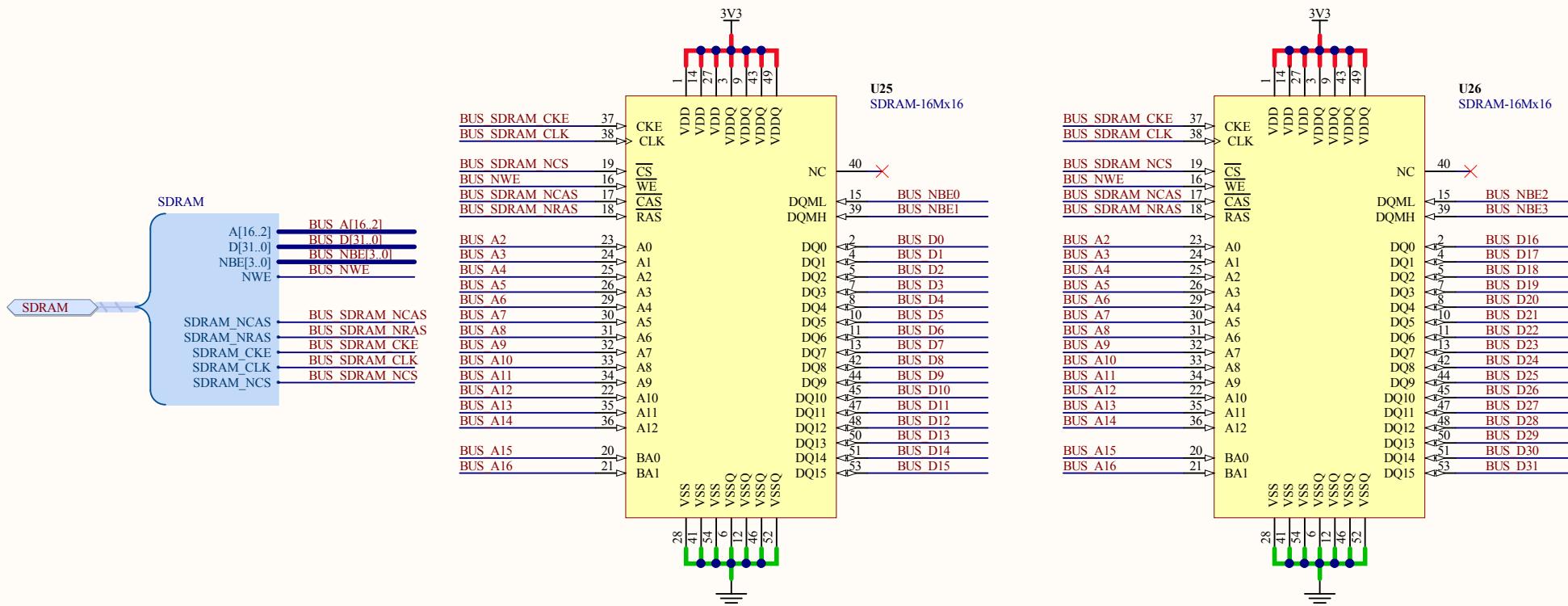


Sheet Title	<i>16Mx16 Flash Memory (BGA)</i>
Project Title	<i>NanoBoard NB2DSK01</i>
Size:	A4
Assy:	D-810-0007
Revision:	08
Date:	2/17/2011
Time:	5:49:57 PM
Sheet	6 of 64
File:	FLASH_S29GL256N11FFIV10_16Mx16.SchDoc

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A



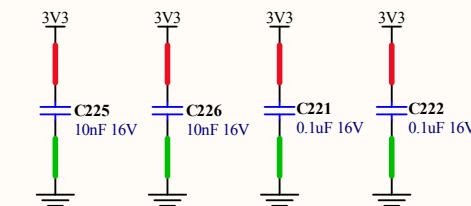
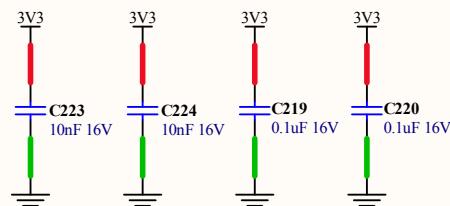
B

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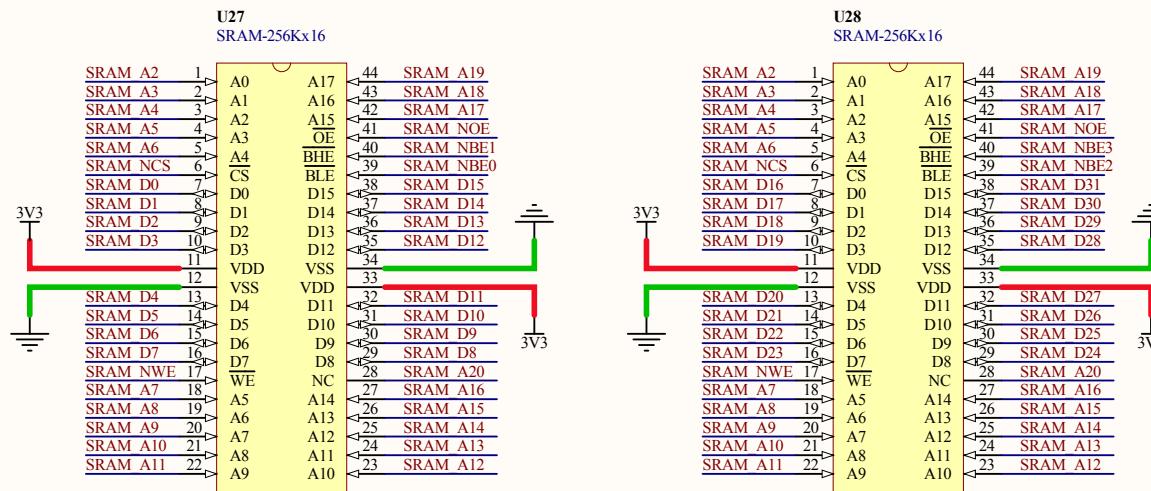
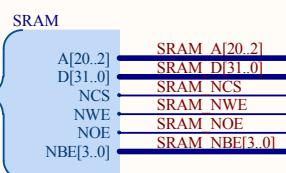
Sheet Title	16M x 32 SDRAM TSOP54 x 2	
Project Title	NanoBoard NB2DSK01	
Size: A4	Assy: D-810-0007	Revision: 08
Date: 2/17/2011	Time: 5:49:58 PM	Sheet 5 of 64
File: SDRAM_MT48LC16M16A2TG_16Mx32.SchDoc		

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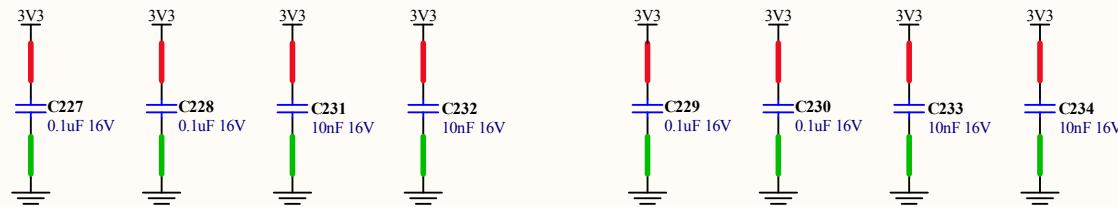


A

A18 is connected so that
512KBx16 device can
be fitted



B



D

Sheet Title	256K x 32 SRAM - TSOP44 x 2	
Project Title	NanoBoard NB2DSK01	
Size: A4	Assy: D-810-0007	Revision: 08
Date: 2/17/2011	Time: 5:49:58 PM	Sheet 7 of 64
File: SRAM_256Kx32_TSOP44_1.SchDoc		

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Standoffs For Peripheral Board A



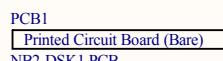
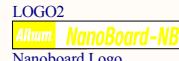
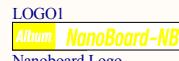
Standoffs For Peripheral Board C



Mounting Holes



PCB Identifiers



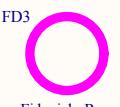
Standoffs For Peripheral Board B



Standoffs For Daughter Board



Fiducial Alignment Components



Sheet Title **NB2DSK01 Holes and Graphics**

Project Title **NanoBoard NB2DSK01**

Size: **A4** Assy: **D-810-0007** Revision: **08**

Date: **2/17/2011** Time: **5:49:58 PM** Sheet **38** of **64**

File: **NB2DSK_Mounts.SchDoc**

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A

A

B

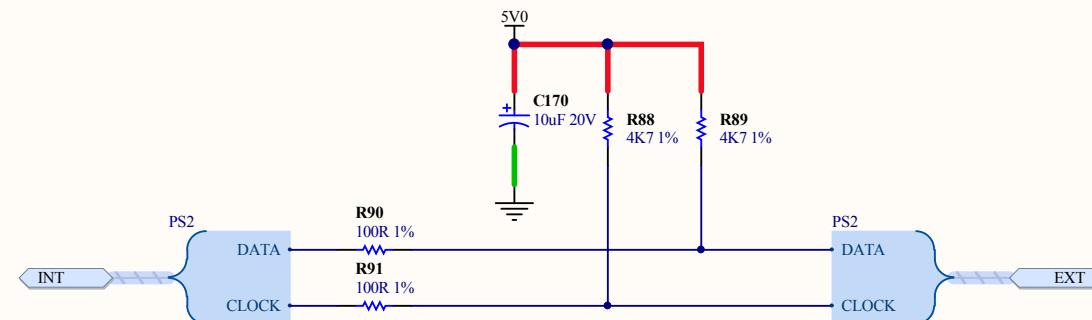
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C

C

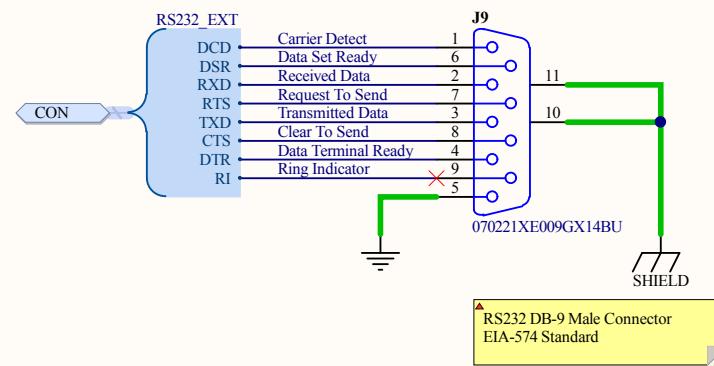
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D



Sheet Title PC PS2		
Project Title NanoBoard NB2DSK01		
Size: A4	Assy: D-810-0007	Revision: 08
Date: 2/17/2011	Time: 5:49:58 PM	Sheet 59 of 64
File: PC_PS2.SchDoc		

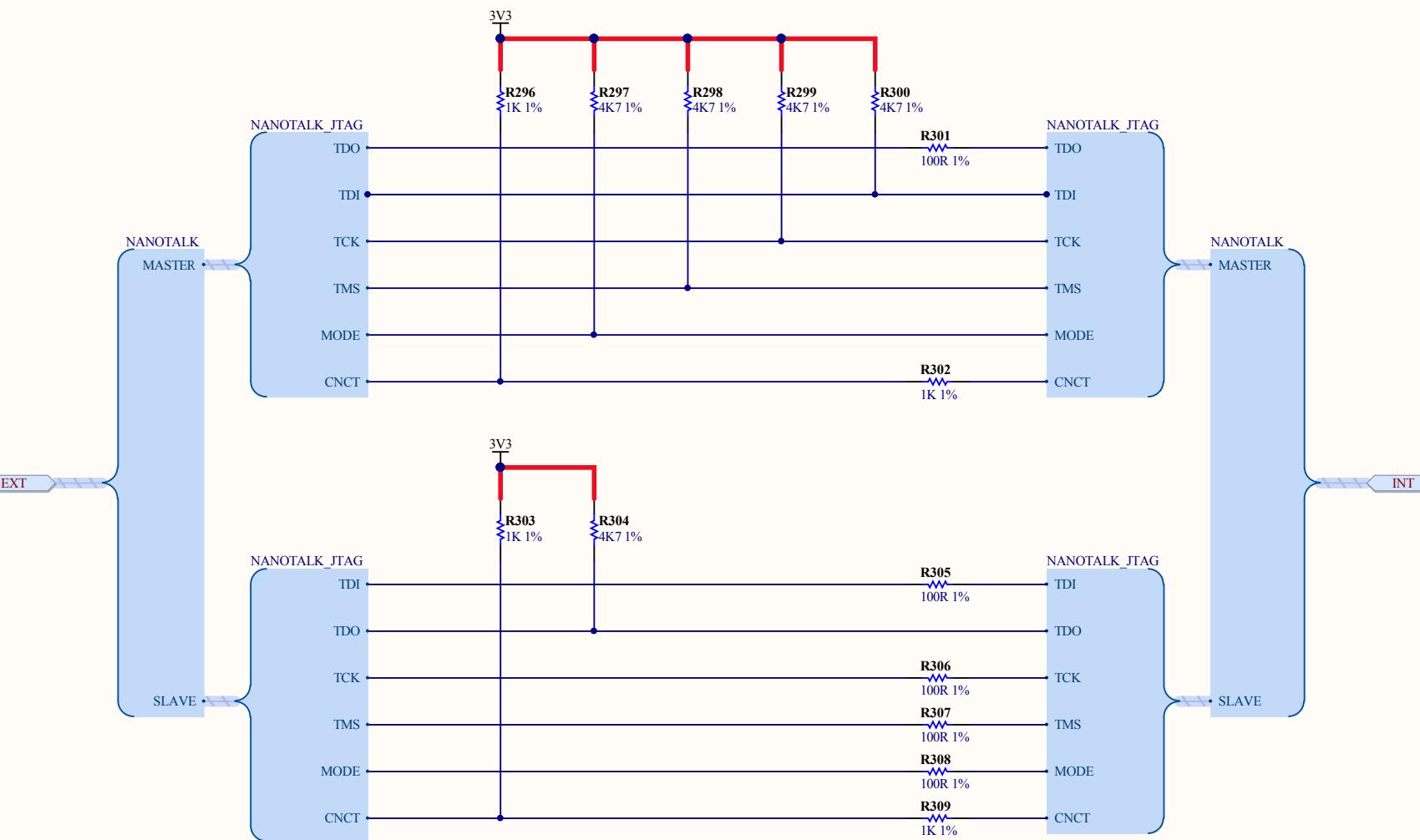


Sheet Title **RS232-DCE DB9**Project Title **NanoBoard NB2DSK01**Size: **A4** Assy: **D-810-0007** Revision: **08**Date: **2/17/2011** Time: **5:49:58 PM** Sheet **50** of **64**File: **CON_RS232DCE_DB9.SchDoc**

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Sheet Title **NanoTalk JTAG Header**Project Title **NanoBoard NB2DSK01**

Size: A4 Assy: D-810-0007 Revision: 08

Date: 2/17/2011 Time: 5:49:58 PM Sheet 22 of 64

File: **JTAG_ALTIUM_NANOTALK.SchDoc**

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A

A

B

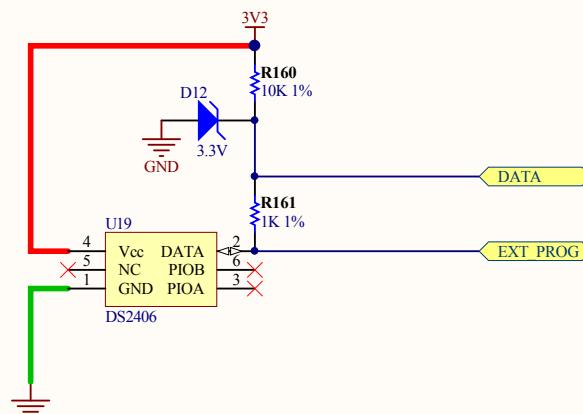
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C

C

D

D



Sheet Title ***Protected 1-Wire EEPROM***

Project Title ***NanoBoard NB2DSK01***

Size: **A4** Assy: **D-810-0007** Revision: **08**

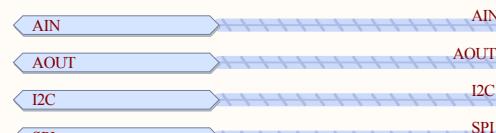
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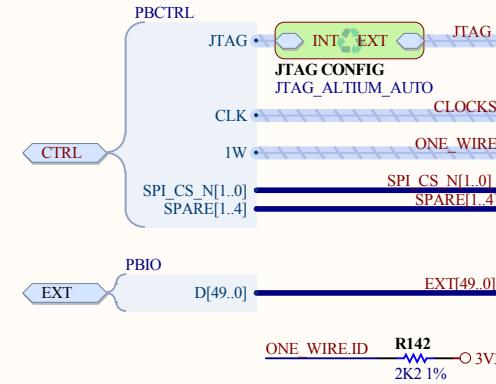
A



B

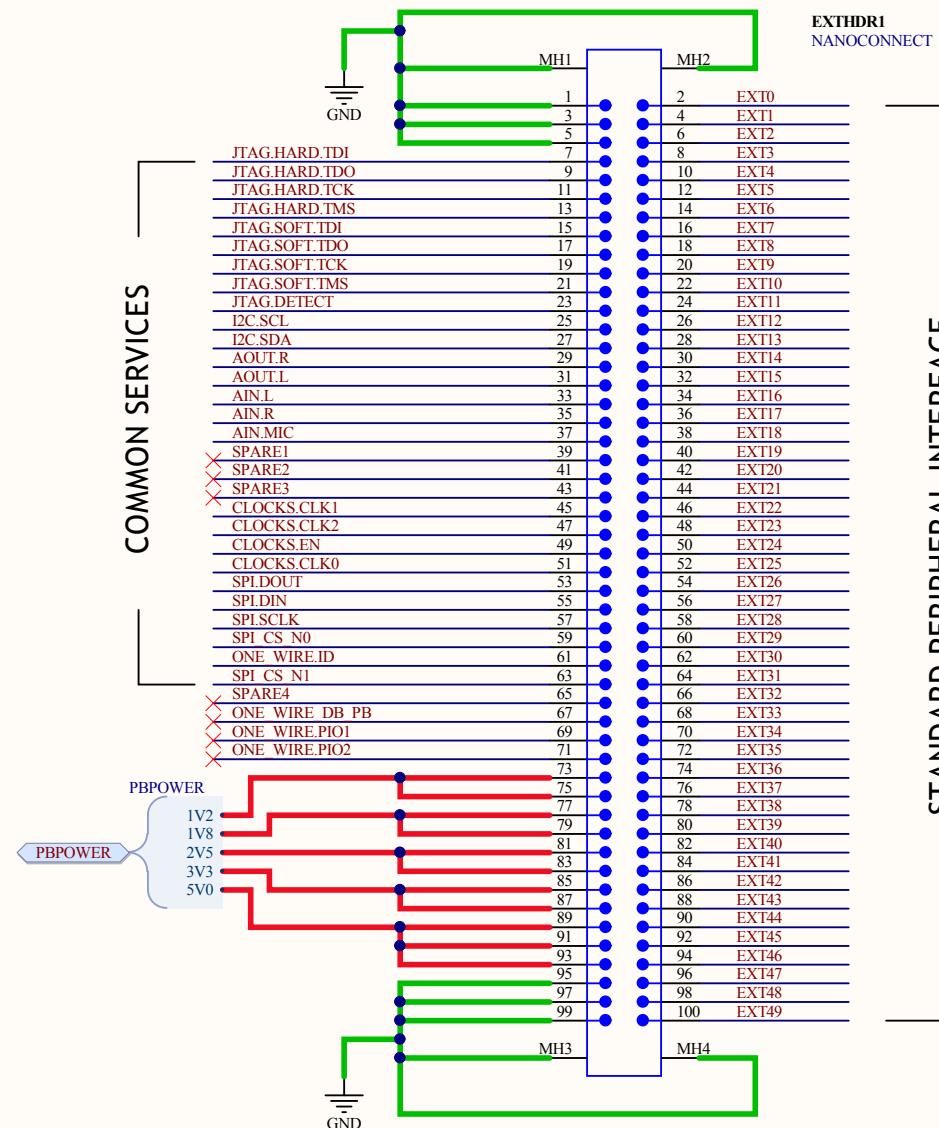


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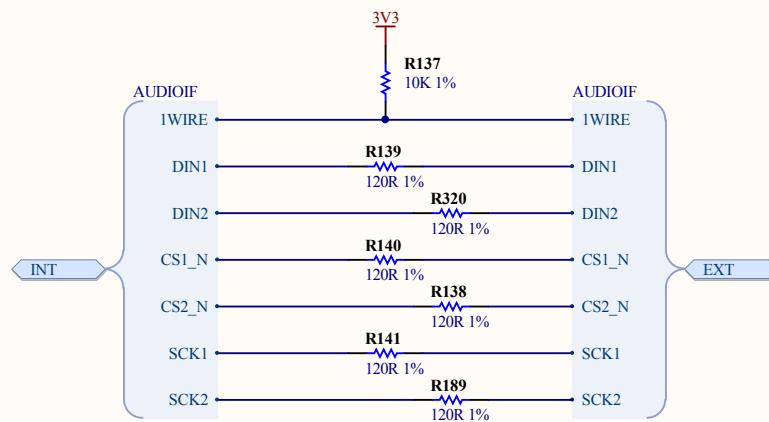
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COMMON SERVICES

Sheet Title **Peripheral Board Connector**Project Title **NanoBoard NB2DSK01**Size: **A4** Assy: **D-810-0007** Revision: **08**Date: **2/17/2011** Time: **5:49:58 PM** Sheet **28** of **64**File: **NB2_PBCON.schdoc**

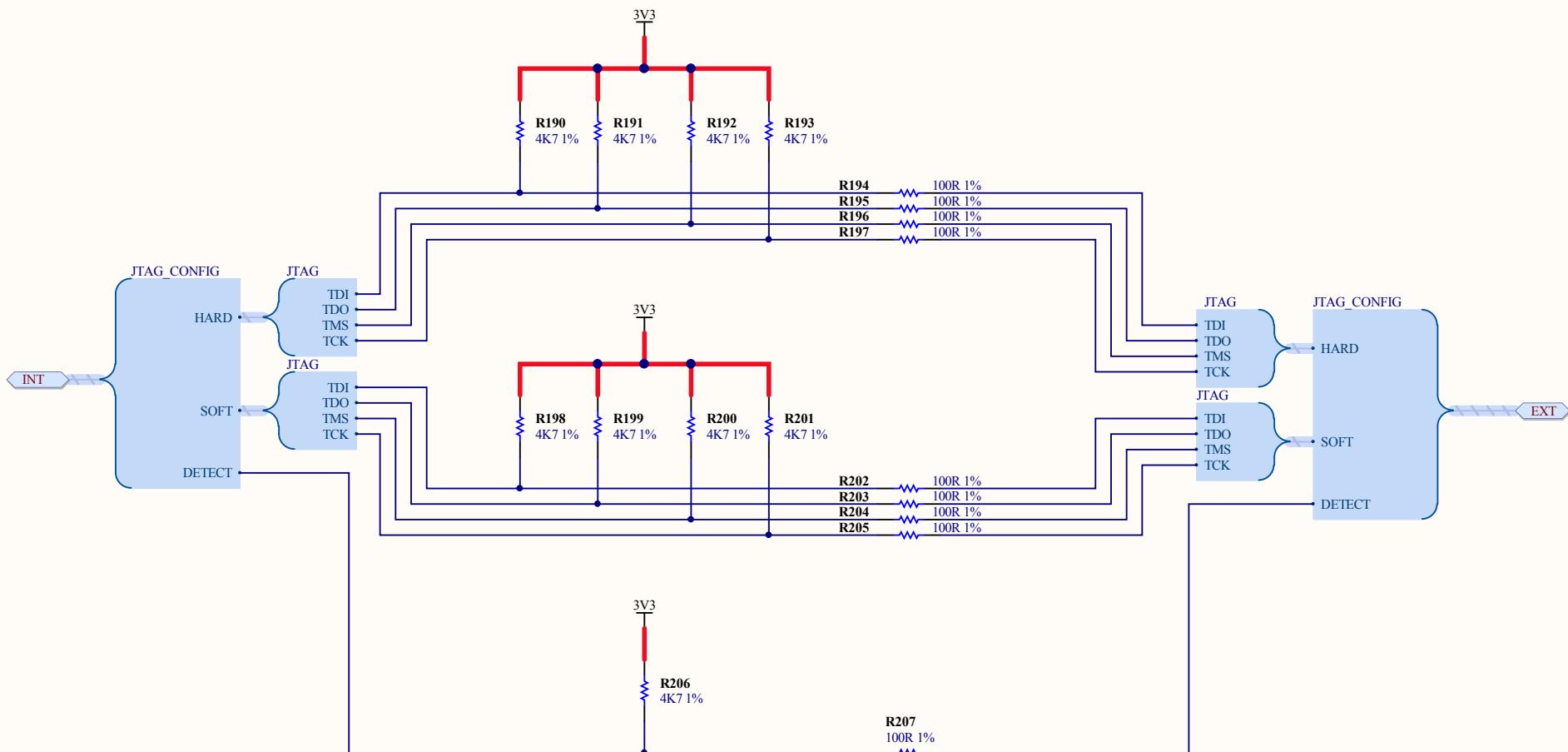
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Sheet Title **NB2-Extender A Interface**Project Title **NanoBoard NB2DSK01**Size: **A4** Assy: **D-810-0007** Revision: **08**Date: **2/17/2011** Time: **5:49:58 PM** Sheet **54** of **64**File: **NB2_EXTEND_A.SchDoc**

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A

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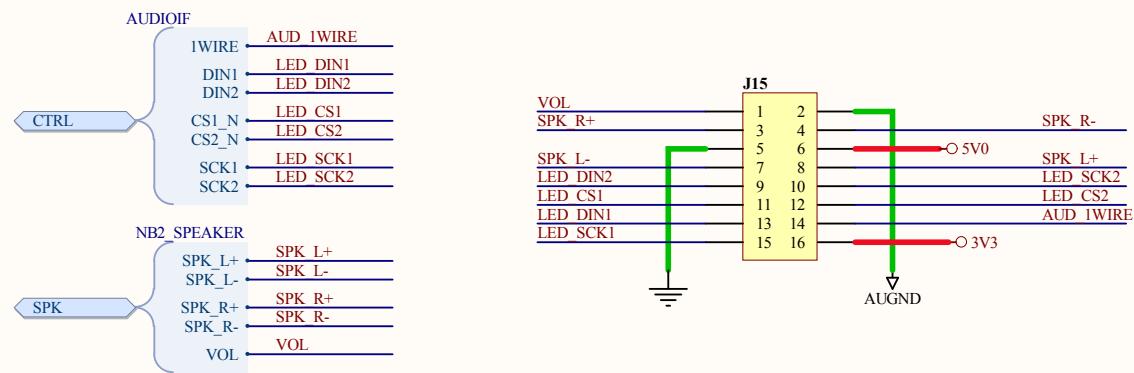
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C

C

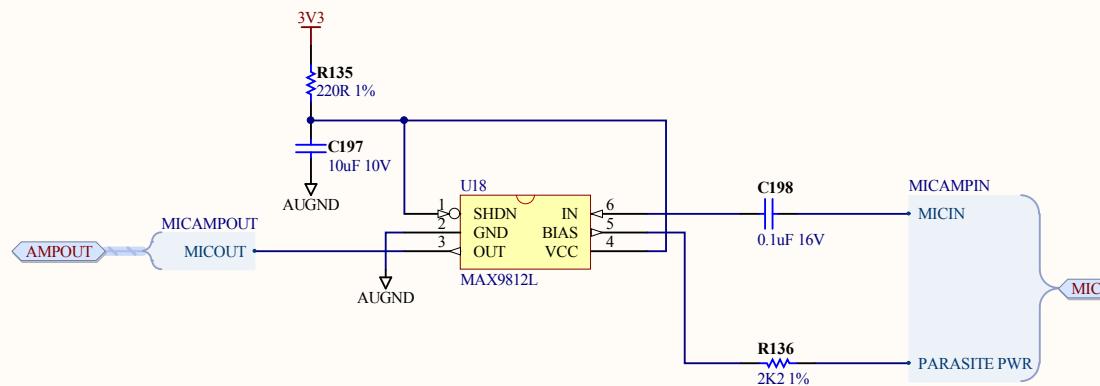
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D

Sheet Title **NB2-Extender A 16-Pin Header**Project Title **NanoBoard NB2DSK01**Size: **A4** Assy: **D-810-0007** Revision: **08**Date: **2/17/2011** Time: **5:49:59 PM** Sheet **54** of **64**File: **CON_NB2_EXTEND_A16.SchDoc**

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Sheet Title **AUDIO AC99 Interface**

Project Title **NanoBoard NB2DSK01**

Size: **A4** Assy: **D-810-0007** Revision: **08**

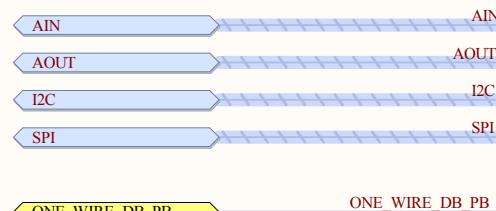
Date: **2/17/2011** Time: **5:49:59 PM** Sheet **54** of **64**

File: **AUDIO_AMP_MAX9812L.SchDoc**

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A



ONE_WIRE DB PB ONE_WIRE DB PB

PBCTRL JTAG INT EXT JTAG

JTAG CONFIG JTAG_ALTIUM_AUTO

CLK CLOCKS

1W ONE_WIRE

SPI_CS_N[1..0] SPI_CS_N[1..0]

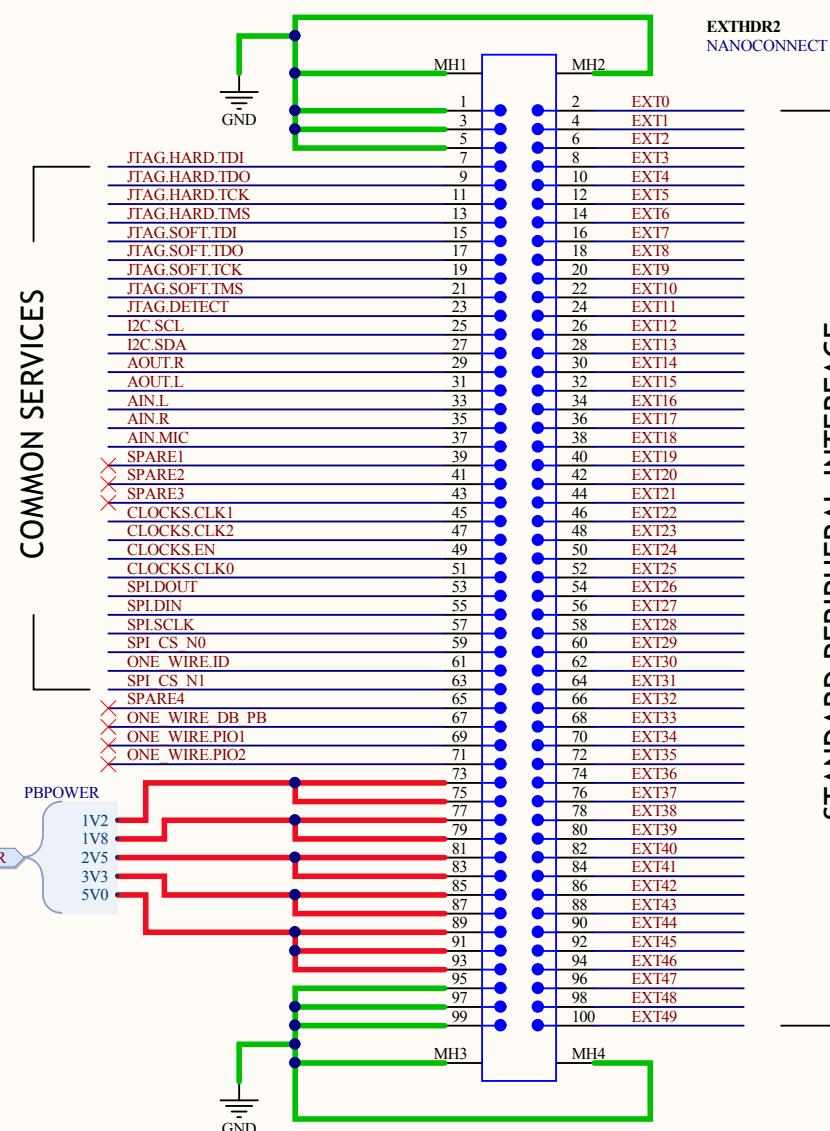
SPARE[1..4] SPARE[1..4]

PBIO EXT

D[49..0] EXT[49..0]

ONE_WIRE.ID R143
2K2 1% 3V3

COMMON SERVICES



Sheet Title **Peripheral Board Connector**

Project Title **NanoBoard NB2DSK01**

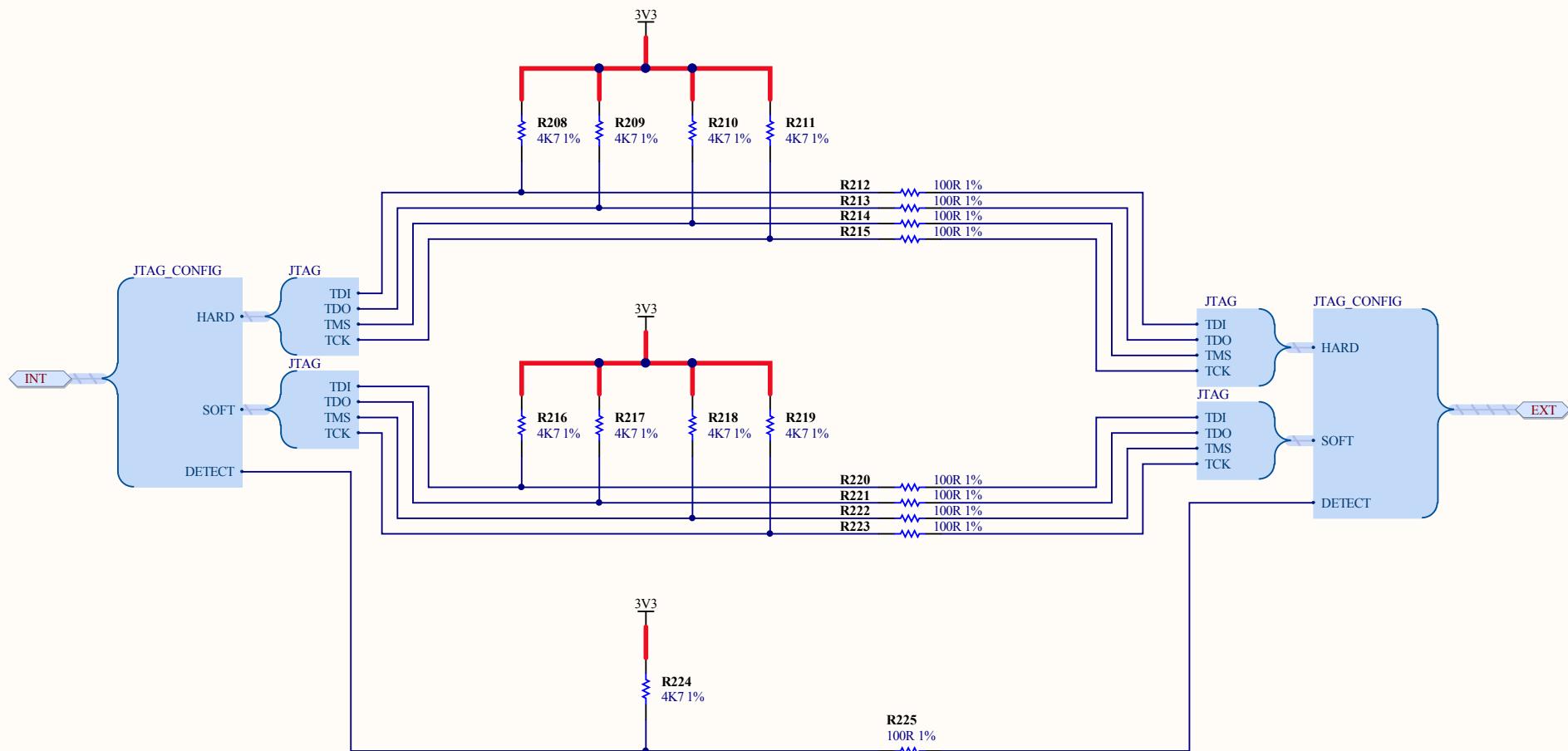
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Date: **2/17/2011** Time: **5:49:59 PM** Sheet **28** of **64**

File: **NB2_PBCON.schdoc**

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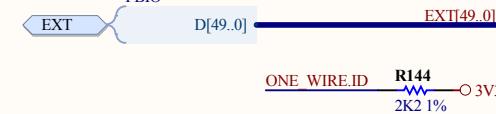
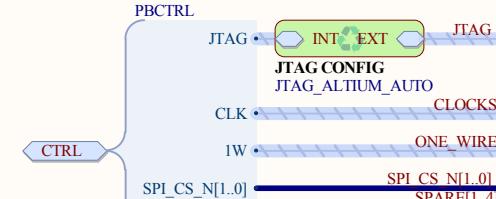
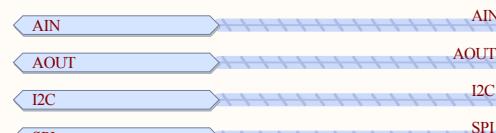


Sheet Title **Auto-Detect JTAG Circuit**Project Title **NanoBoard NB2DSK01**Size: **A4** Assy: **D-810-0007** Revision: **08**Date: **2/17/2011** Time: **5:49:59 PM** Sheet **21** of **64**File: **JTAG_ALTIUM_AUTO.SchDoc**

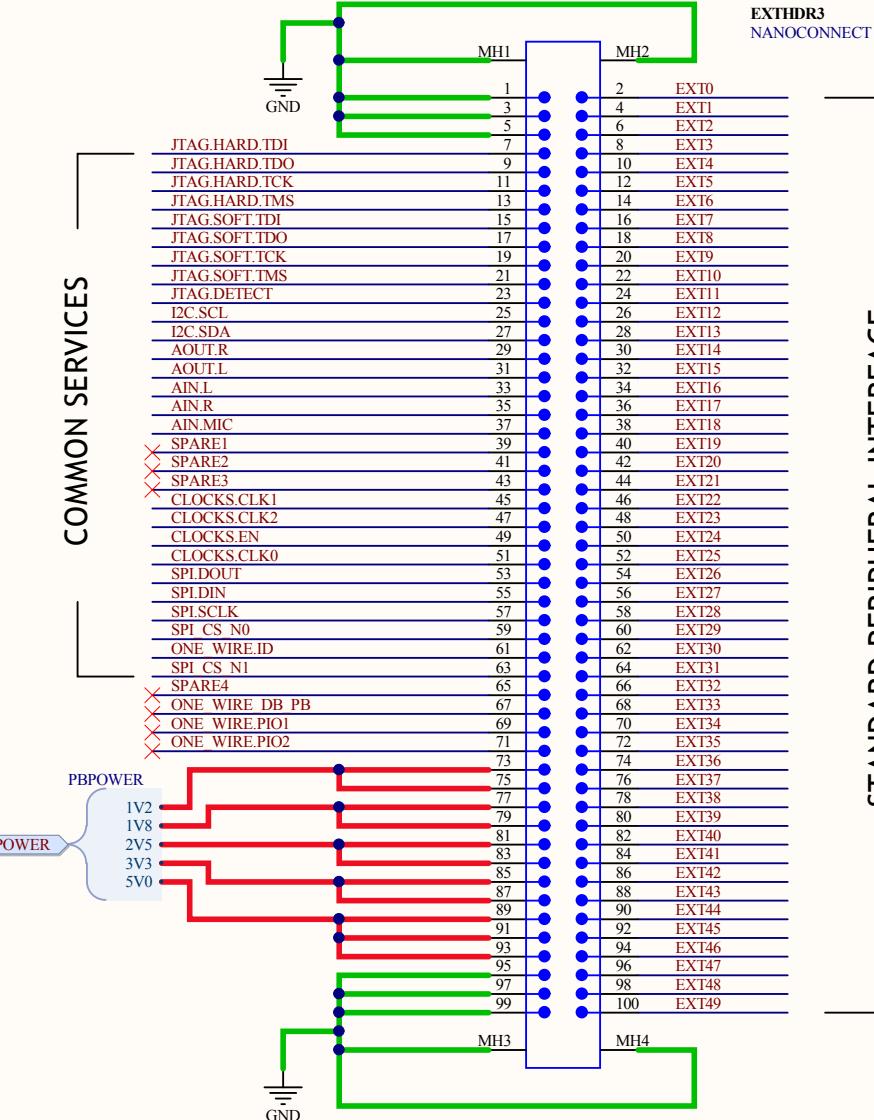
Altium Limited
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A

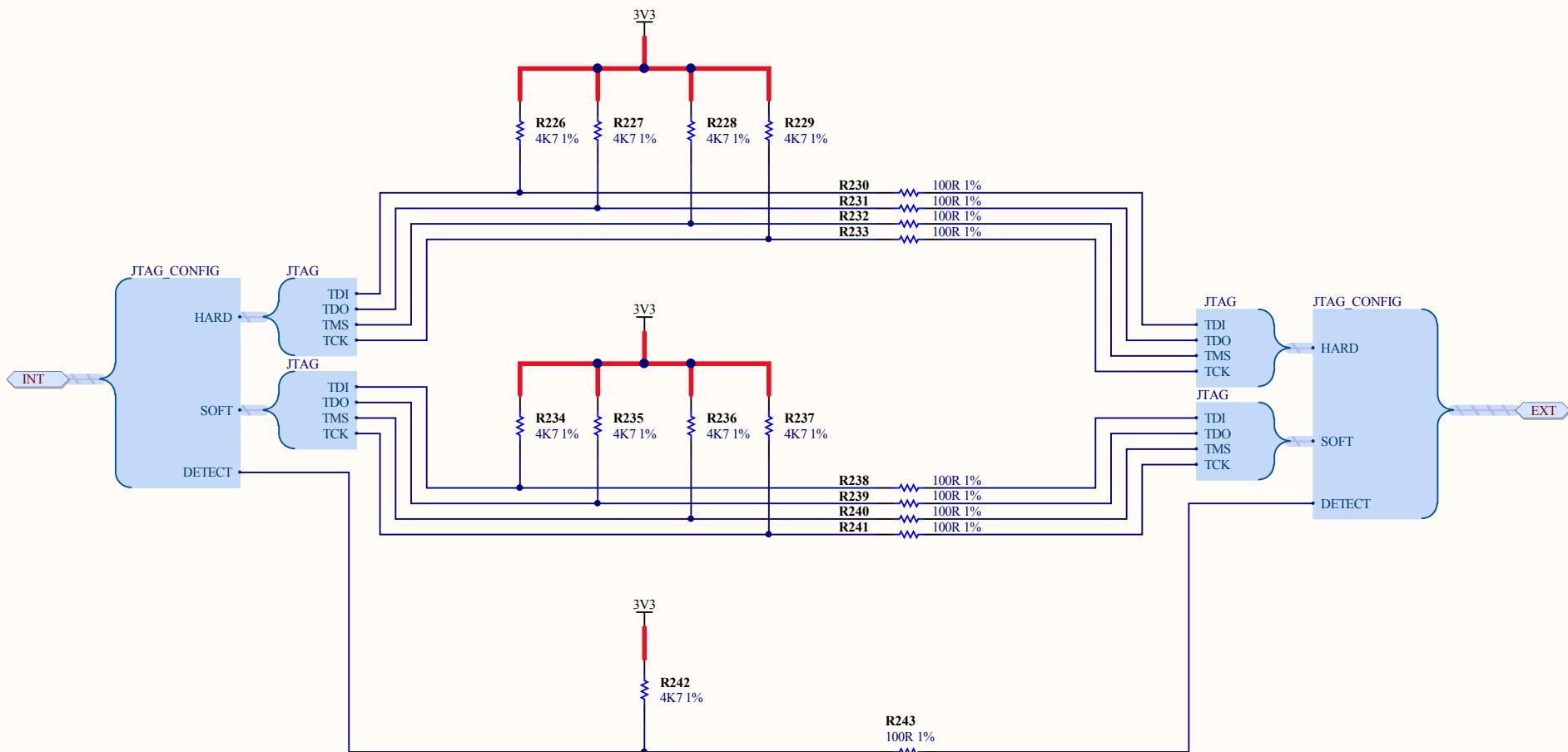


COMMON SERVICES

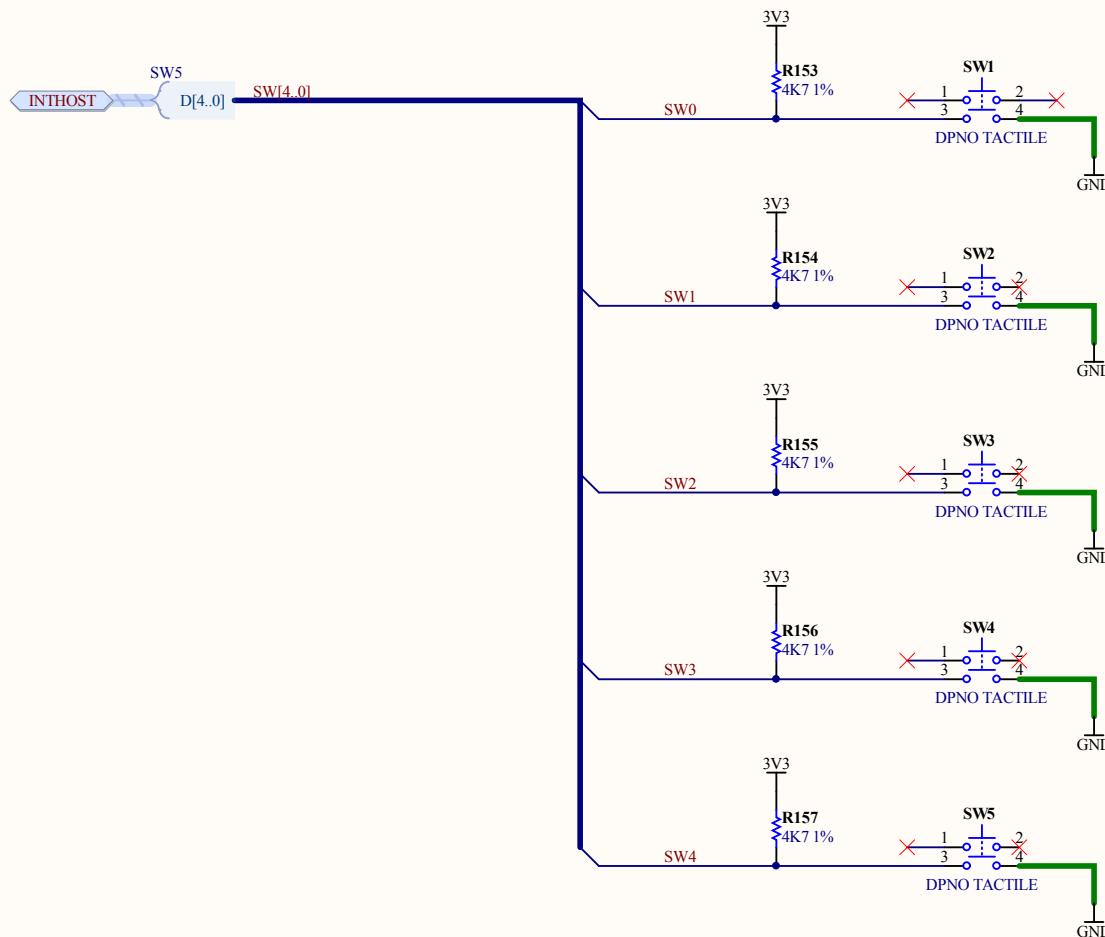
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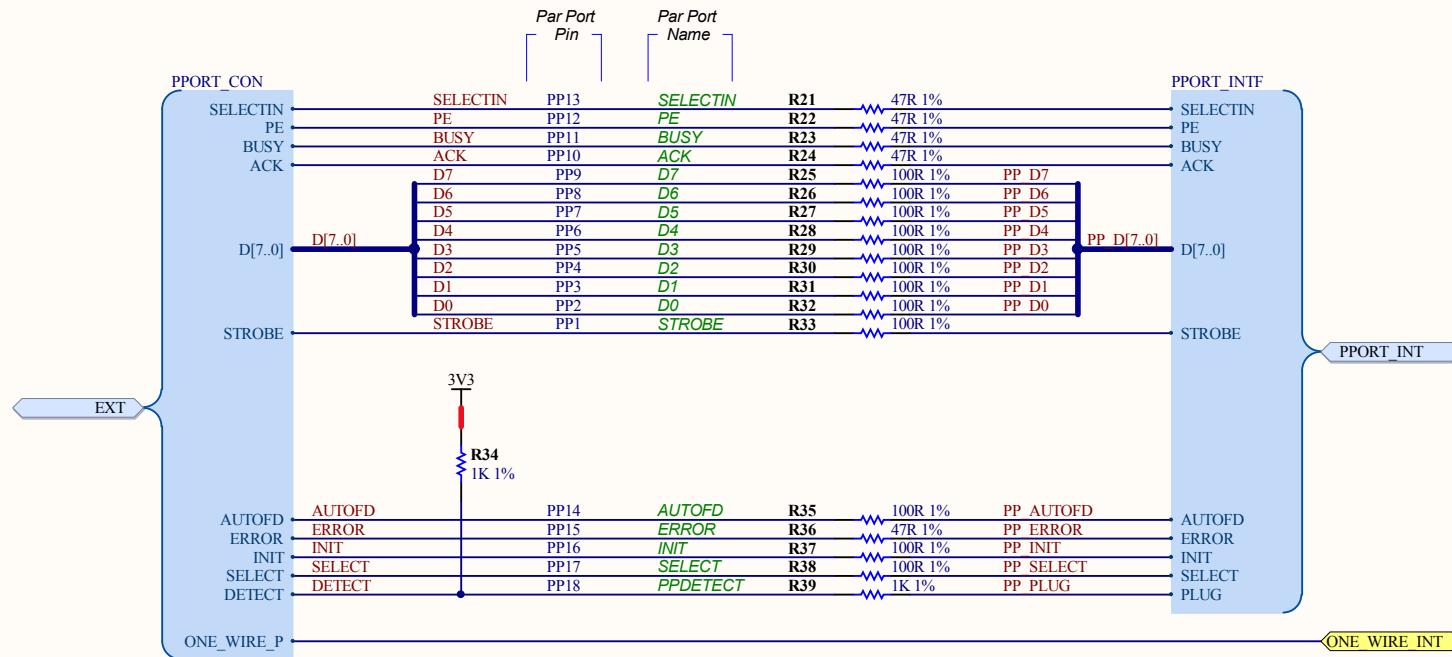
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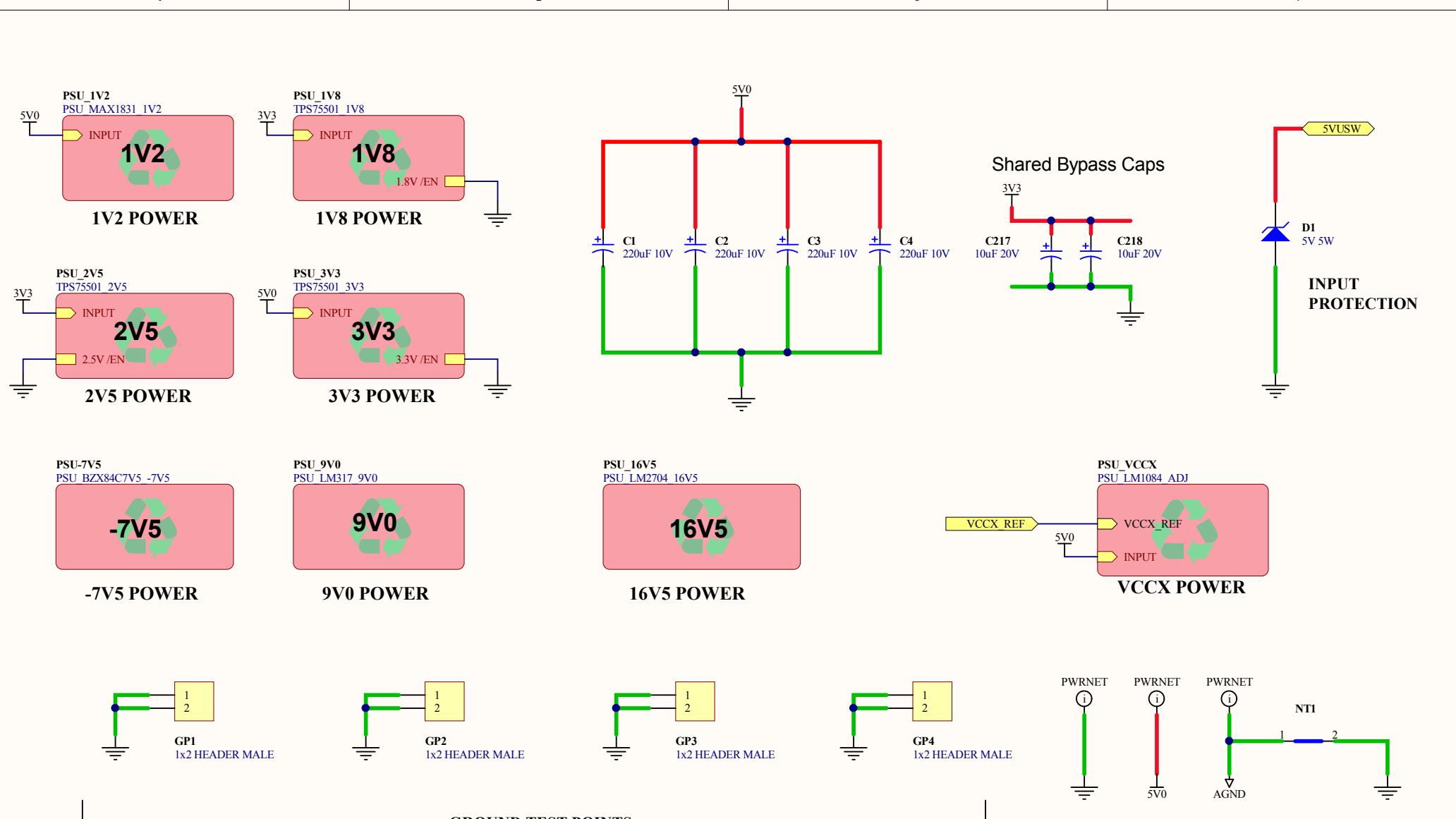
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Sheet Title **PDA-Style 5 x DPNO Switch**Project Title **NanoBoard NB2DSK01**Size: **A4** Assy: **D-810-0007** Revision: **08**Date: **2/17/2011** Time: **5:49:59 PM** Sheet **61** of **64**File: **SW_PDA_DPNOx5.SCHDOC**

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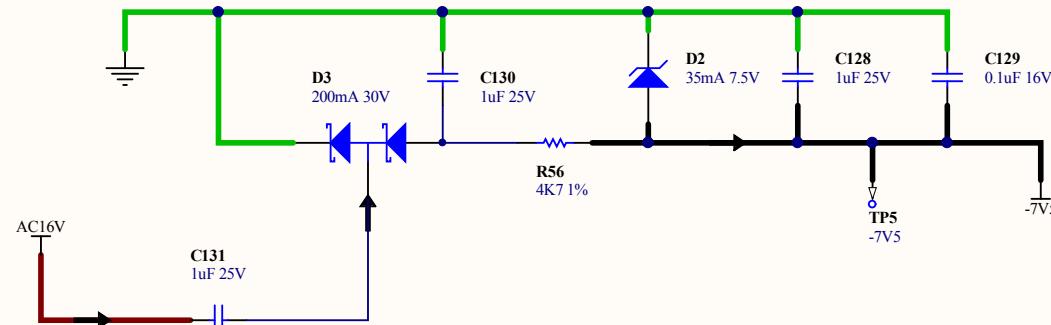




Sheet Title **NB2DSK01 POWER SUPPLIES**Project Title **NanoBoard NB2DSK01**Size: **A4** Assy: **D-810-0007** Revision: **08**Date: **2/17/2011** Time: **5:50:00 PM** Sheet **29** of **64**File: **NB2_PSU.SchDoc**

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Sheet Title ***PSU BZX84C7V5 -7V5***

Project Title ***NanoBoard NB2DSK01***

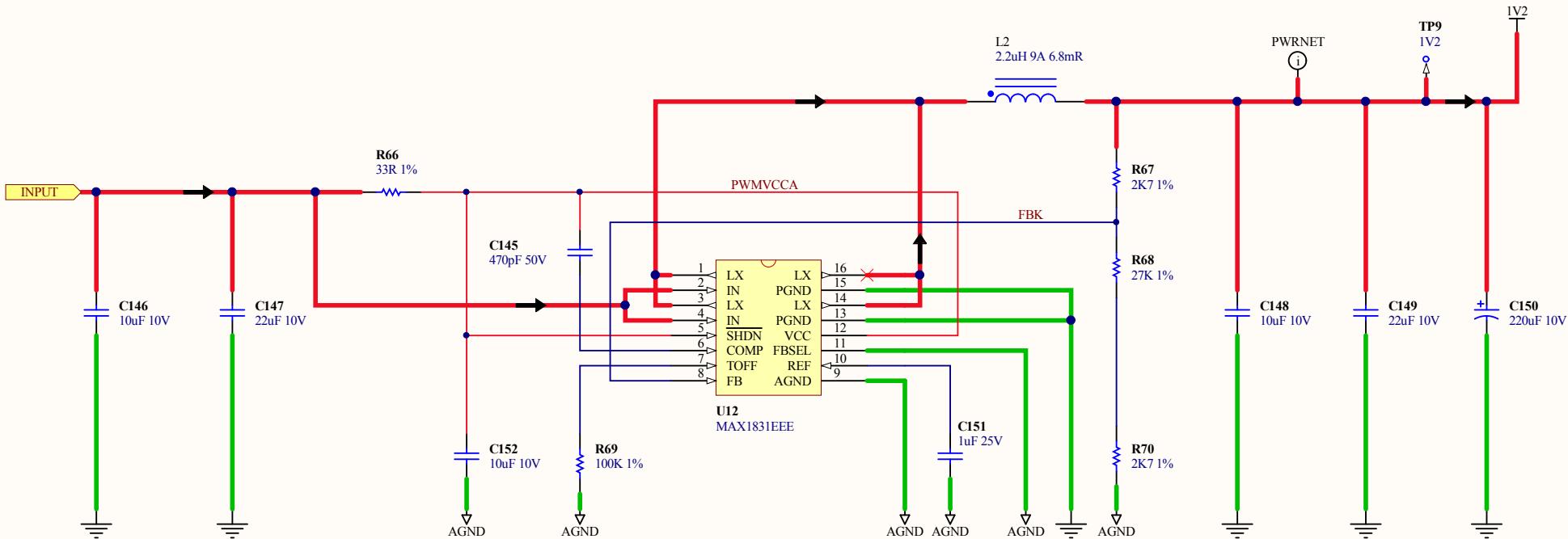
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File: **PSU_BZX84C7V5 -7V5.SchDoc**

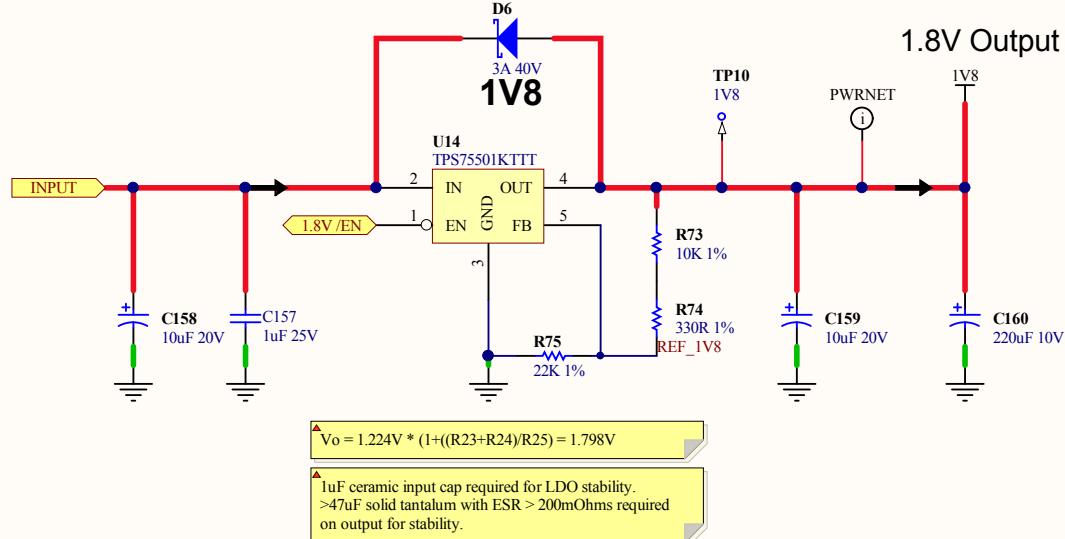
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Sheet Title **PSU MAX1831 1V2**Project Title **NanoBoard NB2DSK01**Size: **A4** Assy: **D-810-0007** Revision: **08**Date: **2/17/2011** Time: **5:50:00 PM** Sheet **37** of **64**File: **PSU MAX1831 1V2.SchDoc**

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Sheet Title **PSU TPS75501 1V8**

Project Title **NanoBoard NB2DSK01**

Size: **A4** Assy: **D-810-0007** Revision: **08**

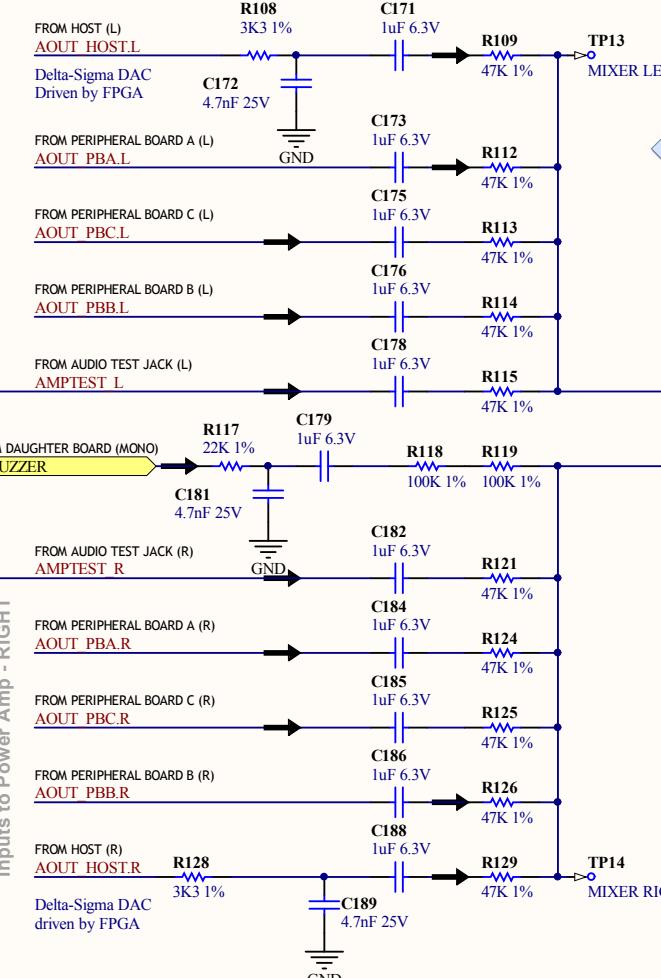
Date: **2/17/2011** Time: **5:50:00 PM** Sheet **30** of **64**

File: **TPS75501_1V8.SchDoc**

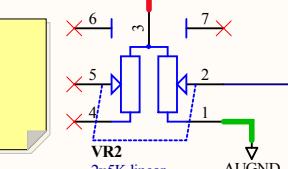
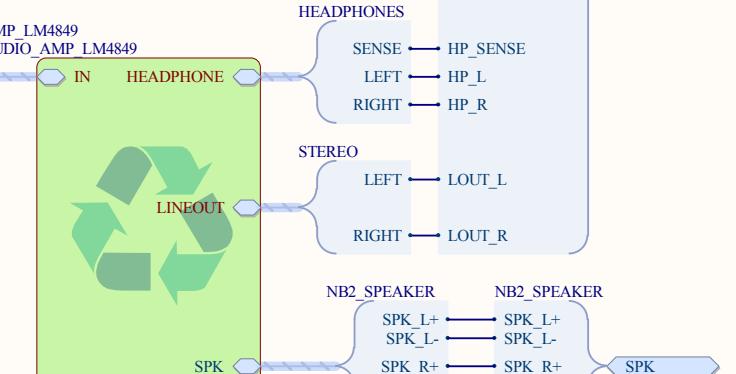
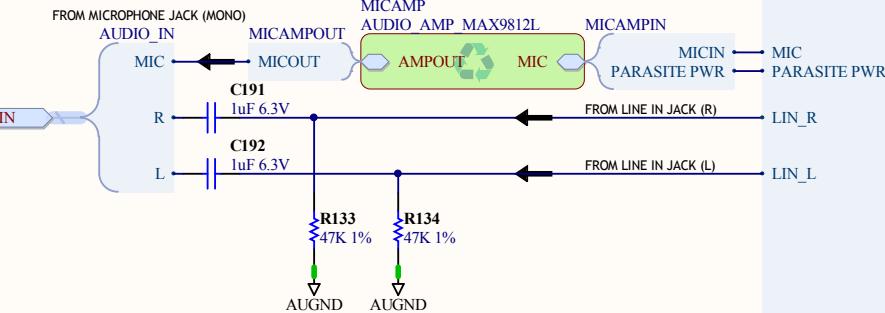
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Audio Mixer - Left Channel

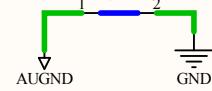


Audio Signal to All Peripheral Boards



Inputs to Power Amp - RIGHT

Audio Mixer - Right Channel



- AOUT_HOST AOUT_HOST
- AOUT_PBA AOUT_PBA
- AOUT_PBB AOUT_PBB
- AOUT_PBC AOUT_PBC

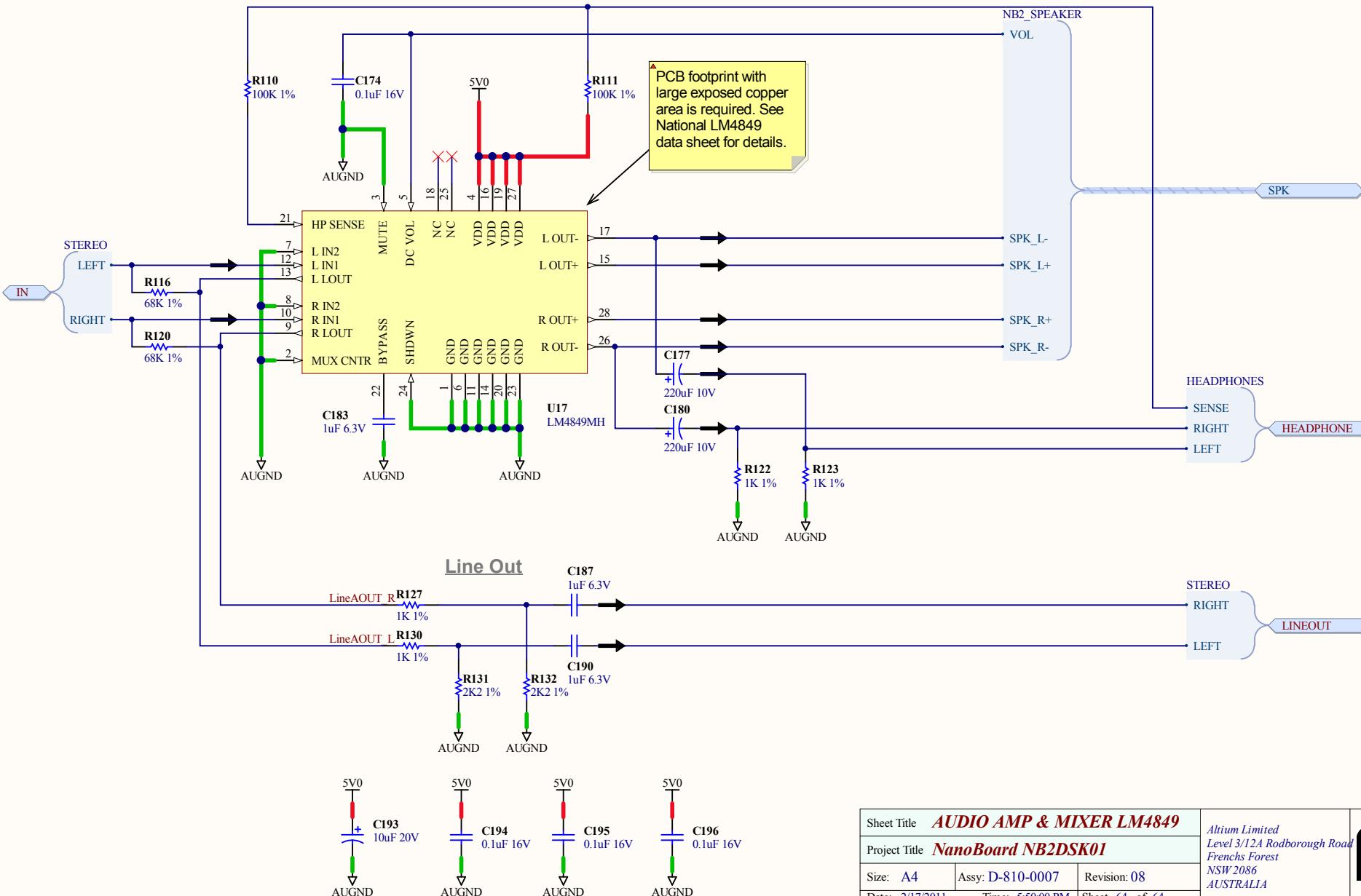
Sheet Title **AUDIO SUB-SYSTEM**Project Title **NanoBoard NB2DSK01**Size: **A4** Assy: **D-810-0007** Revision: **08**Date: **2/17/2011** Time: **5:50:00 PM** Sheet **64** of **64**File: **AUDIO_AMP_NB2A.SchDoc**

AUDIO_EXT
AMP_R
AMP_L

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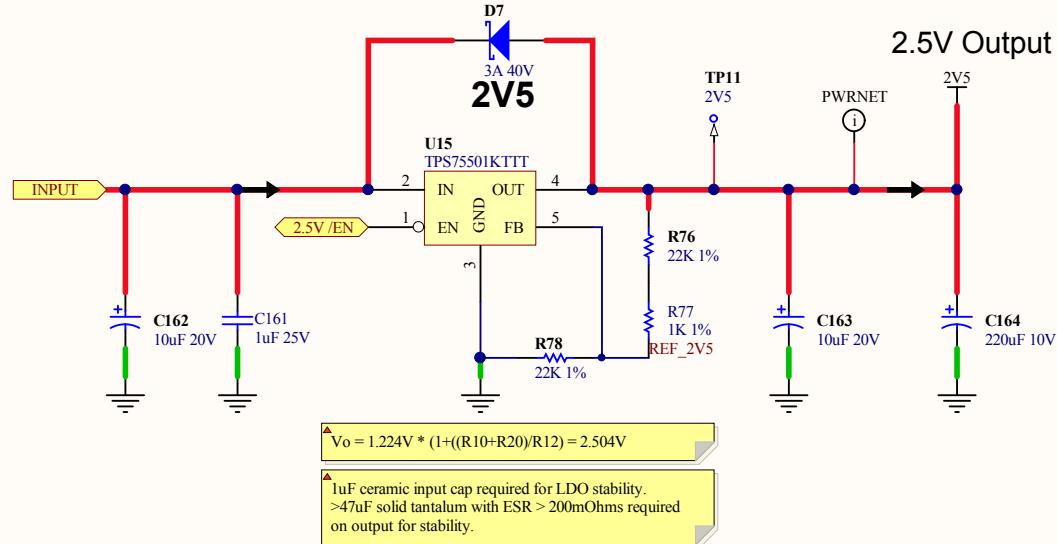


A

Sheet Title **AUDIO AMP & MIXER LM4849**Project Title **NanoBoard NB2DSK01**Size: **A4** Assy: **D-810-0007** Revision: **08**Date: **2/17/2011** Time: **5:50:00 PM** Sheet **64** of **64**File: **AUDIO_AMP_LM4849.SchDoc**

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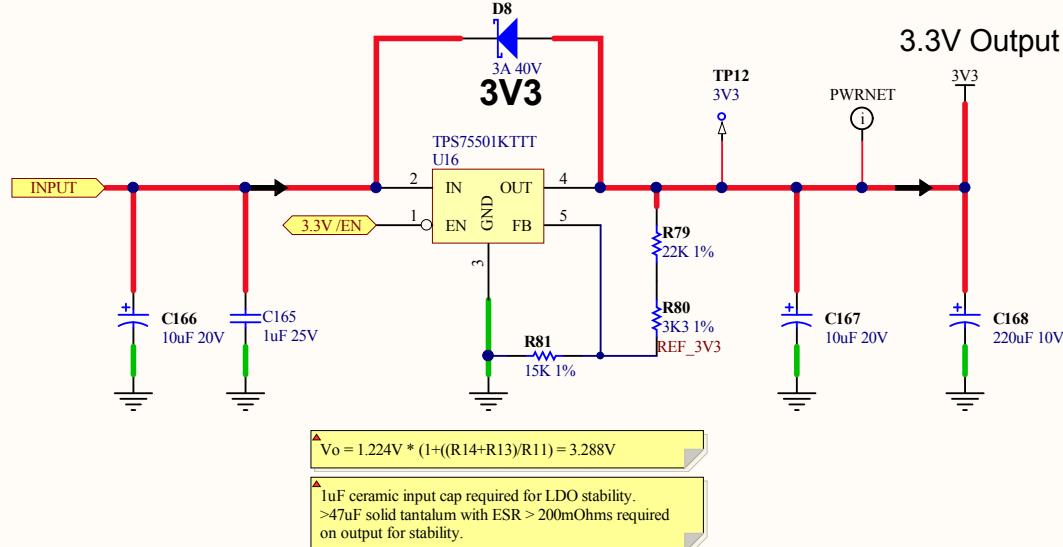




Sheet Title PSU TPS75501 2V5		
Project Title NanoBoard NB2DSK01		
Size: A4	Assy: D-810-0007	Revision: 08
Date: 2/17/2011	Time: 5:50:00 PM	Sheet 31 of 64
File: TPS75501_2V5.SchDoc		

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Sheet Title **PSU TPS75501 3V3**

Project Title **NanoBoard NB2DSK01**

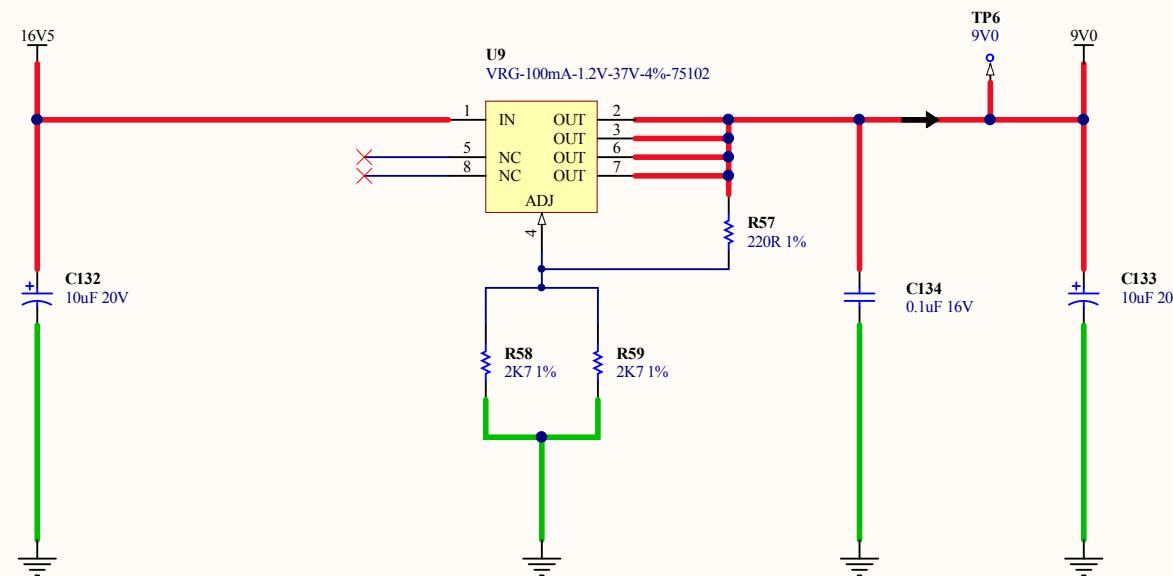
Size: **A4** Assy: **D-810-0007** Revision: **08**

Date: **2/17/2011** Time: **5:50:00 PM** Sheet **32** of **64**

File: **TPS75501_3V3.SchDoc**

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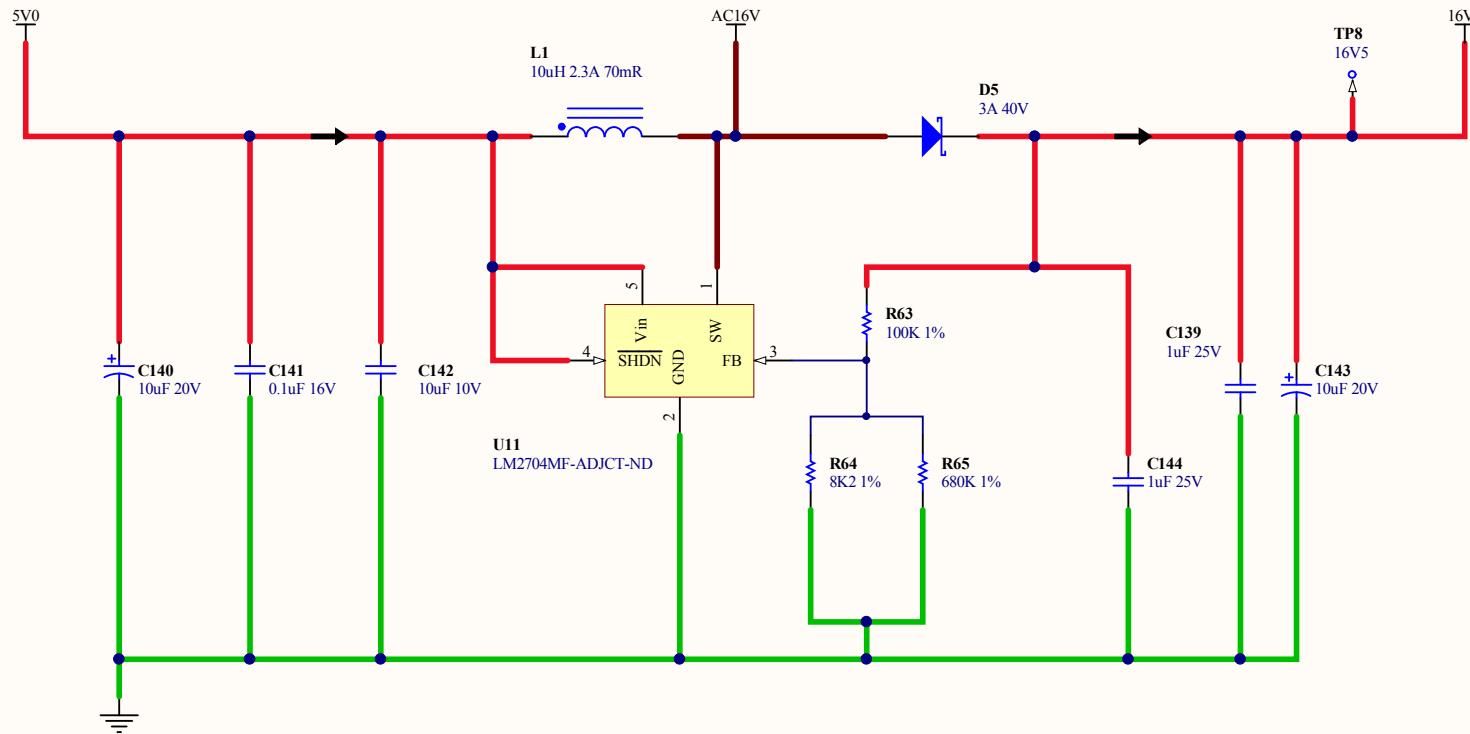
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Project Title <i>NanoBoard NB2DSK01</i>		
Size: A4	Assy: D-810-0007	Revision: 08
Date: 2/17/2011	Time: 5:50:00 PM	Sheet 34 of 64
File: PSU LM317 9V0.SchDoc		

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A

A



D

D

Sheet Title **PSU LM2704 16V5**Project Title **NanoBoard NB2DSK01**Size: **A4** Assy: **D-810-0007** Revision: **08**Date: **2/17/2011** Time: **5:50:00 PM** Sheet **36** of **64**File: **PSU LM2704_16V5.SchDoc**

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A

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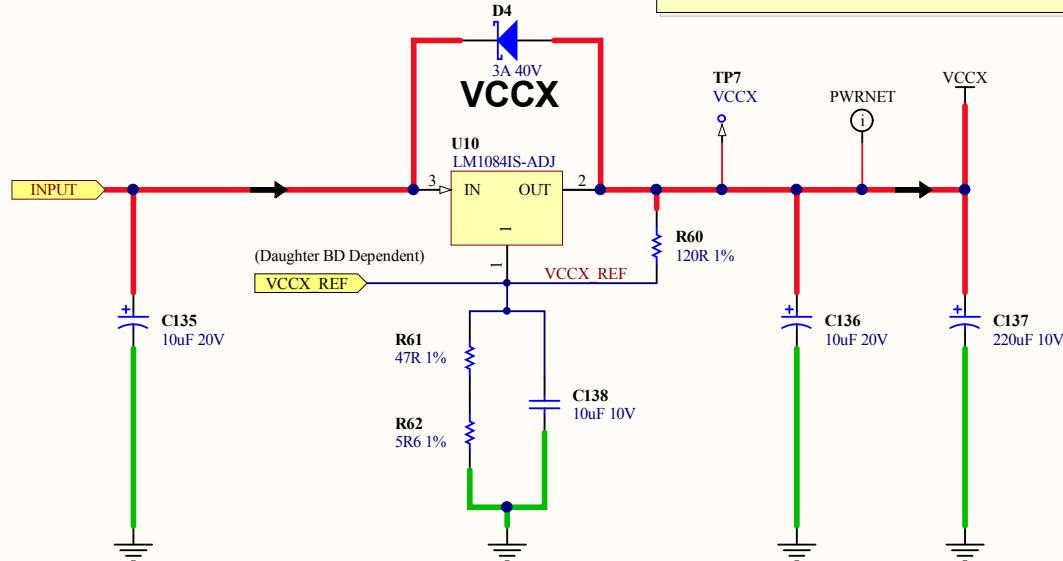
D

The voltage provided by the NB2DSK on VCCX is calculated by the following formula (based on each Daughter Board's sheet "PSU"):

R5 is located on the daughter board between VCCX and VCCX_REF.
R6 is located on the daughter board between VCCX_REF and ground (0V).

$$VCCX = 1.25 * (1 + (R6//52.6) / (R5//120))$$

If R5 & R6 are not loaded,	$VCCX = 1.25 * (1 + 52.6/120) = 1.8 \text{ Volts}$
If R5=82R & R6=680R,	$VCCX = 1.25 * (1 + 48.8/48.7) = 2.5 \text{ Volts}$
If R5 not loaded & R6=680R,	$VCCX = 1.25 * (1 + 48.8/120) = 1.76 \text{ Volts}$

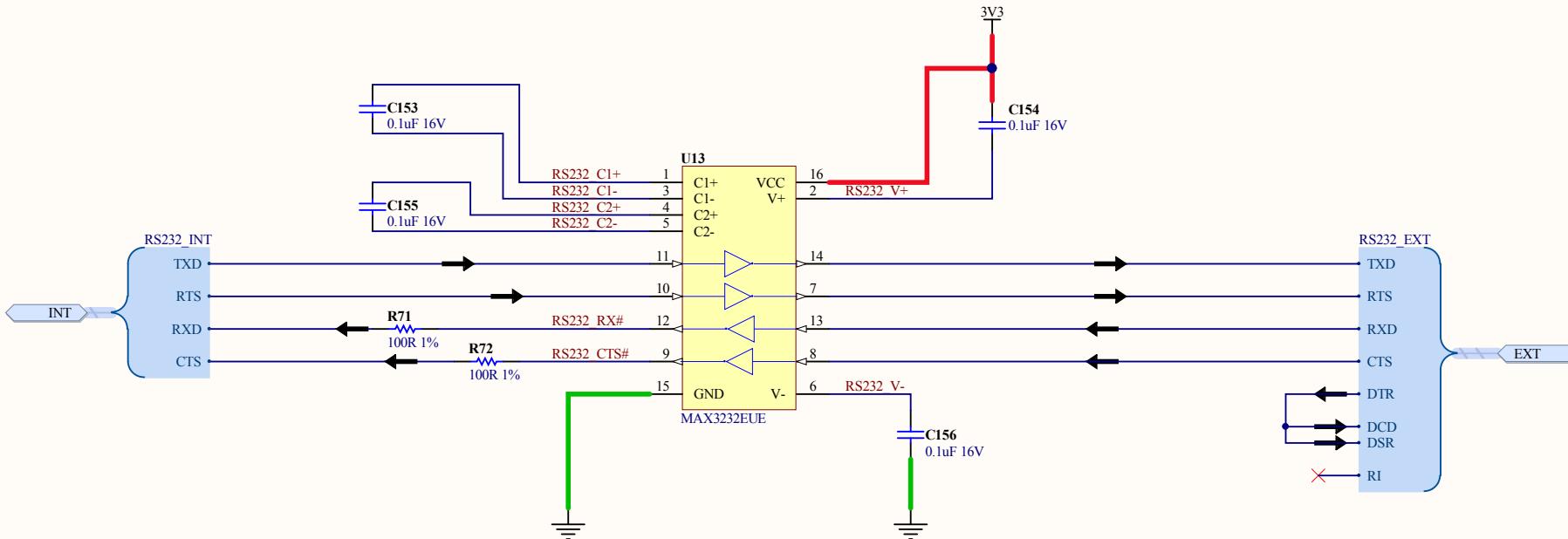


Daughterboard Power Supply VCCX

Sheet Title PSU LM1084 ADJ		
Project Title NanoBoard NB2DSK01		
Size: A4	Assy: D-810-0007	Revision: 08
Date: 2/17/2011	Time: 5:50:00 PM	Sheet 33 of 64
File: PSU LM1084 ADJ.SchDoc		

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Sheet Title	RS232COMMS_1	
Project Title	NanoBoard NB2DSK01	
Size:	A4	Assy: D-810-0007
Date:	2/17/2011	Time: 5:50:00 PM
File:	RS232_MAX3232.SchDoc	Sheet 60 of 64

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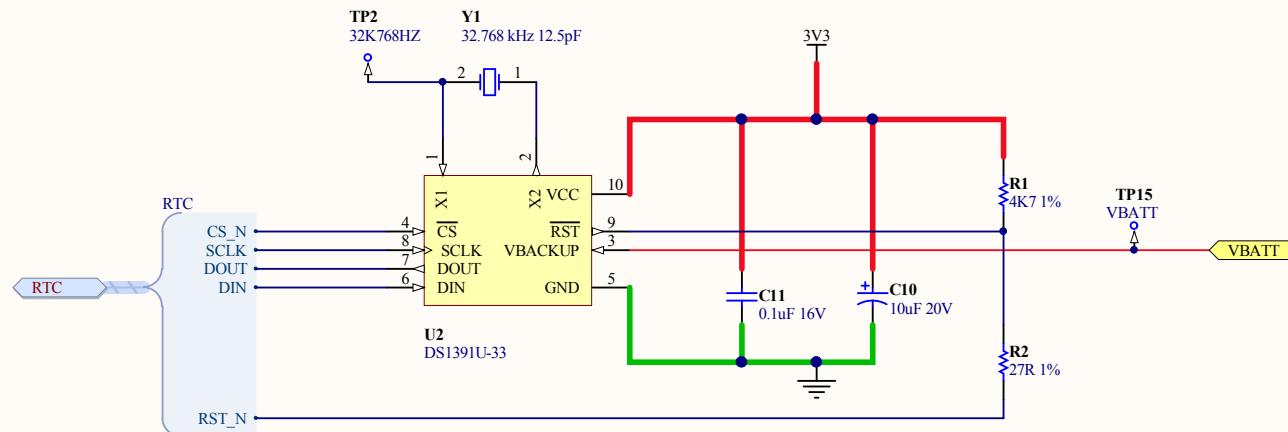
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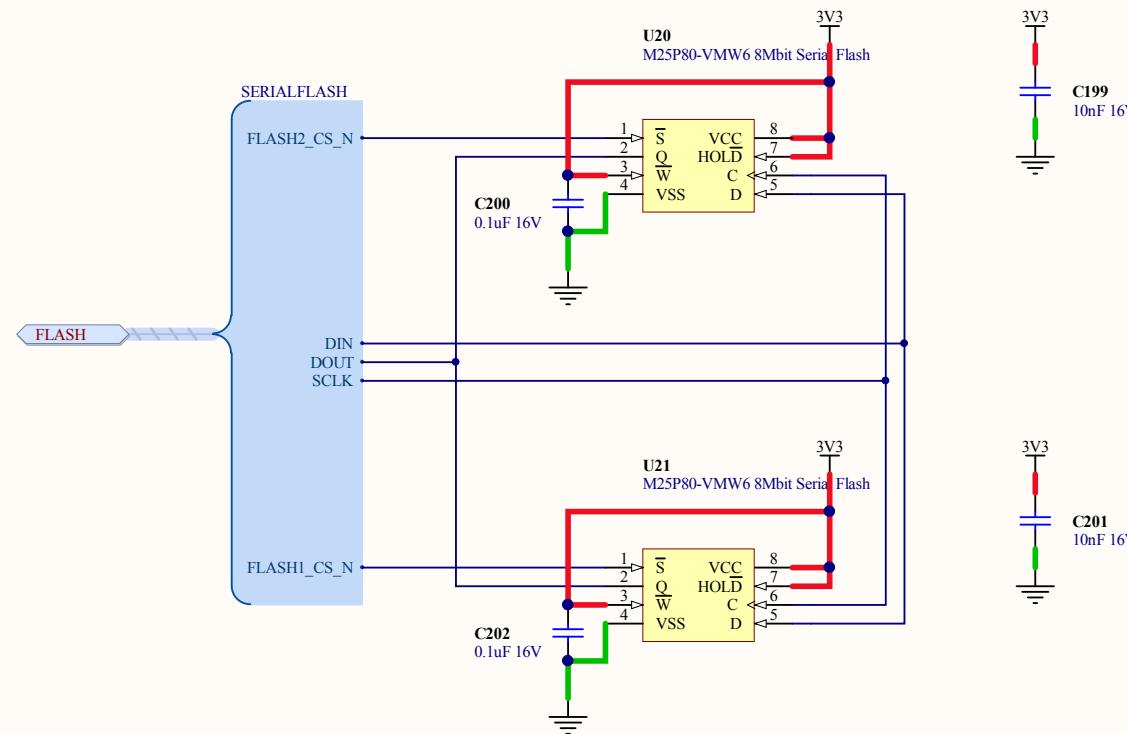
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Sheet Title	SPI Real Time Clock	
Project Title	NanoBoard NB2DSK01	
Size:	A4	Assy: D-810-0007
Date:	2/17/2011	Time: 5:50:01 PM
File:	CLK_DS1391U_RTC.SchDoc	
Revision:	08	Sheet 10 of 64

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Sheet Title **Dual Serial Flash Memory**

Project Title **NanoBoard NB2DSK01**

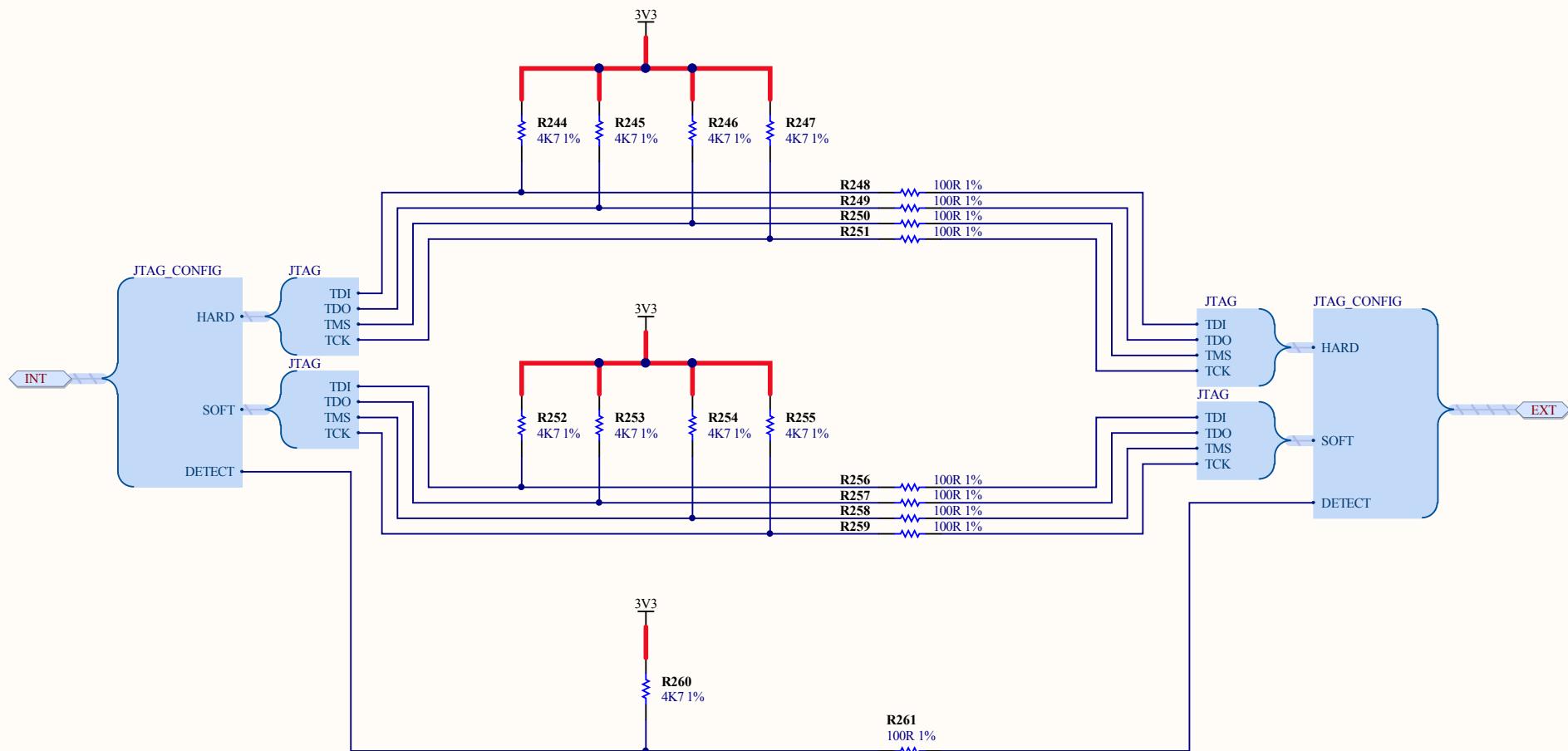
Size: **A4** Assy: **D-810-0007** Revision: **08**

Date: **2/17/2011** Time: **5:50:01 PM** Sheet **8** of **64**

File: **FLASHSPI_M25PX0.SchDoc**

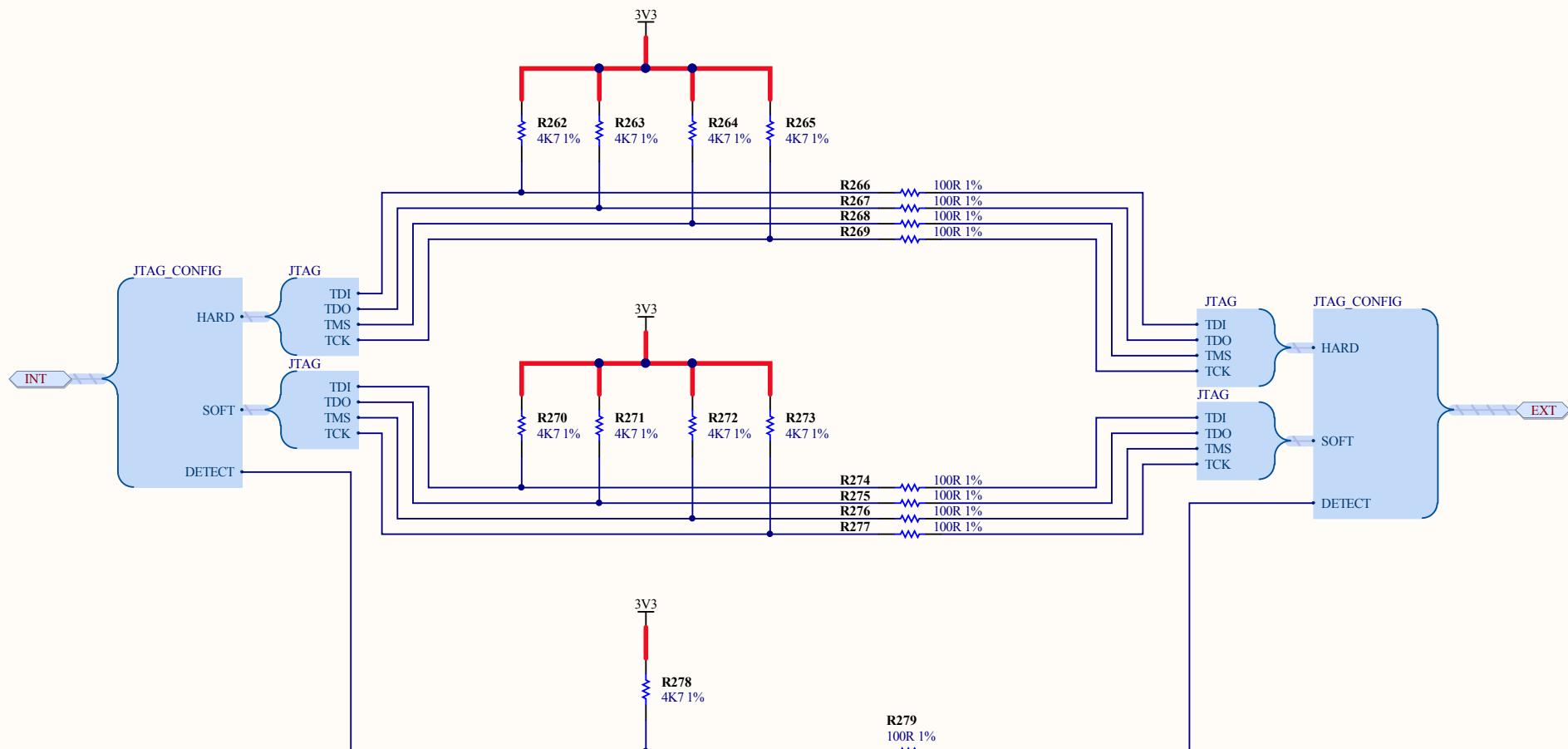
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Sheet Title **Auto-Detect JTAG Circuit**Project Title **NanoBoard NB2DSK01**Size: **A4** Assy: **D-810-0007** Revision: **08**Date: **2/17/2011** Time: **5:50:01 PM** Sheet **21** of **64**File: **JTAG_ALTIUM_AUTO.SchDoc**

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Sheet Title ***Auto-Detect JTAG Circuit***Project Title ***NanoBoard NB2DSK01***Size: **A4** Assy: **D-810-0007** Revision: **08**Date: **2/17/2011** Time: **5:50:01 PM** Sheet **21** of **64**File: **JTAG_ALTIUM_AUTO.SchDoc**

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