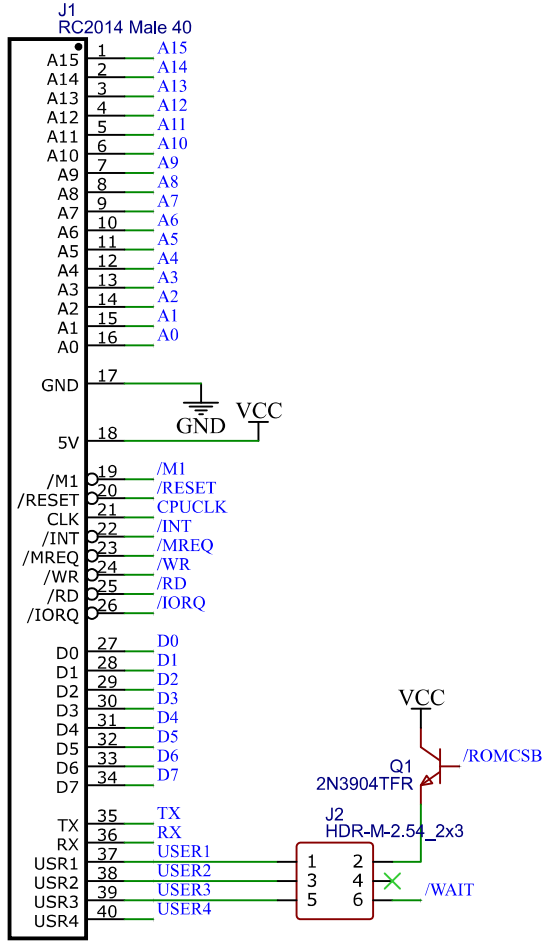
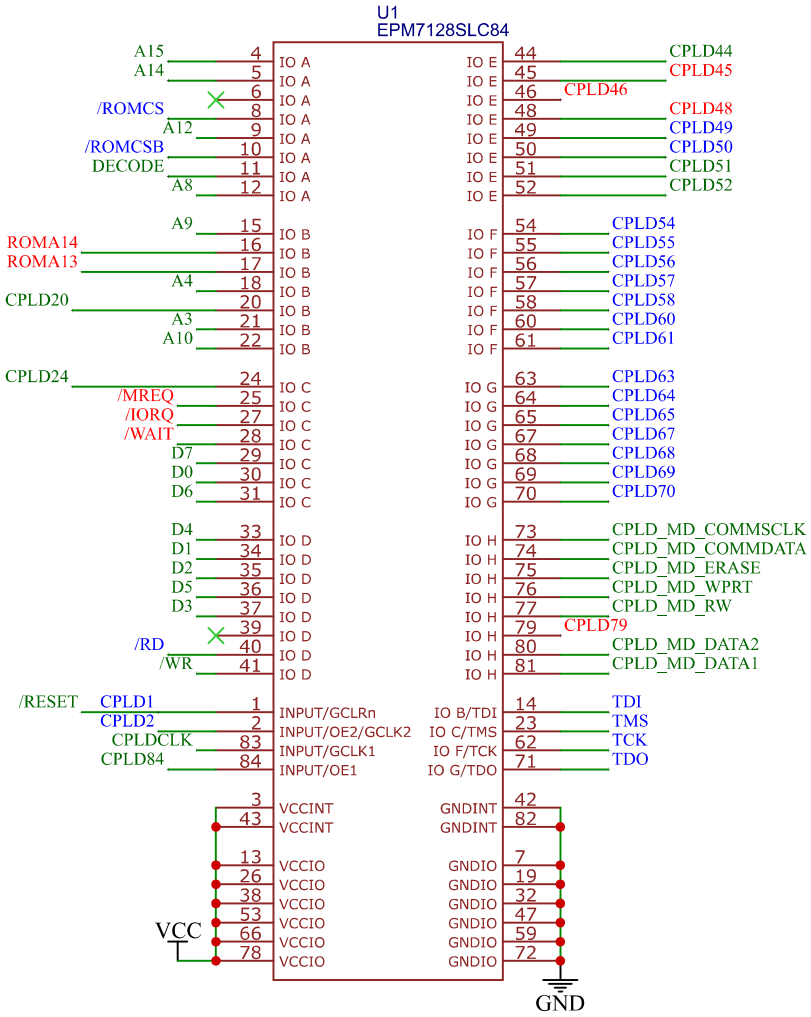
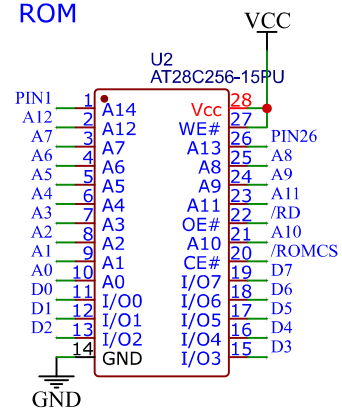
RC2014 BUS CONNECTOR

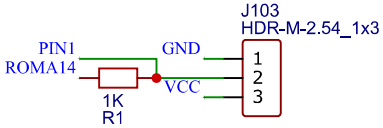


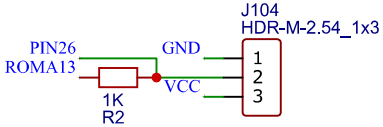
CPLD



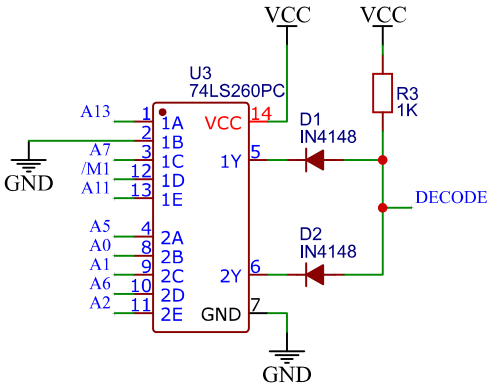
ROM

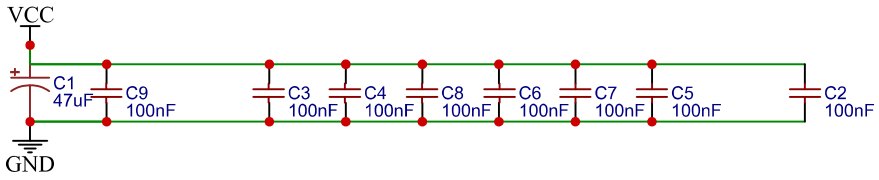


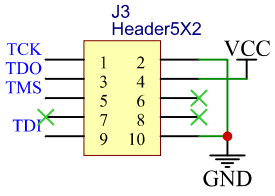




MEMORY ADD DECODER

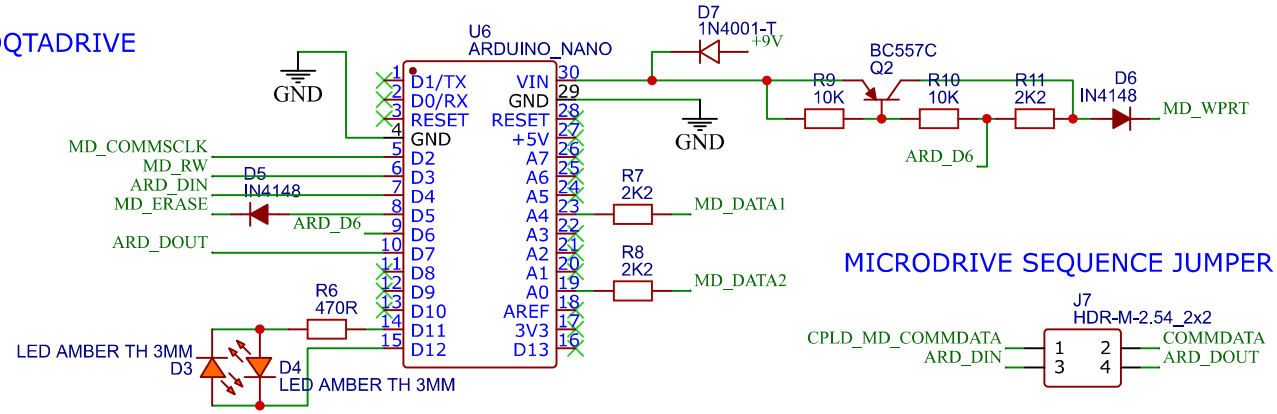






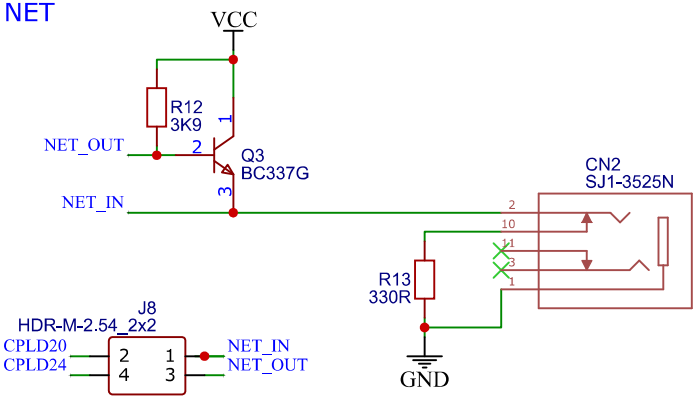
TITLE: ZX INTERFACE 1 DEV BOARD - CPLD & ROM		REV: V1.0
EasyEDA	Company:	Sheet: 1/3
	Date: 24-08-2023 Drawn By:	

OQTADRIVE

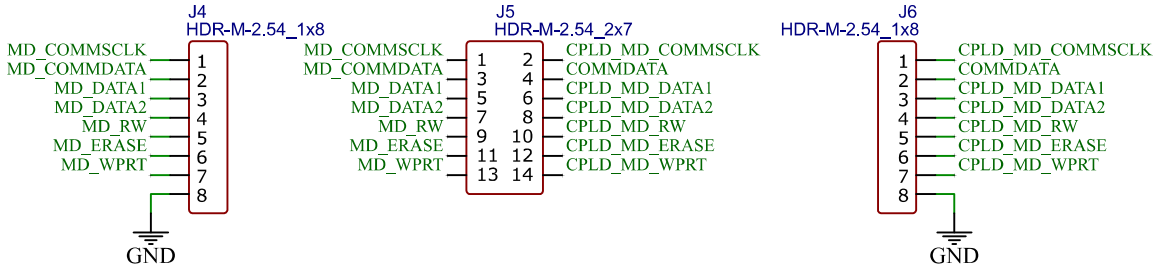


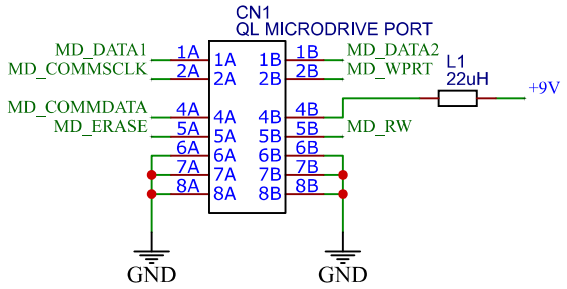
MICRODRIVE SEQUENCE JUMPER

NET

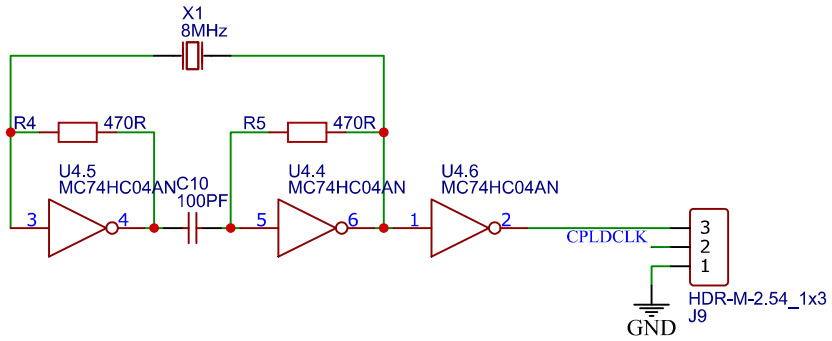


BREAKOUT & EDGE CONNECTOR

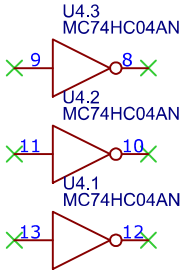




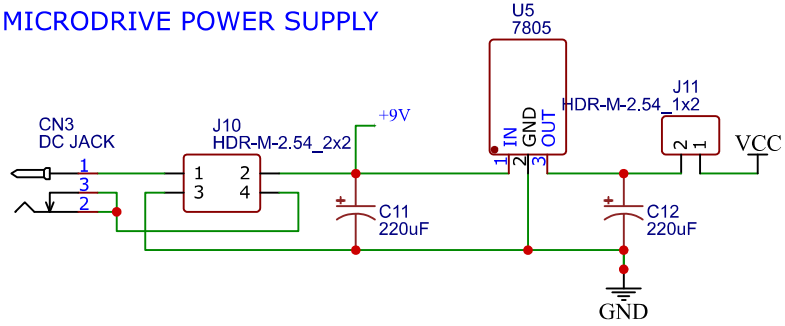
CPLD OSCILLATOR



SPARE GATES



MICRODRIVE POWER SUPPLY



Note: U4 VCC (pin 14) is not connected in V1.0. This will be fixed in V1.1 PCB

TITLE: ZX INTERFACE 1 DEV BOARD - MD, NET & POWER		REV: 1.0
嘉立创EDA	Company:	Sheet: 2/3
	Date: 24-08-2023 Drawn By:	

RC2014 BUS MIRROR

J101
Header-Male-2.54_1x40

1	A15
2	A14
3	A13
4	A12
5	A11
6	A10
7	A9
8	A8
9	A7
10	A6
11	A5
12	A4
13	A3
14	A2
15	A1
16	A0
17	VCC
18	/M1
19	/RESET
20	CPUCLK
21	/INT
22	/MREQ
23	/WR
24	/RD
25	/IORQ
26	D0
27	D1
28	D2
29	D3
30	D4
31	D5
32	D6
33	D7
34	TX
35	RX
36	USER1
37	USER2
38	USER3
39	USER4
40	GND

CPLD BREAKOUT

J102
Header-Male-2.54_1x40

GND	1
CPLD_MD_COMMSCLK	2
CPLD_MD_COMMDATA	3
CPLD_MD_DATA1	4
CPLD_MD_DATA2	5
CPLD_MD_RW	6
CPLD_MD_ERASE	7
CPLD_MD_WPRT	8
CPLD79	9
CPLD24	10
CPLD20	11
GND	12
VCC	13
CPLDCLK	14
CPLD1	15
CPLD2	16
CPLD84	17
CPLD70	18
CPLD69	19
CPLD68	20
CPLD67	21
CPLD65	22
CPLD64	23
CPLD63	24
CPLD61	25
CPLD60	26
CPLD58	27
CPLD57	28
CPLD56	29
CPLD55	30
CPLD54	31
CPLD44	32
CPLD45	33
CPLD46	34
CPLD48	35
CPLD49	36
CPLD50	37
CPLD51	38
CPLD52	39
VCC	40

TITLE: ZX INTERFACE 1 DEV BOARD - TEST POINTS		REV: 1.0
嘉立创EDA	Company:	Sheet: 3/3
	Date: 24-08-2023 Drawn By:	