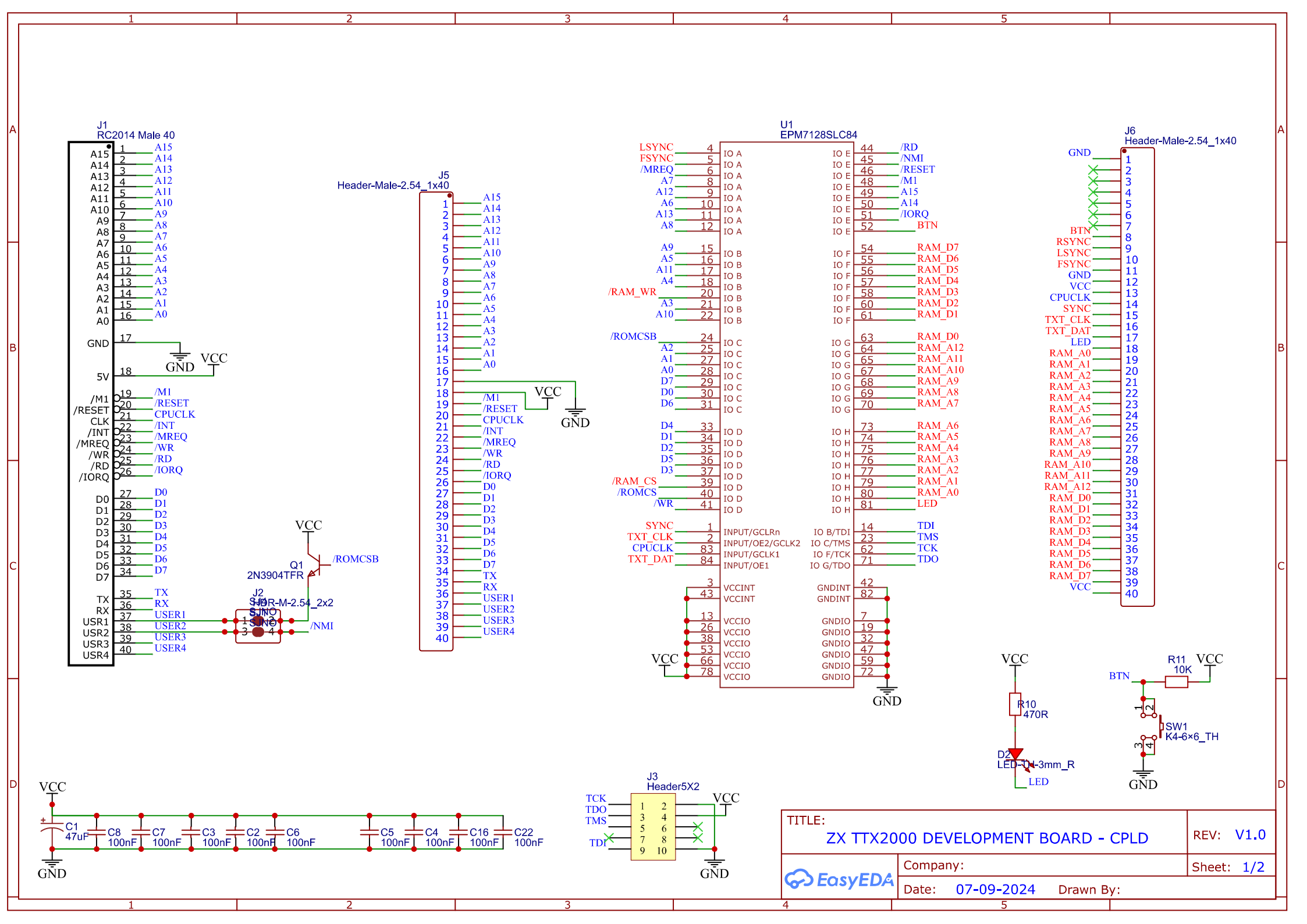
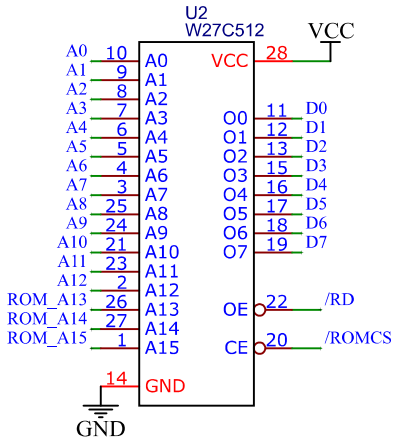
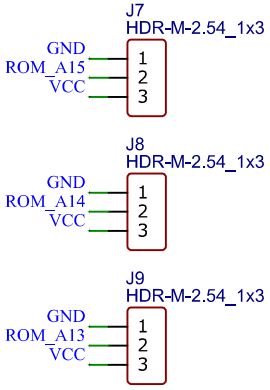
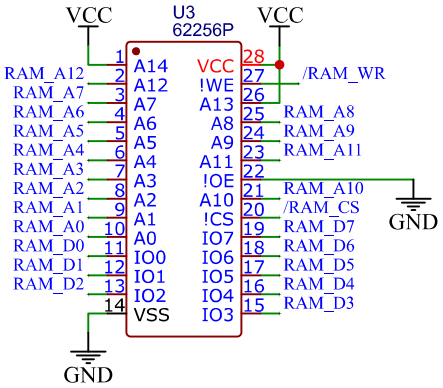

J1
RC2014 Male 40
J5
Header-Male-2.54_1x40
U1
EPM7128SLC84
J6
Header-Male-2.54_1x40
Q1
2N3904TFR
J2
J3
Header5X2
R10
470R
R11
10K
SW1
K4-6×6_TH
D2
LED-TH-3mm_R
C1
47uF
C8
100nF
C7
100nF
C3
100nF
C2
100nF
C6
100nF
C5
100nF
C4
100nF
C16
100nF
C22
100nF
VCC
GND
/ROMCSB
/NMI
LED
BTN
TITLE:
ZX TTX2000 DEVELOPMENT BOARD - CPLD
REV: V1.0
Company:
Sheet: 1/2
Date: 07-09-2024
Drawn By:
EasyEDA

ROM

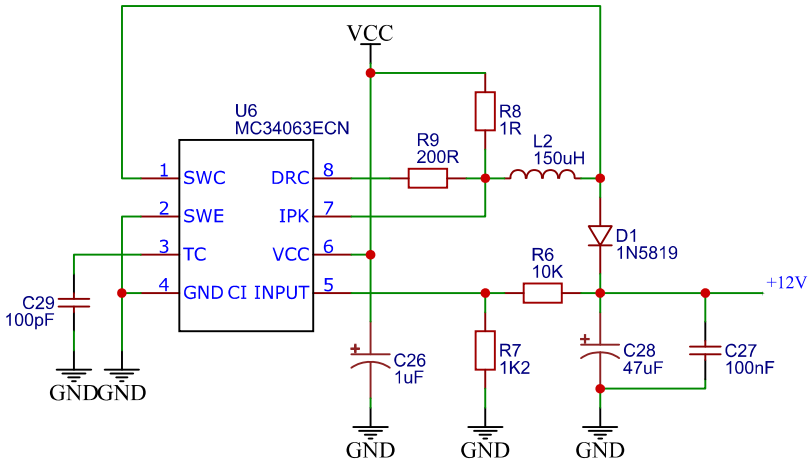




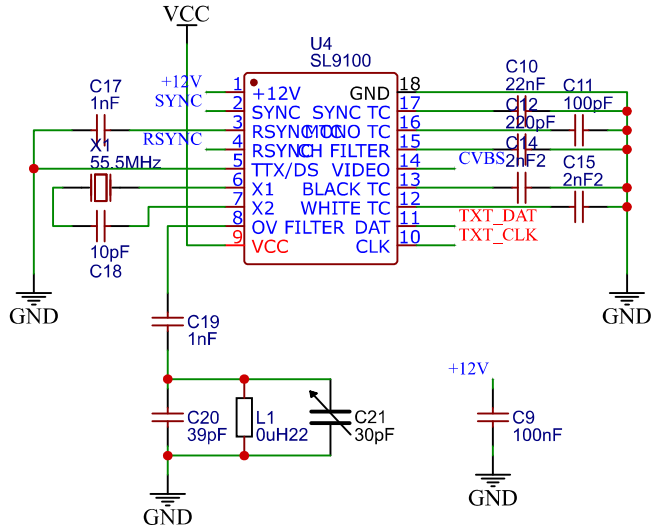
RAM



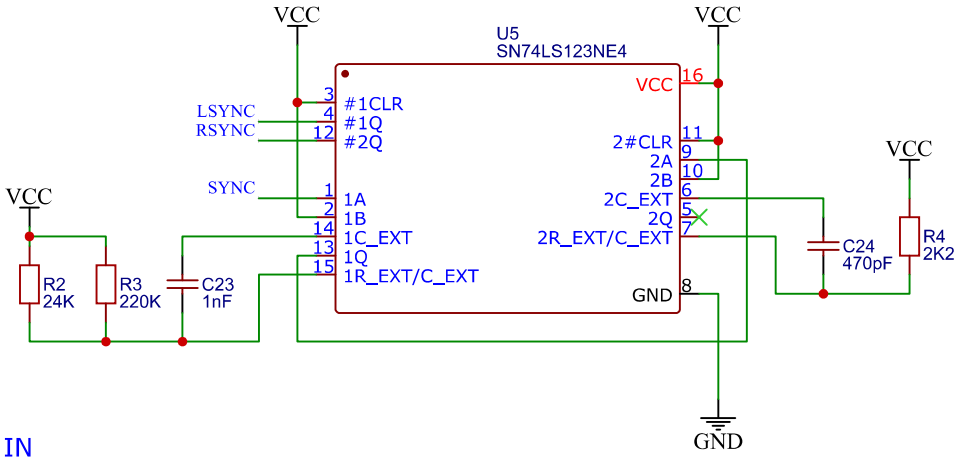
+5V to +12V STEP-UP CONVERTER



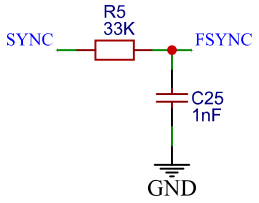
DATA SEPARATOR



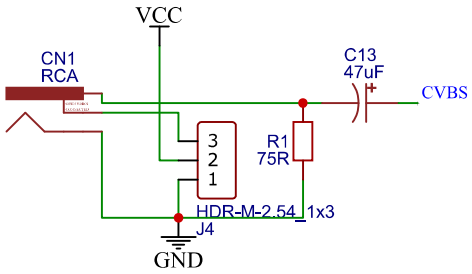
RSYNC TIMING



FSYNC LPF



CVBS IN

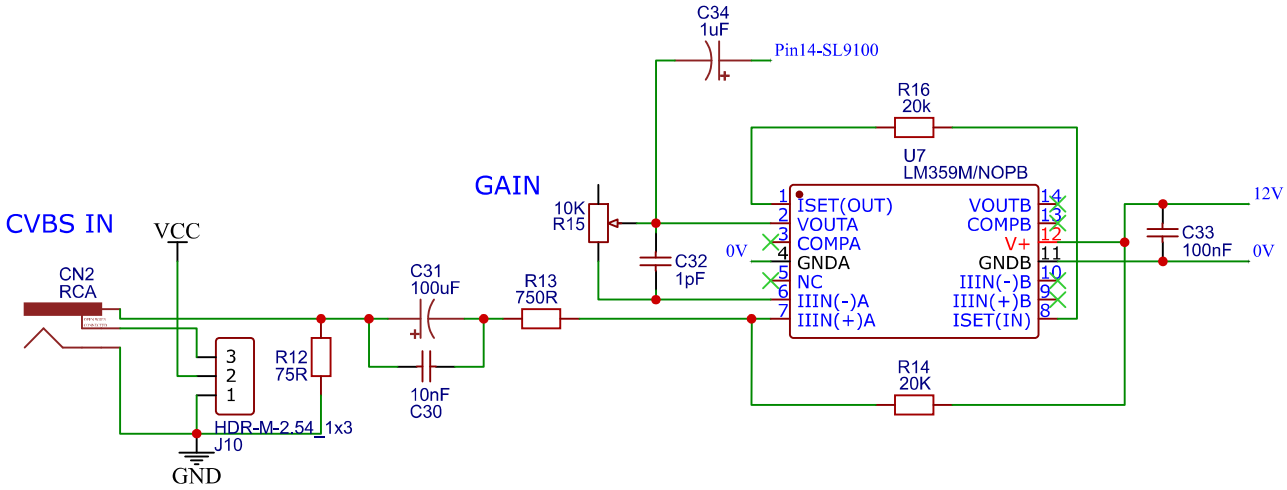


TITLE: ZX TTX2000 DEVELOPMENT BOARD - CPLD		REV: V1.0
嘉立创EDA	Company:	Sheet: 2/2
	Date: 07-09-2024 Drawn By:	

These changes were made to the V1.0 design during development
They will be incorporated into V1.1

CVBS & Video Amp

Do not fit C13 - SL9100 needs ~4.0V P-P video signal to amplify CVBS source



Data Separator

Do not fit C20 - stabilises bit oscillator
Adjust C21 to give 7Mhz clock rate

RSync Generator

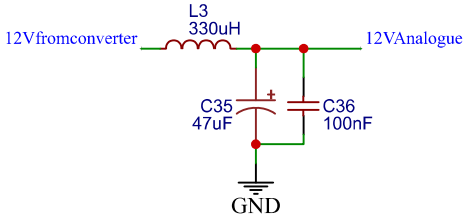
Do not fit R2 and changes R3 to 10K - move RSync pulse earlier so it's active between run-in code bytes

FSync LPF

Change C25 to 470pF

PSU

Use 5V to 12V step-up module instead of U6 etc



TITLE: Fixes to be incorporated in V1.1		REV: 1.0
嘉立创EDA	Company:	Sheet: 1/1
	Date: 2024-10-29 Drawn By:	