

# Part1 Design Document

13302010017 Guo Liangchen

## Find the opcode

I find the two opcodes in the same way. For example, test1. Just the following steps: 1. Disassemble the binary files given:

```
ssllittle-na-ssstrix-objdump -x -d test1 > test1.asm
```

2. Run the sim-fast with gdb:

```
gdb sim-fast
```

3. Set up the breakpoint, then run the simulator:

```
(gdb) b sim-fast.c : 444
Breakpoint 1 at 0x40e377: file sim-fast.c, line 444.
(gdb) r test1
```

4. Get the inst by using gdb's print command:

```
(gdb) p/x inst
```

Then we get the inst is 0x10111300 5. Just find the inst in the file test1.asm which we just generated, we will get:

```
...
00400270 <add0k+30> 0x00000061:10111300
...
```

Then we find the opcode of test1 is 0x61.

## Add the instruction

### addok

The solution is simple. Just copy the add instruction definition and modify it: 1. Modify the opcode to 0x61 and the name of the instruction. 2. Modify the implementation to:

```
1 if (OVER(GPR(RS), GPR(RT)))
2   SET_GPR(RD, 0);
3 else
4   SET_GPR(RD, 1);
```

### bitcount

The solution based on divide-and-conquer. [This page](#) describes the solution. 1. Modify the opcode to 0x62 and the name of the instruction. 2. Modify the implementation to the following:

```
1 unsigned int v = GPR(RS);
2 unsigned int c;
3 c = v - ((v >> 1) & 0x55555555);
4 c = ((c >> 2) & 0x33333333) + (c & 0x33333333);
5 c = ((c >> 4) + c) & 0x0F0F0F0F;
6 c = ((c >> 8) + c) & 0x00FF00FF;
7 c = ((c >> 16) + c) & 0x0000FFFF;
8 if (UIMM == 0)
9   SET_GPR(RT, 32 - c);
10 else
11   SET_GPR(RT, c);
```