An 82% Energy-Saving Change-Sensing Flip-Flop in 40nm CMOS for Ultra-Low Power Applications

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***Abstract*— In this paper, we propose a novel 24-transistor change-sensing flip-flop (CSFF) for ultra-low power applications. With the aid of an internal change-sensing unit, the proposed CSFF eliminates redundant transitions of internal clocked nodes when there is no change in the flip-flop content. No additional transistors are required compared to the conventional transmission-gate flip-flop (TGFF). Measurement results from a test chip fabricated in 40nm CMOS technology show that CSFF achieves the power reduction of 82% and 68% at 10% activity rate and 1.0V, and the C-Q delay improvement of 37% and 11% in the supply voltage range of 0.4V to 1.0V compared to TGFF and SSCFF. While achieving better power and energy efficiencies, CSFF still maintains robust functionality at ultra-low voltage operations. Measurement results also demonstrate that CSFF shows the minimum operating voltage of 0.19V.**

Keywords— flip-flop; ultra-low voltage; ultra-low power

I. INTRODUCTION

Flip-flops are simple but critical components in modern digital integrated circuits (ICs); they typically dominate the total area and power of the overall systems. For example, the SPARC T4 processor in [1] contains 2.6 million flip-flops, consuming more than 20% of the total core power of the processor. In fact, flip-flops are typically responsible for tremendous dynamic power in systems on chips (SoCs) due to unnecessary transitions of their large number of internal clocked nodes when there are no changes in the flip-flop data.

The transmission-gate flip-flop (TGFF) (Fig. 1) is the most widely-used flip-flop since it is static, contention-free, and robust with voltage scaling; but it consumes excessive power caused by many internal clocked nodes that always toggle. These redundant transitions even occur when the input D does not change the content of the flip-flop. Several low-power flip-flops [2-6] have been proposed to resolve this major concern. However, most of them suffer from large area penalty, which is too costly since flip-flops typically occupy a significant amount of logic area in SoCs. The adaptive-coupling flip-flop (ACFF) in [2] could avoid the area overhead by only employing the adaptive-coupling element (ACE) in the master latch and removing the ACE in the slave latch as depicted in Fig. 2, but this could result in higher operating voltages (≥0.75V) due to the contention in the slave latch. The static single-phase contention-free flip-flop (SSCFF) in [7] provides robust energy-saving operations over a wide range of supply voltages with no area overhead, but SSCFF only eliminates unnecessary transitions of its clocked nodes when input data stay at the logic '*high*' level. Indeed, SSCFF still suffers from power penalty due to redundant transitions of its clocked node *CN* when the input D does not change its state from the logic '*low*' level as illustrated in Fig. 3. TABLE I summarizes the comparison of the previous flip-flops.

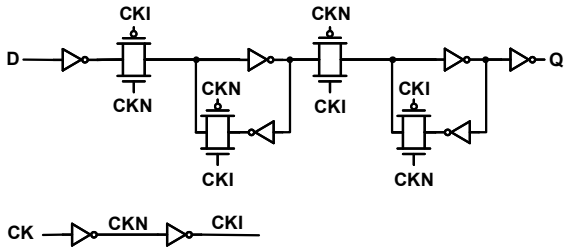

Fig. 1. Schematic of conventional TGFF

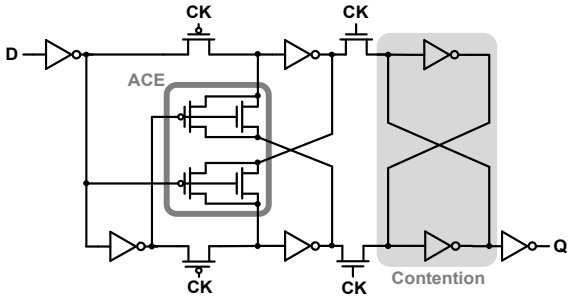

Fig. 2. Schematic of ACFF [2]

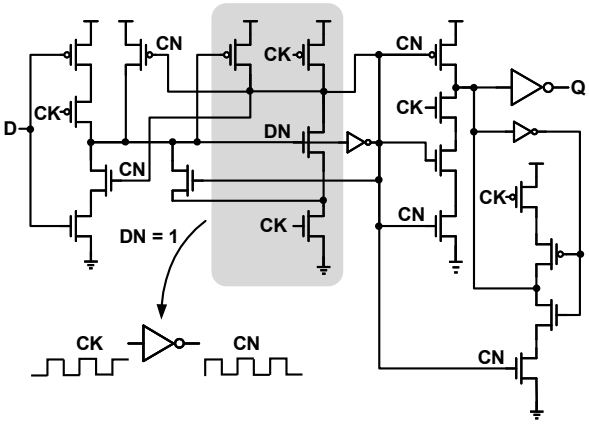

Fig. 3. Schematic of SSCFF [7]

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TABLE I. COMPARISON OF THE PREVIOUS FLIP-FLOPS

	TGFF	ACFF [2]	SSCFF [7]
Ultra-low Voltage Operation	YES	**NO**	YES
Redundant Transitions of Internal Clocked Nodes	**YES**	NO	**YES**
Transistor count	24	22*	24

*It becomes 26 if ACE is employed in the slave latch for ultra-low voltage operations.

In this paper, we present a novel D-flip-flop sensing the changes in the flip-flop data for eliminating redundant transitions of internal clocked nodes. This significantly reduces the dynamic power when there is no change in the flip-flop content. It also achieves robust functionality at ultra-low voltage operations and further improves performance compared to the conventional TGFF and SSCFF.

II. PROPOSED CHANGE-SENSING FLIP-FLOP (CSFF)

Fig. 4 illustrates the schematic of the proposed 24-transistor change-sensing flip-flop (CSFF). The master consists of T1~T3, and its latch (T7, T10~T14) while the slave is composed of T10, T15~T19, and its latch (T9, T20~T24). The change-sensing unit (T4~T9) as highlighted in Fig. 4 detects the change in the data input D. T6 and T7 detect the change from low to high while T8 and T9 detect the change from high to low. With the aid of the internal change-sensing unit, the clocked node *CS* only toggles when the data input D changes its state. When the current input data are continuously the same as the previous data stored in the slave latch, the internal clocked node *CS* is always held high by T4. Thus, CSFF completely removes the redundant transitions, which always happens in TGFF even when there are no changes in the flip-flop data, and occurs in SSCFF when the input D persistently stays at the logic '*low*' level as illustrated in Fig. 5.

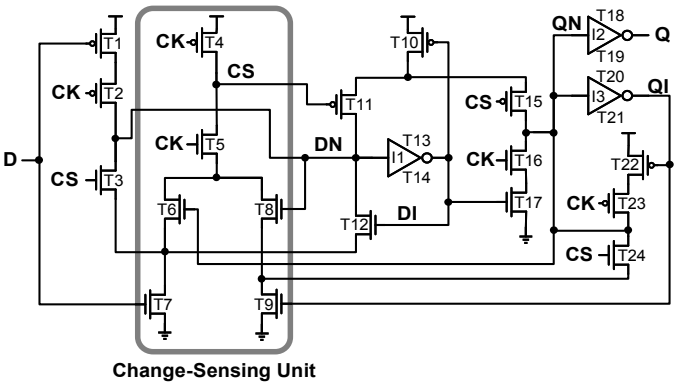

Fig. 4. Schematic of the proposed CSFF

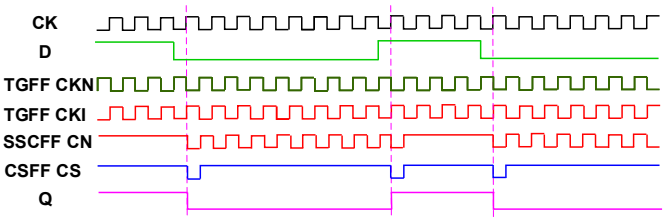

Fig. 5. Transitions of internal clocked nodes in TGFF, SSCFF, and CSFF

Fig. 6 shows the operation details of the proposed CSFF. When CK=0, the clocked node *CS* pre-charges through T4. The master passes the new data to the flip-flop while the slave latch holds the previous data. When CK goes high, the change-sensing unit detects the change in D and discharges the clocked node *CS* through the '*high-to-low-sensing*' path (T5, T8~T9) or the '*low-to-high-sensing*' path (T5~T7). Then, the master latch keeps the updated data, and the slave passes the data to the output. If the updated level is low, *QN* is held high by T10 and T15; thus, the output Q goes low. In the case that the updated level is high, QN is kept low by T16 and T17; then, the output Q goes high.

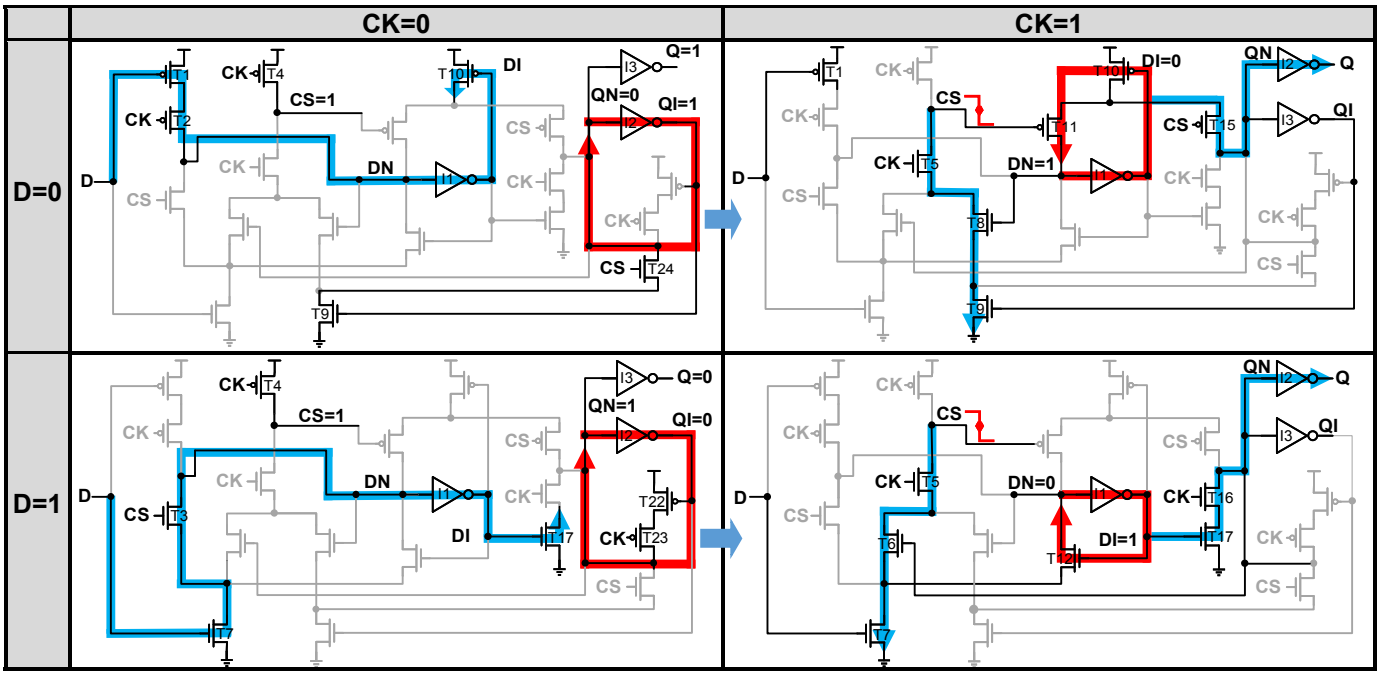

Fig. 6. Operation details of the proposed CSFF

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III. Testing Circuit Implementation

A. C-Q delay/ Setup/ Hold Time Testing Circuit

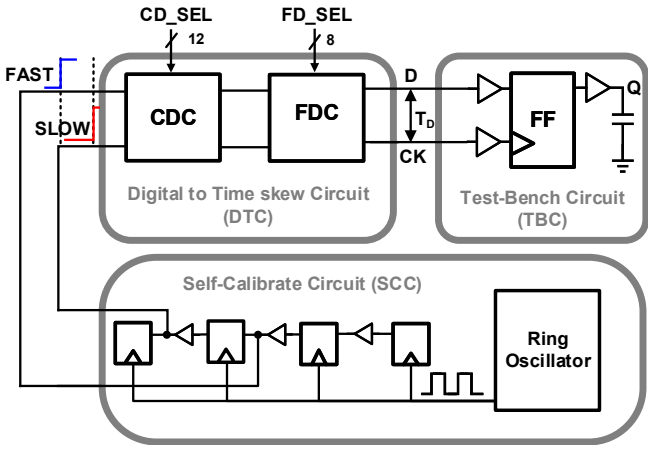

Fig. 7. C-Q delay/ setup/ hold time testing circuit

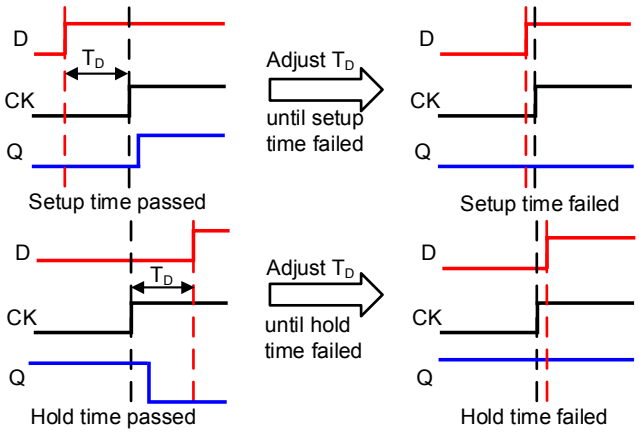

Fig. 8. Setup/hold time measuring method

The C-Q delay/ setup/ hold time testing circuit is illustrated in Fig. 7, which is based on the structure in [8]. It includes Self-Calibration Circuit (SCC), Digital to Time skew Circuit (DTC), and Test-Bench Circuit (TBC). TBC mainly consists of flip-flops and necessary buffers for measuring C-Q delay. DTC includes Coarse Delay Control (CDC) and Fine Delay Control (FDC) blocks for generating digitally-controlled delay skew T_D between the data D and the clock CK. For T_D control with a larger step T_C, CD_SEL in CDC is adjusted to control the number of the coarse delay unit in the data path and the clock path. For T_D control with a smaller step T_F, FD_SEL in FDC is used. The ring oscillator in SCC generates the internal clock for the D-flip-flop chain to create different FAST and SLOW signals for measuring the coarse delay T_C and the fine delay T_F. Once T_C and T_F are known, the setup/ hold time of the flip-flops can be accurately estimated by adjusting the time delay T_D between the clock and the data to the setup/hold time pass/fail point as illustrated in Fig. 8.

B. Power Testing Circuit

Fig. 9 illustrates the power testing circuit for measuring power consumptions of the flip-flops in different activity rates.

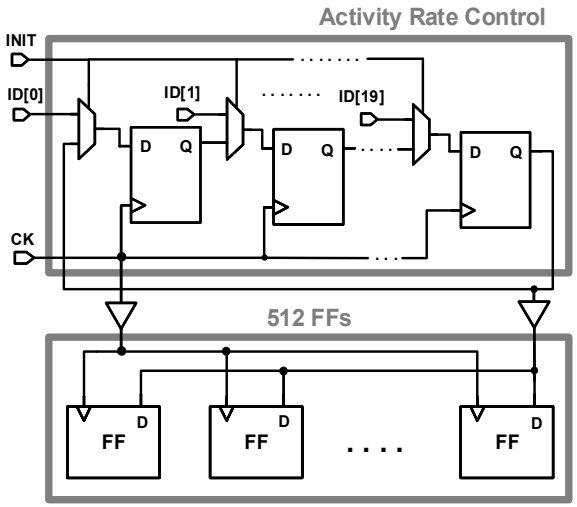

Fig. 9. Power testing circuit

When INIT=0, the activity rate is initialized by a 20-bit data input ID. When INIT goes high, the activity rate is applied, and total power consumption of the flip-flops is measured. To accurately measure power consumptions of the flip-flops (TGFF, SSCFF, and CSFF), 512 units of each flip-flop are implemented, and the average values are determined.

IV. Measurement Results

CSFF was characterized in a 40nm CMOS test chip, and TGFF and SSCFF were also implemented in the same test chip for fair comparisons. Fig. 10 (a) and (b) demonstrate the measured power consumption of the flip-flops at 1.0V and 0.4V, respectively. With the aid of the change-sensing unit, CSFF mostly consumes only leakage power at 0% activity rate, and it also provides more energy-efficient operations at low activity rates compared to TGFF and SSCFF. The average activity rate of flip-flops in SoCs is typically from 5% to 15%; CSFF saves 84% to 60% and 90% to 77% power compared to SSCFF and TGFF, respectively, in this range. From the power measurement, at 10% activity rate, CSFF has 82% and 84% lower power consumption, compared to TGFF, at 1.0V and 0.4V, respectively. When compared to SSCFF, CSFF exhibits the reduction of 68% and 69%. At 20% activity rate, CSFF shows 71% and 74% improvement in total power consumption vs TGFF, at 1.0V and 0.4V, respectively. Compared to SSCFF, CSFF has 51% and 48% improvement. In terms of energy consumption, CSFF exhibits 82% and 84% reduction, compared to TGFF, and 68% and 69% improvement, compared to SSCFF, at 1.0V and 0.4V, respectively, as shown in Fig. 10 (c). Fig. 10 (d) shows the measured leakage power of the flip-flops. CSFF has 40% and 38% lower energy consumption at 1.0V and 0.4V, respectively, compared to TGFF. CSFF also provides a slight improvement of 10% in leakage over SSCFF. Fig. 10 (e) shows the measured C-Q delay of the flip-flops. CSFF shows 37% delay reduction over TGFF in the operating voltage range of 0.4V to 1.0V. Compared to SSCFF, CSFF only provides a modest delay improvement of 11%. Fig. 10 (f) shows the die micrograph of the test chip. TABLE II includes the measured setup and hold time, and summarizes the measurement comparison of the flip-flops. With the same transistor count as TGFF and SSCFF,

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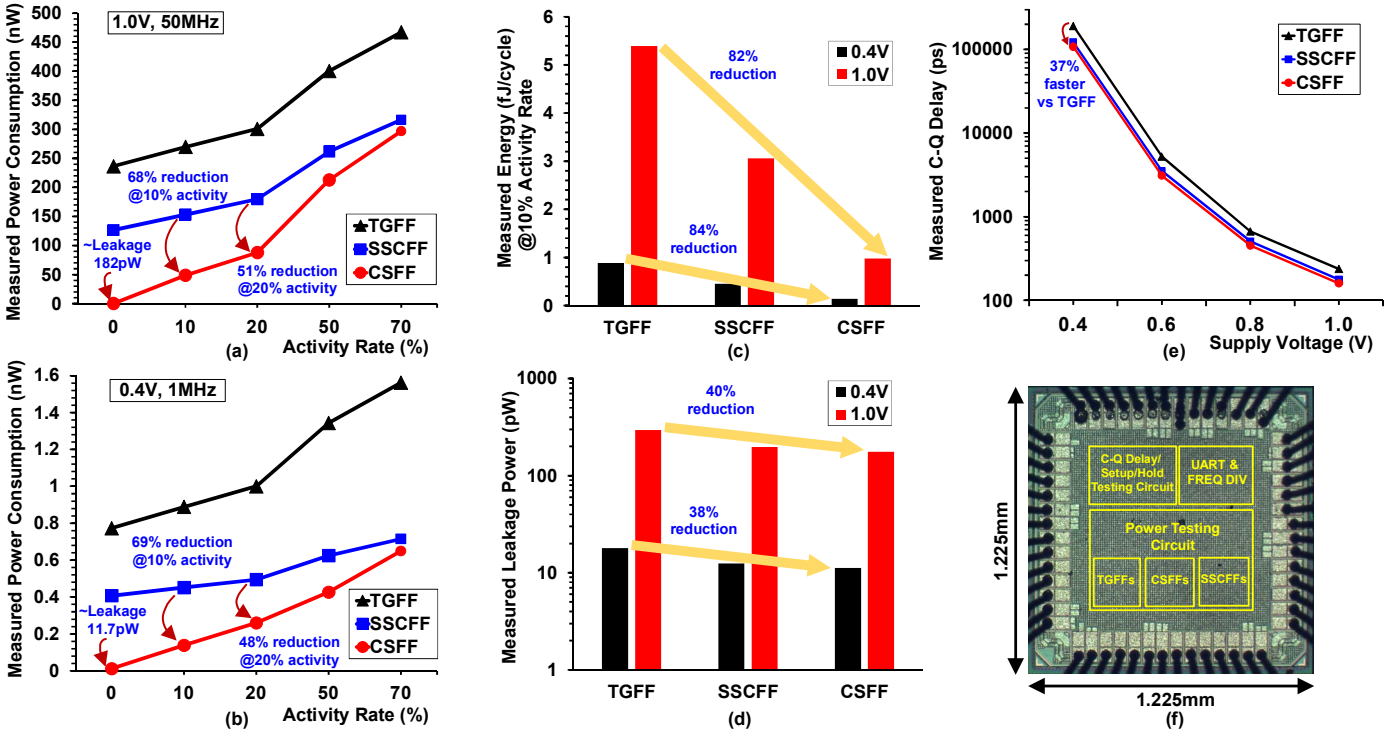

Fig. 10. (a) Measured power at 1.0V, (b) Measured power at 0.4V, (c) Measured energy, (d) Measured leakage, (e) Measured C-Q delay, (f) Die micrograph.

TABLE II. MEASUREMENT COMPARISON OF THE FLIP-FLOPS

	CSFF (This work)	**SSCFF** Y. Kim, ISSCC 2014	**TGFF** Conventional Flip-Flop
Number of Transistors	24	24	24
Normalized Layout Size	1.03	1.03	1.00
Redundant Transitions of Internal Clocked Nodes	**NO**	YES	YES
Measured Total Power @1.0V, 50MHz, 10% Activity	**48.8nW**	153nW	270nW
Measured Leakage @1.0V	**176pW**	197pW	295pW
Measured C-Q delay @1.0V	**160ps**	177ps	238ps
Measured Setup Time @1.0V	266.5ps	271.5ps	195ps
Measured Hold Time @1.0V	**-63ps**	-54ps	-18ps

and with only a 3% layout size increase vs. TGFF that corresponds to a one-minimum-poly-pitch increase in 40nm technology, CSFF eliminates redundant transitions of internal nodes, which always occurs in TGFF, and happens in SSCFF when the flip-flop data continuously stay at the logic '*low*' level. Therefore, CSFF achieves 82% and 68% power improvement over TGFF and SSCFF, respectively, at 1.0V and 10% activity rate. In terms of performance, CSFF exhibits 5% and 1.5% improvement in total setup time and C-Q delay, compared SSCFF and TGFF, respectively. CSFF also provides a better hold time compared to TGFF and SSCFF, requiring a lesser constraint for hold buffers in ICs. Measurement results also show that CSFF is functionally operational down to 0.19V.

V. CONCLUSION

In this paper, we introduced a novel change-sensing flip-flop (CSFF) for ultra-low power applications. The proposed CSFF eliminates redundant transitions of its clocked node without additional transistors when there is no change in the flip-flop content. The test chip fabricated in 40nm technology demonstrates that CSFF achieves more energy-efficient operations than TGFF and SSCFF across a wide operating voltage range (≥0.19V). CSFF shows the energy reduction of 82% and 68% at 1.0V and 10% activity rate, and the C-Q delay improvement of 37% and 11% in the supply voltage range of 0.4V to 1.0V compared to TGFF and SSCFF, respectively. Therefore, CSFF can directly replace many of the flip-flops in ultra-low power applications especially when the input data have relatively low activity rates.

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