A 0.4-V, 0.138-fJ/Cycle Single-Phase-Clocking Redundant-Transition-Free 24T Flip-Flop With Change-Sensing Scheme in 40-nm CMOS

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***Abstract*— This paper presents an extremely low-voltage and low-power single-phase-clocking redundant-transition-free flip-flop (FF), named change-sensing FF (CSFF). By utilizing a local change-sensing scheme for eliminating redundant transitions of internal clocked nodes, CSFF does not consume any dynamic power when there is no data activity. Measurement results from a test chip fabricated in 40-nm CMOS technology show that CSFF saves up to 90% power dissipation at 5% data activity without additional transistors compared to the conventional transmission-gate FF (TGFF). CSFF consumes only 0.138 fJ/cycle, which is 84% lower than that of TGFF, at 0.4 V and 10% activity. In addition to the significant improvement in power and energy efficiencies, CSFF also enhances performance and minimum operating voltage. The test chip measurement demonstrates successful operations of CSFF down to 0.19 V and the delay improvement of 37% compared to TGFF in the supply voltage range of 0.4–1 V.**

***Index Terms*— Flip-flop (FF), low power, low voltage, power measurement, setup and hold time measurement, single-phase clock.**

I. Introduction

THE relentless advancement of process technology has tremendously brought massive performance boosts and much more integration to modern digital circuits and systems. However, this comes at the cost of the increasingly high-power consumption. In addition, there have been increasingly on-going demands for portable hand-held devices and wireless sensor nodes. Nevertheless, their small form factors can accommodate only limited-sized batteries, necessitating low-power consumption. Thus, low power has become one of the most critical design constraints in integrated circuits (ICs) design. Flip-flops (FFs) are fundamental components in modern digital ICs; they dominate the total area and power of the overall systems [1]. FFs typically consume large dynamic power in systems on chips (SoCs) due to redundant transitions of their large number of internal clocked nodes even when FF input data do not change.

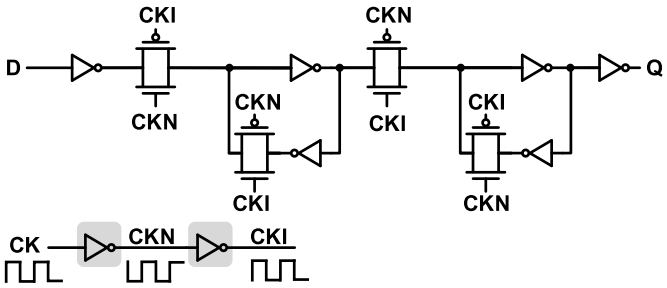

Fig. 1. Conventional TGFF.

The transmission-gate FF (TGFF) is the most popular FF since it is static, contention free, and robust with voltage scaling, but it consumes excessive power caused by internal clocked nodes CKN and CKI that always toggle as shown in Fig. 1. This toggling even occurs when there is no data activity. Several low-power FFs [2]–[7] have been recently proposed for reducing or eliminating the power penalty coming from the redundant transitions. However, they suffer from either large area penalty [2], [3], which is too costly since FFs typically occupy a significant amount of logic area in SoCs, or functional failures at low-voltage operations [4]–[6], which makes these FFs inapplicable for low-voltage applications. In this paper, we present a novel FF circuit that eliminates the redundant transitions of local clocked nodes for achieving extremely low-power consumption without extra transistors while further improving performance and minimum operating voltage. A part of this paper was presented in [8]. This paper presents more comprehensive descriptions and simulations of the previously reported FFs, our detailed design approach and principles of the proposed change-sensing FF (CSFF) with additional simulation and measurement results. The rest of this paper consists of the following. Section II discusses the major drawbacks of the recently introduced FFs. In Section III, we describe our design approach. Section IV presents the proposed CSFF with a change-sensing scheme and extensive simulation results, followed by the test circuit implementation in Section V. Measurement results are explained in Section VI, and Section VII provides the conclusion.

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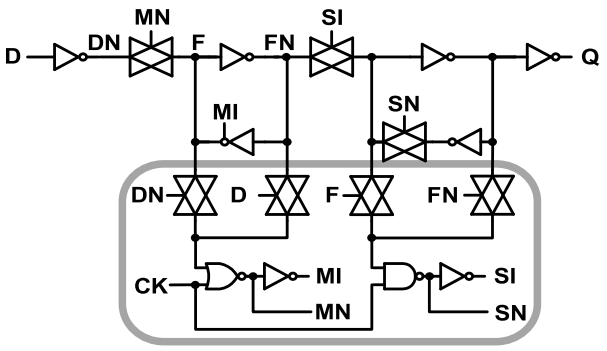


Fig. 2. CCKFF [2].

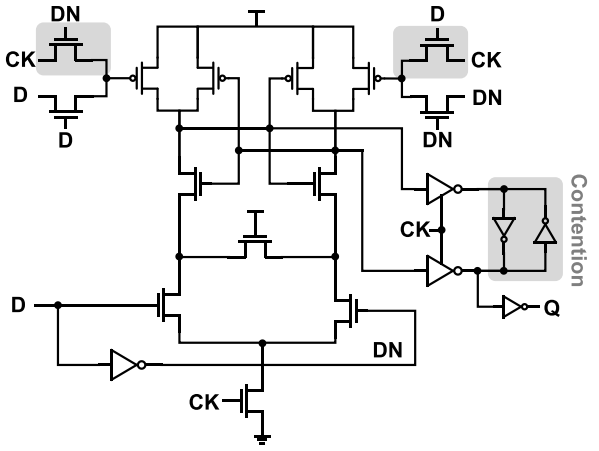


Fig. 3. CPFF [3].

II. State-of-the-Art Low-Power FFs

In this section, we discuss the limitations of the recently introduced low-power FFs [2]–[7] in comparison to the conventional TGFF as shown in Fig. 1.

Fig. 2 describes the schematic of the conditional-clocking FF (CCKFF) in [2]. By adding logic circuits for monitoring the change in the input data, CCKFF entirely avoids redundant transitions of local nodes when no data change is detected. However, it comes at the expense of large C-Q delay and area overhead due to the almost doubled transistor count compared to the regular TGFF.

The conditional pre-charged FF (CPFF) (Fig. 3) [3] also deploys a conditional pre-charge circuit for preventing the unnecessary toggling of internal nodes. Nevertheless, the use of clocked pass gates still causes unwanted transitions at node CL during the "low" phase of the input data and at node CR when the input data are consistently held "high," resulting in high dynamic power. It also induces area penalty and larger delay. In addition, the strong contention at the output latch leads to functional failures at low-voltage operations.

Fig. 4 shows the schematic of the data-mapping FF (DMFF) [4]. DMFF reduces the power dissipation caused by undesired transitions, but it still has a local clock inverter for generating an internal clock CM. This internal clock causes substantial switching power even at low data activity. In addition, the contention in the output latch requires additional

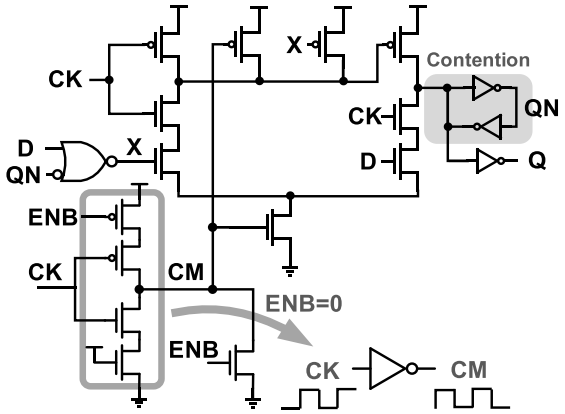


Fig. 4. DMFF [4].

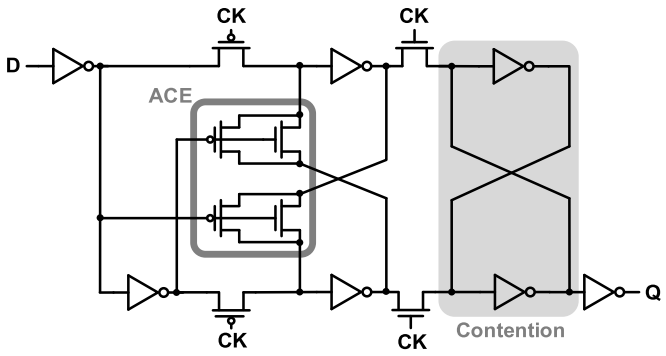


Fig. 5. ACFF [5].

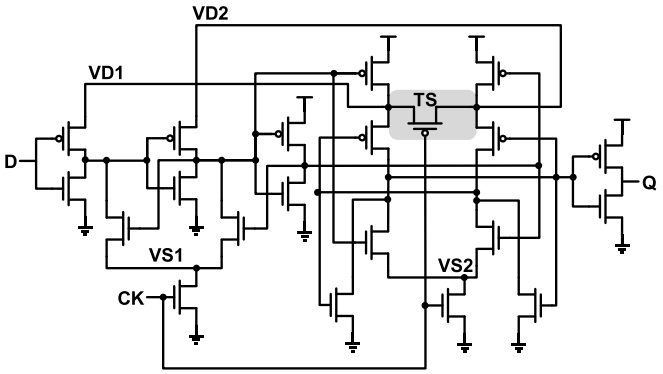


Fig. 6. TCFF [6].

transistors in its transistor stack for reducing contentions and avoiding functional failures at low-voltage operations.

The adaptive-coupling FF (ACFF) [5] could prevent redundant transitions without area penalty by only employing the adaptive-coupling element (ACE) in the master latch and removing the ACE in the slave latch as depicted in Fig. 5. However, this requires higher operating voltages ($\geq$0.75 V) due to the strong contention in the slave latch.

The topologically compressed FF (TCFF) [6] as illustrated in Fig. 6 removes the unwanted toggling of local clocked nodes without large area overhead by topologically compressing the structure of a combinational type FF. However, it leads to

TABLE I
SHORTCOMINGS OF STATE-OF-THE-ART LOW-POWER FFS

	TGFF Conventional	CCKFF [2] CICC, 2005	CPFF [3] ISSCC, 2006	DMFF [4] ISSCC, 2008	ACFF [5] ISSCC, 2011	TCFF [6] JSSC, 2014	SSCFF [7] ISSCC, 2014
Transistor Count	24	**40**	**28**	24 [a]	22 [b]	21	24
Low-Voltage Operations	YES	YES	**NO**	**NO**	**NO**	**NO**	YES
Redundant-Transition-Free	**NO**	YES	**NO**	**NO**	YES	YES	**NO**

[a]Additional transistors required for low-voltage operations, depending on process.
[b]Becomes 26 if ACE is employed in the slave latch for low-voltage operations.

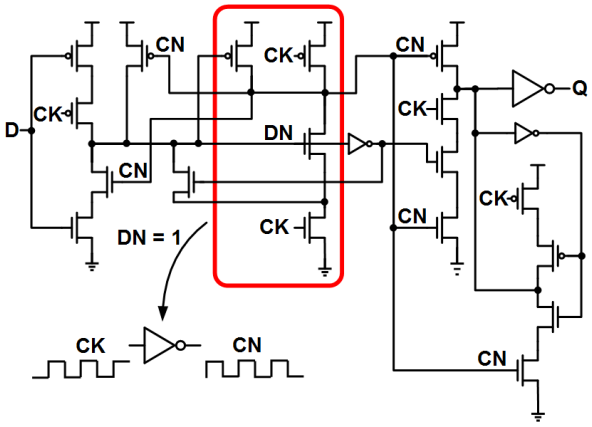


Fig. 7. SSCFF [7].

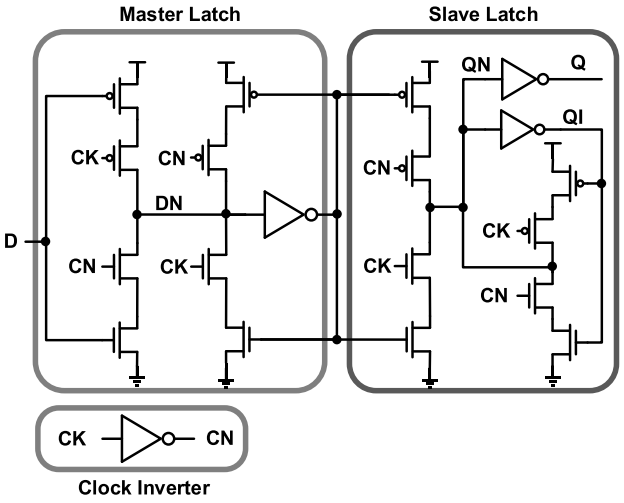


Fig. 8. Conventional master–slave FF using stacking transistors instead of transmission gates.

a large number of shared transistors, degrading the cell's robustness and causing functional failures at low-voltage operations (<0.6 V). For example, the shared transistor TS as highlighted in Fig. 6 causes reduced swing at VD1 and VD2 in the master latch at low-voltage operations. This results in contentions between NMOS and PMOS networks in the master latch, inducing operational failures at low-voltage regimes.

The static single-phase contention-free FF (SSCFF) in [7] provides robust energy-saving operations over a wide range of supply voltages with the same transistor count as TGFF. However, SSCFF only eliminates unnecessary transitions when input data persistently stay "high." Indeed, SSCFF still suffers from power penalty due to the undesired toggling of the internal clocked node CN when the input D does not change its state from the logic "low" level as illustrated in Fig. 7.

Table I summarizes the major shortcomings of the aforementioned state-of-the-art low-power FFs. Note that no FF can address power penalty, area overhead, and functional failures at low-voltage operations at the same time, which is the main goal of this paper.

III. DESIGN APPROACH

With the motivation of reducing power consumption while maintaining the similar cell area, comparable performance, and functionality at low-voltage operations, it is important to eliminate the unnecessary transitions of internal clocked nodes while keeping the same device count without any strong contention in the FF. As discussed in Section I, the mainstream TGFF consumes large dynamic power due to the redundant transitions of the always-toggling nodes CKI and CKN, generated by two local clock inverters. To remove one clock inverter and reduce the number of internal clocked nodes, we started with the conventional master–slave FF, but using stacking transistors instead of transmission gates as illustrated in Fig. 8. This also allows us to reduce the transistor count later by merging logically equivalent transistors. To eliminate the unwanted toggling of the internal clocked node CN caused by the remaining clock inverter while keeping the same transistor count, we developed the proposed FF through the following steps. First, we propose a change-sensing scheme, as shown in Fig. 9, which detects the change in the FF data and toggles the local clocked node CS for storing new data only if the input data change its state. The proposed change-sensing scheme comprises six transistors and prevents the clocked node CS from toggling if there is no data activity. This redundant-transition-free feature significantly reduces the dynamic power of the FF. However, this still requires four additional transistors. Thus, we investigated the functionality of each device and found several functionally equivalent devices that can be merged. After applying the above steps, we developed an FF circuit as shown in Fig. 10 that senses the change in the FF data and eliminates the redundant transitions of internal nodes with the same device count as the typical TGFF.

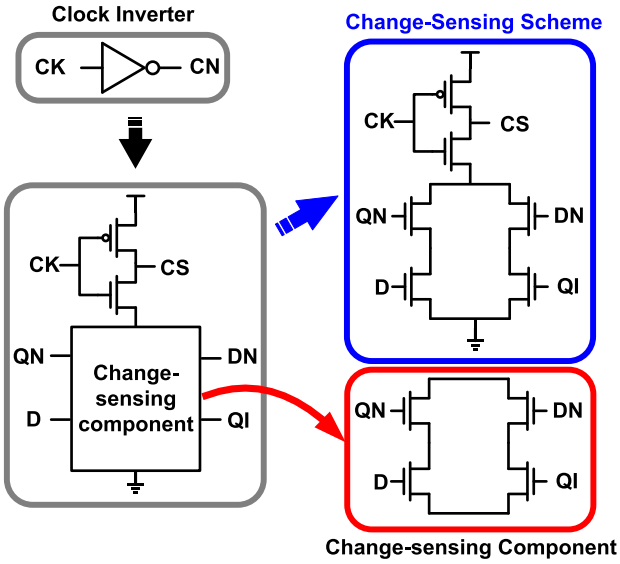


Fig. 9. Change-sensing scheme for eliminating the redundant toggling of the local clocked node CS.

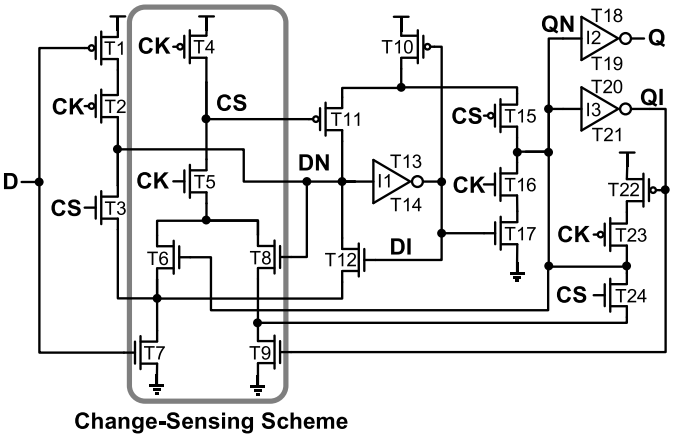


Fig. 10. Schematic of the proposed CSFF with the change-sensing scheme for eliminating unnecessary transitions.

The detailed operation of the proposed FF is explained in Section IV-B.

IV. Proposed Change-Sensing Flip-Flop

A. Proposed Change-Sensing Scheme

This section explains the principle of the proposed change-sensing scheme for eliminating the unnecessary transitions of internal nodes. Fig. 10 describes the schematic of the proposed CSFF including a master latch, the change-sensing scheme, and a slave latch. The master latch consists of T1, T2, T3, and its latch (T7, T10, T11, T12, and I1), and the slave latch is composed of T10, T15, T16, T17, I2, and its latch (T9, T22, T23, T24, and I3). The change-sensing scheme (T4, T5, T6, T7, T8, and T9) as highlighted in Fig. 10 detects the change in the FF data for preventing the redundant transitions of the internal clocked node CS.

Fig. 11 illustrates the operation details of the change-sensing scheme. When the clock signal CK is at the logic "low" level,

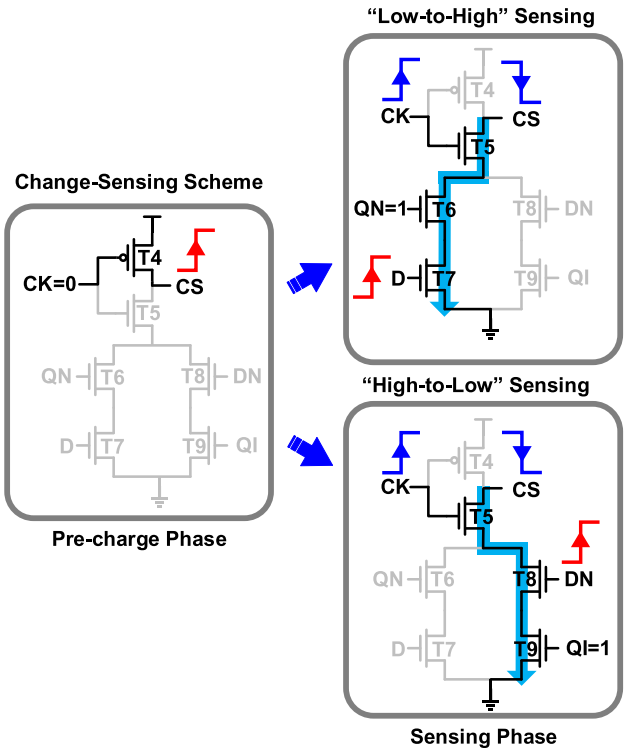


Fig. 11. Operation details of the change-sensing scheme for detecting the change in the FF data. The sensing phase occurs at the rising edge of the clock. The change-sensing scheme toggles the clocked node CS for storing the new data only when the input D changes its state. Otherwise, the local node CS is always kept "high" by T4 in every clock cycle.

the change-sensing configuration is in the pre-charge phase, and the local clocked node CS is pre-charged through T4. At the rising edge of the clock, the change-sensing scheme switches to the sensing phase. When the input D changes from the logic "low-to-high" level, CS is discharged through the "low-to-high-sensing" path (T5, T6, and T7). On the other hand, the data change from "high- to-low" discharges CS through the "high-to-low-sensing" path (T5, T8, and T9). Otherwise, the internal node CS is always held "high" by T4 in every clock cycle. With the aid of the local change-sensing scheme, the clocked node CS is only toggled when the input D changes its state. When the applied input data are continuously the same as the previous data stored in the slave latch, no redundant transitions occur. Therefore, the proposed CSFF completely removes the unnecessary toggling, which always happens in the mainstream TGFF.

Fig. 12 illustrates the transitions of the local clocked nodes in the typical TGFF, DMFF, CPFF, SSCFF, CCKFF, and the proposed CSFF. TGFF and DMFF always show the unnecessary toggling of their internal nodes due to the clock inverters as illustrated in Figs. 1 and 4, respectively, whereas CPFF exhibits redundant transitions at the local nodes CL and CR due to the clocked pass gates as highlighted in Fig. 3. Undesired toggling also happens in SSCFF at the clocked node CN when the input D persistently stays at the logic "low" level as illustrated in Fig. 7. The proposed CSFF and CCKFF eliminate redundant toggling of their local clocked nodes when input data do not change regardless of the input

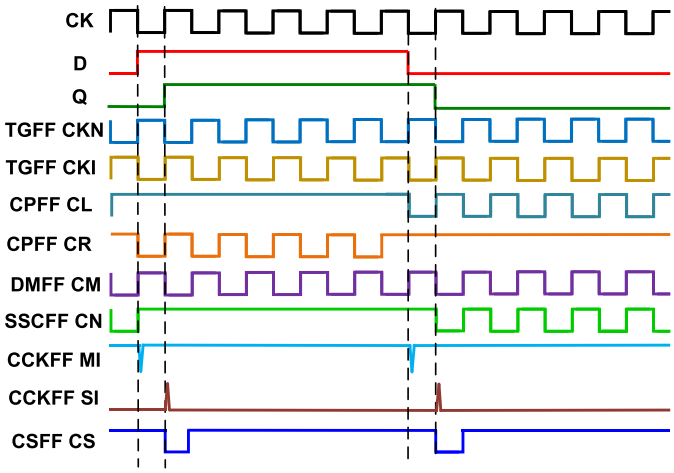


Fig. 12. Transitions of the local clocked nodes in TGFF, CPFF, DMFF, SSCFF, CCKFF, and the proposed CSFF. TGFF and DMFF always show redundant transitions due to the internal clock inverters, whereas CPFF exhibits the unnecessary toggling of the internal nodes CL and CR because of the clocked pass gates. Unwanted transitions of the internal node CN in SSCFF occur during the "low" phase of the input D. CCKFF and CSFF only toggle their local nodes when the input D changes its level, whereas ACFF and TCFF remove internal clocked nodes.

data level, whereas ACFF and TCFF remove internal clocked nodes.

B. Proposed CSFF Operation

Fig. 13 illustrates the detailed operation of the proposed CSFF. When CK is "low," the local clocked node CS pre-charges through T4. The master latch is in the transparent mode to pass the new data to the FF, whereas the slave latch is in the hold mode to keep the previous data. When CK goes "high," the change-sensing scheme switches to the sensing phase. It discharges the internal node CS when the change in the input data is detected. CS is discharged through the "high-to-low-sensing" path when the new data are "low," whereas the new "high" data discharge CS through the "low-to-high-sensing" path. Then, the discharged CS turns the master latch to the hold mode to keep the new data, whereas the slave latch is switched to the transparent mode to pass the updated data to the output. If the updated level is "low," QN is held "high" by T10 and T15; thus, the output Q goes "low." In the case that the stored data are "high," QN is kept "low" by T16 and T17; then, the output Q goes "high."

C. Discussions on Floating Nodes and Race Condition

1) Floating Nodes: The redundant-transition-free feature of the proposed CSFF has three conditional floating nodes including CS, DN, and QN. However, they are not affecting the functionality of the proposed CSFF. The detailed explanations are given as follows.

CS is floating "high" when there is no change in the input data, and CK is "high." However, the degradation of node CS's voltage during the floating condition does not affect the functionality of the CSFF. In the worst case, if the CS voltage is degraded to "low," the master latch is turned to the hold mode, and the slave latch is switched to the transparent mode; then, the same data are passed to the output, which is identical to the normal FF operation.

DN and QN are floating "high" when CK is "high," and the input D does not change its state from the logic "low" level. However, with the aid of the change-sensing scheme with the optimized sizing achieved through extensive simulations, the changes in DN and QN during their floating conditions leading to the corresponding changes of DI and QI are detected. CS is discharged through the change-sensing paths; then, DN and QN are held "high" by T11 and T15, respectively. To speed up the restoring of these nodes, the sizes of the NMOS transistors on the change-sensing paths are increased for shortening the discharging time of CS. In addition, the PMOS transistors including T11, T10, and T15 are also up-sized for quickly recovering the high level of DN and QN once CS is triggered. More importantly, T10 and T15 are strengthened to overpower T9 and T24 for preventing their fighting during the restoring of the QN.

2) Race Condition: A race condition happens when the input D changes from "low" to "high" during the high CK and low data (e.g., DN $=$ 1). However, the change-sensing scheme detects the change in D and discharges CS to hold DN and QN for preventing the wrong Q as follows. During DN $=$ 1, the high CK and QN turn T5 and T6 on, whereas the low DI keeps T10 on. When D changes from "low" to "high," the change in D is detected by the change-sensing scheme through T7; then, CS is discharged through T5, T6, and T7. The discharged CS holds DN and QN through T11 and T15, respectively. Thus, QI is kept low, and the wrong Q is prevented.

Fig. 14 shows the simulated minimum operating voltages of the proposed CSFF and the other FFs at different process corners when sweeping the voltage supply from 0 to 1 V with a step size of 0.01 V. With the aid of the change-sensing scheme, CSFF achieves fully functional operations in the voltage range of 0.3–1 V. With the contention-free and fully static operations, CCKFF, TGFF, and SSCFF are also fully functional at low-voltage operations. ACFF, DMFF, TCFF, and CPFF require higher operating voltages due to their strong contentions at low-voltage regimes.

D. Simulation Analysis and Comparison

The recently introduced low-power FFs in [2]–[7], the mainstream TGFF, and the proposed CSFF are implemented and simulated in 40-nm CMOS for fair comparisons.

Fig. 15 shows the simulated power waveforms of the proposed CSFF and the other FFs at 1 V and 100 MHz. CSFF, CCKFF, TCFF, and ACFF only consume dynamic power when the input D changes. The power waveforms of the other FFs correspondingly reflect the redundant transitions of their internal nodes when there are no changes in the input data D as illustrated in Fig. 12. TGFF and DMFF show dynamic power in every clock cycle due to the local clock inverters. CPFF also exhibits switching power corresponding to the clock toggling because of the clocked pass gates, whereas SSCFF consumes dynamic power whenever the clock toggles during the "low" phase of the input data.

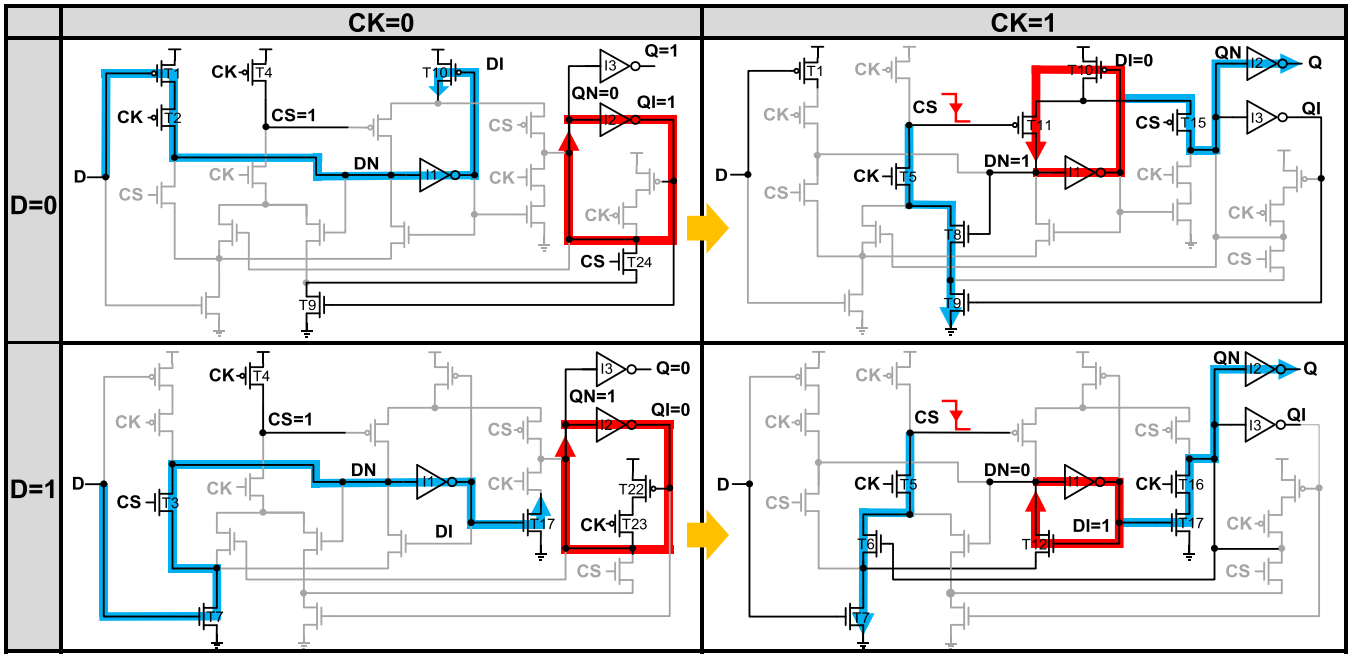
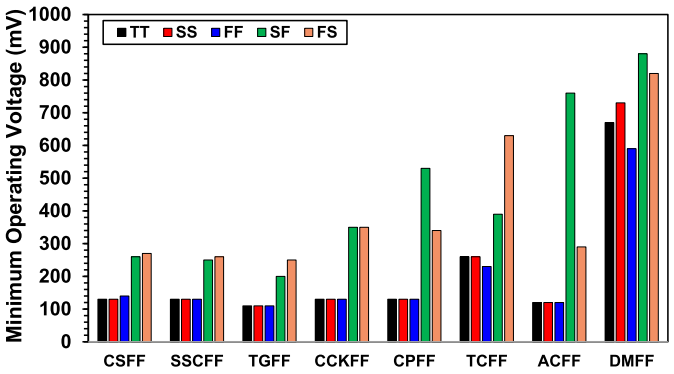


Fig. 13. Operation of CSFF. When CK is "low," CS pre-charges through T4. The master latch passes the new data to the FF, whereas the slave latch keeps the previous data. When CK goes "high," the change-sensing scheme detects the change in the FF data. CS is discharged through the "low-to-high-sensing" path (T5, T6, and T7) if the new data are "high," whereas the new "low" data discharge CS through the "high-to-low-sensing" path (T5, T8, and T9). Then, the master latch holds the updated data, and the slave latch passes the data to the output.



Process: 40nm CMOS
Corners: TT, SS, FF, SF, and FS

Temperature: 27°C
Sweeping Step Size: 10mV

Fig. 14. Simulated minimum operating voltages of the proposed CSFF and the other FFs at different process corners when sweeping the voltage supply from 0 to 1 V. CSFF, CCKFF, TGFF, and SSCFF are fully functional at low-voltage operations. DMFF, TCFF, ACFF, and CPFF require higher operating voltages at FS and SF corners due to their strong contentions at low-voltage regimes.

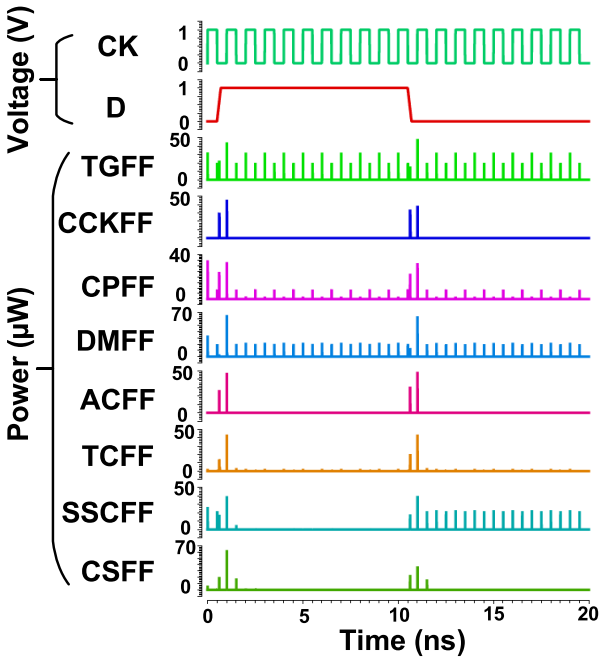
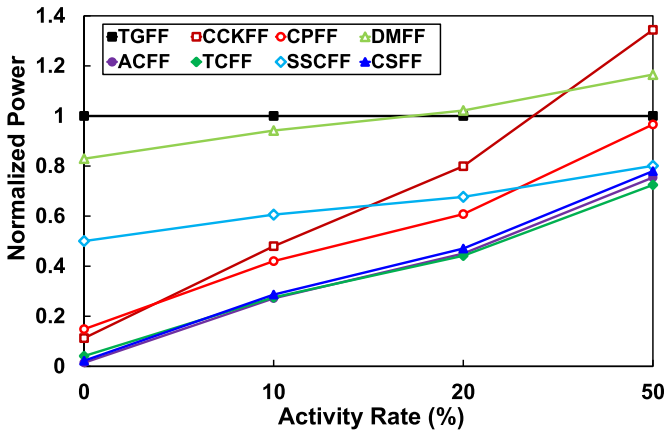


Fig. 15. Simulated power waveforms of the proposed CSFF and the other FFs at 1 V and 100 MHz. CSFF, CCKFF, TCFF, and ACFF only consume dynamic power when the input D changes. The power waveforms of the other FFs correspondingly reflect their redundant transitions as illustrated in Fig. 12.

Fig. 16 demonstrates the simulated normalized power of CSFF and the previously reported low-power FFs compared to the conventional TGFF at different activity rates. CSFF, ACFF, and TCFF exhibit the lowest power consumptions among all of the simulated FFs because of their redundant-transition-free characteristics. CCKFF also eliminates unwanted transitions, but the almost double transistor count and a large number of local clocked nodes (e.g., MI, MN, SI, and SN) result in higher power consumption, especially when data activities increase. TGFF, DMFF, CPFF, and SSCFF consume more significant power due to the unnecessary toggling of their local clocked nodes as illustrated in Fig. 12.

Fig. 17 shows the simulated C-Q delays of CSFF and the other FFs when sweeping the supply voltage from 0.4 to 1 V. The proposed CSFF, ACFF, and TCFF show smaller C-Q delays with lowest power consumptions, but TCFF and



Process: 40nm CMOS Temperature: 27°C
Condition: Typical Supply Voltage: 1.0V
Normalized Power: Each FF's power normalized by TGFF's

Fig. 16. Simulated normalized power of CSFF and the recently proposed low-power FFs compared to the typical TGFF. CSFF, TCFF, and ACFF obtain the lowest power dissipations because of their redundant-transition-free feature. CCKFF also eliminates unwanted transitions, but the almost double transistor count and a large number of local clocked nodes (e.g., MI, MN, SI, and SN) result in higher power consumption, especially when data activities increase.

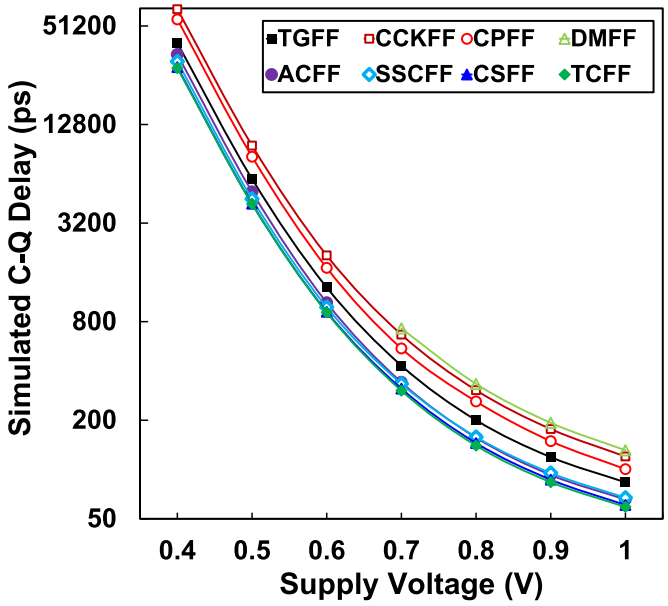


Fig. 17. Simulated C-Q delays of CSFF and the other FFs when sweeping the supply voltage from 0.4 to 1 V. The proposed CSFF, ACFF, and TCFF show smaller C-Q delays with lowest power consumptions, but TCFF and ACFF fail to operate at low-voltage supplies at skewed corners (FS and SF).

ACFF fail to operate at low-voltage supplies at skewed corners (FS and SF) as simulated in Fig. 14. In fact, the 40-nm CMOS chip measurements in [5] and [6] demonstrate that TCFF and ACFF show the minimum operating voltages of 0.6 and 0.75 V, respectively, making them inapplicable for ultra-low-power applications where voltage scaling is required.

Table II illustrates the simulated setup/hold time of CSFF and other low-power FFs at 1 V. The transistor-stacking structure of CSFF requires more setup time compared to the conventional TGFF. Compared to CCKFF, TCFF, ACFF,

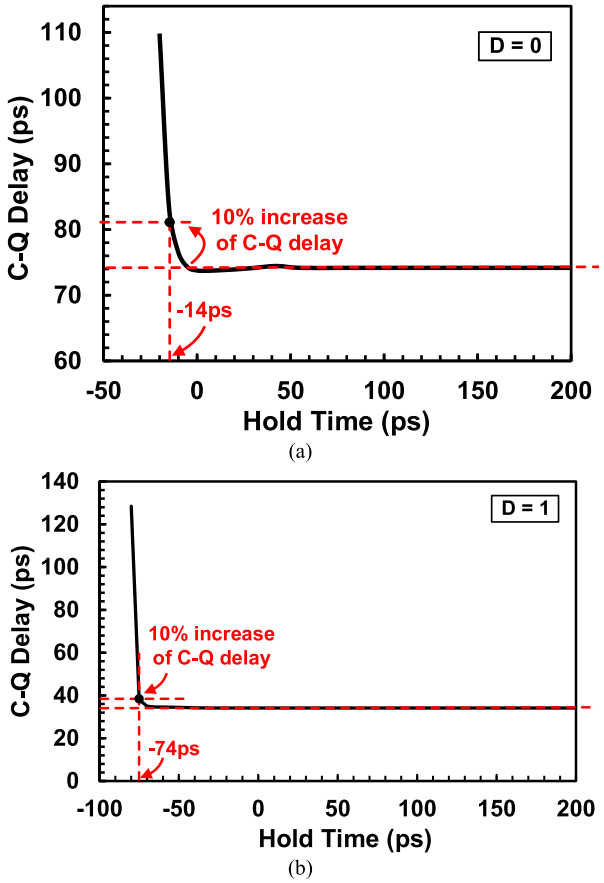


Fig. 18. Simulated hold time when input data are (a) "low" and (b) "high" at $V_{DD} = 1$ V. CSFF obtains negative hold time in both cases of the input data. The worst case hold time of CSFF is when D changes from "low" to "high" just after the CK rising edge, resulting in less negative hold time than the other case.

and SSCFF, the proposed CSFF shows smaller setup time. However, CPFF and DMFF necessitate less setup time than CSFF. In terms of hold time as simulated in Fig. 18, the worst case hold time of CSFF is when D changes from "low" to "high" just after the CK rising edge. The high CK must discharge CS fast enough to turn off T3 before the high D can change the master's stored data; otherwise, hold time failure may occur. The optimized sizing for the change-sensing scheme of CSFF achieved through extensive simulations results in negative hold time in the worst case hold time scenario. TGFF shows lesser negative hold time than CSFF due to the use of the two clock inverters as highlighted in Fig. 1 in hold time paths. Compared to CPFF, DMFF, CCKFF, and SSCFF, CSFF also has more negative hold time, whereas TCFF and ACFF achieve better hold time than CSFF.

Table II illustrates the total powers of the FFs when including external clock driving powers. With the smaller numbers of total clock-related transistors and the redundant-transition-free features, CSFF, TCFF, and ACFF obtain lowest total power consumptions while CCKFF shows higher power due to the almost double device count and a large number of local clock nodes (e.g., MI, MN, SI, and SN). Table II also summarizes the simulation comparisons of the proposed CSFF and the other FFs. CSFF is the only FF among all of the compared FFs

TABLE II
SIMULATION COMPARISONS OF THE CSFF AND THE OTHER FFS

	Device Count	C-Q Delay (ps)	Setup Time (ps)	Hold Time (ps)	Total Power (10% activity)
TGFF	24	83.5	79.5	-17.5	1.000
CCKFF	40	120.0	194.7	-26.9	0.646
CPFF	28	101.0	84.4	29.8	0.528
DMFF	28 [a]	131.2	53.9	17.0	1.265
ACFF	22	65.6	172.5	-57.3	0.362
TCFF	21	59.1	243.2	-90.1	0.394
SSCFF	24	67.2	125.5	-34.3	0.667
CSFF	24	60.7	123.0	-44.0	0.407

Process: 40nm CMOS Temperature: 27ºC
Condition: Typical Supply Voltage: 1.0V
C-Q Delay: Average CK-to-Q delay of low and high input D
Setup and Hold Time: average setup/hold time of low and high input D, defined at 10% increase of C-Q delay from stable value
Total Power: Total power including FF's power and its external clock driving power, normalized by TGFF's
[a]Four transistors are added to the transistor stack of the output latch for reducing contentions

with the lowest power consumption and the smallest delay with fully functional operations at low-voltage regimes and the same transistor count as the regular TGFF.

V. TEST CIRCUIT IMPLEMENTATION

For comparison, we implemented CSFF, TGFF, and SSCFF in a 40-nm CMOS test chip. DMFF, ACFF, and TCFF were not implemented due to their limitations at low-voltage operations. CCKFF and CPFF were also not included because of their large area overhead and delay. The following are the test circuits for measuring power consumptions (Fig. 19) and timing performance (Fig. 20) of the implemented FFs.

A. Test Circuit for Measuring Power Consumptions

Fig. 19 shows the test circuit for measuring power consumptions of the implemented FFs at different activity ratios. The power consumptions of 512 units of each FF are measured at various activity rates, and the average powers are obtained. The activity ratios are set by the activity rate control unit as highlighted in Fig. 19. When INIT is "low," the activity rate is initialized by the 20-bit input ID (ID [19:0]). When INIT goes "high," the activity rate set by ID [19:0] is applied, and the total power consumption of the FFs is measured. It is noted that the external clock driving power is not included in the power measurement of the FFs.

B. Test Circuit for Measuring Delay/Setup/Hold Time

Fig. 20 illustrates the test circuit for measuring delay, setup, and hold time, which is based on the structure in [9]. It includes three main modules: test-bench circuit (TBC), digital-to-time skew circuit (DTC), and self-calibration circuit (SCC). TBC mainly consists of FFs and necessary buffers

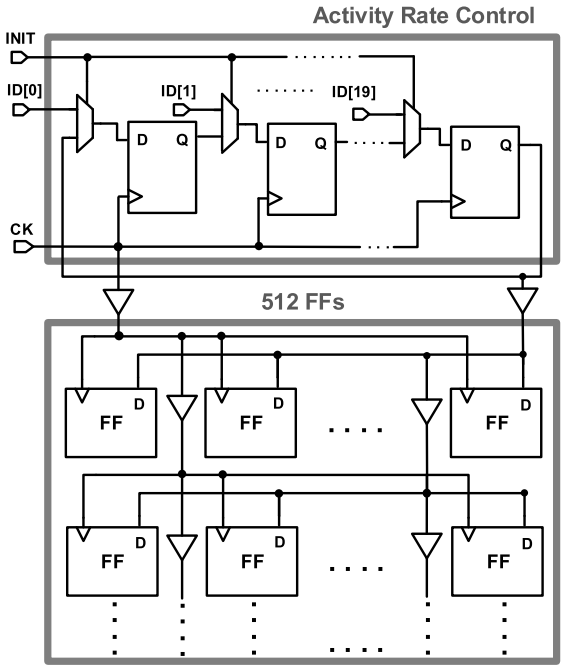


Fig. 19. Test circuit for power measurements at different data activity ratios. The activity ratios are set by the activity rate control unit.

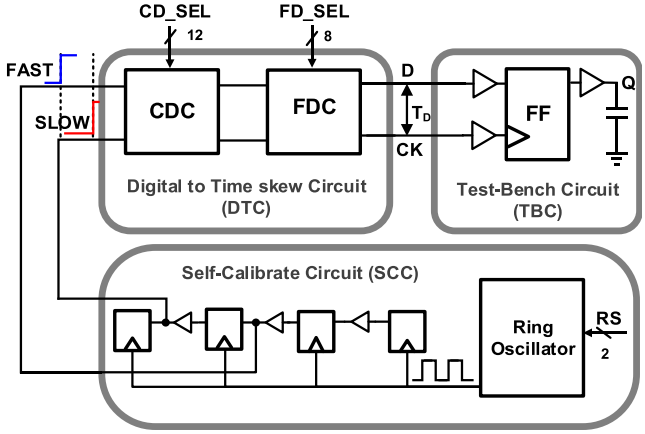


Fig. 20. Test circuit for measuring C-Q delay, setup, and hold time.

for measuring C-Q delay, whereas DTC includes coarse delay control (CDC) and fine delay control (FDC) blocks for generating digitally controlled delay skew T_D between the input data D and the input clock CK. For controlling T_D with a larger step T_C, the 12-bit input CD_SEL in CDC is adjusted to change the number of the coarse delay units in the data path and the clock path. For T_D control with a smaller step T_F, the 8-bit input FD_SEL in FDC is used. In addition, SCC comprising an FF chain and a ring oscillator creates digitally controlled delays between FAST and SLOW signals using the 2-bit input RS for measuring the coarse delay T_C and the fine delay T_F.

Once T_C and T_F are known, the setup/hold time of the FFs could be accurately estimated by adjusting the time delay T_D between the clock and the data signals to the setup/hold time pass/fail point as illustrated in Fig. 21. To measure setup time, we adjust the delay skew T_D between the

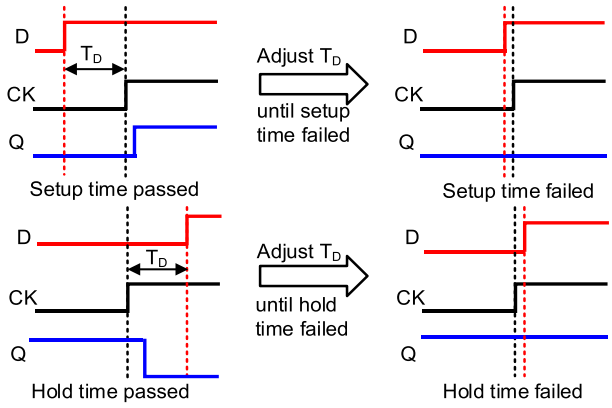


Fig. 21. Measuring setup/hold time by adjusting the time delay T_D between the clock and the data signals to the setup/hold time pass/fail point.

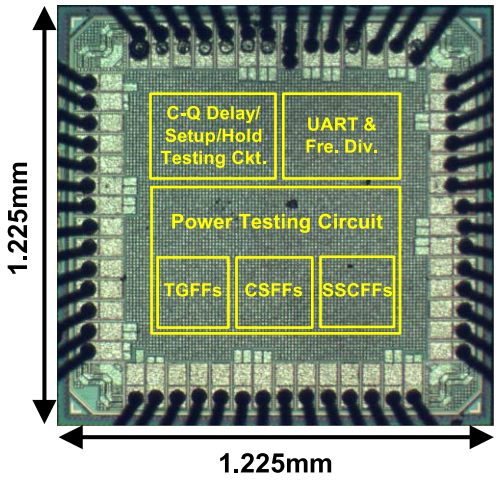


Fig. 22. Microphotograph of the test chip fabricated in the 40-nm CMOS technology. It includes testing circuits for measuring power, delay, and setup/hold time.

data and clock signals until the setup time is not enough to make the FF operational. Similarly, we control the delay T_D between the clock and data until the FF fails due to the hold time violation for measuring hold time.

VI. Measurement Results

Fig. 22 shows the microphotograph of the test chip fabricated in 40-nm CMOS technology. It includes the test circuits for measuring power consumptions, setup/hold time, and C-Q delay. Fig. 23 shows the cell layouts of the proposed CSFF, SSCFF, and conventional TGFF. The proposed CSFF has the same layout size as SSCFF and only 3% layout size increase versus TGFF, which corresponds to only a one-minimum-poly-pitch increase in the 40-nm CMOS technology.

Figs. 24 and 25 demonstrate the measured power consumptions of the FFs over different activity rates at 1 and 0.4 V, respectively. By utilizing the internal change-sensing scheme, CSFF almost consumes only leakage power at 0% activity rate, and it also provides more energy-efficient operations over SSCFF and TGFF, especially at low activity rates. The average activity rate of FFs in SoCs is typically from 5% to 15%; CSFF saves up to 84%–60% and 90%–77% power compared to SSCFF and TGFF, respectively, in this range. From the

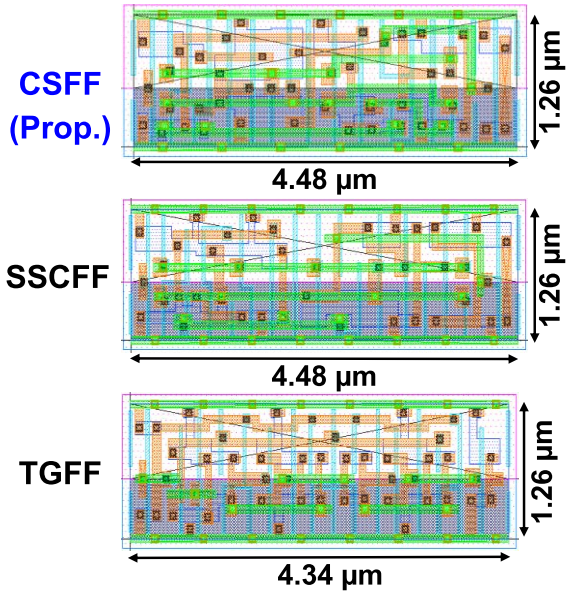


Fig. 23. Cell layouts of the implemented FFs. CSFF has the same layout size as SSCFF and only 3% layout size increase versus TGFF, which corresponds to only a one-minimum-poly-pitch increase in the 40-nm CMOS technology.

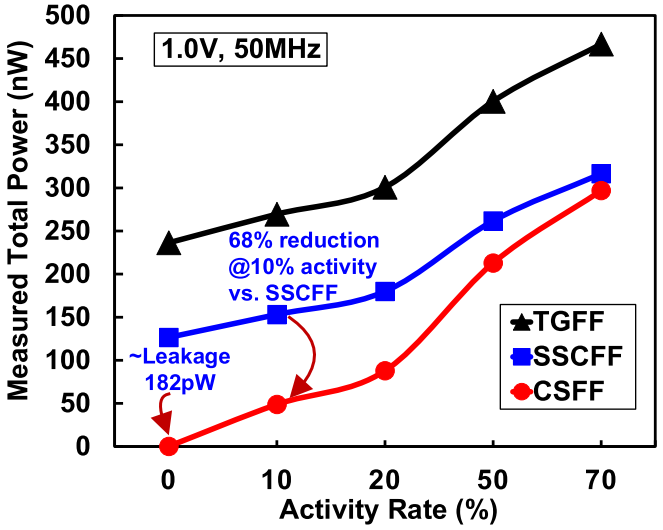


Fig. 24. Measured total power at V_{DD} = 1 V and f_{CK} = 50 MHz. CSFF almost consumes only leakage power when there is no data activity.

power measurement, at 10% activity rate, CSFF has 82% and 84% lower power consumption versus TGFF, at 1 and 0.4 V, respectively. When compared to SSCFF, CSFF exhibits the reduction of 68% and 69%. At 20% activity rate, CSFF shows 71% and 74% improvement in total power consumption versus TGFF, at 1 and 0.4 V, respectively. Compared to SSCFF, CSFF has 51% and 48% improvement. Fig. 26 also shows the measured total power of the FFs at 10% data activity when sweeping the supply voltage from 0.4 to 1 V. CSFF has consistently substantial power reductions of over 80% and 65% compared to TGFF and SSCFF, respectively, across the supply voltage range.

Regarding the energy consumption per cycle at 10% data activity, CSFF exhibits 82% and 84% reduction, compared to TGFF, and 68% and 69% improvement, compared to SSCFF, at 1 and 0.4 V, respectively, as shown in Fig. 27.

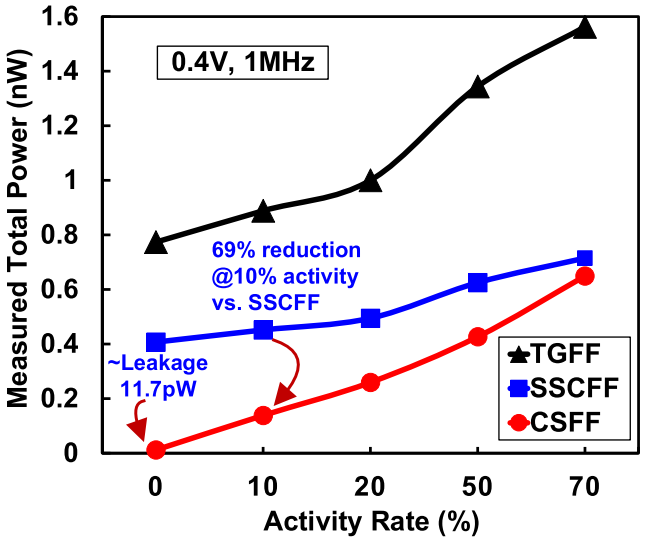


Fig. 25. Measured total power at $V_{DD} = 0.4$ V and $f_{CK} = 1$ MHz. CSFF achieves 84% and 69% reductions over TGFF and SSCFF, respectively, at 10% activity.

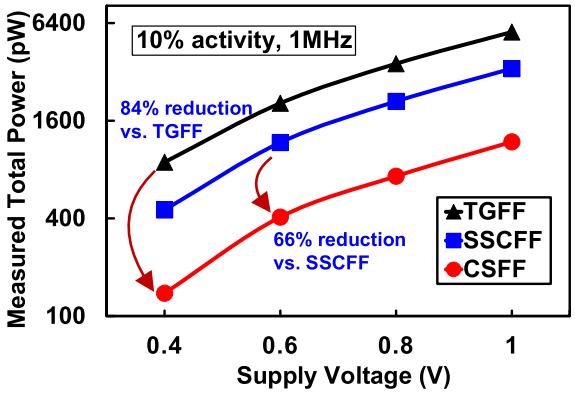


Fig. 26. Measured total power against the supply voltage at 10% activity. CSFF shows consistently significant power reductions of over 80% and 65% compared to TGFF and SSCFF, respectively, across the supply voltage range.

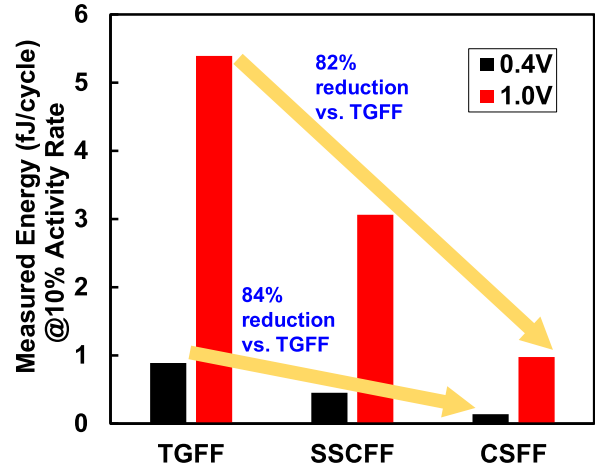


Fig. 27. Measured energy consumption per cycle at 1 and 0.4 V at 10% activity. CSFF consumes only 0.138 fJ/Cycle, which is 84% lower than that of TGFF, at 0.4 V and 10% activity.

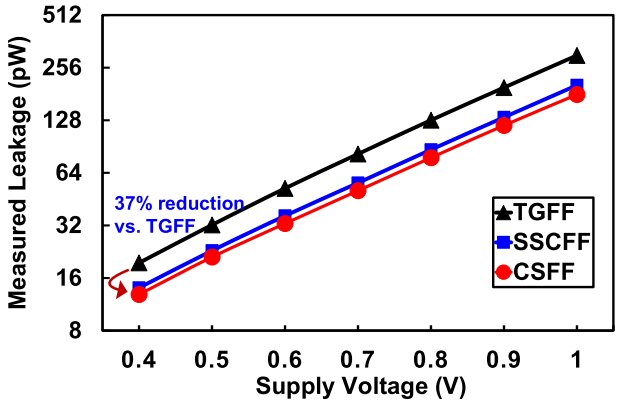


Fig. 28. Measured leakage power versus the supply voltage. CSFF has 37% and 10% leakage improvements over TGFF and SSCFF, respectively.

TABLE III
MEASUREMENT CONDITIONS FOR LEAKAGE POWER

CK	D	Leakage Power
0	0	P_1
0	1	P_2
1	0	P_3
1	1	P_4
Measured Leakage Power		$(P_1+ P_2+ P_3+ P_4)/4$

Temperature: 27°C Number of Samples: 10
Leakage Power: Average leakage power of 10 samples
Measured Leakage Power: Average measured leakage power at four different measurement conditions.

At 0.4 V, CSFF consumes only 0.138 fJ/Cycle. Fig. 28 shows the measured leakage power of the implemented FFs in the supply voltage range of 0.4–1 V with the measurement conditions shown in Table III. CSFF has 37% and 10% leakage improvements over TGFF and SSCFF, respectively, across the voltage range. This is because CSFF has more stacking transistors on leakage paths than TGFF and SSCFF. Fig. 29 shows the measured C-Q delays of the FFs against the supply voltage. CSFF exhibits 37% delay reduction over TGFF in the operating voltage range of 0.4–1 V. When compared to SSCFF, CSFF also provides a modest delay improvement of 11%.

Table IV summarizes the measurements results including the measured setup/hold time of the implemented FFs and shows the comparisons with the recently introduced low-power FFs. By utilizing the internal change-sensing scheme, CSFF completely removes unnecessary transitions of local clocked nodes without adding any extra transistor compared to the mainstream TGFF and SSCFF. This redundant-transition-free feature significantly reduces the dynamic power when there are no changes in the FF data. The test chip measurement in 40-nm CMOS shows that CSFF achieves 82% and 68% power reductions over TGFF and SSCFF, respectively, at 1 V and 10% data activity. In terms of performance, CSFF exhibits modest improvement of 5% and 1.5% in total setup time and C-Q delay, compared to SSCFF and TGFF, respectively. CSFF also provides better hold time, requiring a lesser constraint for hold buffers in ICs. In addition to the significant power reduction and modest performance improvement, CSFF also enhances minimum operating voltage.

TABLE IV
MEASUREMENT COMPARISONS OF THE CSFF AND THE RECENTLY PROPOSED LOW-POWER FFS

	CSFF (*This work*)	**SSCFF** ISSCC, 2014	**TGFF** Conventional FF	**CCKFF** [2] CICC, 2005	**CPFF** [3] ISSCC, 2006	**DMFF** [4] ISSCC, 2008	**ACFF** [5] ISSCC, 2011	**TCFF** [6] JSSC, 2014
Transistor Count	**24**	24	24	40	28	24 [a]	22 [a]	21 [b]
Single-Phase Clock	**YES**	YES	NO [c]	YES	YES	NO [c]	YES	YES
Redundant-Transition-Free	**YES**	NO [d]	NO [e]	YES	NO [f]	NO [e]	YES	YES
Low-Voltage Operations	**YES**	YES	YES	YES	NO [g]	NO [g]	NO [g]	NO [g]
Normalized Layout Size	**1.03**	1.03	1.00	[a]Additional transistors are required for low-voltage operations. [b]Fewer transistors, but it has the same layout size as TGFF. [c]Internal inverted clocks are used. [d]Redundant transitions occur when input data persistently stays at the logic '*low*' level. [e]Unnecessary toggling happens due to the local clock inverters. [f]Unwanted transitions exist due to the clocked pass gates. [g]Functional failures occur at low-voltage operations. [h]The measured power only includes internally consumed power and excludes clock driving power. CCKFF, CPFF, DMFF, ACFF, and TCFF were not implemented in this test chip.				
Measured Total Power (nW) [h] @1.0V, 50MHz, 10% Activity	**48.8**	153	270					
Measured Leakage (pW) @1.0V	**176**	197	295					
Measured C-Q delay (ps) @1.0V	**160**	177	238					
Measured Setup Time (ps) @1.0V	**266.5**	271.5	195					
Measured Hold Time (ps) @1.0V	**-63**	-54	-18					

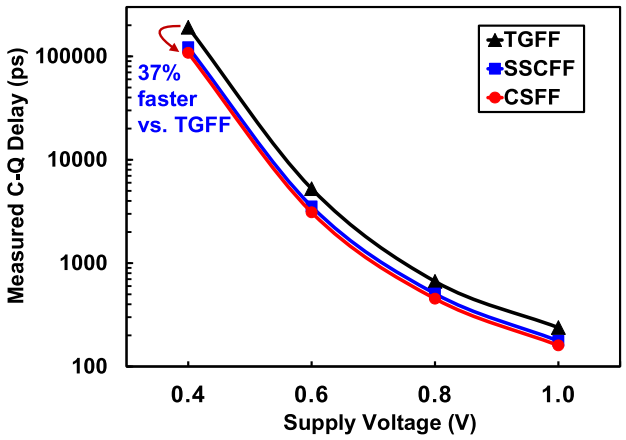


Fig. 29. Measured C-Q delays over the supply voltage. CSFF provides 37% delay reduction versus TGFF in the operating voltage range of 0.4–1 V.

Measurement results of the 40-nm CMOS test chip demonstrate successful operations of CSFF down to 0.19 V with the maximum frequency of 7.4 kHz. Compared to the previously reported low-power FFs [2]–[7], CSFF is the only FF with single-phase-clocking, redundant-transition-free, and low-voltage operations ($\geq$0.19 V) with the smallest area penalty (only one minimum poly pitch) and the same transistor count as the regular TGFF.

VII. CONCLUSION

An extremely low-voltage and low-power single-phase-clocking redundant-transition-free 24-transistor FF, CSFF, is proposed by utilizing a change-sensing scheme for eliminating redundant transitions of internal clocked nodes. The proposed CSFF removes dynamic power at 0% data activity. The test chip measurement in 40-nm CMOS demonstrates that CSFF saves power consumption up to 90% at 5% activity rate, compared to the conventional TGFF. No additional transistors are required. CSFF also provides more energy-efficient operations than TGFF across a wide operating voltage range, especially at low data activities. While achieving better power and energy efficiencies, CSFF further improves performance and maintains functional operations at low-voltage regimes. Measurement results demonstrate the delay improvement of 37% over TGFF and minimum operating voltage of 0.19 V. Compared to the recently introduced low-power FFs [2]–[7], CSFF is the only FF with redundant-transition-free, single-phase-clocking, and low-voltage operations with minimum area penalty and the same transistor count as TGFF. Therefore, CSFF could directly replace many FFs in the low-power applications particularly when the input data have relatively low activity rates.

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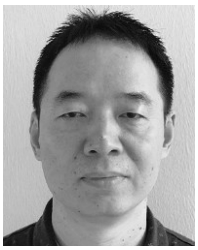

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