An Ultra-Low-Power Fully-Static Contention-Free Flip-Flop With Complete Redundant Clock Transition and Transistor Elimination

Gicheol Shin, *Student Member, IEEE*, Eunyoung Lee, *Student Member, IEEE*, Jongmin Lee, *Student Member, IEEE*, Yongmin Lee, *Student Member, IEEE*, and Yoonmyung Lee, *Senior Member, IEEE*

***Abstract*— A redundancy eliminated flip-flop (REFF) is proposed targeting wide-range voltage scalability (1–0.3 V). Two types of redundancies are eliminated in the REFF to achieve low-power (LP) and reliable operation even in the sub-threshold voltage regime. First, redundant internal clock transitions are eliminated without degrading reliability by finding the optimal way of generating internally inverted clock to reduce dynamic power consumption. Then redundant transistors are identified and eliminated with a topological and logical method while keeping it fully static and contention-free. The simulation results show that the REFF is currently the only FF that fully eliminates redundancy while maintaining static and contention-free operation, and is reliable down to 0.31 V in Monte-Carlo simulations. The measurement results from a test chip fabricated in 28-nm LP CMOS technology show that the measured power is reduced by 69.7%/58.7% with 0%/10% activity at 1 V and by 70.3%/58.2% with 0%/10% activity at 0.4 V compared to the conventional transmission gate flip-flop (TGFF). A total of 100 dies from five corners were tested to demonstrate the reliability, and the REFF was functional down to 0.28 V.**

***Index Terms*— Effective clock load, flip-flop (FF), redundant clock, redundant transistor, reliability.**

I. Introduction

NEAR-THRESHOLD voltage (NTV) computing has emerged as an attractive paradigm for energy efficiency, but its voltage scaling is limited by functional failures caused by increased variation [1]–[7]. Flip-flops (FFs), as the key sequential logic element in most synchronous digital circuits, have a great impact on the performance, robustness, size, and total power consumption of digital systems [8], [9]. Thus, sequential circuits operating at both NTV/above-threshold voltage require not only high-energy efficiency but also high reliability and should have the following characteristics: 1) fully static operation to avoid dynamic nodes that are highly susceptible to variation and leakage at NTV; 2) contention-free transitions to avoid functional failures of ratioed logic at NTV [1]–[7]; 3) no redundant clock transitions; 4) no redundant transistors to minimize dynamic power consumption; and 5) minimum area while achieving goals 1–4. Many FFs have been designed to minimize such redundancies with minimum area overhead [10]–[19], but these designs suffer from residual redundant clock transitions [10]–[13] and/or functional failure at NTV due to a lack of attribute 1 or 2 described above [13]–[18]. The static contention-free differential flip-flop (SCDFF) introduced in [19] fulfilled requirements 1–3 through a static contention-free differential structure, but further improvements could be achieved by eliminating additional redundant transistors and reducing the effective load for the clock.

This article proposes a redundancy eliminated flip-flop (REFF) [20] with all redundant clock transitions and transistors eliminated that is fully static and contention free with a total of 25 transistors including only four clock-loaded transistors. Using a systematic approach to eliminate redundancies, the proposed design achieves significant power reduction compared with prior arts while guaranteeing reliable operation at NTV. The REFF is implemented in 28-nm LP process along with other prior-art FFs, and power, reliability, setup time, hold time, and clock-to-q (c-q) delay are measured with embedded test circuitry to confirm its low-power (LP) and reliable operation at NTV. The remainder of this article is organized as follows. Section II reviews the state-of-the-art FFs, and Section III explains the redundancy elimination method used in the REFF. Section IV shows the simulation results with detailed analysis, and Section V shows the measurement results and comparison.

II. Review of State-of-the-Art FFs

A. Evaluation Metric for Low Voltage, Low Power FFs

Due to the large number of FFs used in a digital circuit, dynamic power consumption is a key metric to be evaluated for a low-power FF design. Because the typical activity ratio in a modern processor circuit is on the order of 5%–15%, the dynamic power consumption in an FF is dominated by

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Gicheol Shin, Jongmin Lee, Yongmin Lee, and Yoonmyung Lee are with the Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon 16419, South Korea (e-mail: yoonmyung@skku.edu).

Eunyoung Lee was with the Department of Semiconductor Display Engineering, Sungkyunkwan University, Suwon 16419, South Korea. He is now with Samsung Electronics, Suwon 18448, South Korea.

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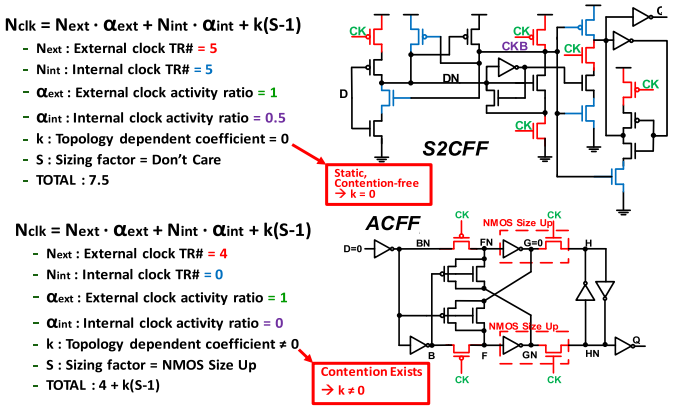


Fig. 1. Effective number of clock load transistor calculation method. Examples of calculations are given for S2CFF/ACFF.

the clock load switching overhead since the chance to have input changed is relatively low. Therefore, practical dynamic power consumption can be estimated to be proportional to the effective clock load, which is equal to the clock load capacitance or the number of transistors driven by the clock (directly or indirectly) multiplied by the clock activity ratio, which can be written as follows:

$$\mathbf{N_{clk} = N_{ext} \times \alpha_{ext} + N_{int} \times \alpha_{int} + k(S-1).} \quad (1)$$

Fig. 1 and (1) describe how the effective number of clock load transistors (N_{clk}) can be modeled. N_{clk} can be calculated as the sum of the effective external load ($N_{\text{ext}} \times \alpha_{\text{ext}}$) and the effective internal load ($N_{\text{int}} \times \alpha_{\text{int}}$). N_{ext} and N_{int} stand for the actual number of transistors driven by external and internally generated clock (or inverted clock), respectively. The activity ratio of the external load (α_{ext}) can be modeled as 1 since the activity ratio of the clock is 1. The activity ratio of the internal load (α_{int}) is topology-dependent: for an SC2FF, an internal clock transition happens only when $D = 0$, making $\alpha_{\text{int}} = 0.5$. For FFs that are not static or contention free, extra overhead "$k(S-1)$" is added due to the size-up requirement for reliability. "S" stands for the scaling factor, which is how much (clock-loaded) transistors must be scaled up to guarantee reliable operation of the FF, whereas "k" is a topology-dependent coefficient that includes the number of transistors that must be sized up and their activity ratio. For example, if the two NMOS transistors driven by the clock in the slave latch of an adaptive coupling flip-flop (ACFF) have been sized up threefold to alleviate contention (Fig. 1), an additional clock load, equivalent to $k(S-1) = 2(3-1) = 4$ unit-sized transistors, is expected.

In addition to dynamic power consumption, reliability needs to be considered when evaluating FFs for low-voltage operation. FFs that rely on current contention are hard to use in a low-voltage regime because of exacerbated variation among transistors. Adjusting the size of the transistors can help, but this requires an extreme sizing ratio to handle the worst case scenario, adding unrealistic power and area overhead. Dynamic nodes are also susceptible to variation in low-voltage regions because floating state nodes are susceptible to noise coupling and leakage. In light of the metrics discussed, the state-of-the-art FFs are reviewed in Section II-B.

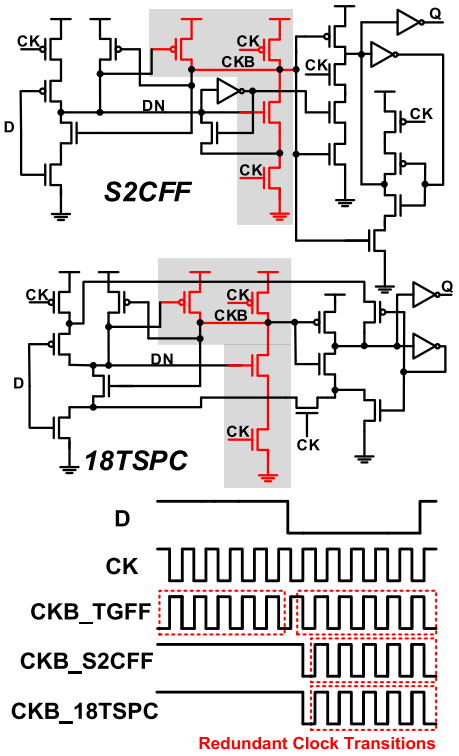


Fig. 2. Redundant clock transitions in TGFF, S2CFF, and 18TSPC.

B. Evaluation of Prior-Art FFs

A transmission gate flip-flop (TGFF) [11] is the most widely and commercially used conventional FF and operates reliably at NTV due to its static and contention-free characteristics. But due to a high effective clock load with a total of 12 transistors, it has many redundant clock transitions and redundant transistors and therefore consumes high dynamic power, making it unattractive for low-power applications.

A single-phase static contention-free flip-flop (S2CFF) [12] also operates reliably at NTV due to static contention-free characteristics. Compared to a TGFF, it partially eliminates redundant clock transitions when the input D is 1, but redundant clock transitions still remain when D is 0. Its total effective clock load transistor count is 7.5, as modeled in Figs. 1 and 2, significantly lower than that of a TGFF but still has room for improvement.

An ACFF [16] uses a differential structure to minimize the effective number of clock load transistors to 4. However, this design allows contention when writing the slave latch [Fig. 3(a)], which prohibits its usage at NTV. To overcome such contention and guarantee reliable NTV operations, the transistors in the slave latch need to be sized up (Fig. 1) and additional load is introduced [$k \neq 0$, $S > 1$ in (1)].

The 18 true single phase clock (18TSP) [13] is similar to an S2CFF in that it partially eliminates redundant clock transitions, but it still suffers from conditional redundant clock transition when $D = 0$. It also suffers from contention when $D = 0$, Qprev $= 1$ and CK $= 0 \rightarrow 1$ [Fig. 3(b)], which

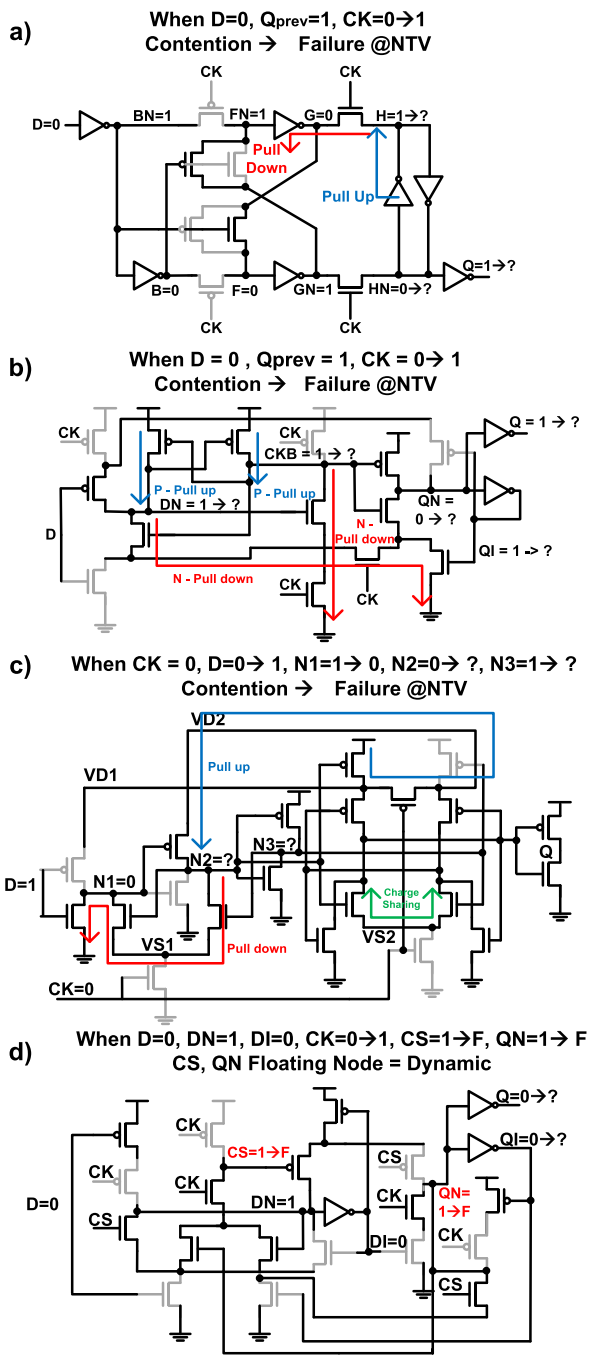


Fig. 3. Reliability issues in (a) ACFF [16], (b) 18TSPC [13], (c) TCFF [15], and (d) CSFF [18].

prohibits its usage at NTV. Although it has only six clock transistors, additional load is incurred when it is sized up to overcome contention.

A topologically compressed flip-flop (TCFF) [14], [15] uses a topological compression method to eliminate redundant transistors, achieving a very low effective clock load of only three transistors. But this design suffers from contention and charge sharing problems [Fig. 3(c)], prohibiting its usage at NTV.

A change-sensing flip-flop (CSFF) [17], [18] uses a change-sensing scheme to eliminate redundant clock transitions and achieves a low effective clock load of five transistors. However, this design suffers from dynamic nodes (CS, QN) [Fig. 3(d)], prohibiting its usage at NTV.

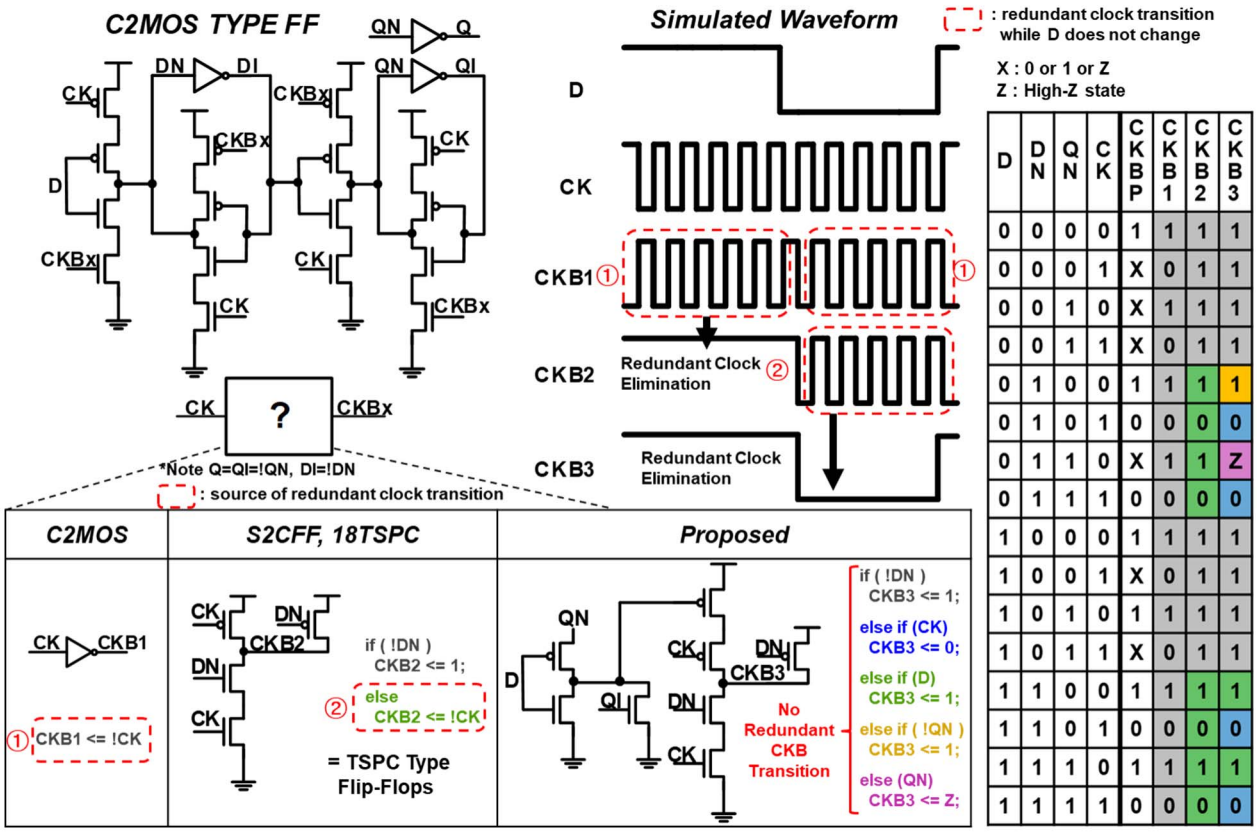
III. Redundancy Eliminated Flip-Flop

Eliminating redundancies with clock transitions and transistors is the key to minimizing dynamic power consumption. While eliminating such redundancies, the static and contention-free nature of the FF should be maintained to avoid the extra loading incurred by transistor size-up required to overcome contention and guarantee reliable operation at NTV.

Many different prior art FF topologies reduced redundancy in an intuitive way, making it difficult to ensure their stable operation. This article presents a systemic approach to eliminating redundancy without losing any of the stable characteristics. Two approaches are proposed in this article to ultimately minimize dynamic power consumption while guaranteeing the static and contention-free nature of the FF: 1) eliminate redundant clock transitions and 2) eliminate redundant transistors.

A. Redundant Clock Elimination

The first type of redundancy to be eliminated is redundant clock transitions. Fig. 4 shows a clocked CMOS (C2MOS) FF [10] that has the robust characteristics required for reliable operation at NTV (static, contention-free). This structure uses two phase clocks, CK/CKB, and an inverter is used to generate CKB from CK. In this case, CKB transitions all the time, even when input D has not changed, and there is no need to update stored data Q/QN. To eliminate such redundant CKB transitions that consume unnecessary dynamic power, many possible solutions for CKB can be found, denoted as CKB possible (CKBP) in the table on the right side of Fig. 4. The table includes all of the state nodes, D, DN, QN, and CK (note DI = !DN, Q = QI = !QN), and the acceptable CKB value for given combination of state node values is written as CKBP. The "X" under CKBP denotes that "1," "0," and "High-Z" are all acceptable for the given state combination. Permitting the High-Z state of CKB does not make the proposed FF dynamic if all of the state nodes are statically driven without contention. Detailed examples of such states that allow High-Z are shown in Fig. 5. When CKB is in High-Z state, i.e., the actual voltage is unknown, all internal state nodes are guaranteed to be statically driven by a parallel conduction path (green arrows) even when all of the CKB-driven transistors are OFF. On the other hand, all paths that need to be blocked (blue arrows) are guaranteed to be disconnected even when all of the CKB-driven transistors are ON since the series-connected transistors are OFF, blocking the undesired conduction path to VDD or GND. For example, when $D = 0$, DN = 1, QN = 1, and CK = 0, CKBP can be any value between GND and VDD, meaning that the transistors driven by CKBP can be either ON or OFF or partially ON. This is not a concern since DN and QN are already driven to VDD by parallel paths ensuring static operation and are not pulled to ground through CKBP transistors since it is blocked by series transistors in this state. This allows many solutions for CKB that still ensure static and contention-free operation, such as CKB1, CKB2, and CKB3, which are all subset of CKBP.



D	DN	QN	CK	CKBP	CKB1	CKB2	CKB3
0	0	0	0	1	1	1	1
0	0	0	1	X	0	1	1
0	0	1	0	X	1	1	1
0	0	1	1	X	0	1	1
0	1	0	0	1	1	1	1
0	1	0	1	0	0	0	0
0	1	1	0	X	1	1	Z
0	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1
1	0	0	1	X	0	1	1
1	0	1	0	1	1	1	1
1	0	1	1	X	0	1	1
1	1	0	0	1	1	1	1
1	1	0	1	0	0	0	0
1	1	1	0	1	1	1	1
1	1	1	1	0	0	0	0

Fig. 4. Redundant clock elimination in REFF.

When the CKB is generated by directly inverting the CK, CKB1 results, which is the case with conventional C2MOS. When CKB2 is chosen by generating CKB by NAND operating DN and CK, the FF operates as S2CFF[12]/true single phase clock (TSPC)18[13] (TSPC-type FF). As depicted with Verilog-formatted statements in Fig. 4, these two cases both have a CKB = !CK statement, making CKB always toggle for a given D condition regardless of the input change, resulting in redundant clock transitions. It is noted that for CKB2, redundant clock transition only happens when DN = 1, reducing redundant clock transitions in half ($\alpha_{\text{int}} = 0.5$). By further conditioning clock transitions with other state nodes (D, DN, QI, and QN), redundant transitions can be reduced, even eliminated eventually.

CKB3 in Fig. 4 is the proposed solution to eliminate redundant clock transitions with the least transistor overhead while staying static and contention free. CKB3 is a subset of CKBP, but it takes advantage of the fact that CKBP allows High-Z state, which conventionally was assumed to be dangerous. The CKB3-generating logic is shown with if-else statements in Verilog format in Fig. 4 along with the corresponding gate circuit structure. The simulated waveform shows CKB for C2MOS (CKB1), S2CFF, TSPC18 (CKB2), and the proposed FF (CKB3), and confirms that CKB2 reduces the redundant clock transitions by half, and CKB3 removes the remaining half.

B. Redundant Transistor Elimination

The second type of redundancy to be eliminated is redundant transistors. There are two methods for redundant transistor elimination, namely, topological and logical methods, as shown in Fig. 6.

The topological method proposed in [15] merges topologically equivalent transistors but does not account for the charge sharing that can occur under certain conditions as shown in Fig. 6. As a result, a TCFF [15] suffers from contention that degrades its robustness against variation. Transistor merging is applied in the proposed FF as shown in Fig. 6, eliminating three clock transistors while avoiding contention conditions. A1, A2 and B1, B2 (in Fig. 6) could be merged because CK = 1 (or CKB = 0) implies DN = QN, and X1, X2 could be merged because DI = !DN always.

A logical method is proposed to eliminate redundant transistors by examining the inclusion relation of the transistor logic. From the truth table on the right side of Fig. 4, when CKB3 = 0 (i.e., CKB in Fig. 6 is 0), it implies DI = 0 (DN = 1). Therefore, two PMOS stacks with CKB, DI gate inputs can be simplified to a single PMOS with CKB gate input, eliminating two additional transistors.

A total of five redundant transistors are eliminated using these two different methods, which makes the proposed REFF a 25-transistor FF with only four clock transistors. Operation of the REFF in each state is shown in Fig. 7. When there is no data transition, CKB does not transit, saving a significant portion of dynamic power. When there is data transition, CKB transits and updates the new value to Q. Also, it can be confirmed that High-Z state does not make this FF dynamic because all of the state nodes (DN, DI, QN, QI) are statically driven in all cases. To prove this, voltage pulses were applied

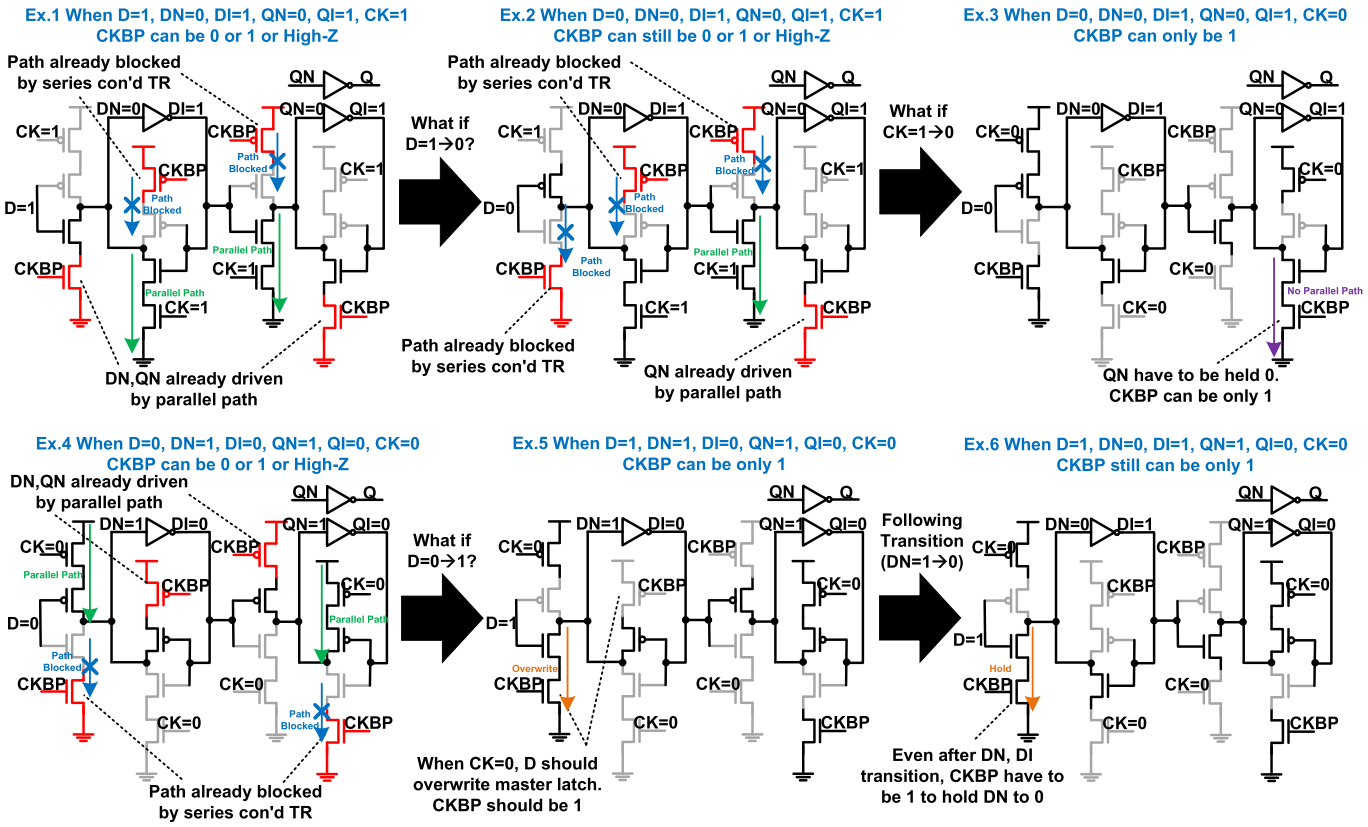


Fig. 5. States that allow high-Z CKB in C2MOS-based FF.

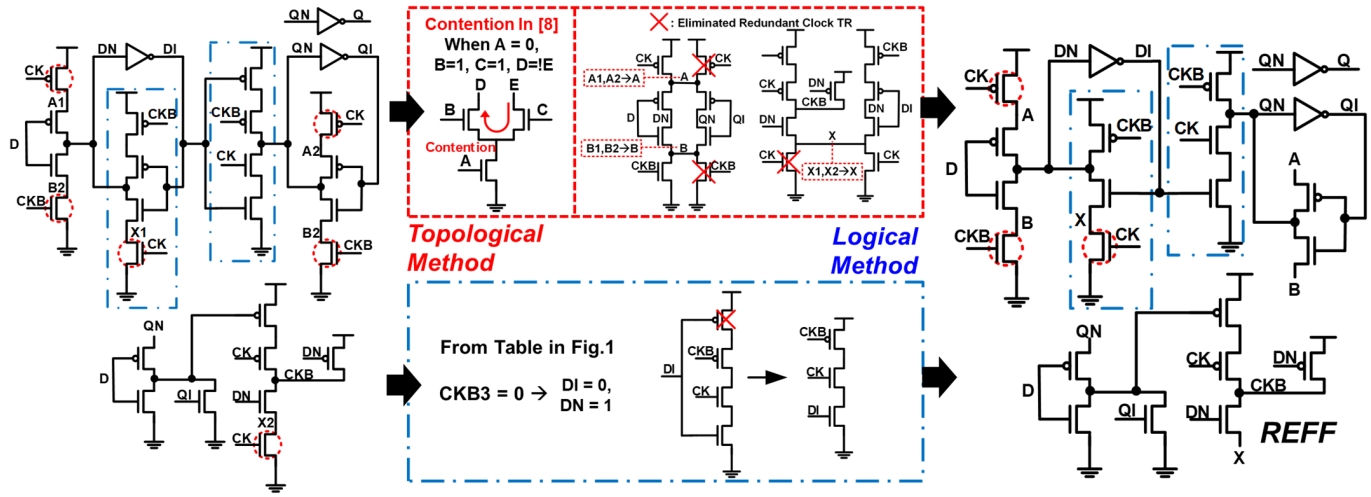


Fig. 6. Redundant transistor elimination.

on the CKB node (0–1 V) in a transient simulation to model voltage changes on the floating node due to capacitive coupling or leakage. All the state nodes were probed, and they were not disrupted. Thus, the REFF is a static contention-free FF with redundancy fully eliminated.

IV. Simulation Results

The table in Fig. 8 summarizes the characteristics and reliability of the state-of-the-art FFs. Prior arts suffer from tradeoffs among key attributes, resulting in conditional redundant clock transition (TGFF, S2CFF, TSPC18), contention (TSPC18, ACFF), or dynamic state nodes (CSFF). Such characteristics incur high power consumption to alleviate contention or prohibit usage under NTV. It can also be seen from the table that the REFF is the only FF that fully eliminates redundancy while maintaining static contention-free operation, enabling low-voltage operation down to the NTV region.

The reliability of FFs at NTV can be verified with Monte Carlo simulations. The test circuit was simulated with 28-nm LP process, and for each condition, 10k Monte Carlo simulations are performed for a voltage range of 0.25–1 V for each FF. For transistor sizing, 0.1-μm NMOS, 0.2-μm PMOS standard transistor sizes were used to simulate all FFs for

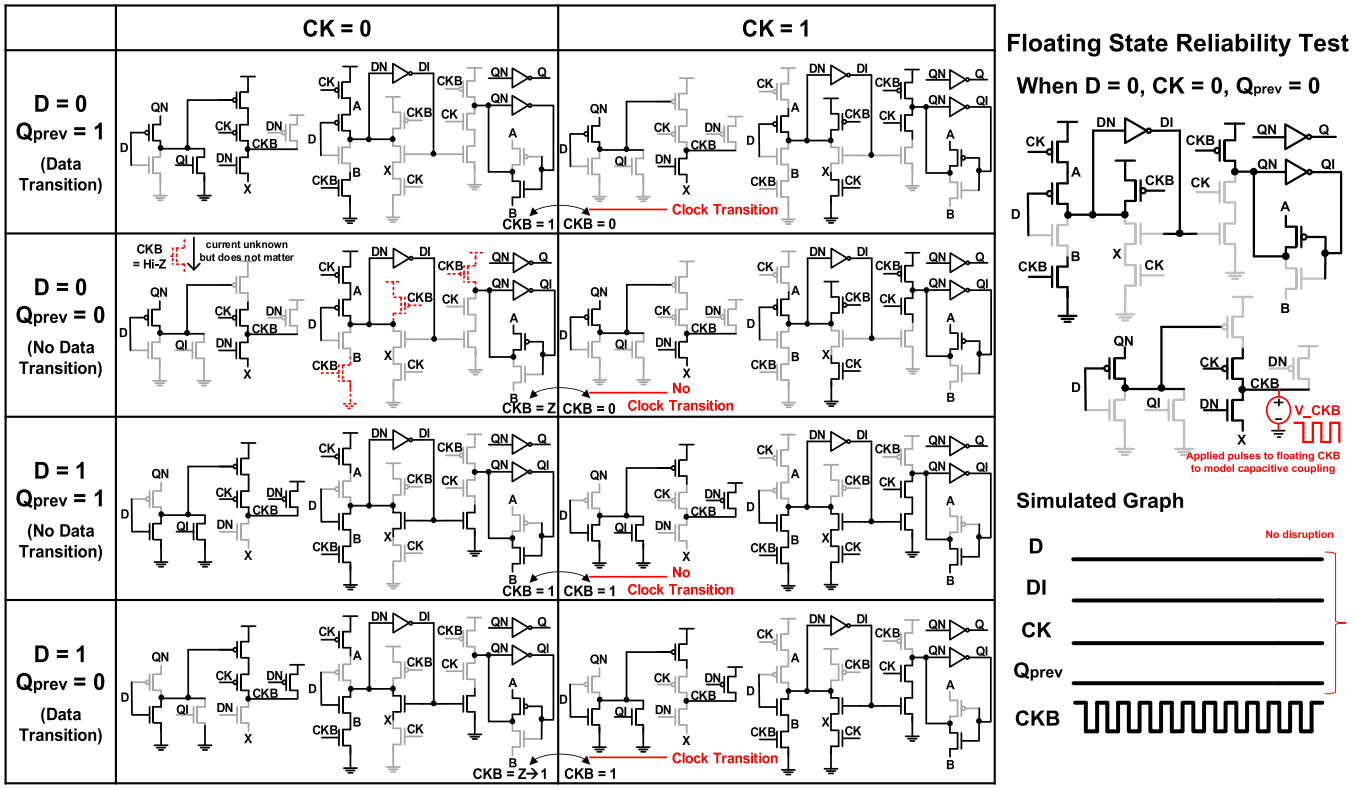


Fig. 7. Schematic of REFF and its operation + floating state reliability test.

	Power	Reliability	
	No Redundant Clock	Static	Contention Free
TGFF	X	O	O
S2CFF	Δ	O	O
18TSPC	Δ	O	X
TCFF	O	O	X
ACFF	O	O	X
CSFF	O	X	O
REFF	O	O	O

Δ : Conditional Redundant Clock (when D = 0)
: Undesired Characteristic

	TGFF	S2CFF	18TSPC	TCFF	ACFF	CSFF	REFF
1V	P	P	F	F	F	F	P
950mV	P	P	F	F	F	F	P
900mV	P	P	F	F	F	F	P
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
550mV	P	P	F	F	F	F	P
500mV	P	P	F	F	F	F	P
450mV	P	P	F	F	F	F	P
400mV	P	P	F	F	F	F	P
350mV	P	P	F	F	F	F	P
300mV	F	P	F	F	F	F	F
250mV	F	F	F	F	F	F	F

* 10k Monte Carlo simulations each (global + local)
* D, CK transition time is assumed to be FO4 transition time

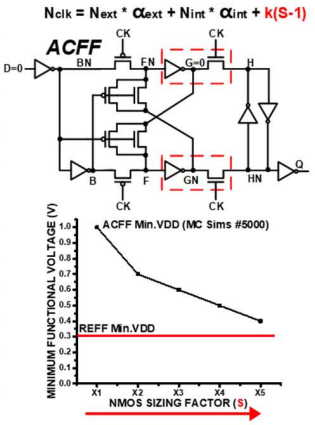


Fig. 8. FF characteristics table and Monte-Carlo simulation results.

a fair comparison, which is similar approach used in [14] and [15]. The analysis results show that FFs with unreliable characteristics (ACFF, TSPC18, TCFF, and CSFF) fail even at full VDD due to contention or dynamic nodes. Failures at super-threshold voltage region can be relieved by sizing transistors with area/power overhead. But failures at NTV cannot be resolved through sizing because the effect of variation is exacerbated in this region, and it would require impractical transistor sizing [4]. FFs with reliable characteristics (TGFF, S2CFF, and REFF) experience no failures even down to sub-threshold regions without additional transistor sizing. Such a tradeoff between area/power versus reliability can be quantified with the effective clock load calculation method proposed in Section II-A. The right side of Fig. 8 clearly describes this tradeoff for an ACFF, one of the unreliable FFs. To make an ACFF operate reliably at a supply voltage down to 0.6 V with #5000 Monte Carlo simulation, the NMOSs have to be sized up threefold. An additional effective clock load for making ACFF reliable at 0.6 V would be "$k(3-1)$." Additional loads for other types of FF are summarized in Table I in the measurement section. Additional Monte-Carlo simulations were conducted to measure c-q delay, setup time, and hold time as shown in Fig. 9. Only FFs with reliable characteristics (TGFF, S2CFF, and REFF) are further analyzed. The three sigma and average values are plotted for a voltage range of 0.4–1 V in terms of fan-out of 4 (FO4) delay. C-q delay is calculated as the average of $0 \rightarrow 1$ delay and $1 \rightarrow 0$ delay. The setup/hold time is calculated by the worst case path when $D = 1$ and $D = 0$. The REFF shows slightly better c-q delay compared to S2CFF and TGFF since it has

TABLE I
COMPARISON TABLE

	REFF	TGFF [11]	ACFF [16]	S2CFF [12]	TCFF [15]	CSFF [18]	18TSPC [13]
	This Work	Std.Cell	ISSCC 2011	ISSCC 2014	JSSC 2014	JSSC 2018	JSSC 2019
Static	Yes	Yes	Yes	Yes	Yes	No	Yes
Contention-Free	Yes	Yes	No	Yes	No	Yes	No
Redundant Clock Transitions	No	Yes	No	Yes	Yes	No	Yes
Transistor Count	25	24	22	24	21	24	18
Effective Clock TR # (N_{clk})[1)]	4 + 0 + 0	2 + 10 + 0	4+0+k_1(S-1)	5 + 2.5 + 0	3+0+k_2(S-1)	5+0+k_3(S-1)	4+2+k_4(S-1)
Power @ 0%, 1.0V, 1GHz[2)]	1.33μW	4.34μW	1.78μW	3.00μW	1) A+B+C: A – load seen by clock driver B – load due to internal clock C – additional load due to size up 2) Equal to clock power 3) For 100 dies total, 20 dies in each corner (NN, FF, SS, FS, SF) 4) FO2 Delay		
Power @ 10%, 1.0V, 1GHz	1.93μW	4.64μW	2.42μW	3.38μW			
Measured Min. VDD[3)]	0.28V	0.3V	0.46V	0.3V			
Measured C-Q Delay[4)] @ 1.0V	123.5ps	116.4ps	79.4ps	138.5ps			
Measured Setup Time @ 1.0V	38.6ps	21.8ps	86.4ps	47.8ps			
Measured Hold Time @ 1.0V	28.0ps	15.2ps	-62.8ps	28.2ps			
Normalized Layout Size	1.17	1.00	1.11	1.00			

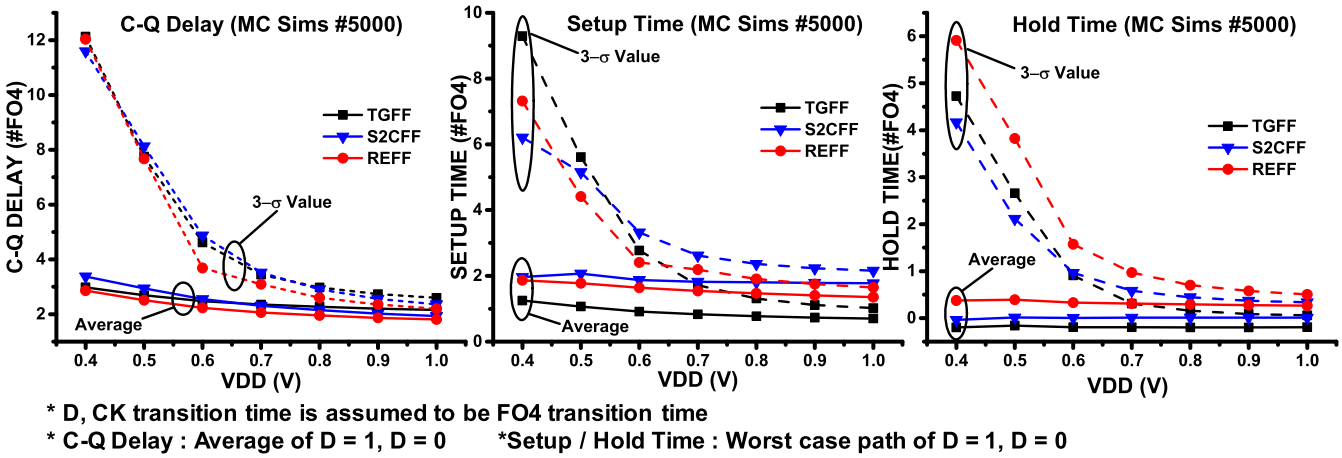


Fig. 9. Monte-Carlo simulation results for c-q delay, setup time, and hold time.

the shortest 0 → 1 c-q delay path with two NMOS pull-down + inverter (three NMOS pull-down + inverter for S2CFF, Transistor (TR) gate + 2 inverters for TGFF). The REFF shows moderate setup time but worse hold time compared to the TGFF and S2CFF. The hold time degradation is mainly due to data-dependent CKB generation of REFF and topological transistor merging of B1/B2 → B in Fig. 2, degrading the average/3-σ hold time.

V. MEASUREMENT RESULTS

A test chip is fabricated in 28-nm LP process (Fig. 10) to characterize the TGFF, S2CFF, and REFF along with ACFF [16], which had to be aggressively sized (NMOS transistors in the slave latch are sized up by 3×) to overcome the contention in the slave latch. Such sizing allows the ACFF to function without failure when 10k Monte Carlo simulations are performed at a supply voltage of 0.6 V. The aggressively sized transistors in the ACFF are intended to model extra power overhead for FFs with unreliable characteristics.

The test circuits are embedded on chip to measure power, c-q delay, setup time, and hold time and detect functional

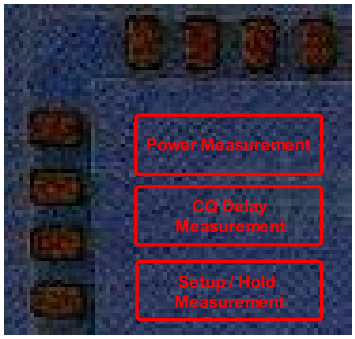


Fig. 10. Die micrograph.

failures as shown in Fig. 11. For power measurement [Fig. 11(a)], the power consumed on clock buffers that drive the clock nodes of the tested FFs and the FF internal power are added and the intrinsic power consumption in the clock buffer is subtracted. The input buffer for "*D*" is included in the test circuit, but its power consumption is not included for the power comparison. This is because the load capacitance of "*D*" input is much smaller than that of the clock input

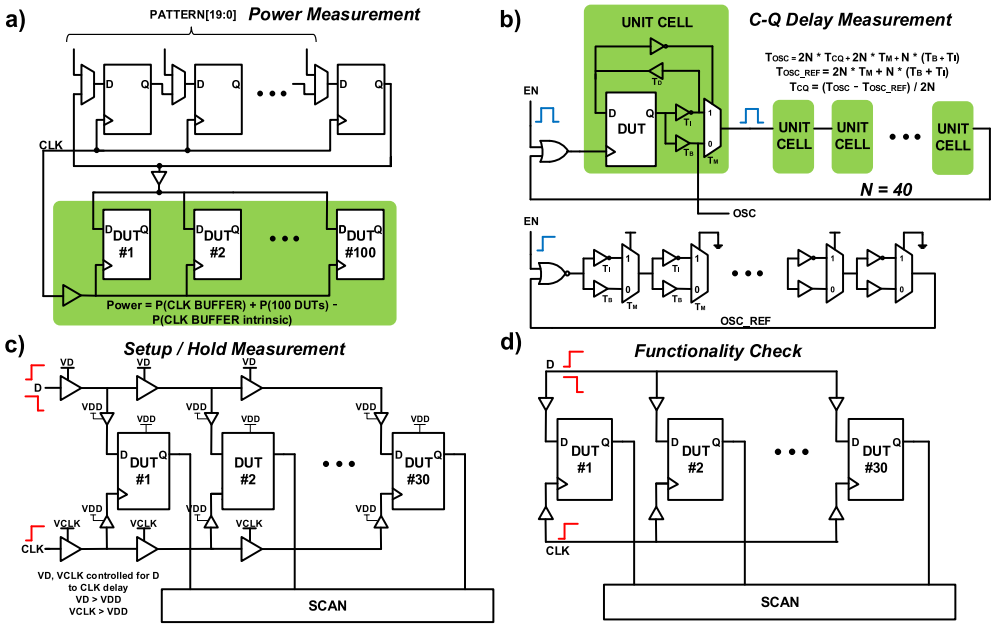


Fig. 11. Test circuit implementation. (a) Power measurement circuit. (b) C-q delay measurement circuit. (c) Setup/hold time measurement circuit. (d) Functionality checking circuit.

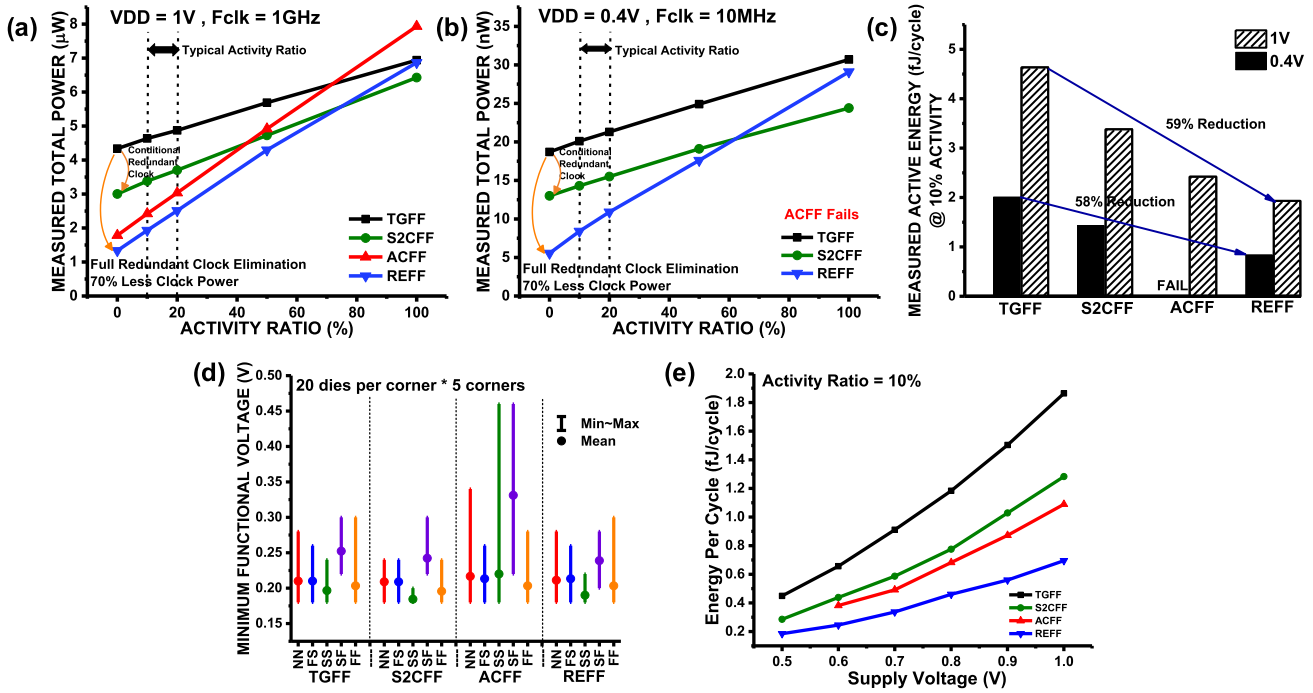


Fig. 12. Measurement results of (a) power at 1 V, (b) power at 0.4 V, (c) active energy, (d) reliability, and (e) simulated energy per cycle for wide range of supply voltages.

and its related internal load, and the activity ratio of the clock is much higher than that of "*D*." Furthermore, an additional output load for *Q* is not considered in the power measurement because the output "*Q*" for all of the tested FFs is internally buffered with an inverter, and hence, adding the output load adds the same amount of power for all of the FFs in the power comparison. The activity ratio can be controlled by altering the PATTERN[19:0] vector. The c-q delay could be measured [Fig. 11(b)] with the same circuit used in [12], which uses oscillation frequency to calculate c-q delay. The setup time/hold time are measured [Fig. 11(c)] through time-delayed *D* and CLK pulses by controlling the inverter chain voltage. By controlling the voltages VD and VCLK, the delay difference between signal *D* and CLK can be controlled for each inverter stage, and the setup/hold time can be determined by reading the *Q* values to see whether valid data is written. The delay time can be calculated using a ring oscillator with the same voltage. The functionality check circuit for reliability measurement [Fig. 11(d)] simply applies signals to *D* and CLK and reads out *Q*s to check whether the valid data are written into the FF without any failure for all voltage regions.

Fig. 12 shows the measured results. Thanks to the full redundant clock transition elimination in the REFF, a clock power reduction of 69.7%/70.3% compared to the TGFF is

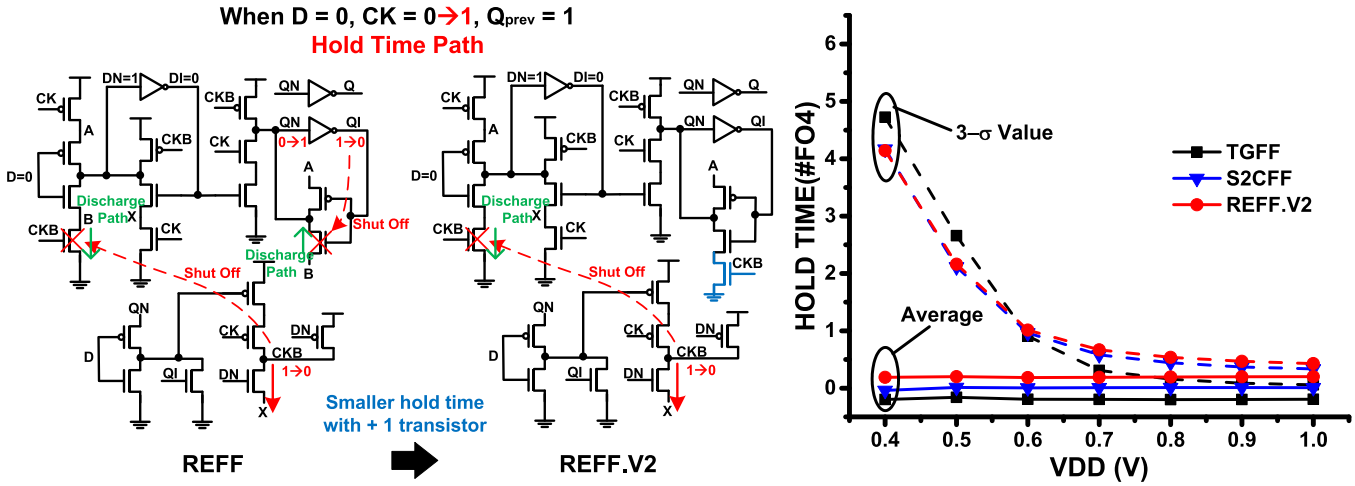


Fig. 13. Hold-time path in REFF and its mitigation scheme (REFF.V2), and estimated hold-time improvement with the mitigation.

observed at 1 V/0.4 V, respectively, with a 0% activity ratio (α) [Fig. 12(a) and (b)]. Note that the S2CFF with conditional redundant clock transition %/30.5% reduction compared to TGFF. When $\alpha = 10\%$, which is a typical operating condition in digital processors, the REFF shows 58.7%/58.2% power reduction at 1 V/0.4 V, respectively, compared to the TGFF [Fig. 12(c)]. Under the same condition, the ACFF's power consumption at 1.0 V is higher than that of the REFF due to the upsized transistor (3× NMOS) used for reliability. To prove that the FFs follow the same power trend across a wide voltage range, the amount of energy per cycle for a wide voltage range (0.5–1.0 V) at 10% activity ratio is simulated [Fig. 12(e)]. All of the FFs show power reduction due only to voltage scaling, proving that there is no unstable operation that adds power overhead across a wide voltage range. To evaluate reliability against process variation, the minimum operating voltages of 20 dies from each corner (NN, SF, FS, SS, and FF), for a total of 100 dies, are measured with 20-mV step as shown in Fig. 12(d). The ACFF fails at <0.46 V at the SF corner even with upsized transistors, which shows that overcoming contention with sizing does not work at NTV. In contrast, the TGFF, S2CFF, and REFF are 100% functional at 0.3 V, and the REFF is functional down to 0.28 V. This result clearly shows why static and contention-free operation is important in the NTV region. The measured setup time/hold time/c-q delay are shown in the comparison table (Table I) and are measured using the test circuits shown in Fig. 11 on the same chip. As was observed in the simulation results, the measurement results show improvement in the c-q delay and setup time for the REFF compared to the S2CFF, but in contrast, the TGFF outperforms the REFF in c-q delay in the measurement results. This is mainly due to the wiring complexity of the S2CFF/REFF, which adds capacitance, degrading the c-q delay. The TGFF outperforms REFF in terms of timing but at the cost of much higher dynamic power.

Table I shows the overall comparison of the REFF with other prior arts FFs. With the redundancy eliminated structure and variation-tolerant design, the proposed REFF requires the least number of effective clock-loaded transistors (considering sizing for reliability in other FFs as explained in Section II-A). As a result, the REFF achieves the lowest power consumption for both 0% and 10% activity ratio among the static contention-free FFs (TGFF, S2CFF, and REFF). Although the ACFF has the same number of transistors directly seen by the clock driver, it consumes more power due to transistor sizing for reliability. The REFF, as well as the TCFF and S2CFF, had very low minimum VDD measured on all corners due to the static, contention-free operation. The ACFF fails at 0.46 V due to contention even with transistor sizing (by a factor of 3 in the test chip). The REFF has one more transistors than the TGFF, but its layout size is 17% larger than the TGFF due to three additional poly gates added for its complex wiring. Metal layers 1–2 were used for the TGFF layout (foundry provided), and metal layers 1–3 were used for the ACFF, REFF, and S2CFF due to complex metal wiring.

Fig. 13 shows the hold-time path of the REFF, which results in hold-time degradation, as can be seen in Fig. 9. When $D = 0$, CK $= 0 \rightarrow 1$, Qprev $= 1$, if D switches and discharges DN near the edge of CK, a hold-time violation can occur. There are two discharge paths for REFF, as shown in Fig. 13. Hold-time degradation is mostly due to transistor sharing between the NMOS B1 and B2 in Fig. 6, which results in a discharge path through B to QN that takes a long time to shut OFF (must wait for CKB discharge + QN/QI switching) as shown in the REFF diagram (Fig. 13). If we choose not to merge B1/B2 → B, one transistor can be added, slightly increasing the area and power but decreasing the hold time almost down to the hold-time level of S2CFF, as shown in Fig. 13.

VI. Conclusion

An REFF with static and contention-free operation for low-voltage and low-power applications is presented. With the complete elimination of redundant clock transitions and redundant transistors, the REFF achieves significant dynamic power reduction while preserving reliable operation at NTV. Due to its redundancy eliminated structure and aggressive voltage scalability, it makes an ideal sequential circuit element not only for low-voltage and low-power applications such as Internet of Things (IoT) systems and miniature sensor

systems but also for regular digital systems with standard supply voltages.

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Gicheol Shin (Student Member, IEEE) received the B.S. degree in electrical engineering from Sungkyunkwan University, Suwon, South Korea, in 2017, where he is currently pursuing the M.S/Ph.D. degree in electronic, electrical and computer engineering.

His research interests include ultra-low-power circuit and hardware accelerator design for deep learning applications.

Eunyoung Lee (Student Member, IEEE) received the B.S. degree in semiconductor systems engineering from Sungkyunkwan University, Suwon, South Korea, in 2019, where she is currently pursuing the M.S. degree in semiconductor systems engineering.

Her current research interests include compute in memory circuit designs and low-power digital circuits.

Jongmin Lee (Student Member, IEEE) received the B.S. degree in semiconductor systems engineering from Sungkyunkwan University, Suwon, South Korea, in 2017, where he is currently pursuing the M.S./Ph.D. degree in electrical and computer engineering.

His research interest includes hardware security.

Yongmin Lee (Student Member, IEEE) received the B.S. degree in biomedical engineering from Konyang University, Daejeon, South Korea, in 2016, and the M.S. degree in electronic, electrical and computer engineering from Sungkyunkwan University, Suwon, South Korea, in 2019.

His research interests include low-power circuit design and digital VLSI design.

Yoonmyung Lee (Senior Member, IEEE) received the B.S. degree in electronic and electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, South Korea, in 2004, and the M.S. and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2008 and 2012, respectively.

From 2012 to 2015, he was a Research Faculty with the University of Michigan. In 2015, he joined Sungkyunkwan University, Suwon, South Korea, where he is currently an Associate Professor. His research interests include energy-efficient integrated circuits design for low-power high-performance integrated systems and millimeter-scale wireless sensor systems.

Dr. Lee was a recipient of Samsung Scholarship in 2005 and Intel Ph.D. Fellowship in 2011. He has been serving as a Technical Program Committee Member for A-SSCC since 2017 and CICC since 2021 and an Associate Editor for IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS since 2019.