上海交通大學
Shanghai Jiao Tong University

Lab1 Inverter chain & OR7 design

Digital Integrated Circuit Design

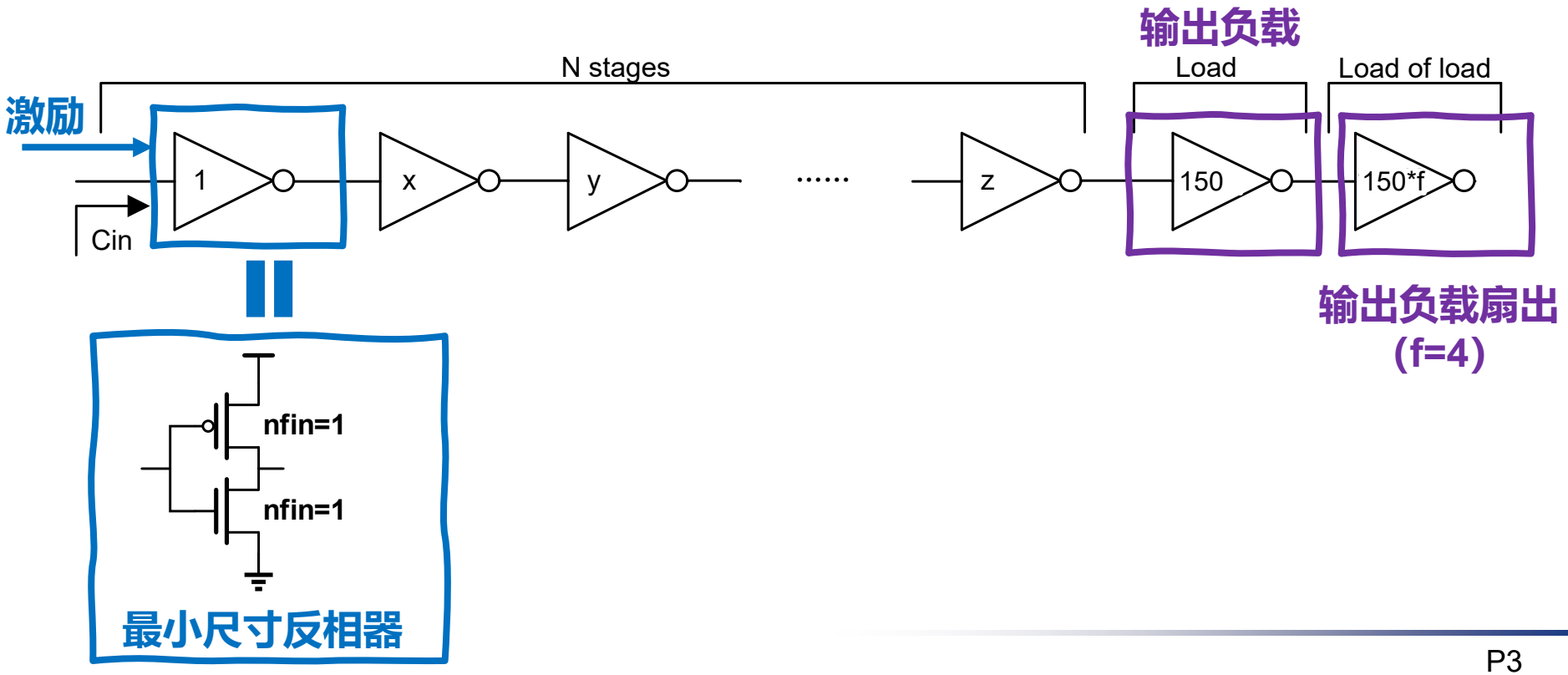
TA1: Zihan Lian - lianzihan@sjtu.edu.cn;
TA2: Yuxuan Qin - qinyuxuan@sjtu.edu.cn;

Outline

- **实验内容**
  - **反相器链路设计**
  - 七输入或门设计
- 实验工具
  - Hspice
  - FinFET
- 实验材料和要求
- 附录

反相器链路设计——实验内容

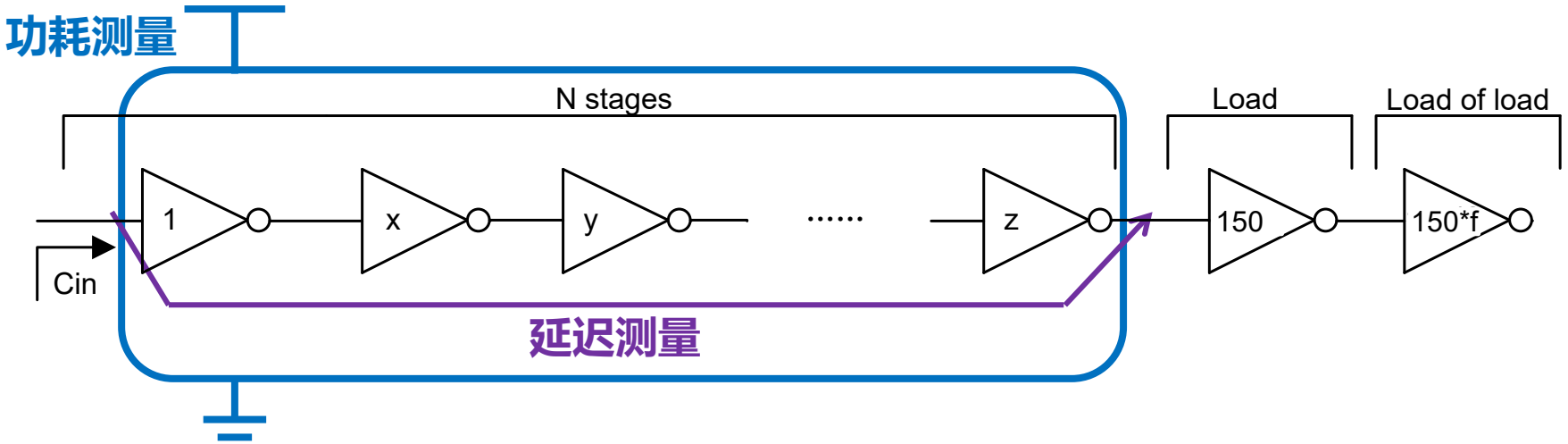
- 输入负载：最小尺寸反相器
- 输出负载：150倍最小尺寸反相器(扇出为4)



反相器链路设计——实验目标

设计目标：

1. 在固定电压为标准电压（PTM 10nm: 0.75V），温度85度的情况下，**设计适当的级数和尺寸**，保证反相器输出上升下降速度基本相等的情况下，**优化t_p**=(t_{pHL}+t_{pLH})/2；
2. 在**1)**的电路基础上，确定**EDP最优**的工作电压；



反相器链路设计——注意事项

- 测功耗时不包括负载反相器的功耗：
  - 反相器链和负载反相器的电源节点命名不同；

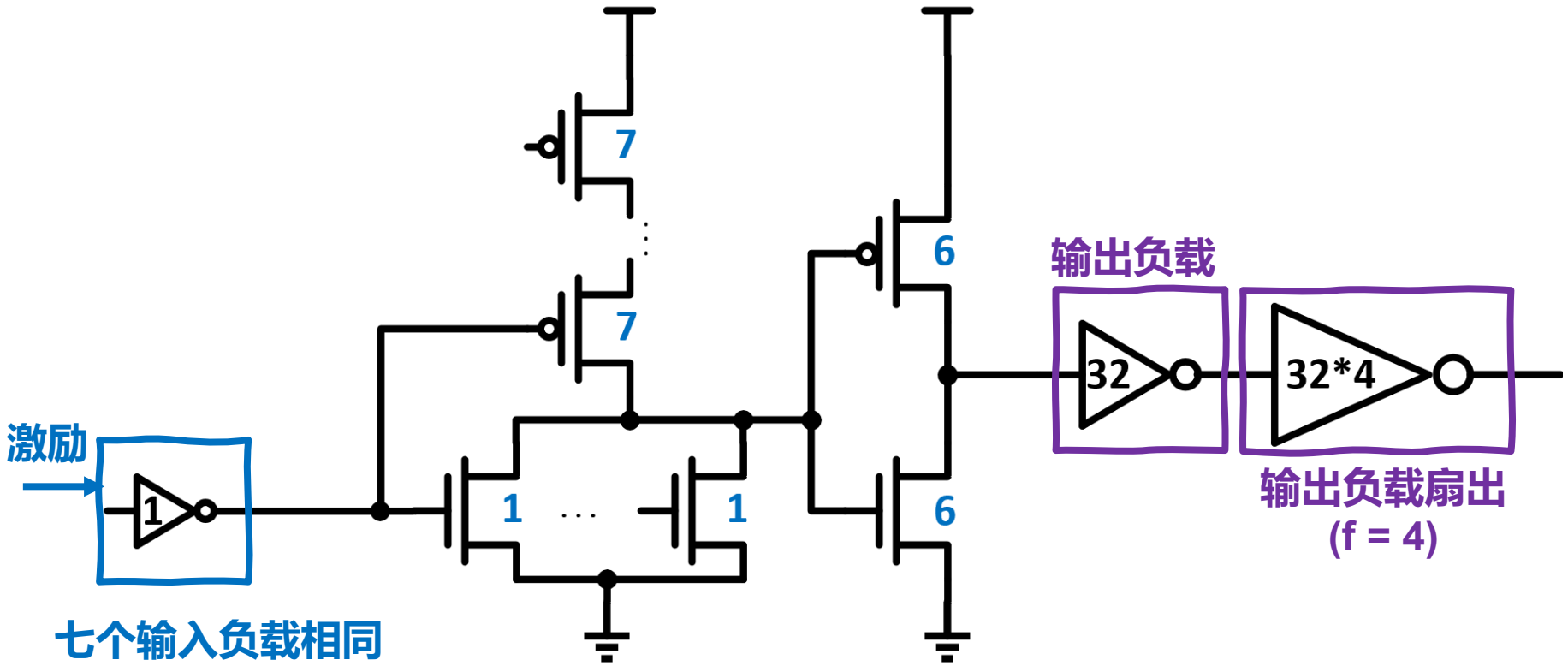
- 电压scaling过程中，当电源电压很低时，输出翻转会很慢。此时应当增大输入信号的周期，使输出有足够长的时间翻转；

Outline

- **实验内容**
  - 反相器链路设计
  - **七输入或门设计**
- 实验工具
  - Hspice
  - FinFET
- 实验材料和要求
- 附录

七输入或门设计——实验内容

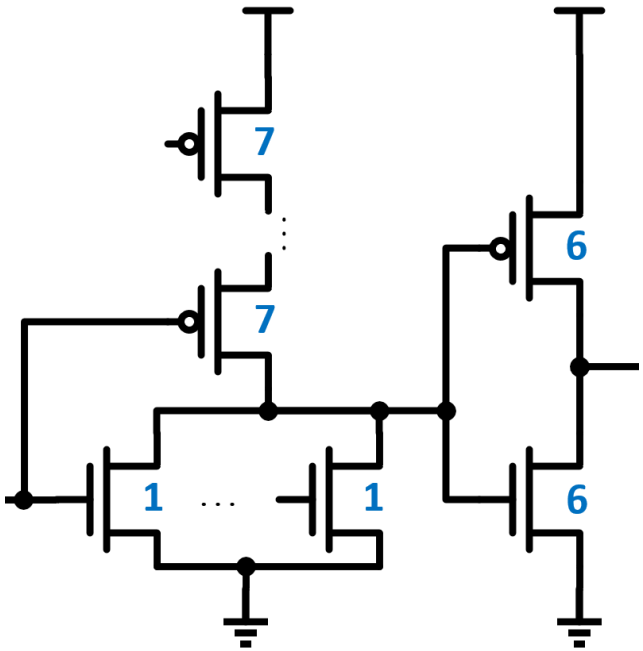
- 输入负载：最小尺寸反相器
- 输出负载：扇出为4的32倍最小尺寸反相器）



七输入或门设计——实验目标

设计目标：

- 进行结构上的选取（多级，动静态，…），设计工作在标准电压（PTM 10nm: 0.75V）温度85度下的五输入与门，**平均延迟**、**面积**、**功耗**都要优于参考电路（下图）



七输入或门设计（注意事项）

- 面积估算方法：
  - $\sum_{all\ T} W \times L$;
- input data pattern的不同会导致单次翻转的延时、动态功耗会有所不同（对可能存在的情况求均值）：
  - 功耗延迟计算7种模式（上升下降延迟各7种）的平均值：

    0000000⇋000000**1**、 0000000⇋00000**1**0、 …、 0000000⇋**1**000000

- 若不能同时取得面积、功耗、延时三者的优化，可考虑设计多个电路（不要求一定使用静态CMOS电路实现），分别完成上述要求的部分。若仍不能满足，需在报告中分析清楚原因

Outline

- 实验内容
  - 反相器链路设计
  - 七输入或门设计
- **实验工具**
  - **Hspice**
  - FinFET
- 实验材料和要求
- 附录

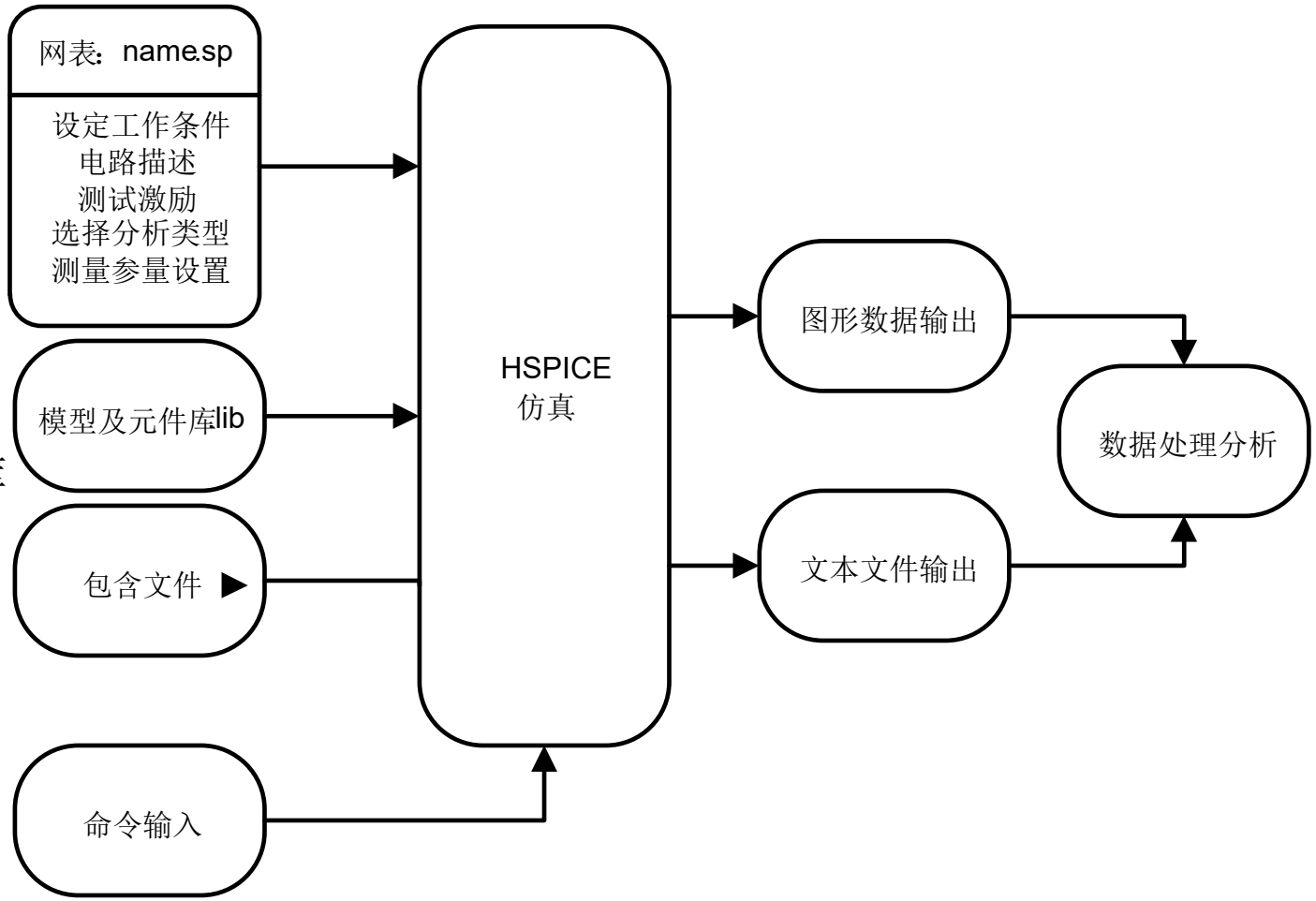
SPICE Introduction

- SPICE – **S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis developed by U.C.Berkeley
- SPICE simulate your electrical circuit designs, based on circuit level
  - Steady-state (DC Analysis)
  - Time (Transient Analysis)
  - Frequency (AC Analysis)

HSPICE仿真流程

Inverter chain、
AND5的电路

NMOS
PMOS
参数模型，元件库



输入输出文件

文件种类	文件后缀名
输入网表文件	**.sp**
模型与库文件	.inc .lib
运行状态文件	.st0
输出列表文件	.lis
测量输出文件	.m*#
瞬态分析文件	.tr#
直流分析文件	.sw#
交流分析文件	.ac#
其他文件	…

输入输出文件

文件种类	文件后缀名
输入网表文件	**.sp**
模型与库文件	.inc .lib
运行状态文件	.st0
输出列表文件	.lis
测量输出文件	.m*#
瞬态分析文件	.tr#
直流分析文件	.sw#
交流分析文件	.ac#
其他文件	…

.sp文件示例

```
.TITLE F04 DELAY
.lib "C:\synopsys\tsmc\hspice\crn40lp_1d8_v2d0_2_shrink0d9_embedded_usage.l" TOP_TT
.OPTION POST
.GLOBAL VDD GND
.TEMP 25.0
.PARAM SUPPLY=1.1
.PARAM H=4
*
VDD VDD GND 'SUPPLY'
*
.SUBCKT INV A Y N=0.12u P=0.24u
xnmos Y A GND GND nch_mac W=N L=0.04u
xpmos Y A VDD VDD pch_mac W=P L=0.04u
.ENDS
*
X1 A B INV
X2 B C INV M='H'
X3 C D INV M='H**2'
X4 D E INV M='H**3'
X5 E F INV M='H**4'
X6 F G INV M='H**5'
*
*
VIN A GND PULSE 0 'SUPPLY' 50ps 10ps 10ps 230ps 500ps
*
.tran 1ps 10ns
.op all

.measure tpdrbc
+    TRIG v(b) VAL='SUPPLY/2' FALL=1
+    TARG v(c) VAL='SUPPLY/2' RISE=1
.measure dprfbc
+    TRIG v(b) VAL='SUPPLY/2' RISE=1
+    TARG V(c) VAL='SUPPLY/2' FALL=1
.end
```

- **文件标题**
- 引用库文件
- 分析及输出配置
- 子电路定义
- 元件描述
- 激励源
- 分析命令
- 输出命令
- 结束

.sp文件示例

```
1  .TITLE F04 DELAY
2  .lib "C:\synopsys\tsmc\hspice\crn40lp_1d8_v2d0_2_shrink0d9_embedded_usage.1" TOP_TT
3  .OPTION POST
4  .GLOBAL VDD GND
5  .TEMP 25.0
6  .PARAM SUPPLY=1.1
7  .PARAM H=4
8  *
9  VDD VDD GND 'SUPPLY'
10 *
11 .SUBCKT INV A Y N=0.12u P=0.24u
```

设置参数（温度、……）

定义子电路

```
12 xnmos Y A GND GND nch_mac W=N L=0.04u
13 xpmos Y A VDD VDD pch_mac W=P L=0.04u
14 .ENDS
35 .end
```

.sp文件示例

```
1  .TITLE F04 DELAY
2  .lib "C:\synopsys\tsmc\hspice\crn40lp_1d8_v2d0_2_shrink0d9_embedded_usage.l" TOP_TT
3  .OPTION POST
4  .GLOBAL VDD GND
5  .TEMP 25.0
6  .PARAM SUPPLY=1.1
7  .PARAM H=4
8  *
9  VDD VDD GND 'SUPPLY'
10 *
X1 A B INV
X2 B C INV M='H'
X3 C D INV M='H**2'
X4 D E INV M='H**3'
X5 E F INV M='H**4'
X6 F G INV M='H**5'
*
*
VIN A GND PULSE 0 'SUPPLY' 50ps 10ps 10ps 230ps 500ps
29 .measure tpdrbc
30 +   TRIG v(b) VAL='SUPPLY/2' FALL=1
31 +   TARG v(c) VAL='SUPPLY/2' RISE=1
32 .measure dprfbc
33 +   TRIG v(b) VAL='SUPPLY/2' RISE=1
34 +   TARG V(c) VAL='SUPPLY/2' FALL=1
35 .end
```

调用子电路模块

输入激励

- 文件标题
- 引用库文件
- 分析及输出配置
- 子电路定义
- 元件描述
- 激励源
- 分析命令
- 输出命令
- 结束

.sp文件示例

```
.TITLE F04 DELAY

.tran 1ps 10ns
.op all

.measure tpdrbc
+    TRIG v(b) VAL='SUPPLY/2' FALL=1
+    TARG v(c) VAL='SUPPLY/2' RISE=1
.measure dprfbc
+    TRIG v(b) VAL='SUPPLY/2' RISE=1
+    TARG V(c) VAL='SUPPLY/2' FALL=1

.tran 1ps 10ns
.op all

.measure tpdrbc
+    TRIG v(b) VAL='SUPPLY/2' FALL=1
+    TARG v(c) VAL='SUPPLY/2' RISE=1
.measure dprfbc
+    TRIG v(b) VAL='SUPPLY/2' RISE=1
+    TARG V(c) VAL='SUPPLY/2' FALL=1
.end
```

.tran 输出仿真波形在*.tr#中

输出测量结果在*.mt#中

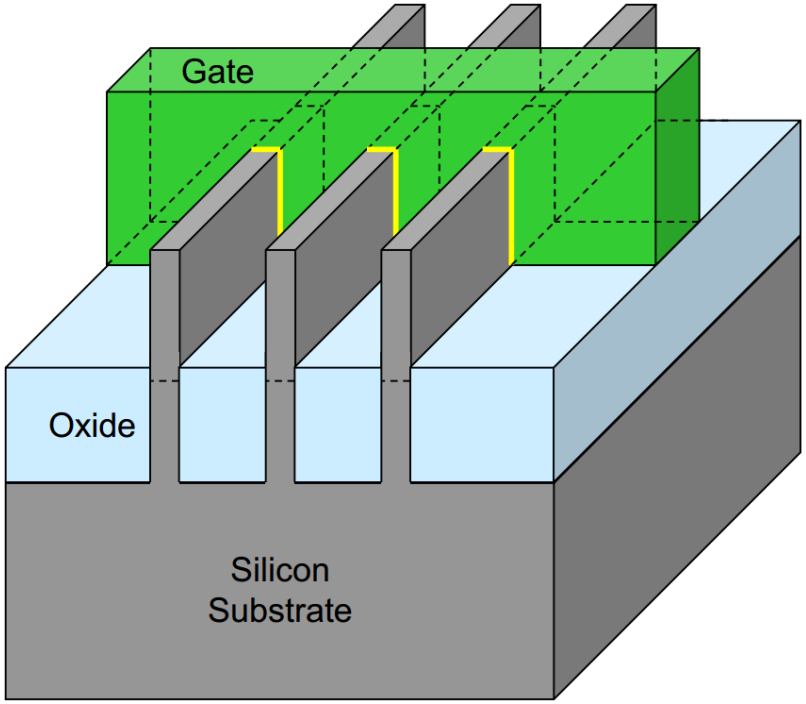
- 文件标题
- 引用库文件
- 分析及输出配置
- 子电路定义
- 元件描述
- 激励源
- 分析命令
- 输出命令
- 结束

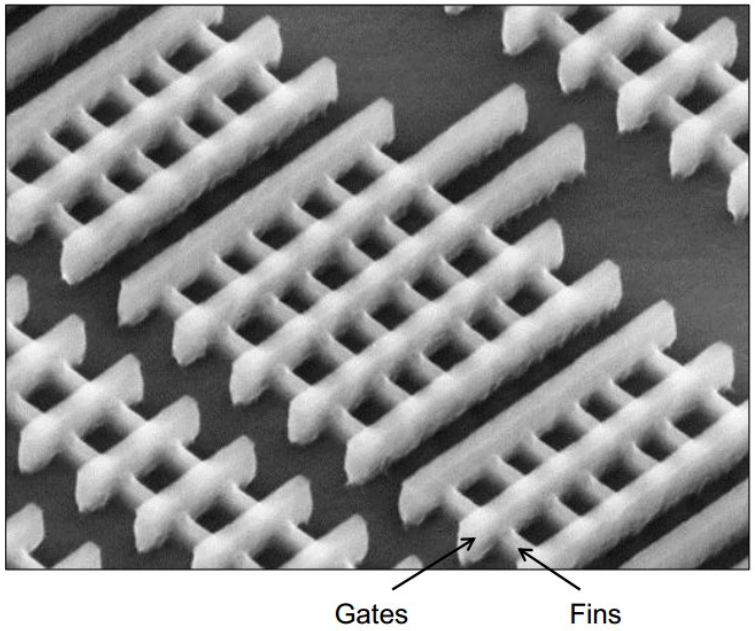
Outline

- 实验内容
  - 反相器链路设计
  - 七输入或门设计
- **实验工具**
  - Hspice
  - **FinFET**
- 实验材料和要求
- 附录

Tri-Gate Transistor with Multiple Fins

- Tri-Gate transistors can have multiple fins connected together to increase total drive strength for higher performance

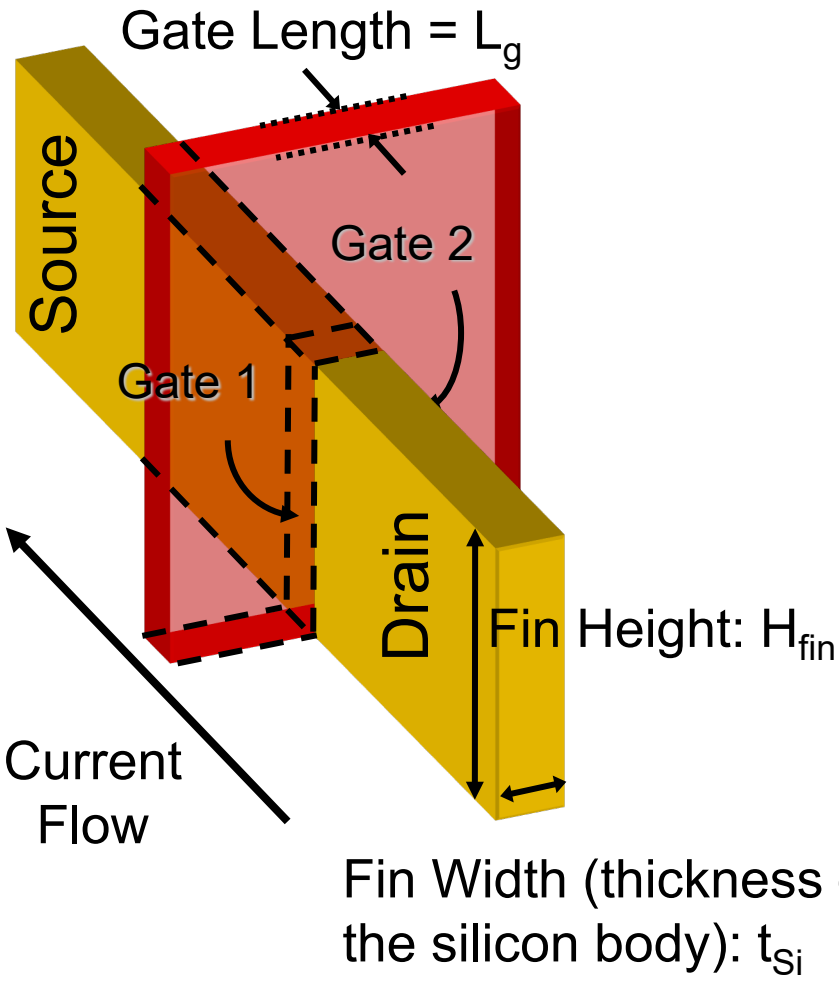




22nm Tri-Gate Transistors

Source: Intel

Width Quantization of FinFET



Single fin:

$$W_{min} = 2 \times H_{fin} + t_{si}$$

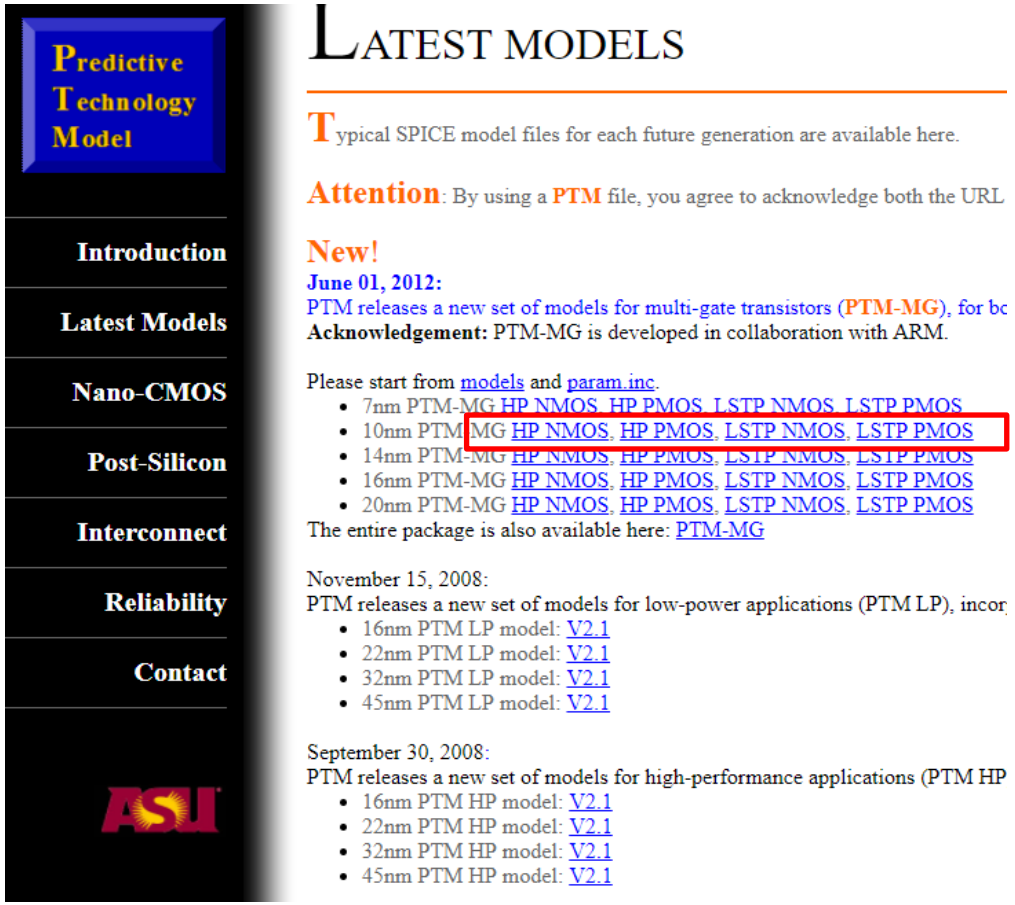
N fins:

$$W_{\text{total}} = n \times W_{min} = n \times \left(2 \times H_{fin} + t_{si}\right)$$

The width quantization of FinFETs introduces interesting design challenges in CMOS circuits whose performances are highly sensitive to transistor sizing

Models for Experiment

- Use the Predictive Technology Model (PTM) to evaluate the DC characteristics of multi-gate (MG) FinFETs



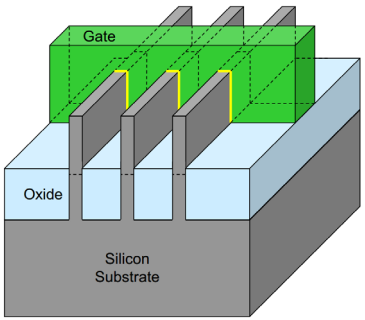
PTM Files

使用方式一：

- 直接下载相应的nmos，pmos模型文件10nfet.pm，10pfet.pm，include并使用：

```
.include '../modelfiles/lstp/10pfet.pm'
…
Mpfet d g s x pfet L=lg NFIN=nfin
```

- 其中，**nfin的值必须是整数**；
- 10nm的沟道长度一般选择lg=14n，工作电压0.75V；



PTM Files

使用方式二：

- 下载完整的PTM-MG模型库；
- 通过引用其中的models文件使用（models文件中的路径可能需要调整）：

```
.LIB "../PTM-MG/modelfiles/models" ptm10lstp
…
Xpfet d g s x pfet L=lg NFIN=nfin
```

Outline

- 实验内容
  - 反相器链路设计
  - 七输入或门设计
- 实验工具
  - Hspice
  - FinFET
- **实验材料和要求**
- 附录

实验材料

实验材料：

- Hspice虚拟机使用教程（使用前先看一下）：https://jbox.sjtu.edu.cn/l/F1Qm7h
- Hspice虚拟机 ： https://jbox.sjtu.edu.cn/l/61LhDT
- Hspice文档 ： https://jbox.sjtu.edu.cn/l/M1RJrd
- PTM模型 ： https://jbox.sjtu.edu.cn/l/W1Se7R

或者直接使用官方网址 http://ptm.asu.edu/

- **JBOX提取码 ： adic**
- **注：** 本次采用PTM中的 **ptm10lstp** 进行实验（在 **./models** 文件中定义），实验**温度均为85度**（.TEMP 85）

报告提交

报告内容：

- 各种指标**测量结果**、优化**设计方案**及结果**分析**（包含仿真结果、波形、数据分析图表）
- HSPICE网表文件（包含必要的注释，与报告内容合并为同一个pdf）

提交方式：

- 上传至CANVAS平台。
- 以 **学号_姓名_ADIC_lab1.pdf** 命名
- Deadline：**2022.4.12**

谢谢

2021

Outline

附录

- **Hspice使用方法**
- FinFET的优点
- FinFET基本参数测量
- Inverter基本参数测量

库文件&网表文件调用

调用工艺库文件

- **.lib “<filepath/>" filename**
- 本实验使用PTM 10nm(**ptm10lstp**)工艺，其工艺库文件下包含lstp与hp两个lib文件，分别针对低功耗与高性能
- 文件定义器件的参数模型
- 一般由foundary提供，对应有TT、SS、FF、SF、FS等工艺角，其他的D2D、mismatch模型

引用网表文件

- **.inc “<filepath/>” filename**
- 将常用、可重复使用的模块写成单独子电路形式以供不同电路中调用，便于模块化设计和验证

分析及输出配置

- .options ： 配置仿真参数及输出格式
  - *e.g.* .options post
- .temp ： 语句设置电路工作温度
  - *e.g.* .temp 85
- .global ： 设置全局节点
  - *e.g.* .global vdd gnd
- .param ： 设置全局变量
  - *e.g.* .param <paraname> = constant
- .ic .nodeset ： 设置仿真起始条件
  - *e.g.* .ic v(node1)=0.85
- .connect ： 设置多节点相连

仿真控制选项

.options 设置仿真及输出方式

- 输出控制类；
- 仿真精度类；
- 算法与收敛控制；
- 硬件资料配置类；
- 输入数据相关类；

语名	功能
.option post	输出高分辨率图形
.option post probe	仅输出probe指明变量
.option postlvl-0..6	将几级子电路内部节点输出
.option brief	输出文本省略某些内容
.option list	输出元器件列表
.option nomod	不输出模型库相关信息
.option dccap	DC仿真时计算C-V特性
.option runlvl=0..6	精度：6精度最高，0速度最快
.option scale=xxx	全局器件参数比例值
.option defl=0.18u	略省MOSFET沟道长度

子电路使用

子电路定义

```
.subckt inv in out l=20n nfinn=1 beta=2
Xmn1 out in gnd gnd nfet l=20n nfin=nfinn
Xmp1 out in vdd vdd pfet l=20n nfin='nfinn*beta'
.ends
```

子电路调用

- 定义子电路inv
- 有输入in、输出out两个端口
- 有l、nfinn、beta三个参数值
- 子电路的定义中包含子电路的调用

原件描述

Xnand ina inb out [xx] nfinn1=1 nfinp1=1
元件名 连接方式 模型名 元件参数

原件描述构成

- 元件名：第一个字母表示该元件的类型，不超过16个字符
- 连接方式：即为电路的接口节点
- 元件参数：指明元件的参数，可以用正负整数、浮点数以及指数，不写则为默认值
- 例子：MOSFET

关键字母	元件类型
R	电阻
C	电容
L	电感
M	MOSFET
Q	BJT
J	JFET or MESFET
D	Diode
X	子电路
W\T\U\S	其他多端口线性器件

Mxx nd ng ns nb 模型名 <W=w><L=l><AD=ad>
+<AS=as><PD=pd> <PS=ps><NRD=nrd>
+<NRS=nrs><OFF><IC=Vds、Vgs、Vbs初值>
一般只需要确定MOS管的长宽比即可：
e.g. M1 a b c VDD pfet W=0.42 L=0.2

激励源

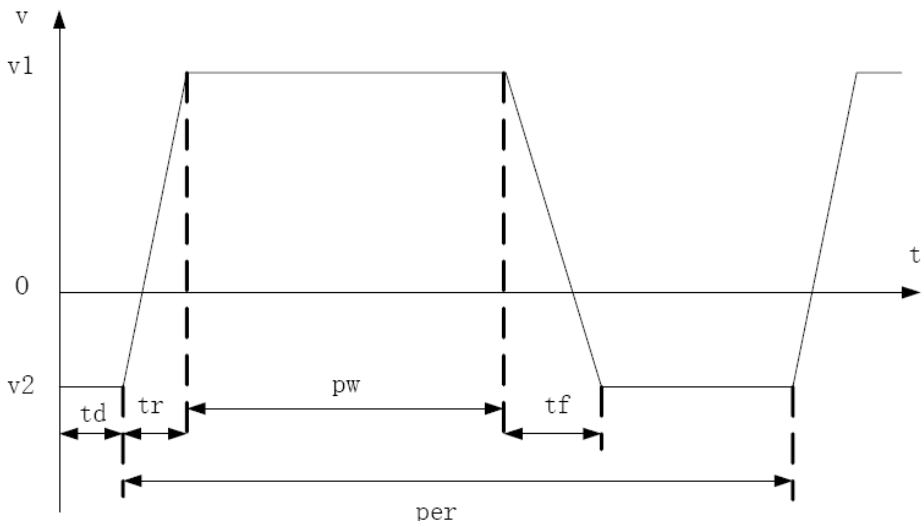
- 独立源分为直流源、交流源、瞬态源，分别在直流、交流、瞬态分析中起作用
- 可用混合源同时包含直流与交流
- 混合源示例：
  - 第一项为电源的直流值
  - 第二项为交流数据
  - 第三选项为瞬态数据

Vxx n+ n- <<DC>直流值>
+<AC<交流振幅<交流相位>>>
+<瞬态值>
e.g. VCC vcc 0 5 AC=10V, 90

关键字母	元件类型
V	独立电压源
I	独立电流源
E	压控电压源
F	流控电流源
G	压控电流源
H	流控电压源

瞬态源

- Trapezoidal pulse : pulse
- Sinusoidal : sin
- Exponential : exp
- Piecewise linear : pwl
- Single-frequency FM : sffm
- Single-frequency AM : am
- Pattern : pat



PULSE (v2 v1 td tr tf pw per)
e.g. VIN in 0 PULSE 0 5 2ns 2ns 2ns 30ns 80ns

直流分析控制

- .DC、.AC、.TRAN分析将自动进行直流操作点计算
- .DC　　：直流仿真
- .OP　　：直流操作点分析
- .PZ　　：零极点分析
- .SENS　：直流小信号敏感度分析
- .TF　　：直流小信号传输函数分析
- .nodeset：初始化仿真节点电压，加快收敛速度

```
.DC var1 start1 stop1 inc
+ <SWEEP var1 type np start2 stop2>
```

瞬态分析控制

- 仿真电路在时域的变化趋势
- .TRAN　：瞬态仿真
- .IC　　：为瞬态分析设置初始值

.tran tstep tstop1 <inc2 stop2 … incN stopN>
+<START=var><UIC><SWEEP …>
e.g. .TRAN 1ns 100ns UIC

注:

1）tstep为时间步长，tstop为瞬态分析的时间终值，tstart为瞬态分析的时间起始值，补缺值为0；

2）UIC表使用.IC设置的值作为仿真初始值，不进行OP计算

参数扫描

在直流、交流、瞬态分析中均可进行参数的扫描

- 扫描参数：
  - 定义扫描参数　.param beta=2
  - 在电路中引用参数　Mn1 d g s b nmos l=20n w='l*beta'
  - 在分析命令中指明参数扫描类型　.tran 10ps 10ns sweep beta 1.2 3 0.1
- 扫描数表、随机分布：
  - sweep <data=dataname/monte=count>
  - 数表定义：

```
.data dataname
+ pname1 pname2…
<data1 data2 …>
…
.enddata
```

关键字	扫描类型
LIN	线性（缺省）
DEC	十倍增量
OCT	二倍增量
POI	指定点

输出控制

.PRINT

- 规定.lis中打印的变量值
- *e.g.* .print I(*) V(*) P(*) var=par('I(node)*V(node)')

.PLOT

- 将选定结果在.lis中绘图输出
- *e.g.* .plot anytype var<(plo1,pli1)>…

.PROBE

- 将变量存储到接口文件和图像数据文件中，不打印

.GRAPH

- 生成一高分辨率的绘图结果

.MEASURE

- 对选定结果进行测量，得到精确值，可做积分、微分、表达式运算（AVG / RMS / MIN / MAX）

MEASURE语句

测量延迟

- .MEASURE <DC|AC|TRAN> result TRIG… TARG…
- *e.g.* .MEASURE TRAN td TRIG vin val='supply/2' RISE=2 TARG vout +val='supply/2' RISE=2

测量功耗

- .MEASURE <DC|AC|TRAN> result func out_var FROM=val +TO=val
- *e.g.* TRAN avgpower AVG P(VDD) FROM=1ns TO=80ns

测量阈值电压

- .MEASURE <DC|AC|TRAN> result 条件
- *e.g.* .MEASURE TRAN vth FIND Vgs WHEN I(nmos)='0.1u*width'

Outline

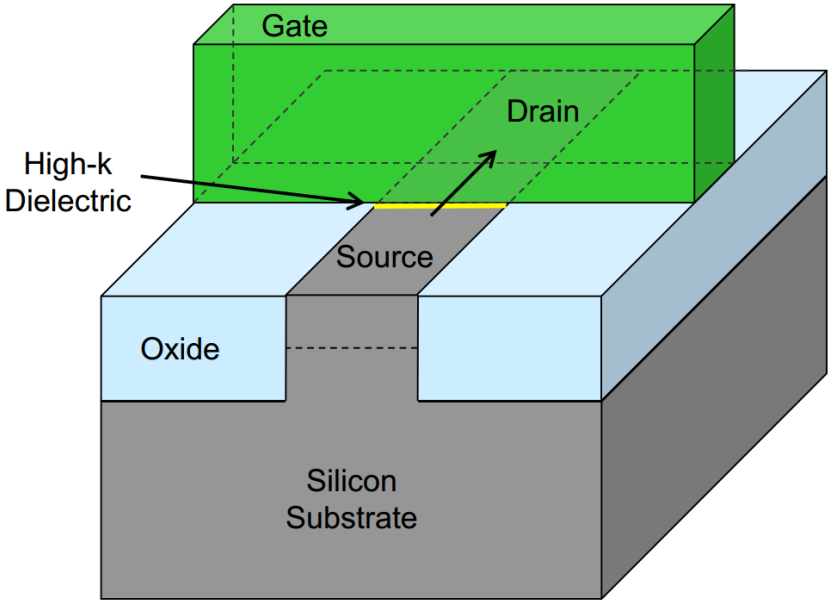
附录

- Hspice使用方法
- **FinFET的优点**
- FinFET基本参数测量
- Inverter基本参数测量

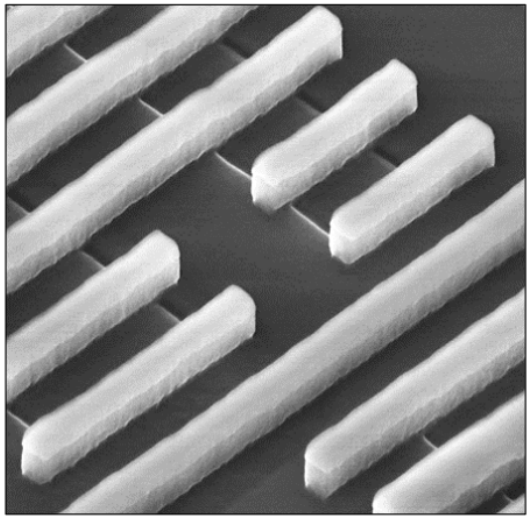
Traditional Bulk Silicon Transistor

- 2D structure
- Conducting channel only on the surface

As the channel length decreases, the gate control over the channel of device is reduced



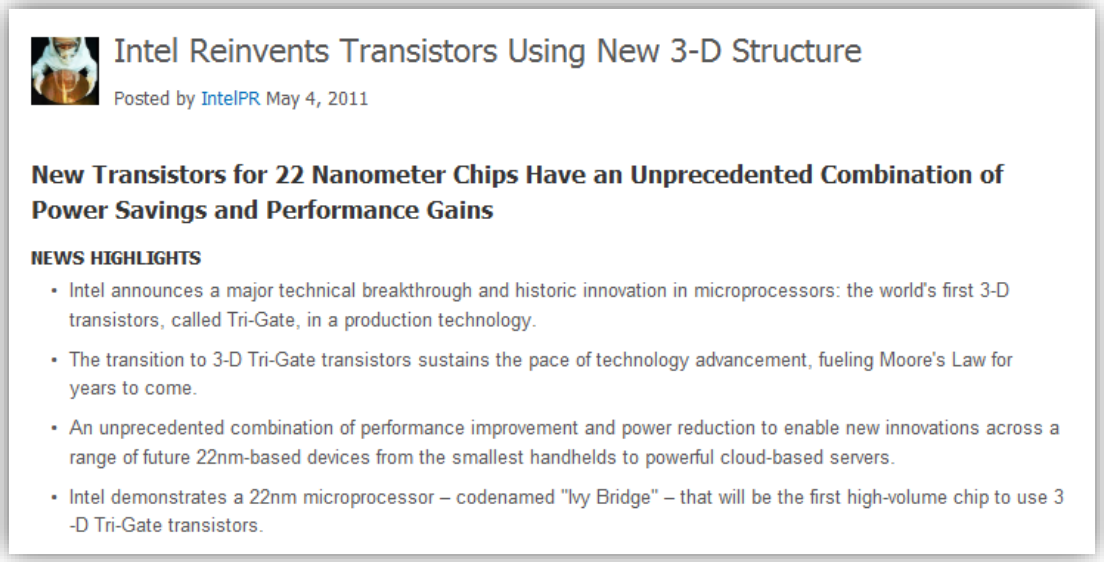
Source: Intel



32nm Planar Transistors

The End of the 2D Planar Transistor

- On May 4, 2011, Intel Corporation announced what it called the most radical shift in semiconductor technology in 50 years
- The new 3D Tri-Gate transistors enable the production of integrated-circuit chips that operate faster with less power



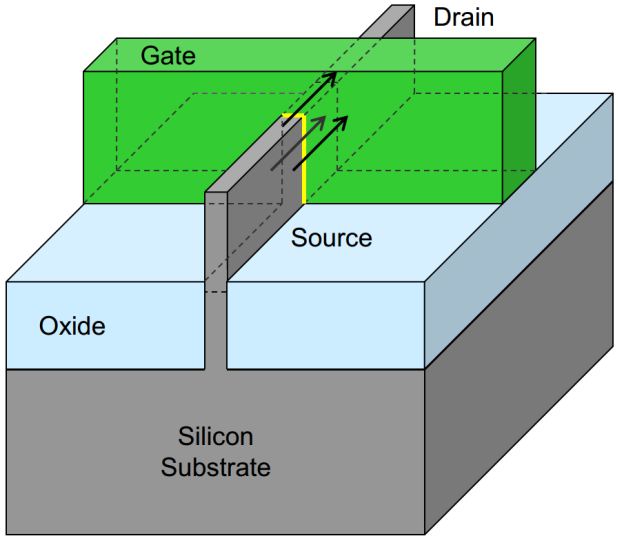
Intel Reinvents Transistors Using New 3-D Structure

Posted by IntelPR May 4, 2011

New Transistors for 22 Nanometer Chips Have an Unprecedented Combination of Power Savings and Performance Gains

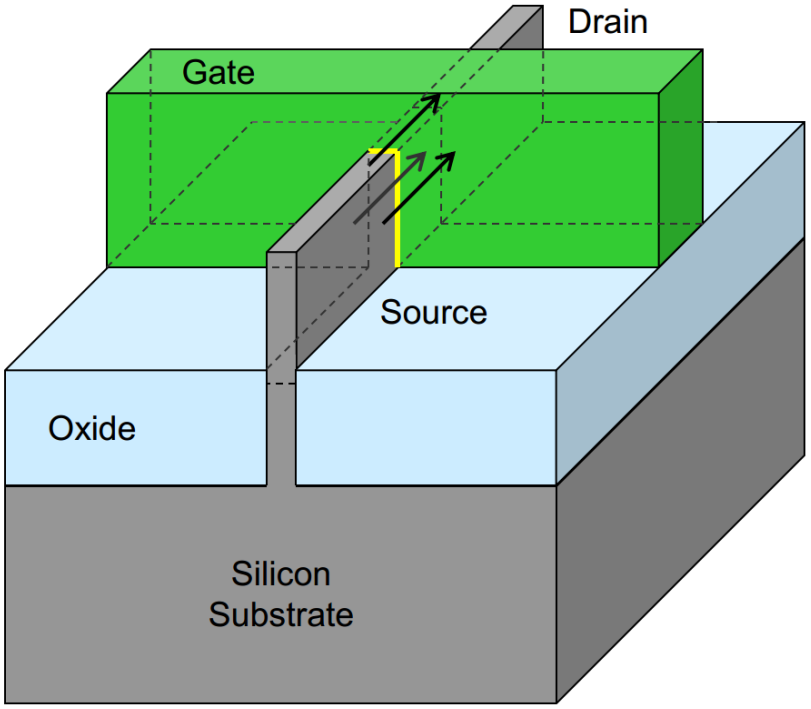
NEWS HIGHLIGHTS

- Intel announces a major technical breakthrough and historic innovation in microprocessors: the world's first 3-D transistors, called Tri-Gate, in a production technology.
- The transition to 3-D Tri-Gate transistors sustains the pace of technology advancement, fueling Moore's Law for years to come.
- An unprecedented combination of performance improvement and power reduction to enable new innovations across a range of future 22nm-based devices from the smallest handhelds to powerful cloud-based servers.
- Intel demonstrates a 22nm microprocessor – codenamed "Ivy Bridge" – that will be the first high-volume chip to use 3 -D Tri-Gate transistors.



Tri-Gate Transistor

- 3-D Tri-Gate transistors form conducting channels on three sides of a vertical fin structure, providing "fully depleted" operation

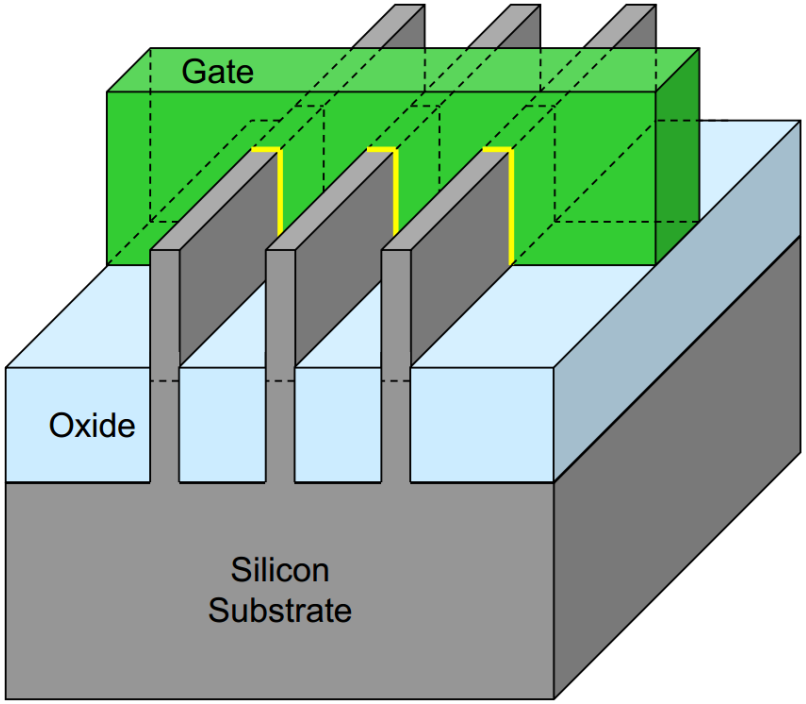


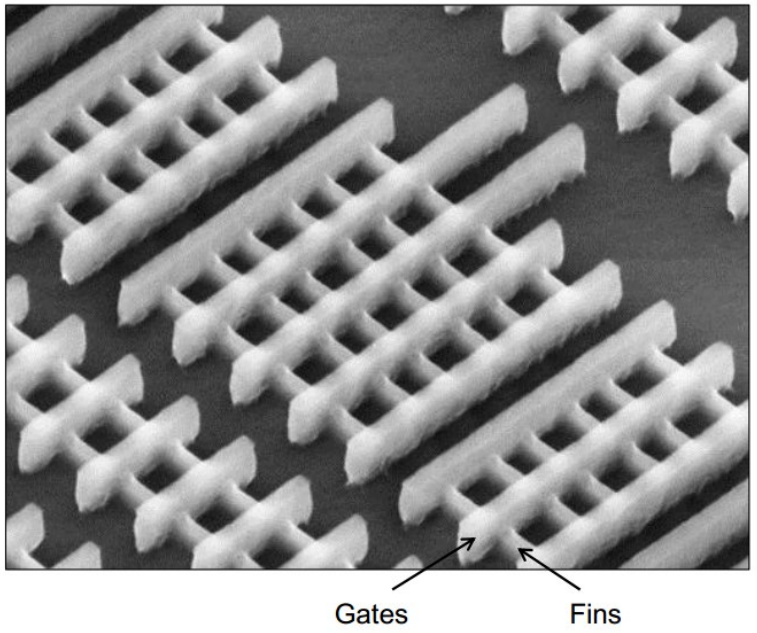
- ✓ 3D structure
- ✓ Conducting channel on three sides
- ✓ Very little leakage

Transistors have now entered the third dimension!

Tri-Gate Transistor with Multiple Fins

- Tri-Gate transistors can have multiple fins connected together to increase total drive strength for higher performance

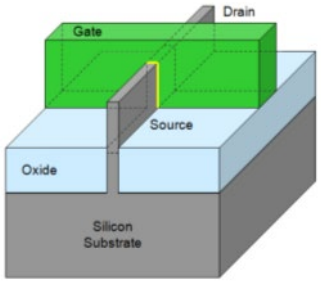


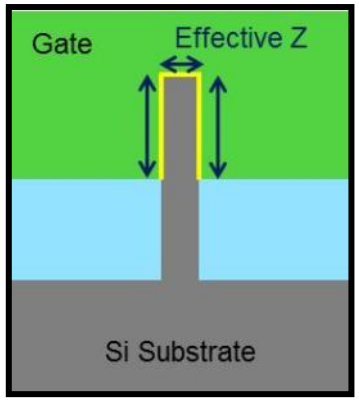


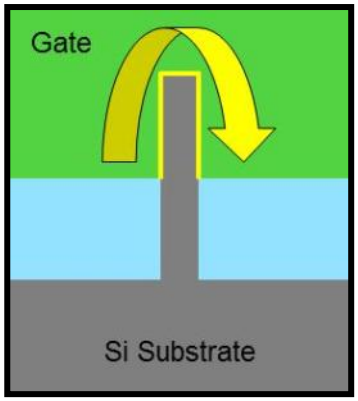
22nm Tri-Gate Transistors

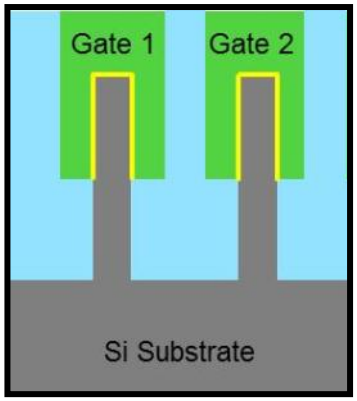
Source: Intel

3D Transistor (Tri-Gate and FinFET) Advantage Summary









Intel's 22 nm Tri-Gate Technology

Higher Effective Channel Width

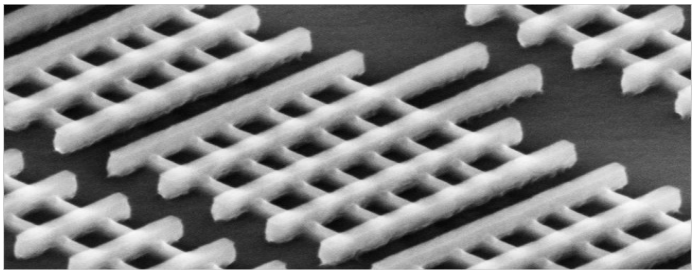
> 2X Core Performance

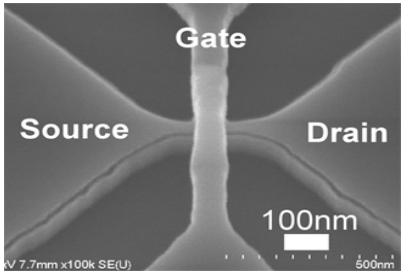
Lower Leakage Current

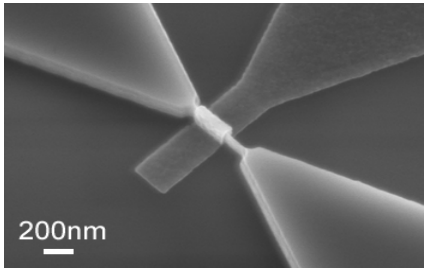
> 50% Power Reduction

Allows smaller junction sizes

Higher Densities



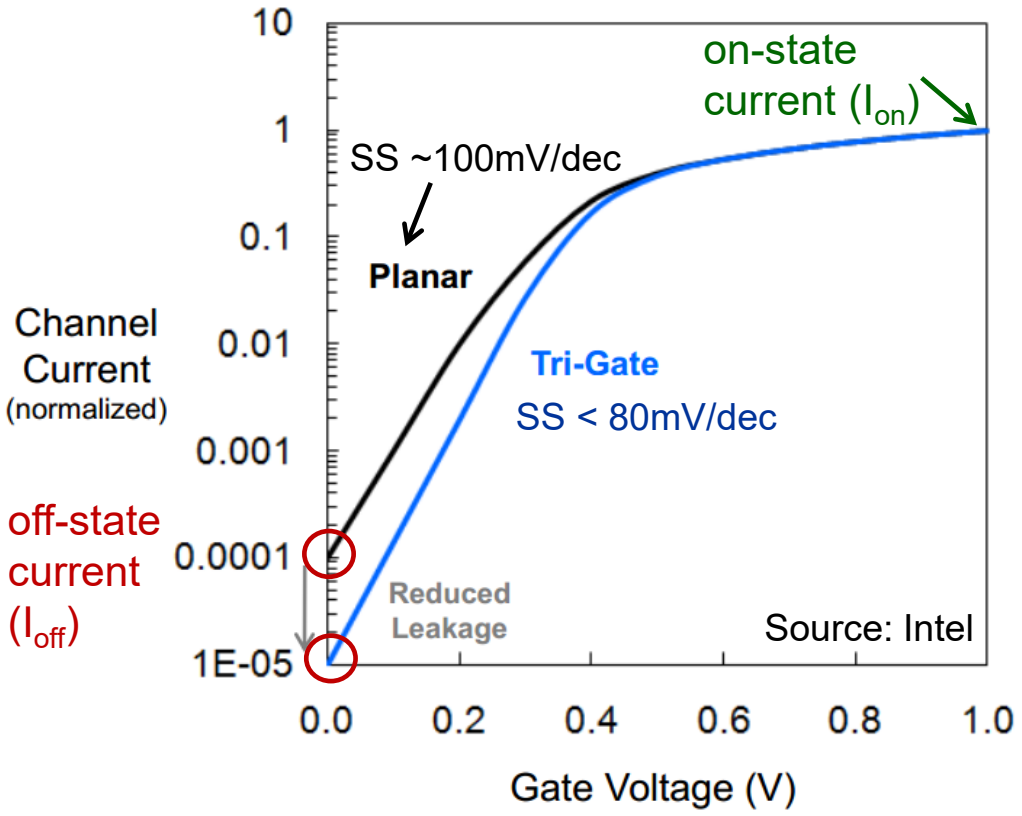




http://www.intel.sg/content/www/xa/en/silicon-innovations/standards-22-nanometers-technology-backgrounder.html?wapkw=22nm+logic+technologies

Transistor Current-Voltage Characteristics

- Tri-Gate transistor provides a steeper subthreshold slope (SS) that reduces leakage current
  - SS indicates how effectively a transistor can be turned off when V_{GS} is decreased below V_{th}
  - Lower subthreshold slope is desirable for achieving lower subthreshold leakage current



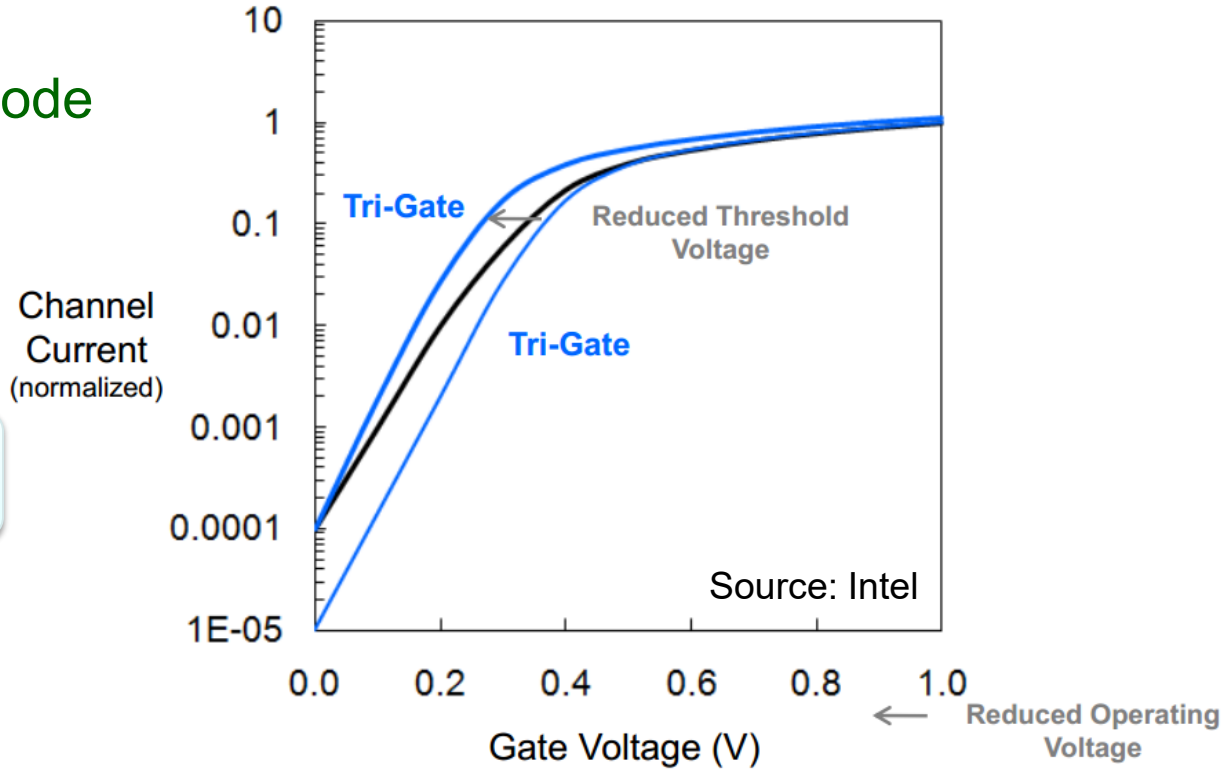
Improved SS: Better Low-Voltage Performance

- The steeper (lower) subthreshold slope allows for lower Vth for the same Ioff, allowing the transistors to operate at lower voltage to reduce power and improve switching speed

⇩

Key for advanced node V_{DD} scaling

$$\text{Power} \propto C*V_{DD}^2$$



Outline

附录

- Hspice使用方法
- FinFET的优点
- **FinFET基本参数测量**
- Inverter基本参数测量

I_{on} & I_{off}

- Take the n-channel device as an example:
  - The on-state current (I_{on}) is measured when:
    - $V_{gs} = V_{DD}$
    - $V_{ds} = V_{DD}$
  - The off-state current (I_{off}) is measured when:
    - $V_{gs} = 0$
    - $V_{ds} = V_{DD}$

Threshold Voltage (V_t)

- Constant current method defines threshold as the gate voltage at a given drain current I_{crit}
  - A typical choice of I_{crit} is 0.1uA×(W/L)
  - You can also determine a reasonable I_{crit}

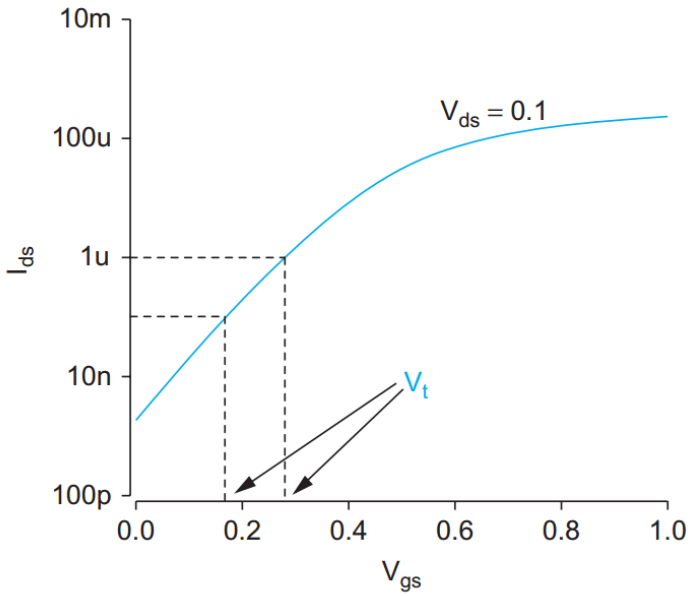
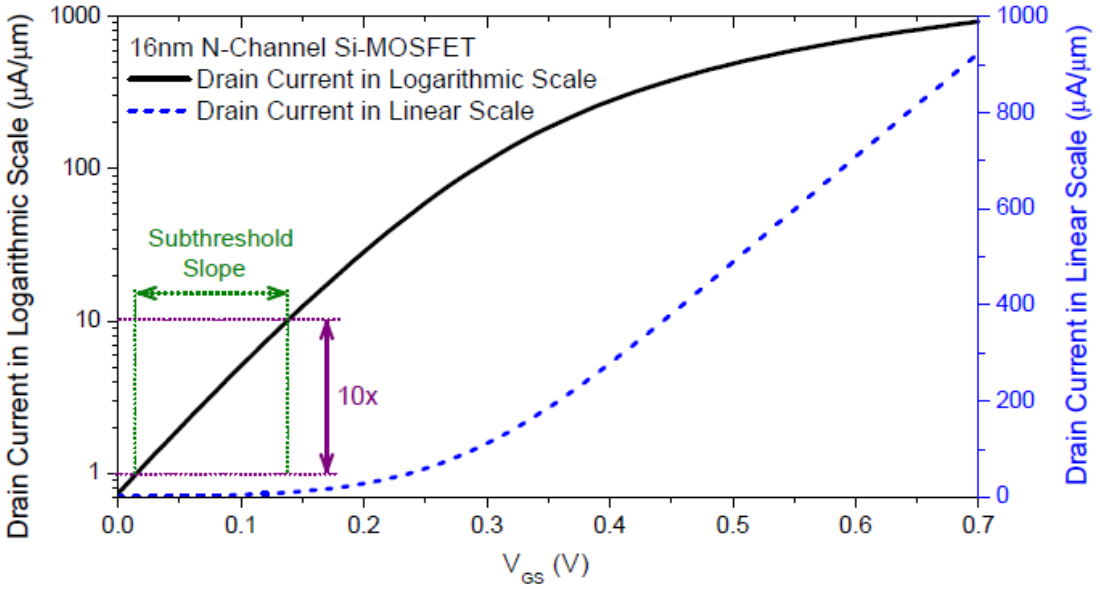


FIGURE 8.19 Constant current threshold voltage extraction method

Subthrehold Slope (SS)

- According to the definition, you can:
  - Find the V_{gs} when I_{ds}= 0.1uA×(W/L) ,denoted by V_1
  - Find the V_{gs} when I_{ds}= 0.01uA×(W/L) ,denoted by V_2
  - The subthreshold slope (SS) = V1-V2;

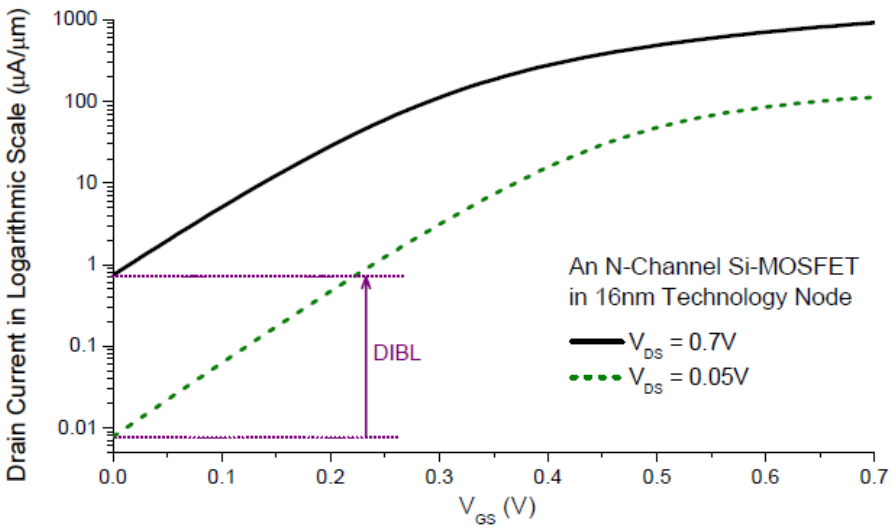


Drain Induced Barrier Lowering (DIBL)

DIBL can be calculated as following:

$$DIBL = \frac{|\delta V_t|}{|\delta V_{DS}|} = \frac{|V_t(V_{DS2}) - V_t(V_{DS1})|}{|V_{DS2} - V_{DS1}|}$$

- $V_t(V_{DS2})$ is the threshold voltage that is measured at a high drain voltage (typically $V_{DS2} = V_{DD}$)
- $V_t(V_{DS1})$ is the threshold voltage that is measured at a very low drain voltage (typically $V_{DS1} = 0.05V$)



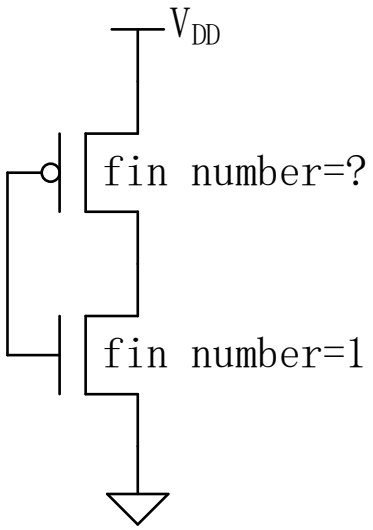
Outline

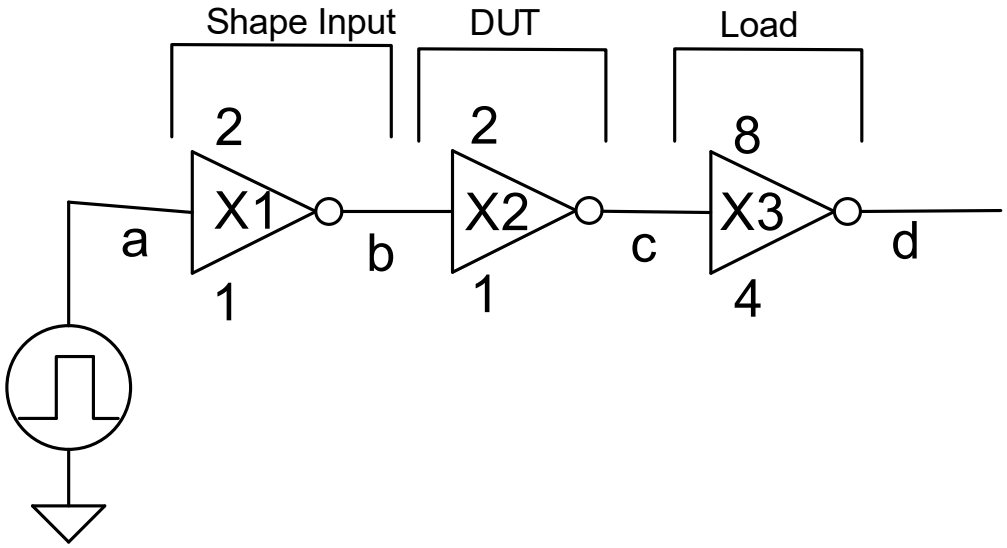
附录

- Hspice使用方法
- FinFET的优点
- FinFET基本参数测量
- **Inverter基本参数测量**

最小反相器设计

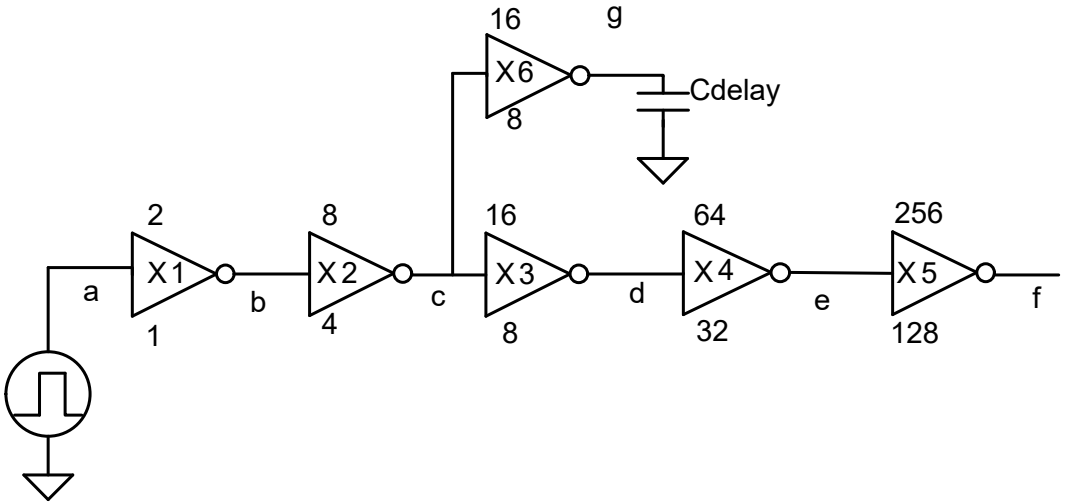
- 固定NMOS fin number为1，确定PMOS的fin number：
  - 使得t_{pHL}和t_{pLH}基本相同；





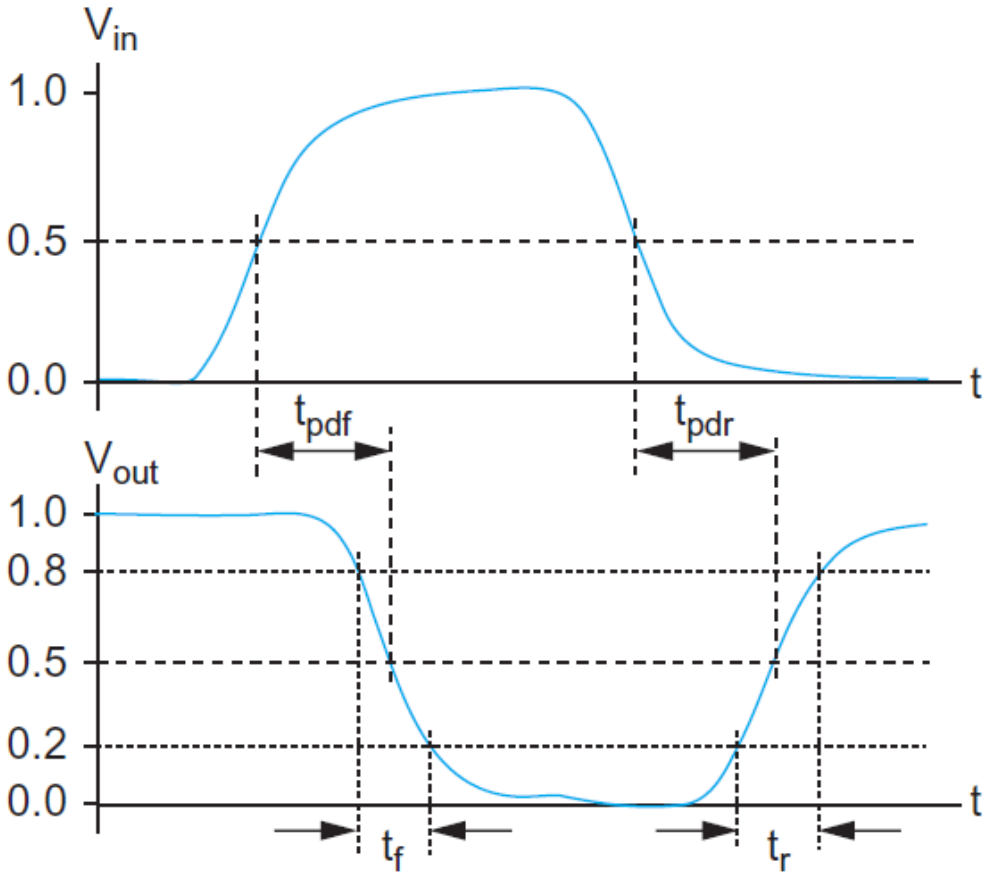
反相器门电容测量

- 测量门电容方法：
  - 扫描Cdelay的值，使c->g的延迟基本与c->d延迟相等；
  - 此时Cdelay的值就等于X4反相器的门电容；
  - 仿真方法详细介绍和代码示例在如下引用书籍的8.4.3章节处；



t_p测量方法

$$t_p = \frac{t_{pLH} + t_{pHL}}{2}$$



PDP&EDP 测量方法

- power delay product (PDP)描述每次开关事件平均消耗的能量：
  - 使用一段时间的平均功耗乘以总时间，再除以开关的次数
- Energy delay product (EDP)：
  - $EDP = PDP \times t_p$