SHANGHAI JIAO TONG UNIVERSITY

研究生课程实验报告

GRADUATE COURSE PROJECT REPORT

课 程： 高等数字电路设计

报告题目： Lab 1 Inverter chain & OR7 design

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# 实验目的

试验一中分为两个部分，分别为反相器链路设计与七输入或门设计。运用所学理论知识，完成CMOS工艺数字集成电路的设计，并用 HSPICE软件验证电路设计的正确性。加深对 MOS晶体管理论、CMOS数字电路的理解，掌握MOS晶体管尺寸调整对时序电路性能参数影响的规律，设计正确的数字缓冲器电路。

# 实验要求

采用所学过的 CMOS数字集成电路结构，分别设计反相器链路与七输入或门，满足下列指标（采用10nm FinFET工艺，栅极长度采用默认值lg为14nm，宽度为最小宽度整数倍数，电源电压0.75V）：

## 2.1 反相器链路要求

固定标准电压（PTM 10nm: 0.75V）的情况下，设计适当的级数和尺寸，保证反相器输出上升下降速度基本相等的情况下，优化；除此之外，在满足之前的情况下，确定EDP最优的工作电压。

## 2.2 七输入或门要求

进行结构上的选取（多级，动静态，…）,设计工作在标准电压（PTM 10nm: 0.75V）的七输入或门，平均延迟、面积、功耗都要优于参考电路，如下图所示。

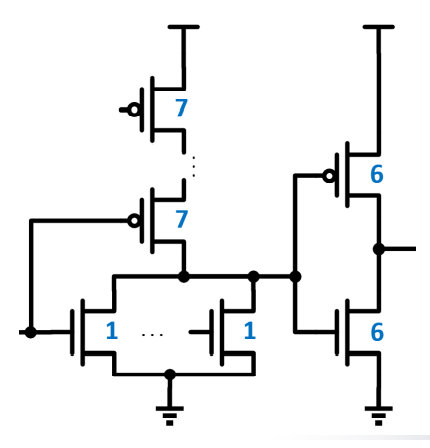


图 1 七输入或门参考电路

# 实验流程

## 3.1 反相器链路设计流程

### 3.1.1 模型

反相器链路如下图所示，其中输入负载为最小尺寸反相器，输出负载为150倍最小尺寸反相器(扇出为4)，设计的内容即为需要确定链路的级数N和每一级反相器的大小，即NFIN的数值。设计的前提需要尽量保证反相器输出上升下降速度基本相等，即= 。

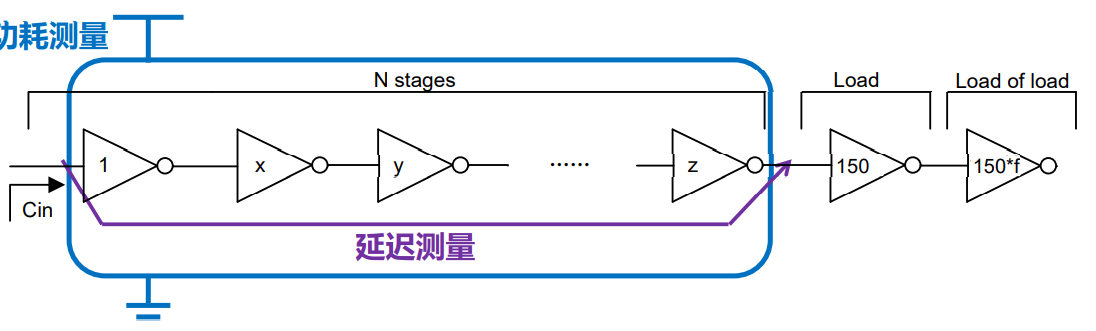


图 2 反相器链路模型

### 3.1.2 参数计算

计算反相器链路延时，满足，为使最小，得到，当γ约等于1时，最优解约为3.6。为了得到N，求解,其中 ,对于本次实验的链路来说，F=150，代入公式后可以计算得到N=3.912，所以最终取N=4，即为四级的反相器链路，每级的等效扇出为3.6。

### 3.1.3 结果分析

设计4级反相器链路，NFIN的数值大小依据大小分别为1、4、13和47，将得到的参数代入实际的电路中。测量连接相同负载的情况下，使用1级反相器链路、2级反相器链路、3级反相器链路、4级反相器链路的延时特性，结果如下表所示，通过合理的尺寸和级数设计可以大幅度减小延时。

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | **()** |  |  |
| **1级反相器链路** | 1.146e-10 | 1.088e-10 | 1.117e-10 | 5.18% |
| **2级反相器链路** | 3.354e-11 | 3.218e-11 | 3.286e-11 | 4.14% |
| **3级反相器链路** | 2.109e-11 | 2.048e-11 | 2.079e-11 | 2.93% |
| **4级反相器链路** | 2.059e-11 | 2.090e-11 | 2.075e-11 | 1.49% |

表 1 延时测量

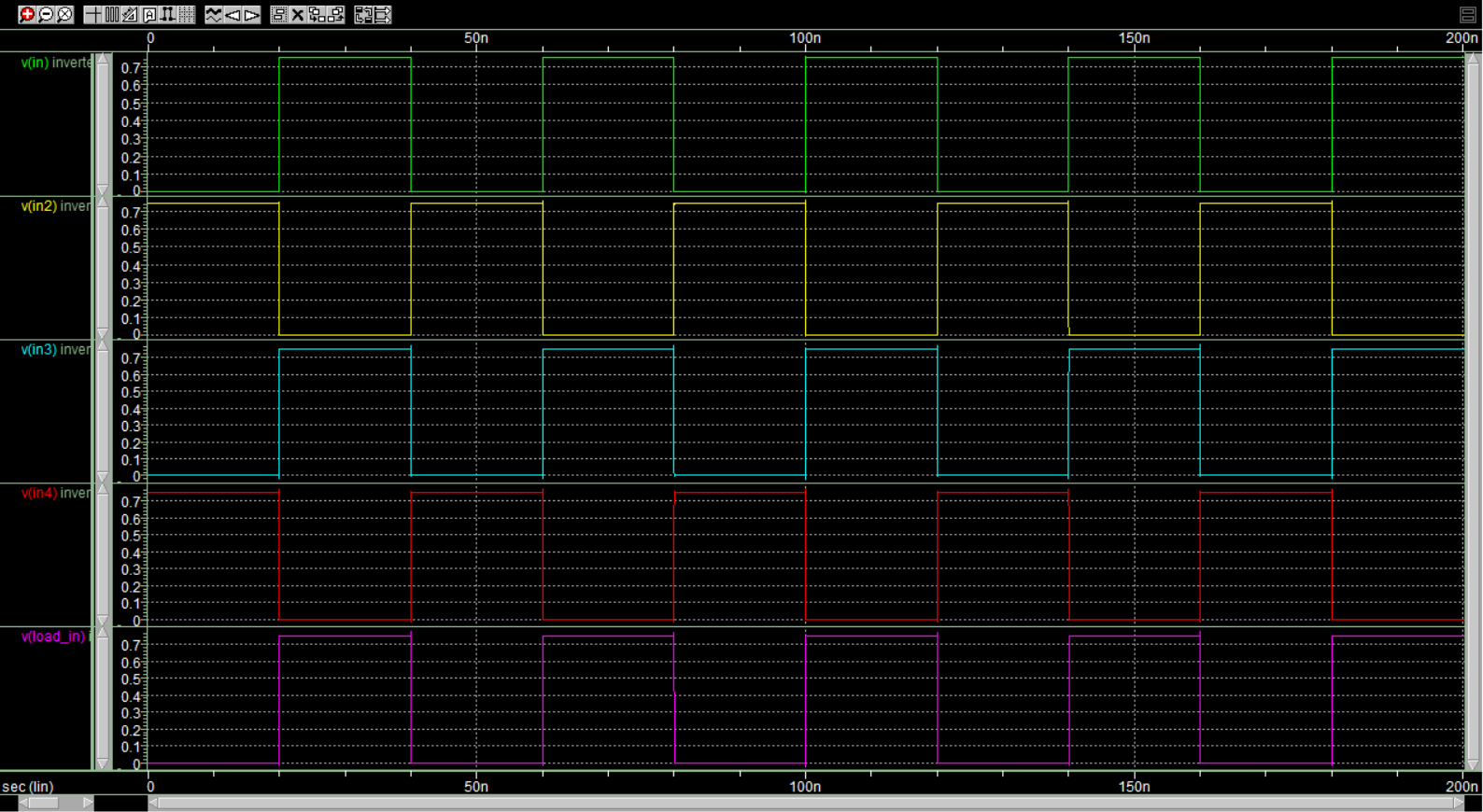


图 3 各节点波形。in，输入激励；in2，1级反相器的输出/2级反相器的输入；in3，2级反相器的输出/3级反相器的输入；in4，3级反相器的输出/4级反相器的输入；load\_in，4级反相器的输出/负载电路的输入。



图 4 上升延迟

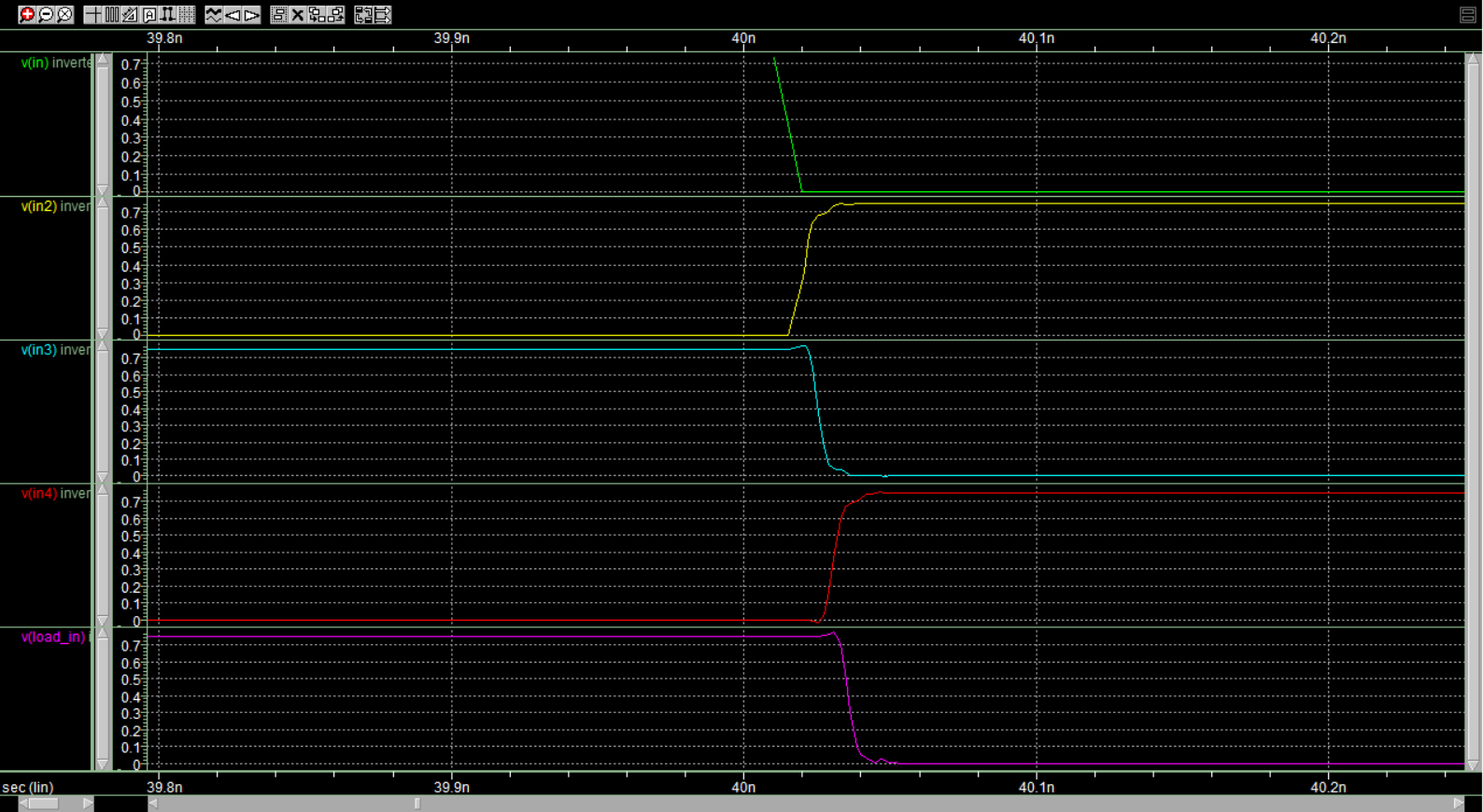


图 5 下降延迟

实验的第二部分对的降低，得到的EDP与的变化如下图所示。当为0.68V至0.69V之间可能出现最小值，在此区间以更小的步长进行扫描，如下表所示。

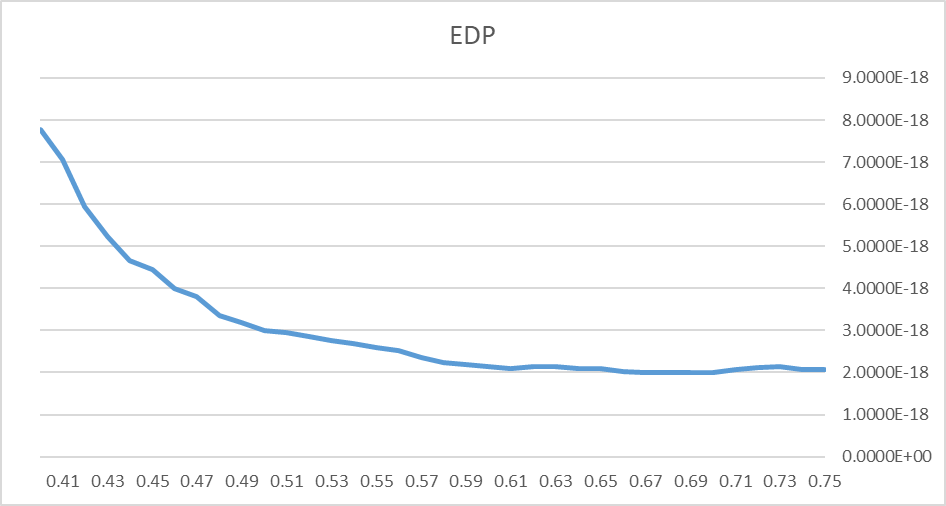


图 6 EDP-VDD

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| ***Vdd*** |  | **()** | **()** | **power(W)** | **EDP** |
| 0.689 | 2.4100E-11 | 2.4420E-11 | 2.4260E-11 | 8.2313E-08 | 1.9969E-18 |
| 0.688 | 2.4170E-11 | 2.4490E-11 | 2.4330E-11 | 8.2048E-08 | 1.9962E-18 |
| 0.687 | 2.4240E-11 | 2.4560E-11 | 2.4400E-11 | 8.1801E-08 | 1.9959E-18 |
| 0.686 | 2.4310E-11 | 2.4630E-11 | 2.4470E-11 | 8.1527E-08 | 1.9950E-18 |
| 0.685 | 2.4390E-11 | 2.4710E-11 | 2.4550E-11 | 8.1269E-08 | 1.9952E-18 |
| 0.684 | 2.4460E-11 | 2.4780E-11 | 2.4620E-11 | 8.1043E-08 | 1.9953E-18 |
| 0.683 | 2.4530E-11 | 2.4860E-11 | 2.4695E-11 | 8.0778E-08 | 1.9948E-18 |
| 0.682 | 2.4610E-11 | 2.4930E-11 | 2.4770E-11 | 8.0540E-08 | 1.9950E-18 |
| 0.681 | 2.4680E-11 | 2.5010E-11 | 2.4845E-11 | 8.0293E-08 | 1.9949E-18 |
| 0.68 | 2.4760E-11 | 2.5080E-11 | 2.4920E-11 | 8.0068E-08 | 1.9953E-18 |
| 0.679 | 2.4840E-11 | 2.5160E-11 | 2.5000E-11 | 7.9842E-08 | 1.9961E-18 |
| 0.678 | 2.4910E-11 | 2.5240E-11 | 2.5075E-11 | 7.9615E-08 | 1.9963E-18 |
| 0.677 | 2.5000E-11 | 2.5320E-11 | 2.5160E-11 | 7.9389E-08 | 1.9974E-18 |
| 0.676 | 2.5080E-11 | 2.5400E-11 | 2.5240E-11 | 7.9161E-08 | 1.9980E-18 |
| 0.675 | 2.5160E-11 | 2.5480E-11 | 2.5320E-11 | 7.8944E-08 | 1.9989E-18 |
| 0.674 | 2.5240E-11 | 2.5560E-11 | 2.5400E-11 | 7.8728E-08 | 1.9997E-18 |
| 0.673 | 2.5320E-11 | 2.5640E-11 | 2.5480E-11 | 7.8520E-08 | 2.0007E-18 |
| 0.672 | 2.5380E-11 | 2.5720E-11 | 2.5550E-11 | 7.8303E-08 | 2.0006E-18 |
| 0.671 | 2.5450E-11 | 2.5810E-11 | 2.5630E-11 | 7.8098E-08 | 2.0017E-18 |

表 2 最小EDP

最终得到，在0.683 V时对应的EDP最低。

## 3.2 七输入或门设计流程

七输入或门设计，其中输入负载为最小尺寸反相器，输出负载为32倍最小尺寸反相器(扇出为4)。

### 3.2.1 参考七输入或门电路性能指标

电路模型和尺寸如下图所示。

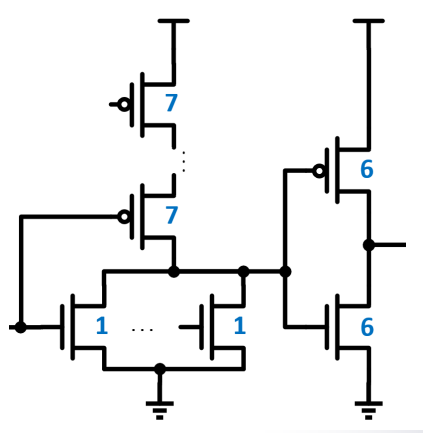


图 7 参考七输入或门电路模型和尺寸

按照实验要求，对不同的input data pattern的测量单次翻转的延时和动态功耗，并求平均值。测量结果如下表所示。平均延时，平均功耗。由于采用FinFET搭建电路，整个电路的面积正比于鳍的数量。

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **输入负载激励** | |  | | **()** | **()** | **power(W)** |
| 1111111<=>1111110 | | 2.3930E-11 | | 1.9000E-11 | 2.1465E-11 | 5.3450E-08 |
| 1111111<=>1111101 | | 2.6750E-11 | | 2.1880E-11 | 2.4315E-11 | 5.6160E-08 |
| 1111111<=>1111011 | | 2.9230E-11 | | 2.4190E-11 | 2.6710E-11 | 5.9220E-08 |
| 1111111<=>1110111 | | 3.1010E-11 | | 2.6140E-11 | 2.8575E-11 | 6.1270E-08 |
| 1111111<=>1101111 | | 3.3140E-11 | | 2.7780E-11 | 3.0460E-11 | 6.3650E-08 |
| 1111111<=>1011111 | | 3.5180E-11 | | 2.9160E-11 | 3.2170E-11 | 6.5610E-08 |
| 1111111<=>0111111 | | 3.6730E-11 | | 3.0340E-11 | 3.3535E-11 | 6.9190E-08 |
| **鳍数量** | 68 | | **平均值** | | 2.8176E-11 | 6.1221E-08 |

表 3参考七输入或门电路的性能指标

### 3.2.2 多级七输入或门电路性能指标

将七输入或门拆分为两级，第一级包含两个二输入与非门、一个三输入与非门，每个门的输出通过反相器输入到第二级；第二级为一个三输入与非门，最后的反相器不再是最小尺寸，根据负载对尺寸进行调整。结构如下图所示。

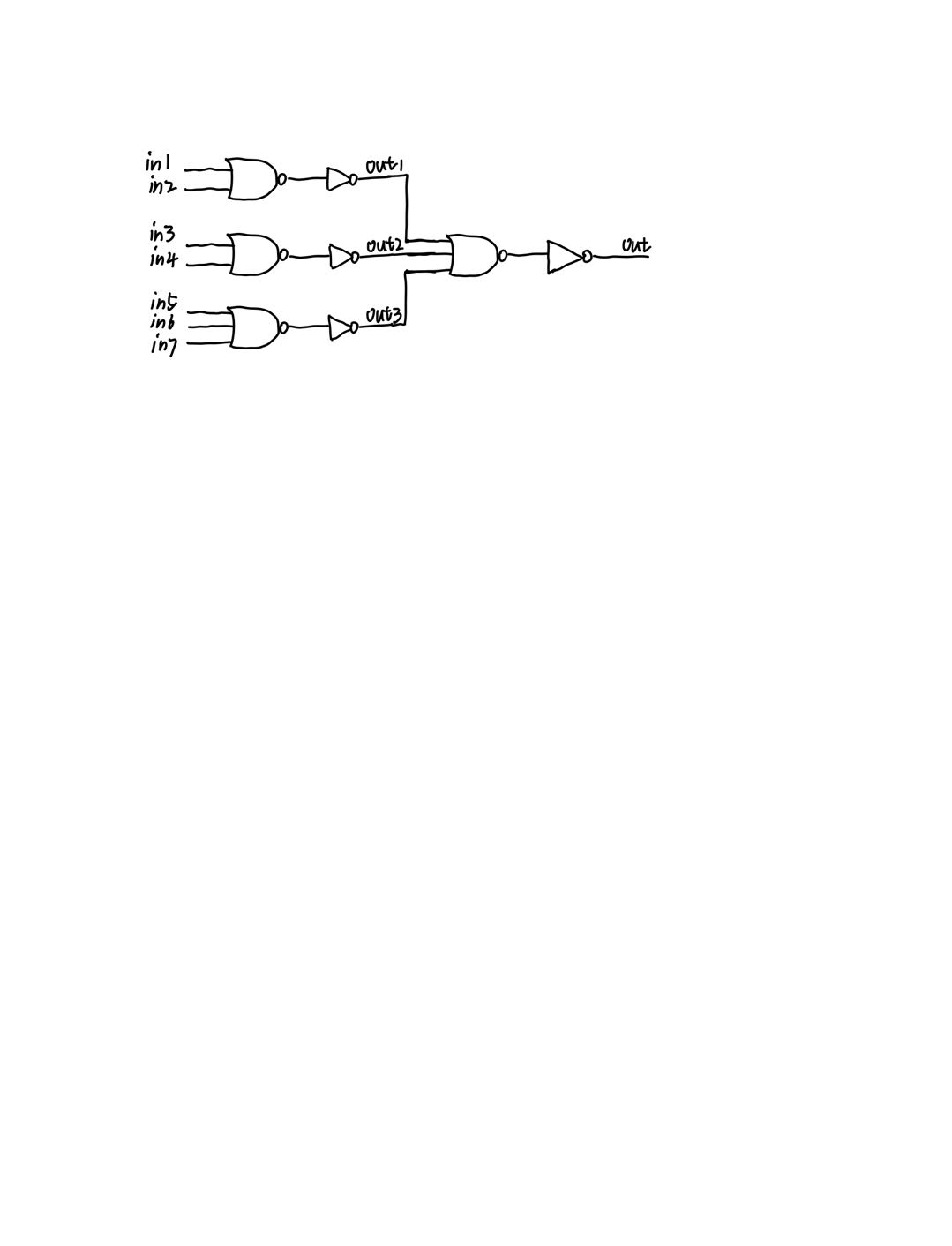


图 8多级七输入或门

第一级反相器均为最小尺寸，PMOS和NMOS的尺寸大小均为1。二输入与非门，PMOS的尺寸大小为2，NMOS的尺寸大小为1。三输入与非门，PMOS的尺寸大小为3，NMOS的尺寸大小为1。第二级反相器，PMOS的尺寸大小为4，NMOS的尺寸大小为3。性能指标入下表所示。

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **输入负载激励** | |  | | **()** | **()** | **power(W)** |
| 1111111<=>1111110 | | 2.3100E-11 | | 2.2870E-11 | 2.2985E-11 | 5.3150E-08 |
| 1111111<=>1111101 | | 2.3710E-11 | | 2.3690E-11 | 2.3700E-11 | 5.3970E-08 |
| 1111111<=>1111011 | | 2.4090E-11 | | 2.3920E-11 | 2.4005E-11 | 5.4140E-08 |
| 1111111<=>1110111 | | 2.4700E-11 | | 2.4760E-11 | 2.4730E-11 | 5.4940E-08 |
| 1111111<=>1101111 | | 2.6350E-11 | | 2.5730E-11 | 2.6040E-11 | 5.5670E-08 |
| 1111111<=>1011111 | | 2.7390E-11 | | 2.6820E-11 | 2.7105E-11 | 5.6690E-08 |
| 1111111<=>0111111 | | 2.8410E-11 | | 2.7810E-11 | 2.8110E-11 | 5.7750E-08 |
| **鳍数量** | 49 | | **平均值** | | 2.5239E-11 | 5.5187E-08 |

表 4多级七输入或门电路的性能指标

在面积和平均功耗均低于参考七输入或门电路的情况下，实现了更低的平均延时。

### 3.2.3 pseudo-NMOS七输入或门电路性能指标

电路结构如下图所示。pseudo-NMOS七输入或非门为有比逻辑，out节点的逻辑1为电压值为，逻辑0的电压值与PMOS和NMOS的电阻值有关。为了保证后面输出反相器的延时不至于过大，七输入或非门输出逻辑0的电压值应该尽可能趋向于0，即NMOS的尺寸应该大于PMOS。可以预见的是，当out节点输出为逻辑0时，存在到地的导电通路，势必造成功耗的上升，应尽可能选择小尺寸的PMOS的NMOS。

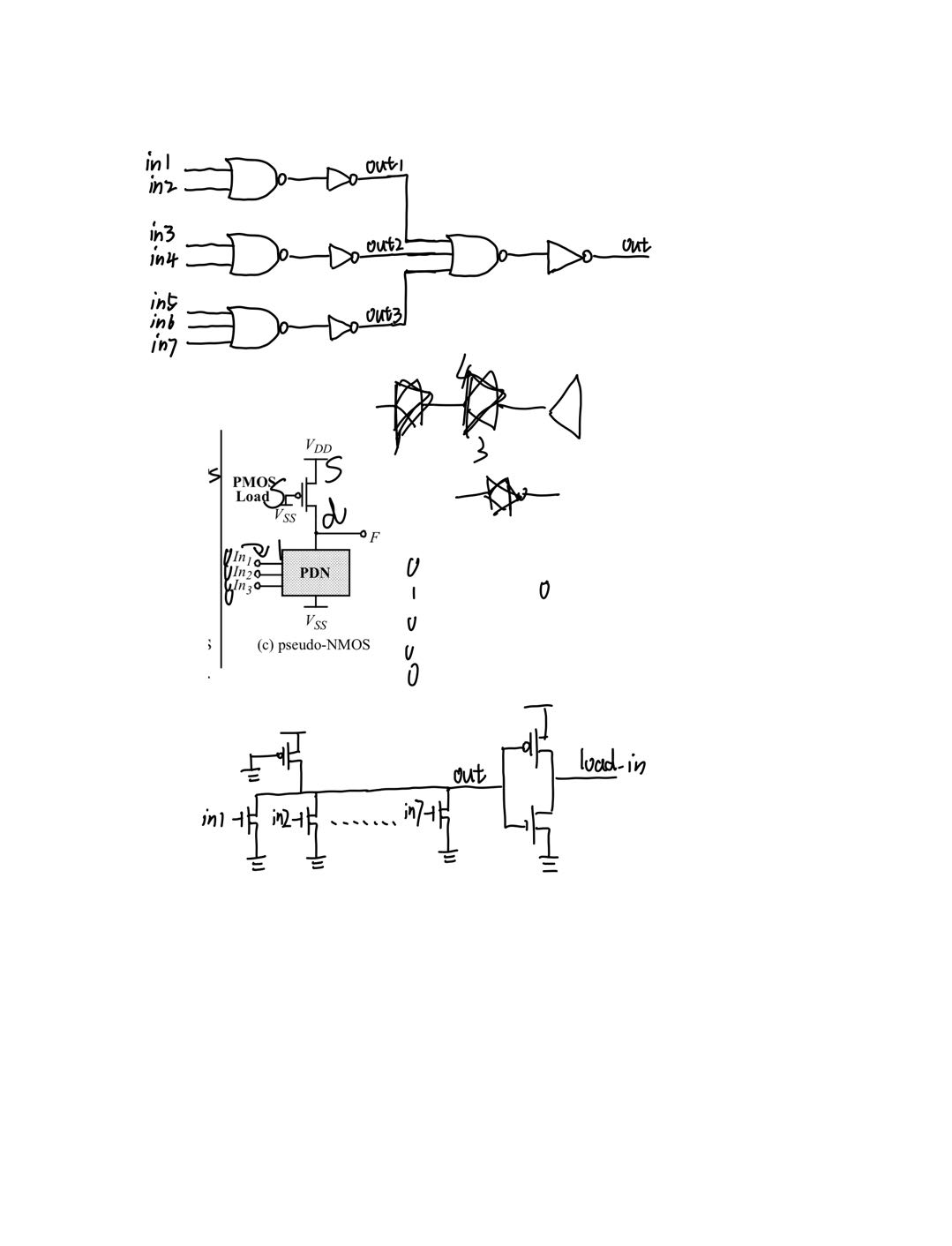


图 9 pseudo-NMOS七输入或门

pseudo-NMOS七输入或非门的PMOS尺寸为1，NMOS尺寸为2。输出反相器的PMOS尺寸为4，NMOS尺寸为3。性能指标入下表所示，另外此电路的输入端是对称的，不同input pattern的测量结果应该相同。

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **输入负载激励** | |  | | **()** | **()** | **power(W)** |
| 1111111<=>1111110 | | 1.8300E-11 | | 1.7520E-11 | 1.7910E-11 | 2.0610E-05 |
| 1111111<=>1111101 | | 1.8300E-11 | | 1.7520E-11 | 1.7910E-11 | 2.0610E-05 |
| 1111111<=>1111011 | | 1.8300E-11 | | 1.7520E-11 | 1.7910E-11 | 2.0610E-05 |
| 1111111<=>1110111 | | 1.8300E-11 | | 1.7520E-11 | 1.7910E-11 | 2.0610E-05 |
| 1111111<=>1101111 | | 1.8300E-11 | | 1.7520E-11 | 1.7910E-11 | 2.0610E-05 |
| 1111111<=>1011111 | | 1.8300E-11 | | 1.7520E-11 | 1.7910E-11 | 2.0610E-05 |
| 1111111<=>0111111 | | 1.8300E-11 | | 1.7520E-11 | 1.7910E-11 | 2.0610E-05 |
| **鳍数量** | 22 | | **平均值** | | 1.7910E-11 | 2.0610E-05 |

表 5 pseudo-NMOS七输入或门电路的性能指标

以更小的面积实现更小的延时，但是功耗被大幅度提升。

### 3.2.4 动态七输入或门电路性能指标

引入时钟信号，结构如下图所示。引入时钟信号后，应该测量输出相对于时钟上升沿的延时。当时钟信号为低电平时，进行预充，输出为逻辑0；当时钟信号为高电平时，建立输出，当输入信号存在逻辑1时，输出变为逻辑1，意味着仅存在逻辑0到1的输出延时。另外电路结构中存在有比逻辑，所以下拉网络的尺寸应该更大，减小下拉网络的电阻，以实现输出反相器可以正常反转。

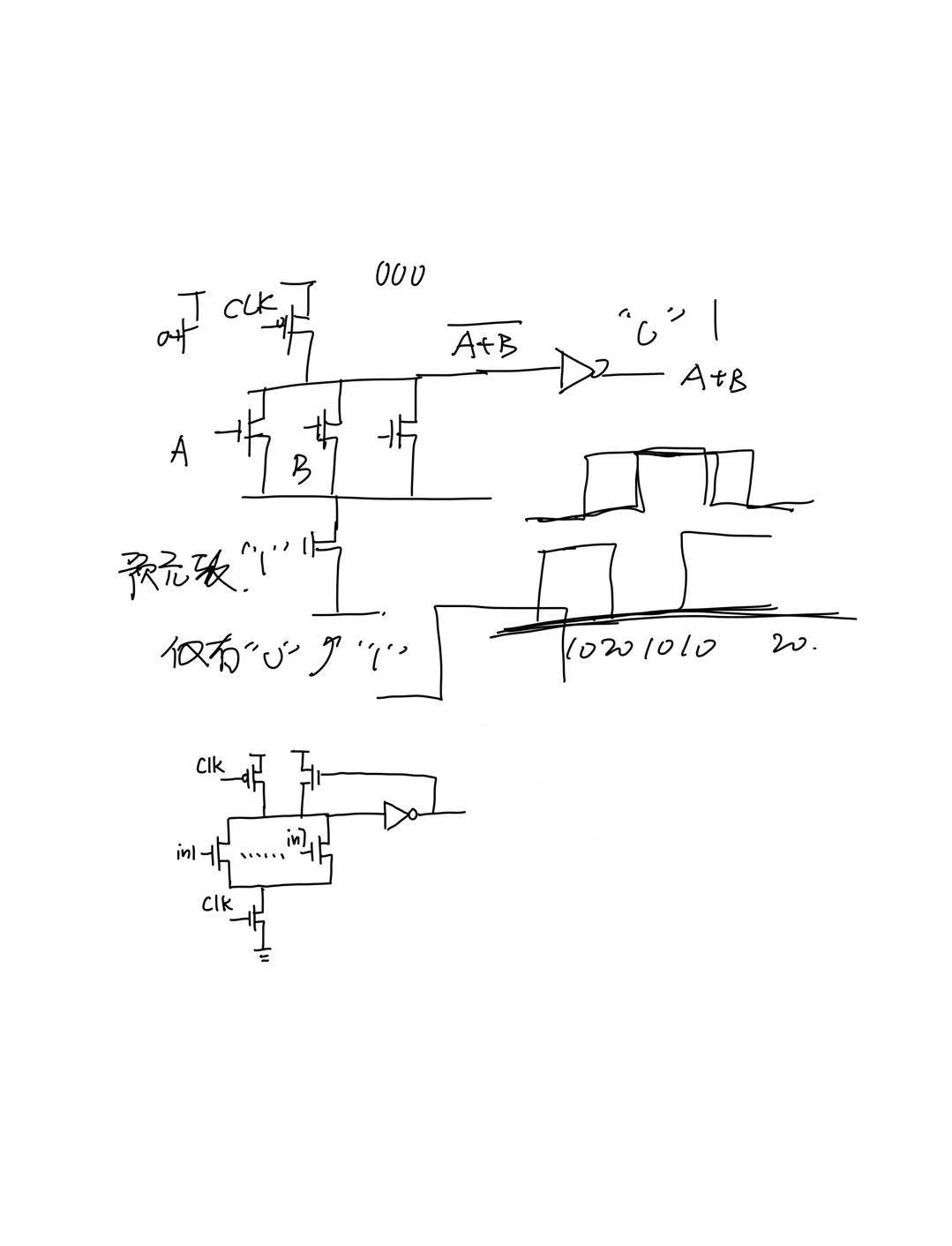


图 10 动态七输入或门

动态七输入或门电路中的PMOS采用最小尺寸，下拉网络中与输入相关的NMOS尺寸为2，与时钟信号有关的NMOS尺寸为3。输出反向器的PMOS尺寸为2，NMOS尺寸为1。性能指标如下图所示，此电路的输入端同样是对称的，不同input pattern的测量结果应该相同。

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **输入负载激励** | |  | | **()** | **()** | **power(W)** | **时钟功耗(W)** |
| 1111111<=>1111110 | | 2.4690E-11 | | 0 | 1.2345E-11 | 5.8510E-08 | 9.5500E-09 |
| 1111111<=>1111101 | | 2.4690E-11 | | 0 | 1.2345E-11 | 5.8510E-08 | 9.5500E-09 |
| 1111111<=>1111011 | | 2.4690E-11 | | 0 | 1.2345E-11 | 5.8510E-08 | 9.5500E-09 |
| 1111111<=>1110111 | | 2.4690E-11 | | 0 | 1.2345E-11 | 5.8510E-08 | 9.5500E-09 |
| 1111111<=>1101111 | | 2.4690E-11 | | 0 | 1.2345E-11 | 5.8510E-08 | 9.5500E-09 |
| 1111111<=>1011111 | | 2.4690E-11 | | 0 | 1.2345E-11 | 5.8510E-08 | 9.5500E-09 |
| 1111111<=>0111111 | | 2.4690E-11 | | 0 | 1.2345E-11 | 5.8510E-08 | 9.5500E-09 |
| **鳍数量** | 22 | | **平均值** | | 1.2345E-11 | 5.8510E-08 | 9.5500E-09 |

表 6 动态七输入或门电路的性能指标

通过引入时钟信号进行预充，大幅度减小了时钟延时，同时面积相对于标准七输入或门电路更小。引入时钟信号也会引入额外的功耗。

# 附录

## 4.1 load\_circuit.net

\* 输出反相器

.subckt load\_inv in out vdd gnd size='LOAD\_SIZE'

Xpfet out in vdd vdd pfet l=lg nfin=size

Xnfet out in gnd gnd nfet l=lg nfin=size

.ends load\_inv

\* 1级负载

Xload\_inv\_out load\_in out VDD\_LOAD VSS load\_inv size='LOAD\_SIZE'

\* 2级负载

Xload\_inv\_fanout\_1 out out2 VDD\_LOAD VSS load\_inv size='LOAD\_SIZE'

Xload\_inv\_fanout\_2 out out2 VDD\_LOAD VSS load\_inv size='LOAD\_SIZE'

Xload\_inv\_fanout\_3 out out2 VDD\_LOAD VSS load\_inv size='LOAD\_SIZE'

Xload\_inv\_fanout\_4 out out2 VDD\_LOAD VSS load\_inv size='LOAD\_SIZE'

## 4.2 inverter.sp

INVERTER

\* 引用库文件，分析及输出配置

.lib "../../PTM-MG/modelfiles/models" ptm10lstp

.inc "./load\_circuit.net"

.option acct list post

.global VDD\_DESIGN VDD\_LOAD VSS

.temp 85.0

.param SUPPLY = 0.75v

+ LOAD\_SIZE = 150

\* 电路描述

.subckt inv in out vdd gnd psize=1 nsize=1

Xpfet out in vdd vdd pfet l=lg nfin=psize

Xnfet out in gnd gnd nfet l=lg nfin=nsize

.ends inv

Xinv\_1 in in2 VDD\_DESIGN VSS inv psize=1 nsize=1

Xinv\_2 in2 in3 VDD\_DESIGN VSS inv psize=4 nsize=4

Xinv\_3 in3 in4 VDD\_DESIGN VSS inv psize=13 nsize=13

Xinv\_4 in4 load\_in VDD\_DESIGN VSS inv psize=47 nsize=47

\* 外部激励

VVDD\_DESIGN VDD\_DESIGN 0 'SUPPLY'

VVDD\_LOAD VDD\_LOAD 0 'SUPPLY'

VVSS VSS 0 0

\* 脉冲激励 延时20ns 周期40ns 占空比50%

Vin in VSS pulse 0 'SUPPLY' 20n .01n .01n 20n 40n

\* 电路分析

.tran 0.001n 200n

.dc Vin 0 'SUPPLY' 0.001

\*tplh以及tphl的测量

.measure tran tplh\_odd\_inv trig v(in) val=0.375 fall=1 targ v(load\_in) val=0.375 rise=1

.measure tran tphl\_odd\_inv trig v(in) val=0.375 rise=1 targ v(load\_in) val=0.375 fall=1

.measure tran tplh\_even\_inv trig v(in) val=0.375 rise=1 targ v(load\_in) val=0.375 rise=1

.measure tran tphl\_even\_inv trig v(in) val=0.375 fall=1 targ v(load\_in) val=0.375 fall=1

\* 输出设置

.probe dc v(load\_in)

.probe tran v(in) v(load\_in)

.end

## 4.3 change\_vdd.sp

EDP

\* 引用库文件，分析及输出配置

.lib "../../PTM-MG/modelfiles/models" ptm10lstp

.inc "./load\_circuit.net"

.option acct list post

.global VDD\_DESIGN VDD\_LOAD VSS

.temp 85.0

.param SUPPLY = 0.75v

+ LOAD\_SIZE = 150

+ STEP = -0.001v

\* 电路描述

.subckt inv in out vdd gnd psize=1 nsize=1

Xpfet out in vdd vdd pfet l=lg nfin=psize

Xnfet out in gnd gnd nfet l=lg nfin=nsize

.ends inv

Xinv\_1 in in2 VDD\_DESIGN VSS inv psize=1 nsize=1

Xinv\_2 in2 in3 VDD\_DESIGN VSS inv psize=4 nsize=4

Xinv\_3 in3 in4 VDD\_DESIGN VSS inv psize=13 nsize=13

Xinv\_4 in4 load\_in VDD\_DESIGN VSS inv psize=47 nsize=47

\* 外部激励

VVDD\_DESIGN VDD\_DESIGN 0 'SUPPLY'

VVDD\_LOAD VDD\_LOAD 0 'SUPPLY'

VVSS VSS 0 0

\* 脉冲激励 延时50ns 周期100ns 占空比50%

Vin in VSS pulse 0 'SUPPLY' 50n .01n .01n 50n 100n

\* 电路分析

.tran 0.001n 800n sweep SUPPLY 0.69 0.67 'STEP'

\*tplh以及tphl的测量

.measure tran tplh trig v(in) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran tphl trig v(in) val='SUPPLY/2' fall=1 targ v(load\_in) val='SUPPLY/2' fall=1

.measure tran avg\_power\_Xinv\_1 avg p(Xinv\_1) from=1n to=800n

.measure tran avg\_power\_Xinv\_2 avg p(Xinv\_2) from=1n to=800n

.measure tran avg\_power\_Xinv\_3 avg p(Xinv\_3) from=1n to=800n

.measure tran avg\_power\_Xinv\_4 avg p(Xinv\_4) from=1n to=800n

\* 输出设置

.probe tran v(in) v(load\_in)

.end

## 4.4 7or.sp

7OR

\* 引用库文件，分析及输出配置

.lib "../../PTM-MG/modelfiles/models" ptm10lstp

.inc "./load\_circuit.net"

.option acct list post

.global VDD\_DESIGN VDD\_LOAD VSS

.temp 85.0

.param SUPPLY = 0.75v

+ LOAD\_SIZE = 32

\* 电路描述

.subckt inv in out vdd gnd psize=1 nsize=1

Xpfet out in vdd vdd pfet l=lg nfin=psize

Xnfet out in gnd gnd nfet l=lg nfin=nsize

.ends inv

Xinv\_input\_1 in1 in1\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_2 in2 in2\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_3 in3 in3\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_4 in4 in4\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_5 in5 in5\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_6 in6 in6\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_7 in7 in7\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xpfet\_1 out\_temp in1\_i p\_node\_1 VDD\_DESIGN pfet l=lg nfin=7

Xpfet\_2 p\_node\_1 in2\_i p\_node\_2 VDD\_DESIGN pfet l=lg nfin=7

Xpfet\_3 p\_node\_2 in3\_i p\_node\_3 VDD\_DESIGN pfet l=lg nfin=7

Xpfet\_4 p\_node\_3 in4\_i p\_node\_4 VDD\_DESIGN pfet l=lg nfin=7

Xpfet\_5 p\_node\_4 in5\_i p\_node\_5 VDD\_DESIGN pfet l=lg nfin=7

Xpfet\_6 p\_node\_5 in6\_i p\_node\_6 VDD\_DESIGN pfet l=lg nfin=7

Xpfet\_7 p\_node\_6 in7\_i VDD\_DESIGN VDD\_DESIGN pfet l=lg nfin=7

Xnfet\_1 out\_temp in1\_i VSS VSS nfet l=lg nfin=1

Xnfet\_2 out\_temp in2\_i VSS VSS nfet l=lg nfin=1

Xnfet\_3 out\_temp in3\_i VSS VSS nfet l=lg nfin=1

Xnfet\_4 out\_temp in4\_i VSS VSS nfet l=lg nfin=1

Xnfet\_5 out\_temp in5\_i VSS VSS nfet l=lg nfin=1

Xnfet\_6 out\_temp in6\_i VSS VSS nfet l=lg nfin=1

Xnfet\_7 out\_temp in7\_i VSS VSS nfet l=lg nfin=1

Xinv\_output\_1 out\_temp load\_in VDD\_DESIGN VSS inv psize=6 nsize=6

\* 设置外部激励

VVDD\_DESIGN VDD\_DESIGN 0 'SUPPLY'

VVDD\_LOAD VDD\_LOAD 0 'SUPPLY'

VVSS VSS 0 0

.tran 0.0001n 50n

\* in1

.alter

Vin1 in1 VSS pulse 0 'SUPPLY' 20n .01n .01n 20n 40n

Vin2 in2 VSS 'SUPPLY'

Vin3 in3 VSS 'SUPPLY'

Vin4 in4 VSS 'SUPPLY'

Vin5 in5 VSS 'SUPPLY'

Vin6 in6 VSS 'SUPPLY'

Vin7 in7 VSS 'SUPPLY'

.measure tran tplh trig v(in1) val='SUPPLY/2' fall=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran tphl trig v(in1) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' fall=1

.measure tran avg\_power avg p(VVDD\_DESIGN) from=0.0001n to=50n

\* in2

.alter

Vin1 in1 VSS 'SUPPLY'

Vin2 in2 VSS pulse 0 'SUPPLY' 20n .01n .01n 20n 40n

Vin3 in3 VSS 'SUPPLY'

Vin4 in4 VSS 'SUPPLY'

Vin5 in5 VSS 'SUPPLY'

Vin6 in6 VSS 'SUPPLY'

Vin7 in7 VSS 'SUPPLY'

.measure tran tplh trig v(in2) val='SUPPLY/2' fall=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran tphl trig v(in2) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' fall=1

.measure tran avg\_power avg p(VVDD\_DESIGN) from=0.0001n to=50n

\* in3

.alter

Vin1 in1 VSS 'SUPPLY'

Vin2 in2 VSS 'SUPPLY'

Vin3 in3 VSS pulse 0 'SUPPLY' 20n .01n .01n 20n 40n

Vin4 in4 VSS 'SUPPLY'

Vin5 in5 VSS 'SUPPLY'

Vin6 in6 VSS 'SUPPLY'

Vin7 in7 VSS 'SUPPLY'

.measure tran tplh trig v(in3) val='SUPPLY/2' fall=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran tphl trig v(in3) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' fall=1

.measure tran avg\_power avg p(VVDD\_DESIGN) from=0.0001n to=50n

\* in4

.alter

Vin1 in1 VSS 'SUPPLY'

Vin2 in2 VSS 'SUPPLY'

Vin3 in3 VSS 'SUPPLY'

Vin4 in4 VSS pulse 0 'SUPPLY' 20n .01n .01n 20n 40n

Vin5 in5 VSS 'SUPPLY'

Vin6 in6 VSS 'SUPPLY'

Vin7 in7 VSS 'SUPPLY'

.measure tran tplh trig v(in4) val='SUPPLY/2' fall=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran tphl trig v(in4) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' fall=1

.measure tran avg\_power avg p(VVDD\_DESIGN) from=0.0001n to=50n

\* in5

.alter

Vin1 in1 VSS 'SUPPLY'

Vin2 in2 VSS 'SUPPLY'

Vin3 in3 VSS 'SUPPLY'

Vin4 in4 VSS 'SUPPLY'

Vin5 in5 VSS pulse 0 'SUPPLY' 20n .01n .01n 20n 40n

Vin6 in6 VSS 'SUPPLY'

Vin7 in7 VSS 'SUPPLY'

.measure tran tplh trig v(in5) val='SUPPLY/2' fall=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran tphl trig v(in5) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' fall=1

.measure tran avg\_power avg p(VVDD\_DESIGN) from=0.0001n to=50n

\* in6

.alter

Vin1 in1 VSS 'SUPPLY'

Vin2 in2 VSS 'SUPPLY'

Vin3 in3 VSS 'SUPPLY'

Vin4 in4 VSS 'SUPPLY'

Vin5 in5 VSS 'SUPPLY'

Vin6 in6 VSS  pulse 0 'SUPPLY' 20n .01n .01n 20n 40n

Vin7 in7 VSS 'SUPPLY'

.measure tran tplh trig v(in6) val='SUPPLY/2' fall=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran tphl trig v(in6) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' fall=1

.measure tran avg\_power avg p(VVDD\_DESIGN) from=0.0001n to=50n

\* in7

.alter

Vin1 in1 VSS 'SUPPLY'

Vin2 in2 VSS 'SUPPLY'

Vin3 in3 VSS 'SUPPLY'

Vin4 in4 VSS 'SUPPLY'

Vin5 in5 VSS 'SUPPLY'

Vin6 in6 VSS 'SUPPLY'

Vin7 in7 VSS pulse 0 'SUPPLY' 20n .01n .01n 20n 40n

.measure tran tplh trig v(in7) val='SUPPLY/2' fall=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran tphl trig v(in7) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' fall=1

.measure tran avg\_power avg p(VVDD\_DESIGN) from=0.0001n to=50n

.probe tran

.end

## 4.5 7or\_pseudo.sp

7OR\_PSEUDO

\* 引用库文件，分析及输出配置

.lib "../../PTM-MG/modelfiles/models" ptm10lstp

.inc "./load\_circuit.net"

.option acct list post

.global VDD\_DESIGN VDD\_LOAD VSS

.temp 85.0

.param SUPPLY = 0.75v

+ LOAD\_SIZE = 32

\* 电路描述

\* 可定义尺寸的反相器

.subckt inv in out vdd gnd psize=1 nsize=1

Xpfet out in vdd vdd pfet l=lg nfin=psize

Xnfet out in gnd gnd nfet l=lg nfin=nsize

.ends inv

\* 输入负载

Xinv\_input\_1 in1 in1\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_2 in2 in2\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_3 in3 in3\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_4 in4 in4\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_5 in5 in5\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_6 in6 in6\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_7 in7 in7\_i VDD\_LOAD VSS inv psize=1 nsize=1

\* d g s x

Xpfet\_1 out\_temp VSS VDD\_DESIGN VDD\_DESIGN pfet l=lg nfin=1

Xnfet\_1 out\_temp in1\_i VSS VSS nfet l=lg nfin=2

Xnfet\_2 out\_temp in2\_i VSS VSS nfet l=lg nfin=2

Xnfet\_3 out\_temp in3\_i VSS VSS nfet l=lg nfin=2

Xnfet\_4 out\_temp in4\_i VSS VSS nfet l=lg nfin=2

Xnfet\_5 out\_temp in5\_i VSS VSS nfet l=lg nfin=2

Xnfet\_6 out\_temp in6\_i VSS VSS nfet l=lg nfin=2

Xnfet\_7 out\_temp in7\_i VSS VSS nfet l=lg nfin=2

Xinv\_output\_1 out\_temp load\_in VDD\_DESIGN VSS inv psize=4 nsize=3

VVDD\_DESIGN VDD\_DESIGN 0 'SUPPLY'

VVDD\_LOAD VDD\_LOAD 0 'SUPPLY'

VVSS VSS 0 0

.tran 0.0001n 50n

\* in1

.alter

Vin1 in1 VSS pulse 0 'SUPPLY' 20n .01n .01n 20n 40n

Vin2 in2 VSS 'SUPPLY'

Vin3 in3 VSS 'SUPPLY'

Vin4 in4 VSS 'SUPPLY'

Vin5 in5 VSS 'SUPPLY'

Vin6 in6 VSS 'SUPPLY'

Vin7 in7 VSS 'SUPPLY'

.measure tran tplh trig v(in1) val='SUPPLY/2' fall=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran tphl trig v(in1) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' fall=1

.measure tran avg\_power avg p(VVDD\_DESIGN) from=0.0001n to=50n

\* in2

.alter

Vin1 in1 VSS 'SUPPLY'

Vin2 in2 VSS pulse 0 'SUPPLY' 20n .01n .01n 20n 40n

Vin3 in3 VSS 'SUPPLY'

Vin4 in4 VSS 'SUPPLY'

Vin5 in5 VSS 'SUPPLY'

Vin6 in6 VSS 'SUPPLY'

Vin7 in7 VSS 'SUPPLY'

.measure tran tplh trig v(in2) val='SUPPLY/2' fall=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran tphl trig v(in2) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' fall=1

.measure tran avg\_power avg p(VVDD\_DESIGN) from=0.0001n to=50n

\* in3

.alter

Vin1 in1 VSS 'SUPPLY'

Vin2 in2 VSS 'SUPPLY'

Vin3 in3 VSS pulse 0 'SUPPLY' 20n .01n .01n 20n 40n

Vin4 in4 VSS 'SUPPLY'

Vin5 in5 VSS 'SUPPLY'

Vin6 in6 VSS 'SUPPLY'

Vin7 in7 VSS 'SUPPLY'

.measure tran tplh trig v(in3) val='SUPPLY/2' fall=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran tphl trig v(in3) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' fall=1

.measure tran avg\_power avg p(VVDD\_DESIGN) from=0.0001n to=50n

\* in4

.alter

Vin1 in1 VSS 'SUPPLY'

Vin2 in2 VSS 'SUPPLY'

Vin3 in3 VSS 'SUPPLY'

Vin4 in4 VSS pulse 0 'SUPPLY' 20n .01n .01n 20n 40n

Vin5 in5 VSS 'SUPPLY'

Vin6 in6 VSS 'SUPPLY'

Vin7 in7 VSS 'SUPPLY'

.measure tran tplh trig v(in4) val='SUPPLY/2' fall=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran tphl trig v(in4) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' fall=1

.measure tran avg\_power avg p(VVDD\_DESIGN) from=0.0001n to=50n

\* in5

.alter

Vin1 in1 VSS 'SUPPLY'

Vin2 in2 VSS 'SUPPLY'

Vin3 in3 VSS 'SUPPLY'

Vin4 in4 VSS 'SUPPLY'

Vin5 in5 VSS pulse 0 'SUPPLY' 20n .01n .01n 20n 40n

Vin6 in6 VSS 'SUPPLY'

Vin7 in7 VSS 'SUPPLY'

.measure tran tplh trig v(in5) val='SUPPLY/2' fall=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran tphl trig v(in5) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' fall=1

.measure tran avg\_power avg p(VVDD\_DESIGN) from=0.0001n to=50n

\* in6

.alter

Vin1 in1 VSS 'SUPPLY'

Vin2 in2 VSS 'SUPPLY'

Vin3 in3 VSS 'SUPPLY'

Vin4 in4 VSS 'SUPPLY'

Vin5 in5 VSS 'SUPPLY'

Vin6 in6 VSS  pulse 0 'SUPPLY' 20n .01n .01n 20n 40n

Vin7 in7 VSS 'SUPPLY'

.measure tran tplh trig v(in6) val='SUPPLY/2' fall=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran tphl trig v(in6) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' fall=1

.measure tran avg\_power avg p(VVDD\_DESIGN) from=0.0001n to=50n

\* in7

.alter

Vin1 in1 VSS 'SUPPLY'

Vin2 in2 VSS 'SUPPLY'

Vin3 in3 VSS 'SUPPLY'

Vin4 in4 VSS 'SUPPLY'

Vin5 in5 VSS 'SUPPLY'

Vin6 in6 VSS 'SUPPLY'

Vin7 in7 VSS pulse 0 'SUPPLY' 20n .01n .01n 20n 40n

.measure tran tplh trig v(in7) val='SUPPLY/2' fall=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran tphl trig v(in7) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' fall=1

.measure tran avg\_power avg p(VVDD\_DESIGN) from=0.0001n to=50n

.probe tran

.end

## 4.6 7or\_hier\_resize.sp

7OR\_HIER\_RESIZE

\* 引用库文件，分析及输出配置

.lib "../../PTM-MG/modelfiles/models" ptm10lstp

.inc "./load\_circuit.net"

.option acct list post

.global VDD\_DESIGN VDD\_LOAD VSS

.temp 85.0

.param SUPPLY = 0.75v

+ LOAD\_SIZE = 32

\* 电路描述

\* 可定义尺寸的反相器

.subckt inv in out vdd gnd psize=1 nsize=1

Xpfet out in vdd vdd pfet l=lg nfin=psize

Xnfet out in gnd gnd nfet l=lg nfin=nsize

.ends inv

\* 两输入或非门

.subckt nor2 in1 in2 out vdd gnd

Xpfet\_1 out in1 p\_node\_1 vdd pfet l=lg nfin=2

Xpfet\_2 p\_node\_1 in2 vdd vdd pfet l=lg nfin=2

Xnfet\_1 out in1 gnd gnd nfet l=lg nfin=1

Xnfet\_2 out in2 gnd gnd nfet l=lg nfin=1

.ends nor2

\* 三输入或非门

.subckt nor3 in1 in2 in3 out vdd gnd

Xpfet\_1 out in1 p\_node\_1 vdd pfet l=lg nfin=3

Xpfet\_2 p\_node\_1 in2 p\_node\_2 vdd pfet l=lg nfin=3

Xpfet\_3 p\_node\_2 in3 vdd vdd pfet l=lg nfin=3

Xnfet\_1 out in1 gnd gnd nfet l=lg nfin=1

Xnfet\_2 out in2 gnd gnd nfet l=lg nfin=1

Xnfet\_3 out in3 gnd gnd nfet l=lg nfin=1

.ends nor3

\* 输入负载

Xinv\_input\_1 in1 in1\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_2 in2 in2\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_3 in3 in3\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_4 in4 in4\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_5 in5 in5\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_6 in6 in6\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_7 in7 in7\_i VDD\_LOAD VSS inv psize=1 nsize=1

\* 一级与非门

Xnor2\_1 in1\_i in2\_i out\_1 VDD\_DESIGN VSS nor2

Xnor2\_2 in3\_i in4\_i out\_2 VDD\_DESIGN VSS nor2

Xnor3\_3 in5\_i in6\_i in7\_i out\_3 VDD\_DESIGN VSS nor3

Xinv\_out\_1 out\_1 out\_1\_i VDD\_DESIGN VSS inv psize=1 nsize=1

Xinv\_out\_2 out\_2 out\_2\_i VDD\_DESIGN VSS inv psize=1 nsize=1

Xinv\_out\_3 out\_3 out\_3\_i VDD\_DESIGN VSS inv psize=1 nsize=1

\* 二级与非门

Xnor3\_4 out\_1\_i out\_2\_i out\_3\_i out\_temp VDD\_DESIGN VSS nor3

Xinv\_out\_4 out\_temp load\_in VDD\_DESIGN VSS inv psize=4 nsize=3

VVDD\_DESIGN VDD\_DESIGN 0 'SUPPLY'

VVDD\_LOAD VDD\_LOAD 0 'SUPPLY'

VVSS VSS 0 0

.tran 0.0001n 50n

\* in1

.alter

Vin1 in1 VSS pulse 0 'SUPPLY' 20n .01n .01n 20n 40n

Vin2 in2 VSS 'SUPPLY'

Vin3 in3 VSS 'SUPPLY'

Vin4 in4 VSS 'SUPPLY'

Vin5 in5 VSS 'SUPPLY'

Vin6 in6 VSS 'SUPPLY'

Vin7 in7 VSS 'SUPPLY'

.measure tran tplh trig v(in1) val='SUPPLY/2' fall=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran tphl trig v(in1) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' fall=1

.measure tran avg\_power avg p(VVDD\_DESIGN) from=0.0001n to=50n

\* in2

.alter

Vin1 in1 VSS 'SUPPLY'

Vin2 in2 VSS pulse 0 'SUPPLY' 20n .01n .01n 20n 40n

Vin3 in3 VSS 'SUPPLY'

Vin4 in4 VSS 'SUPPLY'

Vin5 in5 VSS 'SUPPLY'

Vin6 in6 VSS 'SUPPLY'

Vin7 in7 VSS 'SUPPLY'

.measure tran tplh trig v(in2) val='SUPPLY/2' fall=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran tphl trig v(in2) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' fall=1

.measure tran avg\_power avg p(VVDD\_DESIGN) from=0.0001n to=50n

\* in3

.alter

Vin1 in1 VSS 'SUPPLY'

Vin2 in2 VSS 'SUPPLY'

Vin3 in3 VSS pulse 0 'SUPPLY' 20n .01n .01n 20n 40n

Vin4 in4 VSS 'SUPPLY'

Vin5 in5 VSS 'SUPPLY'

Vin6 in6 VSS 'SUPPLY'

Vin7 in7 VSS 'SUPPLY'

.measure tran tplh trig v(in3) val='SUPPLY/2' fall=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran tphl trig v(in3) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' fall=1

.measure tran avg\_power avg p(VVDD\_DESIGN) from=0.0001n to=50n

\* in4

.alter

Vin1 in1 VSS 'SUPPLY'

Vin2 in2 VSS 'SUPPLY'

Vin3 in3 VSS 'SUPPLY'

Vin4 in4 VSS pulse 0 'SUPPLY' 20n .01n .01n 20n 40n

Vin5 in5 VSS 'SUPPLY'

Vin6 in6 VSS 'SUPPLY'

Vin7 in7 VSS 'SUPPLY'

.measure tran tplh trig v(in4) val='SUPPLY/2' fall=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran tphl trig v(in4) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' fall=1

.measure tran avg\_power avg p(VVDD\_DESIGN) from=0.0001n to=50n

\* in5

.alter

Vin1 in1 VSS 'SUPPLY'

Vin2 in2 VSS 'SUPPLY'

Vin3 in3 VSS 'SUPPLY'

Vin4 in4 VSS 'SUPPLY'

Vin5 in5 VSS pulse 0 'SUPPLY' 20n .01n .01n 20n 40n

Vin6 in6 VSS 'SUPPLY'

Vin7 in7 VSS 'SUPPLY'

.measure tran tplh trig v(in5) val='SUPPLY/2' fall=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran tphl trig v(in5) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' fall=1

.measure tran avg\_power avg p(VVDD\_DESIGN) from=0.0001n to=50n

\* in6

.alter

Vin1 in1 VSS 'SUPPLY'

Vin2 in2 VSS 'SUPPLY'

Vin3 in3 VSS 'SUPPLY'

Vin4 in4 VSS 'SUPPLY'

Vin5 in5 VSS 'SUPPLY'

Vin6 in6 VSS  pulse 0 'SUPPLY' 20n .01n .01n 20n 40n

Vin7 in7 VSS 'SUPPLY'

.measure tran tplh trig v(in6) val='SUPPLY/2' fall=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran tphl trig v(in6) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' fall=1

.measure tran avg\_power avg p(VVDD\_DESIGN) from=0.0001n to=50n

\* in7

.alter

Vin1 in1 VSS 'SUPPLY'

Vin2 in2 VSS 'SUPPLY'

Vin3 in3 VSS 'SUPPLY'

Vin4 in4 VSS 'SUPPLY'

Vin5 in5 VSS 'SUPPLY'

Vin6 in6 VSS 'SUPPLY'

Vin7 in7 VSS pulse 0 'SUPPLY' 20n .01n .01n 20n 40n

.measure tran tplh trig v(in7) val='SUPPLY/2' fall=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran tphl trig v(in7) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' fall=1

.measure tran avg\_power avg p(VVDD\_DESIGN) from=0.0001n to=50n

.probe tran

.end

## 4.7 7or\_dynamic.sp

7OR\_DYNAMIC

*\* 引用库文件，分析及输出配置*

.lib "../../PTM-MG/modelfiles/models" ptm10lstp

.inc "./load\_circuit.net"

.option acct list post

.global VDD\_DESIGN VDD\_LOAD VSS

.temp 85.0

.param SUPPLY = 0.75v

+ LOAD\_SIZE = 32

*\* 电路描述*

.subckt inv in out vdd gnd psize=1 nsize=1

Xpfet out in vdd vdd pfet l=lg nfin=psize

Xnfet out in gnd gnd nfet l=lg nfin=nsize

.ends inv

Xinv\_input\_1 in1 in1\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_2 in2 in2\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_3 in3 in3\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_4 in4 in4\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_5 in5 in5\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_6 in6 in6\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xinv\_input\_7 in7 in7\_i VDD\_LOAD VSS inv psize=1 nsize=1

Xpfet\_clk\_1 out\_temp clk VDD\_DESIGN VDD\_DESIGN pfet l=lg nfin=1

Xpfet\_clk\_2 out\_temp load\_in VDD\_DESIGN VDD\_DESIGN pfet l=lg nfin=1

Xnfet\_1 out\_temp in1\_i clk\_node VSS nfet l=lg nfin=2

Xnfet\_2 out\_temp in2\_i clk\_node VSS nfet l=lg nfin=2

Xnfet\_3 out\_temp in3\_i clk\_node VSS nfet l=lg nfin=2

Xnfet\_4 out\_temp in4\_i clk\_node VSS nfet l=lg nfin=2

Xnfet\_5 out\_temp in5\_i clk\_node VSS nfet l=lg nfin=2

Xnfet\_6 out\_temp in6\_i clk\_node VSS nfet l=lg nfin=2

Xnfet\_7 out\_temp in7\_i clk\_node VSS nfet l=lg nfin=2

Xnfet\_clk clk\_node clk VSS VSS nfet l=lg nfin=3

Xinv\_output out\_temp load\_in VDD\_DESIGN VSS inv psize=2 nsize=1

VVDD\_DESIGN VDD\_DESIGN 0 'SUPPLY'

VVDD\_LOAD VDD\_LOAD 0 'SUPPLY'

VVSS VSS 0 0

Vclk clk VSS PWL 0n 0v 15n 0v 15.001n 'SUPPLY' 20n 'SUPPLY' 20.001n 0v 35n 0v 35.001n 'SUPPLY'

.tran 0.0001n 50n

*\* in1*

.alter

Vin1 in1 VSS  PWL 0n 'SUPPLY' 10n 'SUPPLY' 10.001n 0v 30n 0v 30.001n 'SUPPLY'

Vin2 in2 VSS 'SUPPLY'

Vin3 in3 VSS 'SUPPLY'

Vin4 in4 VSS 'SUPPLY'

Vin5 in5 VSS 'SUPPLY'

Vin6 in6 VSS 'SUPPLY'

Vin7 in7 VSS 'SUPPLY'

.measure tran tplh trig v(clk) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran avg\_power avg p(VVDD\_DESIGN) from=0.0001n to=50n

.measure tran avg\_clk\_power avg p(Vclk) from=0.0001n to=50n

*\* in1*

.alter

Vin1 in1 VSS 'SUPPLY'

Vin2 in2 VSS PWL 0n 'SUPPLY' 10n 'SUPPLY' 10.001n 0v 30n 0v 30.001n 'SUPPLY'

Vin3 in3 VSS 'SUPPLY'

Vin4 in4 VSS 'SUPPLY'

Vin5 in5 VSS 'SUPPLY'

Vin6 in6 VSS 'SUPPLY'

Vin7 in7 VSS 'SUPPLY'

.measure tran tplh trig v(clk) val='SUPPLY/2' rise=1 targ v(load\_in) val='SUPPLY/2' rise=1

.measure tran avg\_power avg p(VVDD\_DESIGN) from=0.0001n to=50n

.measure tran avg\_clk\_power avg p(Vclk) from=0.0001n to=50n

.probe tran

.end