DATA SHEET:

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1 Features:

- Low temperature coefficient: Lower than 137ppm/℃.
- Process compensated covering all corners.
- High accuracy: less than 1.78%.
- Includes current mirror.

2 Description:

The current reference combines three circuit building blocks on a single chip. One PTAT self-biased current reference, one NTAT (CTAT) self-biased current referenced and a summation circuit which add two circuits together then output through a current mirror. This temperature compensated current reference can achieve process variation compensation from 6 uA to 15 uA and 1 uA as a step which covers all four corner variations.

3 The packaged chip and its usage:

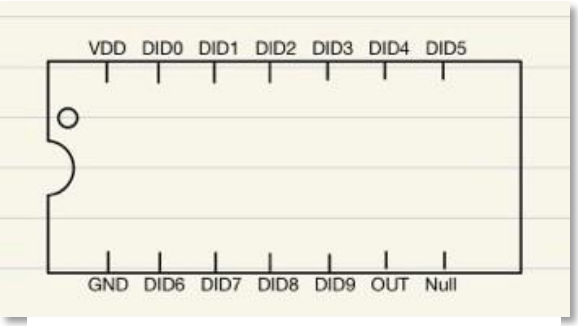


Figure 1 The packaged chip pin specification

There are 13 pins on my design which consists of VDD and GND as the power supply. Digital input data from 0 to 9 and an output. The last pin is null pin which can be ignored.

VDD should be connected to 1.8 volts and GND to 0 volts. DID input means the process variation compensation. DID0 is the nominal output which gives 10 μA output current. DID1 gives 6 μA. DID2 gives 7 μA. DID3 gives 8 μA. DID4 gives 9 μA. DID5 gives 11 μA. DID6 gives 12 μA. DID7 gives 13 μA. DID8 gives 14 μA. DID9 gives 15 μA. When one of the DID pin is set up. The other pin should be set to 0 to ensure the correct function. The final output comes out from the OUT pin. The output pin should have 100k ohms output load on it to activate the current mirror at the output port.

As shown in figure2, there are three blocks in this design. The NTAT circuit is on the left-hand side, with five mosfets and its corresponding start up circuit which consists of 3 mosfets named M15, M17, M18. M4, M5, M6, M7 build the self-biased current reference and the other mosfet named M8 is used to provide negative temperature coefficient is: $I_{NTAT} = \theta(\frac{T}{T\_NOM})^{UTE}\left[V_{THNO} + KT1 \times \left(\frac{T}{T_{NOM}} - 1\right)\right]^2$ (1)

Where $\theta = \frac{\frac{1}{2}\mu_0 C_{ox}^2}{\left(\frac{1}{\sqrt{(\frac{W}{L})_1}} - \frac{1}{\sqrt{(\frac{W}{L})_2}} - \frac{1}{\sqrt{(\frac{W}{L})_3}}\right)^2}$

The PTAT circuits is located on the right-hand side with start-up circuit. M0, M1, M2, M3 build another self biased current reference and resistor R0 is used to generate a positive temperature coefficient and the current equation is shown below:

$$I_{PTAT} = \frac{2}{R^2 \mu_n C_{ox} \frac{W_n}{L_n}}(1 - \frac{1}{\sqrt{K}})^2 \quad (2)$$

Having both positive and negative coefficient. I can build a low temperature coefficient current reference by adding them together using the current mirrors and merge two branch into one. The nominal 10 μA

summation circuit is shown in the upper circuit. M13, M14 is the current mirrors deriving from the two circuit and M32 is a switch to control whether it's open or close. The way I make it digital trimmable is I copy the summation circuit multiple times with different mosfet sizing to give various current. Therefore, there are 10 sets of summation circuit connected in parallel and each of which is controlled by a switch. If there are process variation, designers can easily change the current by switch on and off the control switch.

4 Specifications:

	Value	MIN	TYP	MAX	unit
Operating voltage			1.8		V
Operating temperature range		0		65	°C
Current accuracy		0.897	1.434	1.78	%
Temperature drift		65.6	114.4	137	ppm/°C
Output Impedance		19.25k		196.9k	Ohms

5 The design schematic and layout:

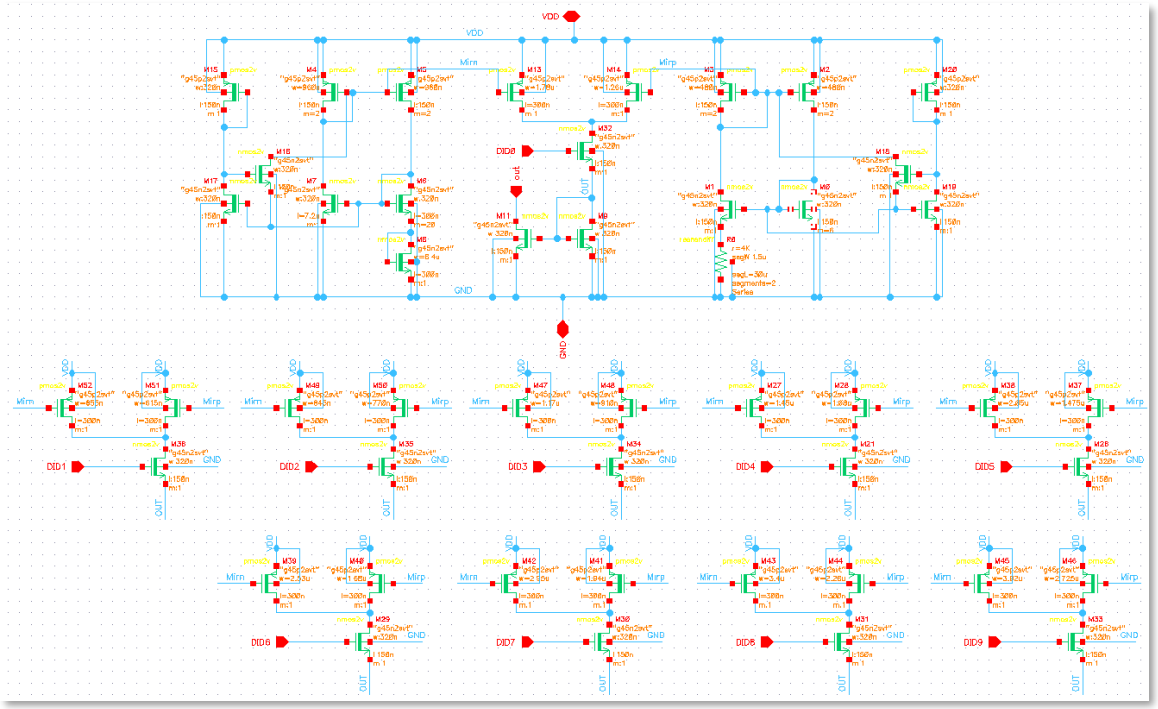


Figure 2 The schematic of design

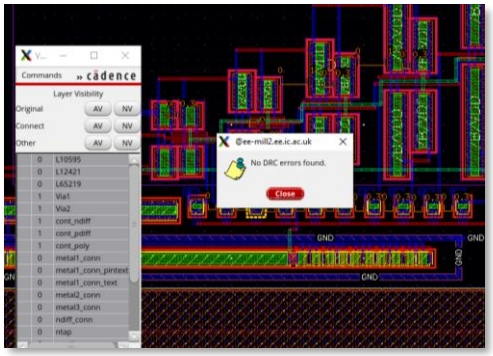


Figure 3 The DRC test of layout

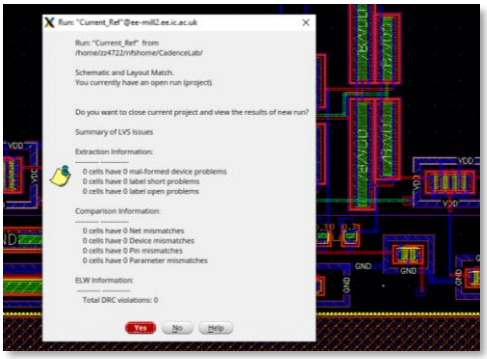


Figure 4 The LVS test of layout

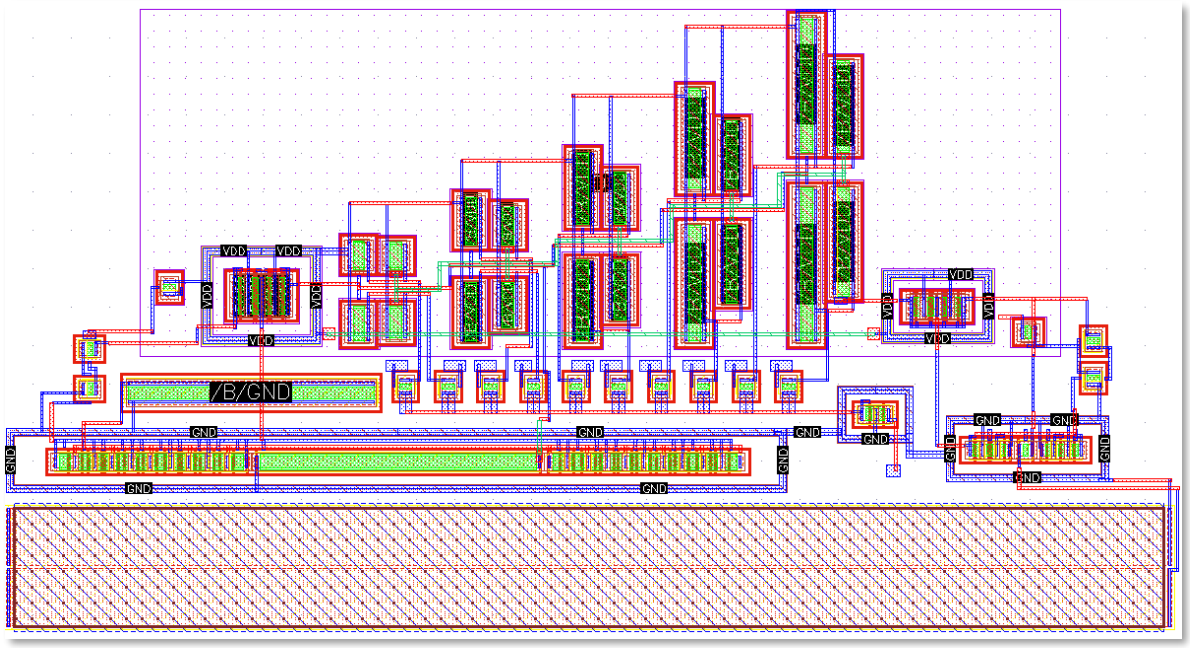


Figure 5 The top-level layout

5 Test and compensation of process variation:

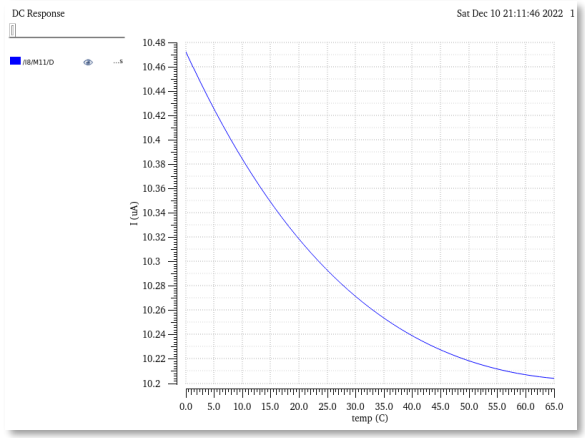


Figure 6 The SS corner compensated curve

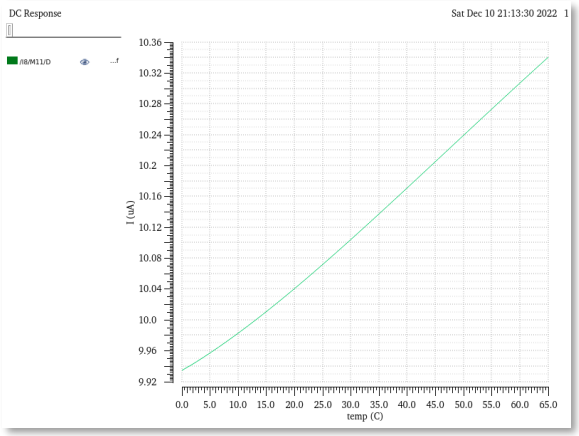


Figure 7 The SF corner compensated curve

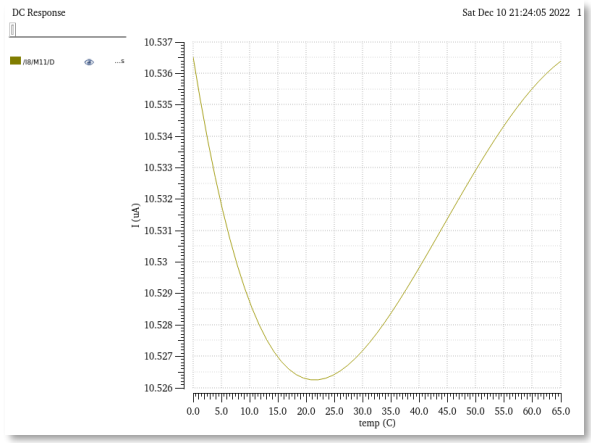


Figure 8 The FS corner compensated curve

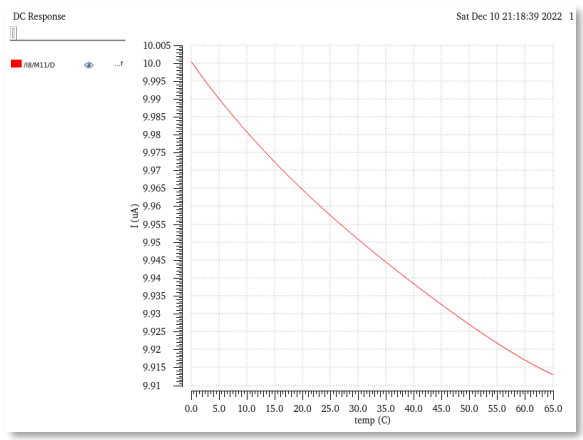


Figure 9 The FF corner compensated curve

6: Simulation and targets

The accurate circuit simulation results are shown below:

Table 1 The simulation results

The switch	Current Accuracy (%)	Temperature Drift (ppm/degree)	Output impedance (ohms)	Power consumption (W)
0	1.78	136	77877.92	1.82147E-05
1	1.57	112	196903.3	1.09126E-05
2	1.24	105	154743.5	1.27187E-05
3	1.6	134	122727.3	1.45469E-05
4	1.65	137	97811.11	1.63793E-05
5	1.43	118	61962.26	2.00047E-05
6	1.62	125	48430.35	2.18284E-05
7	1.34	117	37300.82	2.35978E-05
8	1.21	94	27505.84	2.54106E-05
9	0.897	65.6	19245.57	2.71708E-05
Average	1.4337	114.36	N/A	1.90785E-05
Min	0.897	65.6	19245.57	1.09126E-05
Max	1.78	137	196903.3	2.71708E-05

The specifications in the presentation are mostly achieve. however, there are some targets is failed.

1. **Current accuracy.** Under typical condition, the error should not exceed 1%.

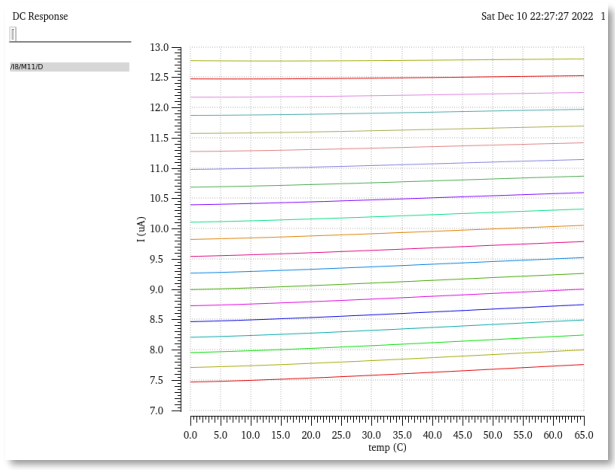
This specification is failed where only one condition is below 1 % as shown above. However, the error of all the cases is below 1.8% which is slightly exceeding the target.

2. **Temperature drift of the output current.** Expected to be within 5%.

The temperature drift is no more than 137 ppm/℃ which means the drift is below 0.02%. which fully satisfy and exceed the target.

3. **Output impedance.** As much as possible to provide the best output current.

The actual output impedance varies with respect to the value of the current. All the output impedance is larger than 19.23k.



4. **The power supply voltage range from 1.7-1.9 volts.**

Ensue that the power supply swing wouldn't affect the output current very much. Expected to be within 1%.

The results show a huge variation and It's hard to get rid of the voltage variation. Because in the paper, the proposed circuit has a cascode current mirror both on the self-biased current reference and the output which will consume larger voltage drop. Therefore, this target is hard to achieve.

5. **Power Consumption.** Below 5mW

The power consumption is all much smaller than 5mW, which gives very efficient current reference.