ECE 483—Analog IC Design

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LDO Design Project Report

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Contents

1 Overall Design Approach

To start designing the error amplifier, the most simple approach uses the five transistor OTA model discussed in class. However, the gain is on the order of $g_m r_{ds}$, which is too small for this particular LDO design and specification. A large gain is desired as the line regulation specification is $L_R \leq 1\text{mV/V}$. $L_R \approx \frac{1}{\beta A_{EA0}} \leq 1\text{mV/V} \longrightarrow \beta A_{EA0} \geq 1000$; so, having a large gain for the error amplifier is key. As such, the telescopic cascode is a reasonable topology to go to since its gain is on the order of $(g_m r_{ds})^2$. While that is okay, the folded cascode OTA is more advantageous due to its improved ICMR (input common mode range) and output swing, which are relevant performance metrics. At first, a PMOS-input pair was used for the folded cascode OTA. Most of the specs were matched but there were concerns about the PMOS input pair going out of saturation or turning off for higher voltages. As such, a NMOS input pair was considered since it would avoid such problems. Yet despite that benefit, the NMOS input pair has a similar issue in that too low of an input voltage could turn off the pair. In the end, a dual NMOS and PMOS differential input pair was chosen as seen in Figure 1. Instead of trying to implement two separate OTAs and juggling which one will turn on or off depending on the voltage level, using both input pairs in tandem allows for seamless switching between the two. The benefit of this topology is that if the input voltage is too high, the PMOS pair turns off and the NMOS pair will turn on automatically. Essentially, the PMOS input pair will be active for low input common voltages and the NMOS input pair will be active for higher input common voltages. In essence, this design choice increases the range of the input voltage while keeping all the aforementioned benefits of a folded cascode topology. While using an NMOS amplifier and PMOS output stage is the best combination for yielding optimal PSR, having both types does allow one to reap some of the benefits compared to using a pure PMOS input pair as was originally decided upon.

The first approach to sizing was to utilize the common standard of first having PMOS transistors generally being twice the size of the NMOS transistors since the mobility of electrons is larger than that of holes. Additionally, a common sizing scheme for a folded cascode amplifier topology was chosen. One adjustment that was made was using the course provided MATLAB code to calculate the optimal lengths. After using the MATLAB code, a length sizing was chosen such that $L_N = 450\text{nm}$ and $L_P = 225\text{nm}$. The width sizing for all the saturated transistors followed the regular logic where the drain current equation $I_D = \frac{1}{2}\mu c_{ox}\frac{W}{L}V_{OV}^2$ was used. By analyzing the optimal bias voltages necessary for the PMOS and NMOS tail transistors and the various nodes in the main amplifier network, a bias network was designed in Figure 1. Optimal biasing voltage is achieved for V_{BN_1} $(V_{OV} + V_{TH_n})$, V_{BN_2} $(2V_{OV} + V_{TH_n})$, and V_{BP_2} $(V_{DD} - |V_{TH_p}| - 2V_{OV})$. And thus we achieve an output swing of $[2V_{OV}, V_{DD} - 2V_{OV}]$. The triode transistors were sized to have a large length in order to ensure all the transistors were in saturation as V_{TH} decreases as length increases.

As can be seen in Tables 1 and 2, the sizing of the transistors relative to the small bias current resulted in an overall lower threshold voltage than the usual $V_{ov} \approx 200\text{mV}$. While the large sizing and small bias current works in this particular design, it is important to note that across various process sizes, temperature fluctuations, and other design variations, some of the transistors can very well turn off. In future design approaches, it would be prudent to keep in mind the relative order of magnitudes between the transistor sizings and the bias current in order to ensure any variations do not accidentally move transistors out of saturation. For the LDO schematic, since $\beta A_{EA0} \geq 1000 \rightarrow \beta \geq \frac{1000}{1955} = 0.5115$, β was chosen to be 0.75 since having β right at the edge of the inequality can be risky for the line regulation. With such a β value, $R_{F_1} = 100k\Omega$ and $R_{F_2} = 300k\Omega$. Not only do the resistor values play a part in determining β, they also affect the stability of the LDO as they play a role in the poles, which ultimately affects the bandwidth. Furthermore, the PMOS transistor of the second stage was also sized with this consideration in mind.

2 Amplifier Schematic and Simulated Performance

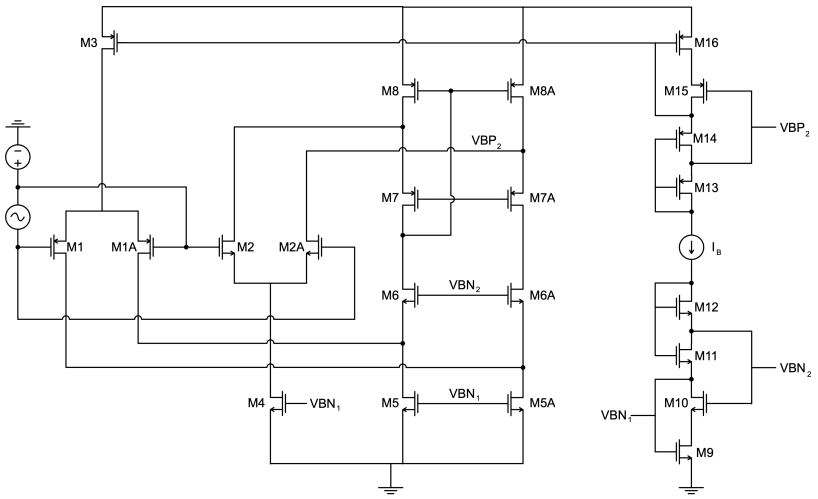

Figure 1: Complete Error Amplifier Schematic with $I_B = 780$nA

Device	Type	Width (m)	Length (m)	$g_m\left(\frac{A}{V}\right)$	$\lvert\Delta\rvert$(V)	$\lvert I_{DS}\rvert$ (A)
M1, M1A	PMOS	1.62μ	225n	14μ	4.581m	908.1n
M7, M7A	PMOS	1.62μ	225n	17.56μ	28.02m	908.1n
M8, M8A	PMOS	1.62μ	225n	31.05μ	66.6m	3.677μ
M13	PMOS	1.62μ	225n	16.68μ	18.1m	780n
M15	PMOS	1.62μ	225n	16.36μ	24.77m	780n
M16	PMOS	1.62μ	225n	16.1μ	26.73m	780n
M2, M2A	NMOS	810μ	450n	18.29μ	30.1m	3.062μ
M6, M6A	NMOS	810μ	450n	17.68μ	35.91m	3.062μ
M9	NMOS	810μ	450n	16.23μ	40.44m	780n
M10	NMOS	810μ	450n	16.57μ	35.26m	780n
M12	NMOS	810μ	450n	17.04μ	26.27m	3.062μ
M3	PMOS	3.24μ	225n	27.76μ	21m	1.816μ
M4	NMOS	1.62μ	450n	35.19μ	43.4m	6.125μ
M5, M5A	NMOS	1.62μ	450n	31.5μ	40.49m	1.522μ

Table 1. Saturated Transistors Table

Device	Type	Width (m)	Length (m)	$g_m\left(\frac{A}{V}\right)$	$\lvert\Delta\rvert$ (V)	$\lvert I_{DS}\rvert$ (A)
M11	NMOS	270n	3.24μ	3.924μ	308.9m	780n
M14	PMOS	540n	3.24μ	2.764μ	475.1m	-780n

Table 2. Triode Transistors Table

Design Parameter/Variable	Simulated Performance	Specification
Input Voltage	1.8V	$\leq$ 1.8V
Output Voltage	1.0V - 1.4V	1.0V - 1.4V
Load Current	1mA - 15mA	1mA - 15mA
DC Load Regulation	[-39.4μV/mA, -6.5μV/mA]	$\leq$ 50μV/mA
DC Line Regulation	[741μV/V, 876μV/V]	$\leq$ 1mV/V
Quiescent Current (I_L = 1mA/I_L = 15mA)	2.533μA, 2.533μA	Minimum
PSR (@ F_{in} = 1KHz/F_{in} = 1MHz)	2.499, 2.282	-
Worst-case PSR	2.499	-
DC Loop Gain (I_L = 1mA/I_L = 15mA)	84.18dB, 78.85dB	-
Loop-gain Unity Gain Frequency (I_L = 1mA/I_L = 15mA)	3.536MHz, 3.308MHz	-
Loop-gain Phase Margin (I_L = 1mA/I_L = 15mA)	59.63°, 84.06°	-
Loop-gain Gain Margin (I_L = 1mA/I_L = 15mA)	29.46dB, 31.85dB	-
Output Noise (I_L = 1mA/I_L = 15mA)	49.14E-9, 41.30E-9	-

Table 2. Performance Summary

3 Transient Response

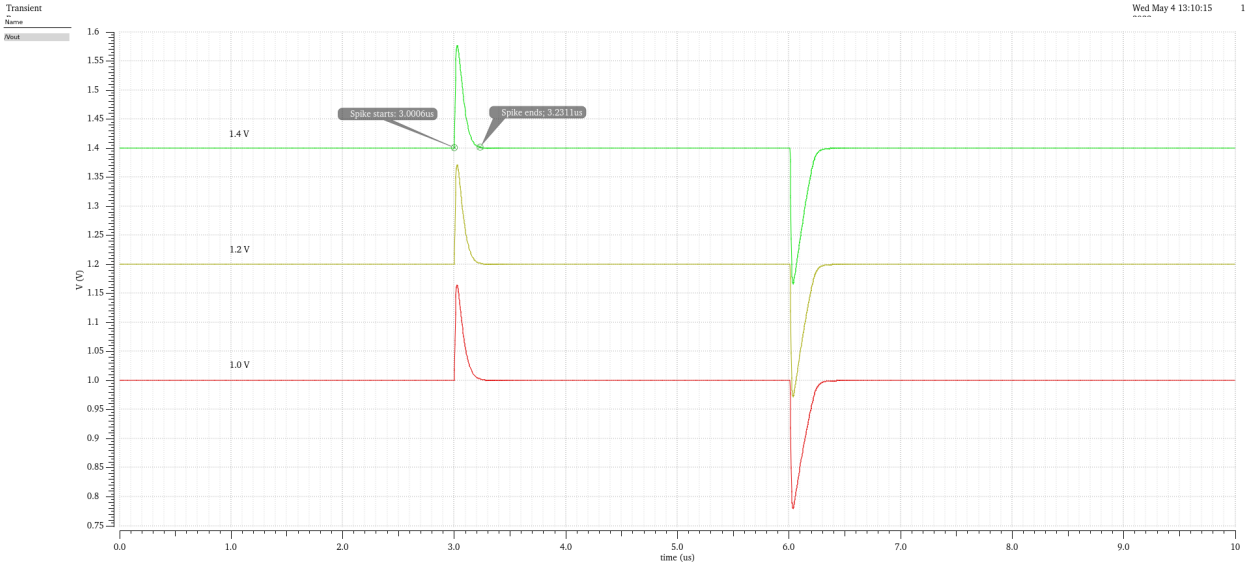

Figure 2: The transient response for $V_{OUT} = 1, 1.2, 1.4$V is shown. There is a brief spike up and down of about 0.175V and 0.225V respectively that occurs for $\sim 0.2305\mu$s for all output voltage values.

4 Loop-gain AC Response

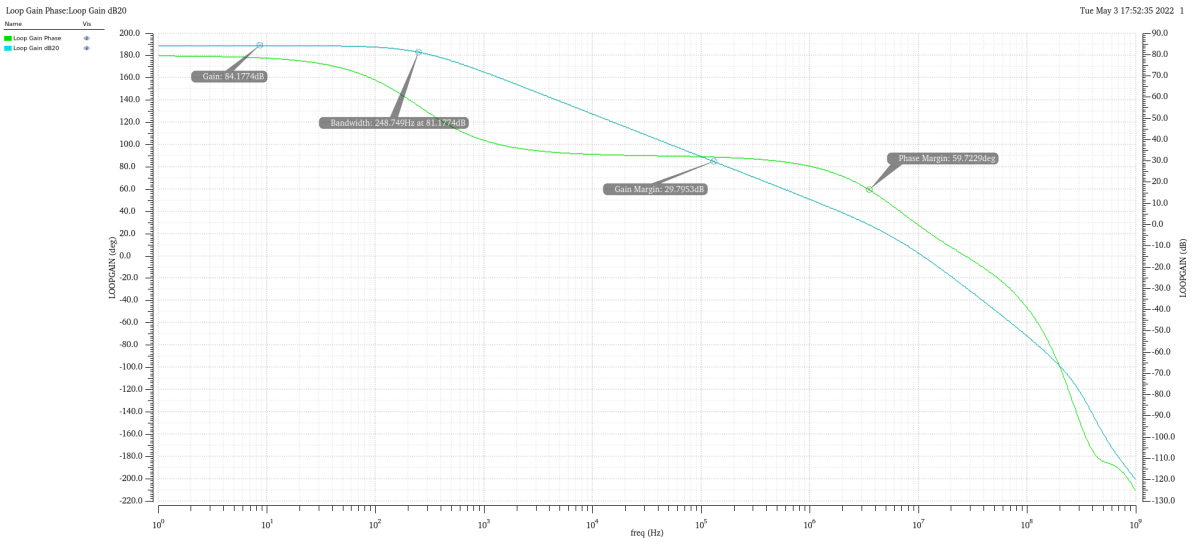

Figure 3: AC loop gain with $I_{\text{load}} = 1mA$; At a lower load current, one can observe that there is slightly higher gain, lower bandwidth, and lower phase margin.

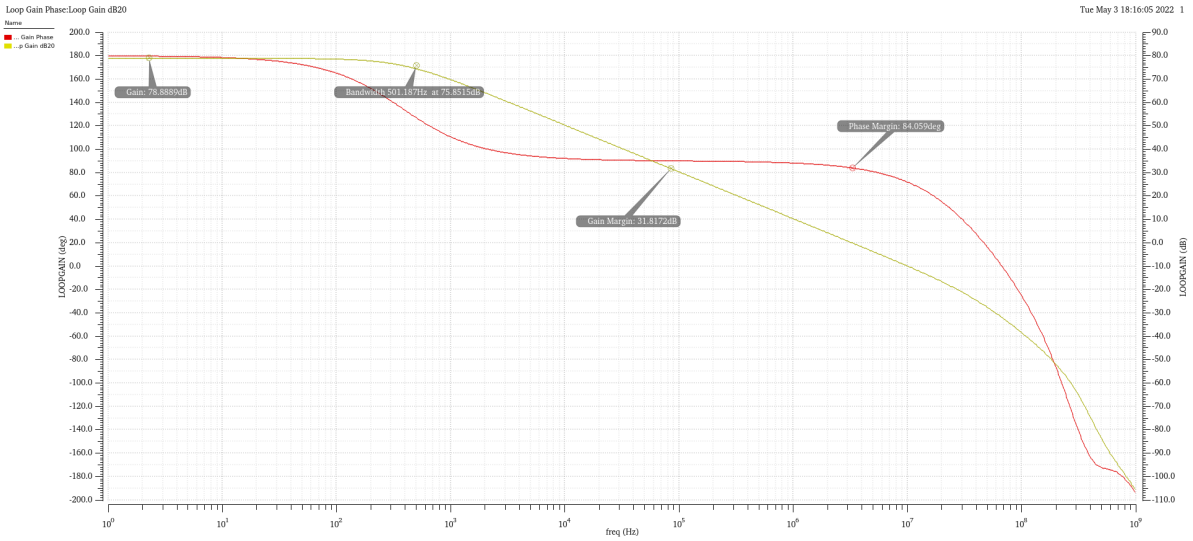

Figure 4: AC loop gain with $I_{\text{load}} = 15mA$; At a higher load current, one can observe that there is slightly lower gain, higher bandwidth, and higher phase margin. These trade-offs are considerations the user can take when using this LDO design.

5 DC Load Regulation and Line Regulation

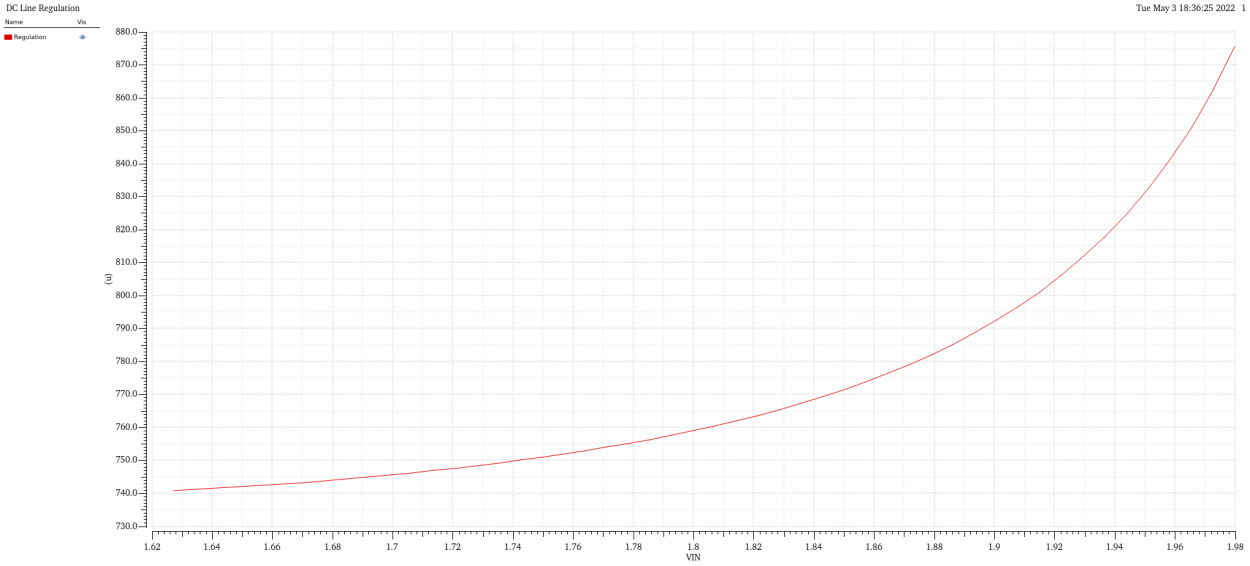

Figure 5: The DC Line Regulation varies from about 740mV/V to 875mV/V, which is underneath the 1mV/V specification.

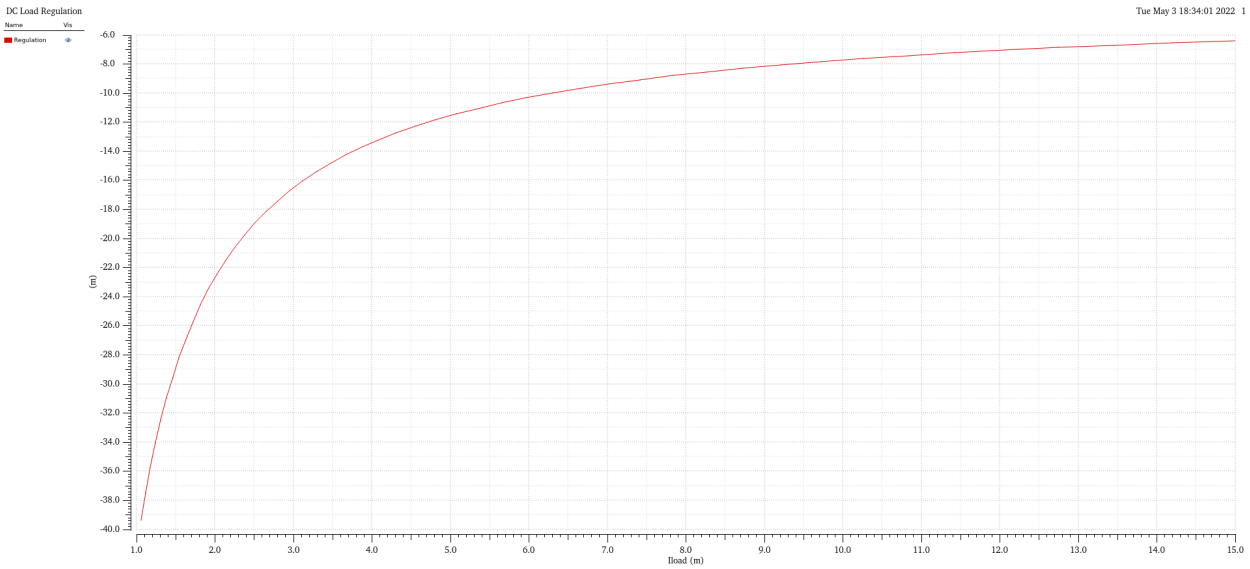

Figure 6: The DC Load Regulation varies from about 7μV/mA to 38μV/mA, which is underneath the 50μV/mA specification.

6 Power Supply Rejection and Output Noise

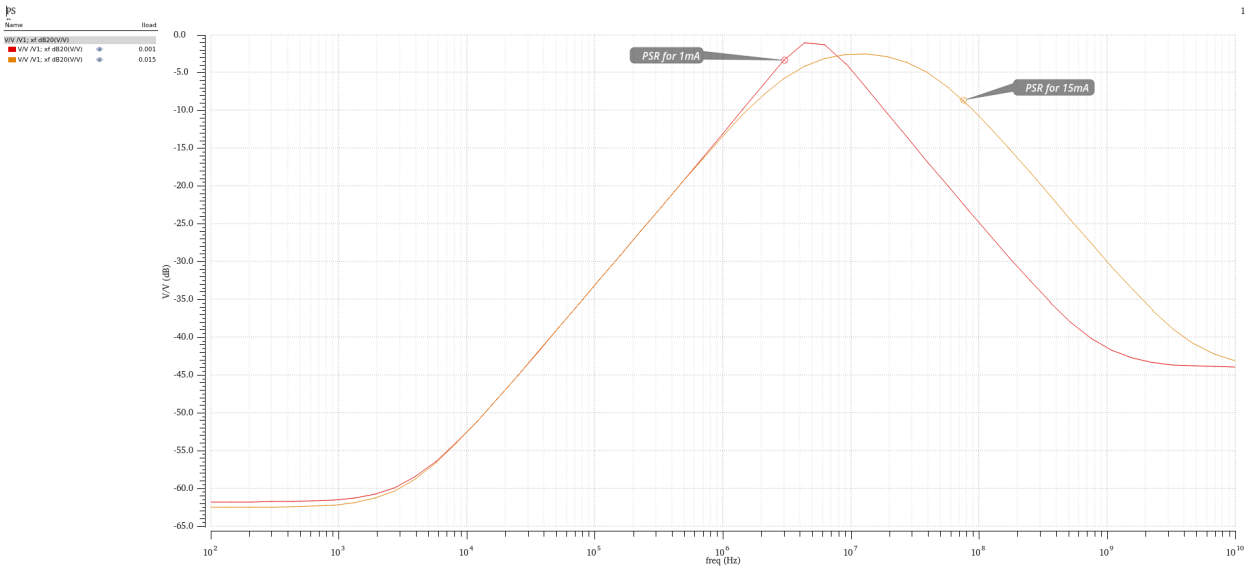

Figure 7: PSR for $I_{\text{load}} = 1mA, 15mA$; The location of ω_o is shifted towards the right as the load current increases.

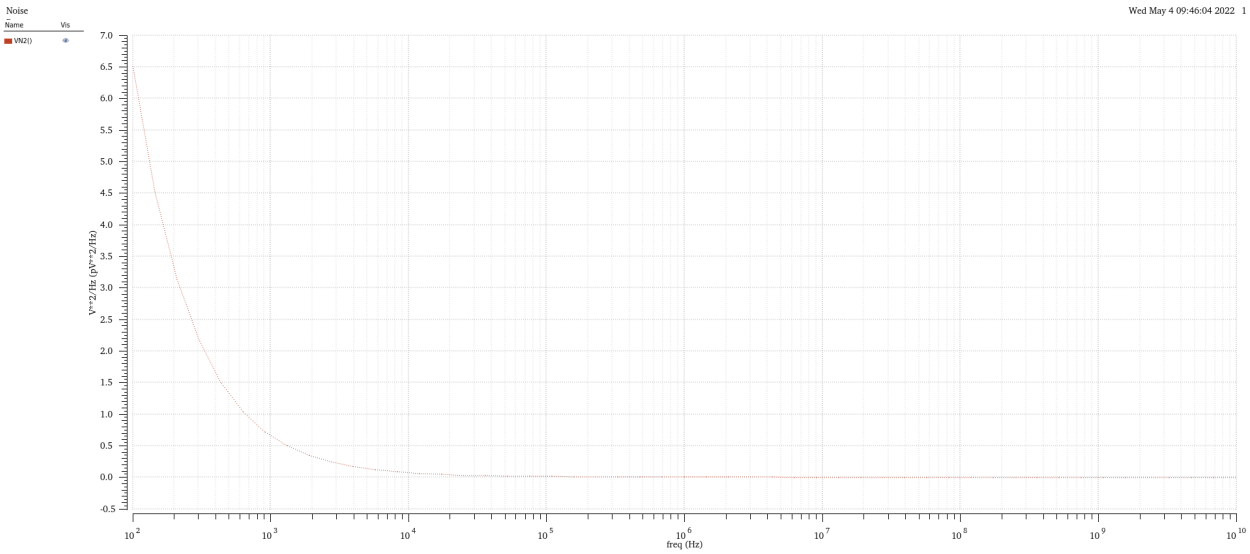

Figure 8: Output Noise: Except at very low frequencies, the output noise is at a near constant minimum value.