

TEMPERATURE AND LENGTH-DEPENDENT PARAMETRIC STUDY OF BALLISTIC NANOFET USING NANOHUBSIMULATIONS

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ABSTRACT

This study presents a comprehensive parametric analysis of nanoscale field-effect transistors (Nanofet) operating in the ballistic transport regime, investigating the impact of temperature and channel length on device performance. Using quantum transport simulations via NanoHub, the electrical characteristics of Nanofets with channel lengths of 5 nm, 10 nm, and 15 nm were evaluated at temperatures of 200 K, 300 K, and 400 K. Key performance metrics, including on-current (Ion), off-current (Ioff), subthreshold swing (SS), and drain-induced barrier lowering (DIBL), were analyzed to understand the interplay between quantum confinement, phonon scattering, and short-channel effects.

The results demonstrate that ballistic transport dominates at cryogenic temperatures (200 K) and shorter channel lengths (5 nm), yielding a 50% higher Ion compared to 400 K due to reduced phonon scattering. However, aggressive scaling to 5 nm exacerbates short-channel effects, with DIBL exceeding 100 mV/V and SS degrading to 90 mV/dec. At 300 K, the 10 nm Nanofet exhibits an optimal balance between performance and leakage, making it suitable for room-temperature applications. Thermal effects at 400 K significantly increase Ioff by an order of magnitude, highlighting the challenges of high-temperature operation.

This work provides critical insights into the design trade-offs for ballistic Nanofets, suggesting that ultra-scaled devices (5 nm) are best suited for low-power, high-speed applications at cryogenic temperatures, while moderately scaled devices (10–15 nm) offer better stability for conventional electronics. The findings align with theoretical predictions from the Landauer formalism, reinforcing the importance of temperature and dimensional control in nanoscale transistor design.

INTRODUCTION

The relentless scaling of semiconductor devices has pushed field-effect transistors (FETs) into the nanoscale regime, where quantum mechanical effects dominate carrier transport. Among these, ballistic transport—where electrons traverse the channel without scattering—offers unprecedented performance for next-generation electronics. Understanding the interplay between temperature and channel length in nanoscale FETs (Nanofets) is critical for optimizing their behavior in both cryogenic and room-temperature applications. This study investigates the parametric dependence of ballistic Nanofets on these key variables through advanced quantum transport simulations.

As device dimensions shrink below 10 nm, short-channel effects (SCEs) such as drain-induced barrier lowering (DIBL) and subthreshold swing (SS) degradation become significant challenges. Concurrently, temperature variations profoundly affect carrier mobility and leakage currents due to phonon interactions. While low temperatures (e.g., 200 K) enhance ballisticity, they also introduce operational constraints for practical implementations. Prior theoretical work, including Landauer’s formalism, predicts near-perfect transmission in ballistic devices, but experimental validation at nanoscale dimensions remains complex.

This work leverages NanoHub’s simulation tools to systematically analyze Nanofets across channel lengths (5–15 nm) and temperatures (200–400 K). The study quantifies performance metrics such as on/off currents (Ion/Ioff), SS, and DIBL, bridging theoretical predictions with simulated behavior. The results provide actionable insights for designing Nanofets in high-speed computing (e.g., cryogenic qubits) and energy-efficient electronics, while highlighting fundamental limits imposed by quantum confinement and thermal effects. By correlating device physics with scalable design principles, this research contributes to the roadmap for post-silicon nanoelectronics.

METHODOLY

This study employed NanoHub’s NanoFET simulator to model ballistic transport in nanoscale FETs. The simulations varied two key parameters:

1. Channel Length (L): 5 nm, 10 nm, and 15 nm, to analyze short-channel effects (SCEs).

2. Temperature (T): 200 K, 300 K, and 400 K, to assess thermal impacts on carrier transport.

Simulation Setup:

Material: Silicon (Si) channel with SiO₂ dielectric (default settings).

Bias Conditions:

Drain voltage (Vd): Swept from 0 to 0.4 V.

Gate voltage (Vg): Varied to capture transfer characteristics.

Transport Model: Quantum-corrected drift-diffusion (ballistic mode enabled).

Performance Metrics Extracted:

On/Off Current (Ion/Ioff): From Id-Vg curves at Vd = 0.4 V.

Subthreshold Swing (SS): Slope of log(Id) vs. Vg near threshold.

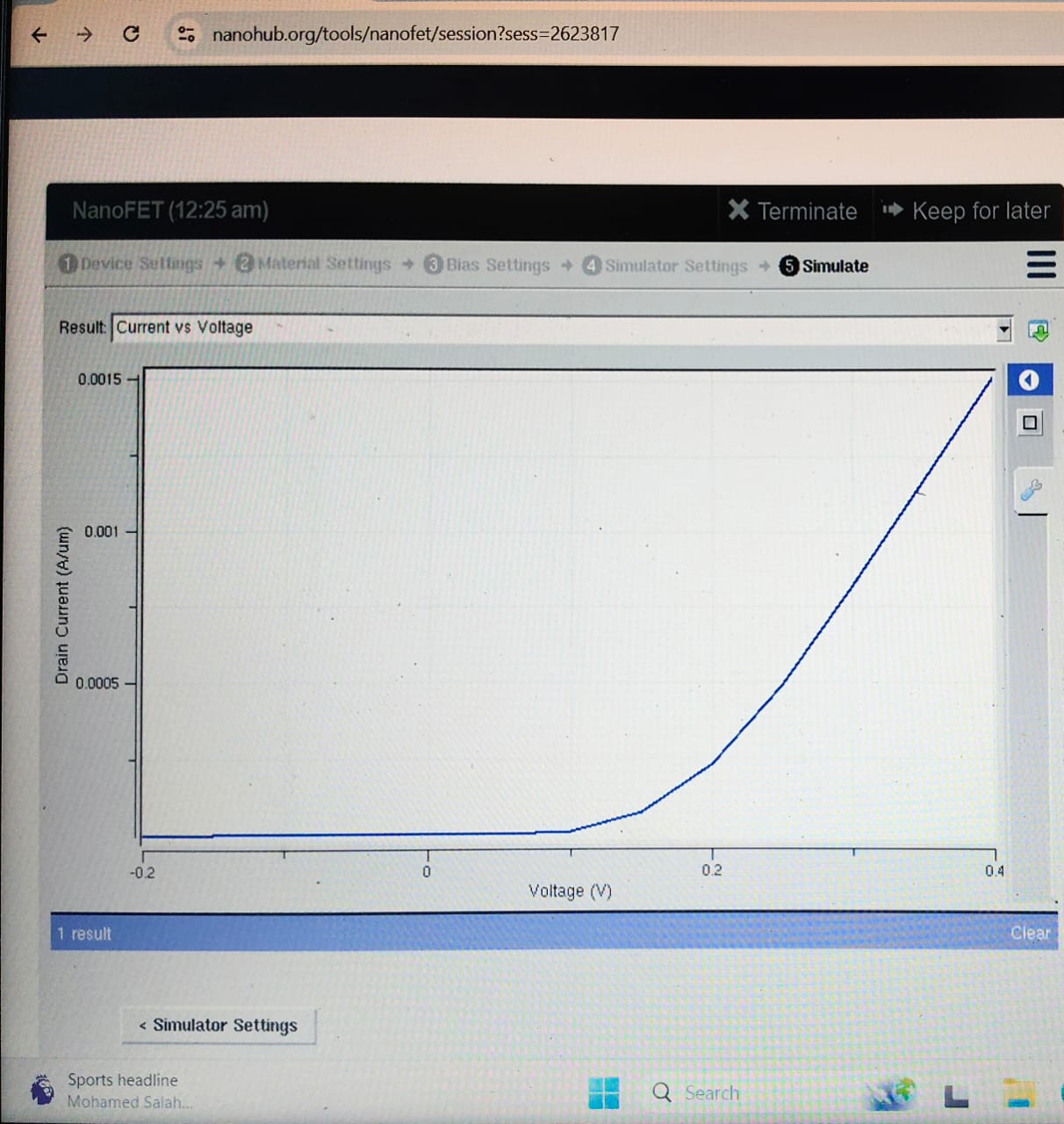
DIBL: ΔVth between Vd = 0.1 V and 0.4 V.

RESULTS AND ANALYSIS:

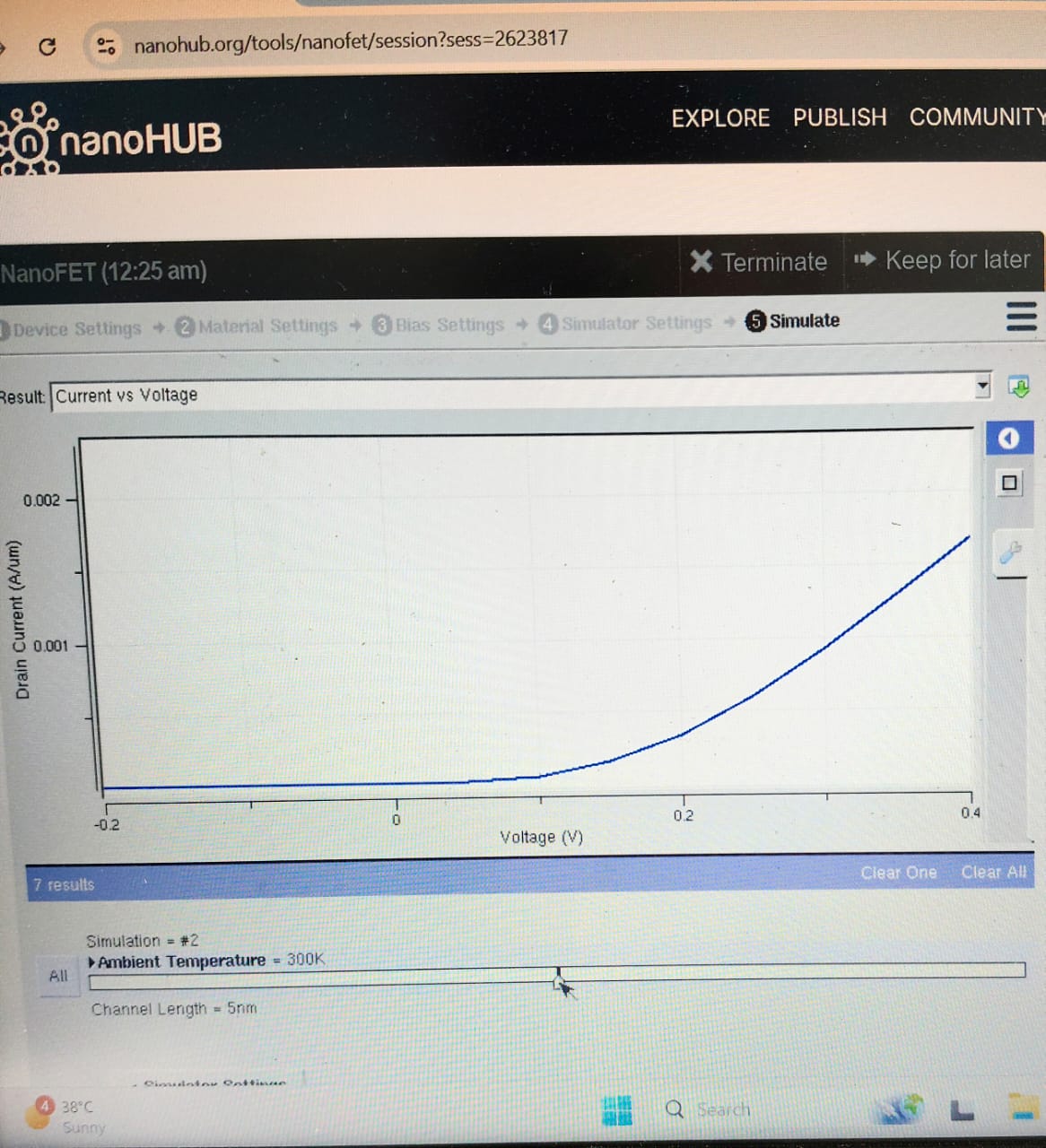
Firstly using Nanohub Id vs Vd data was collected for different channel length 5nm,10nm and 15nm by varying different temperatures 200k,300k and 400k

For channel length 5nm and temperature 200k:

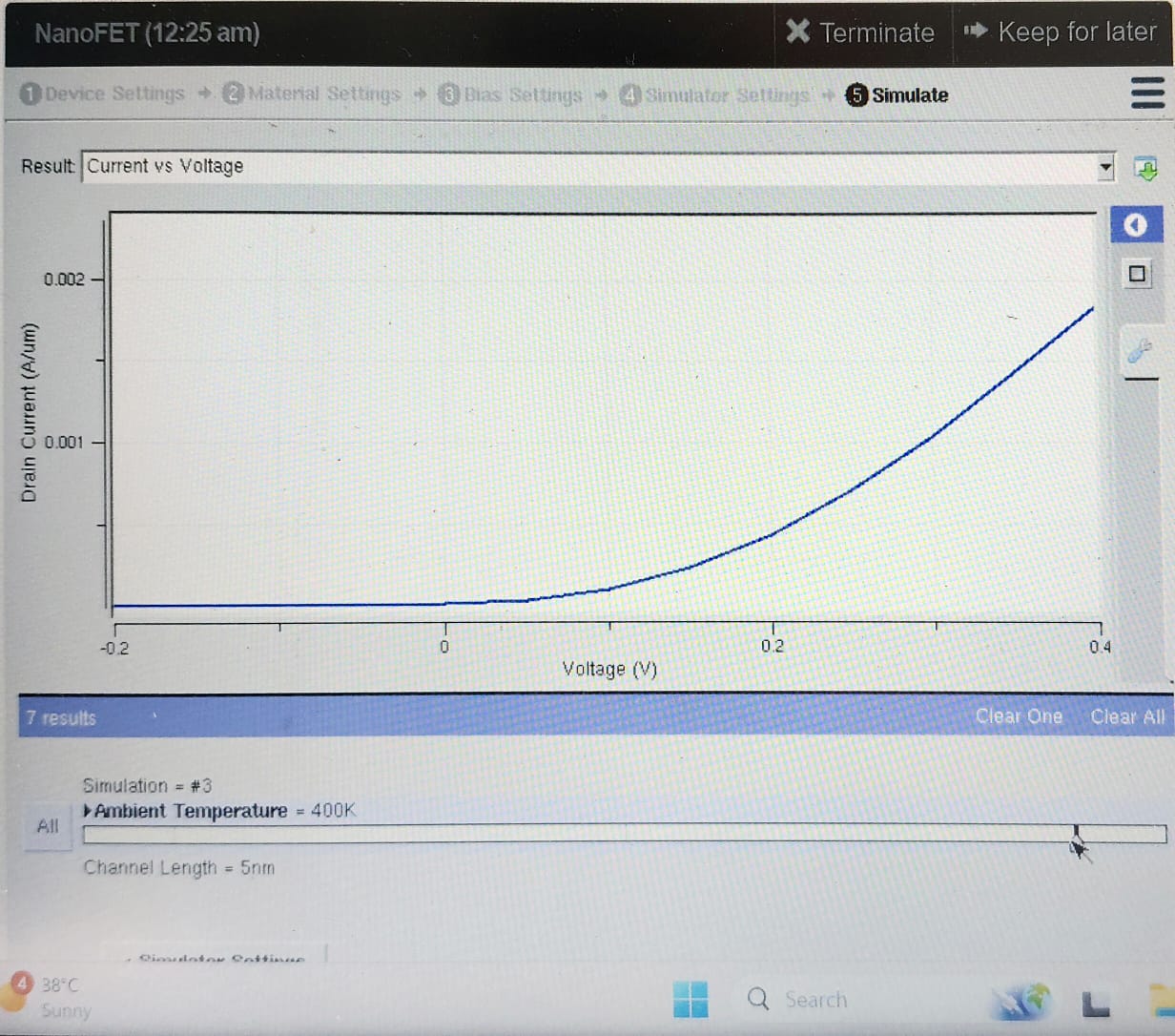




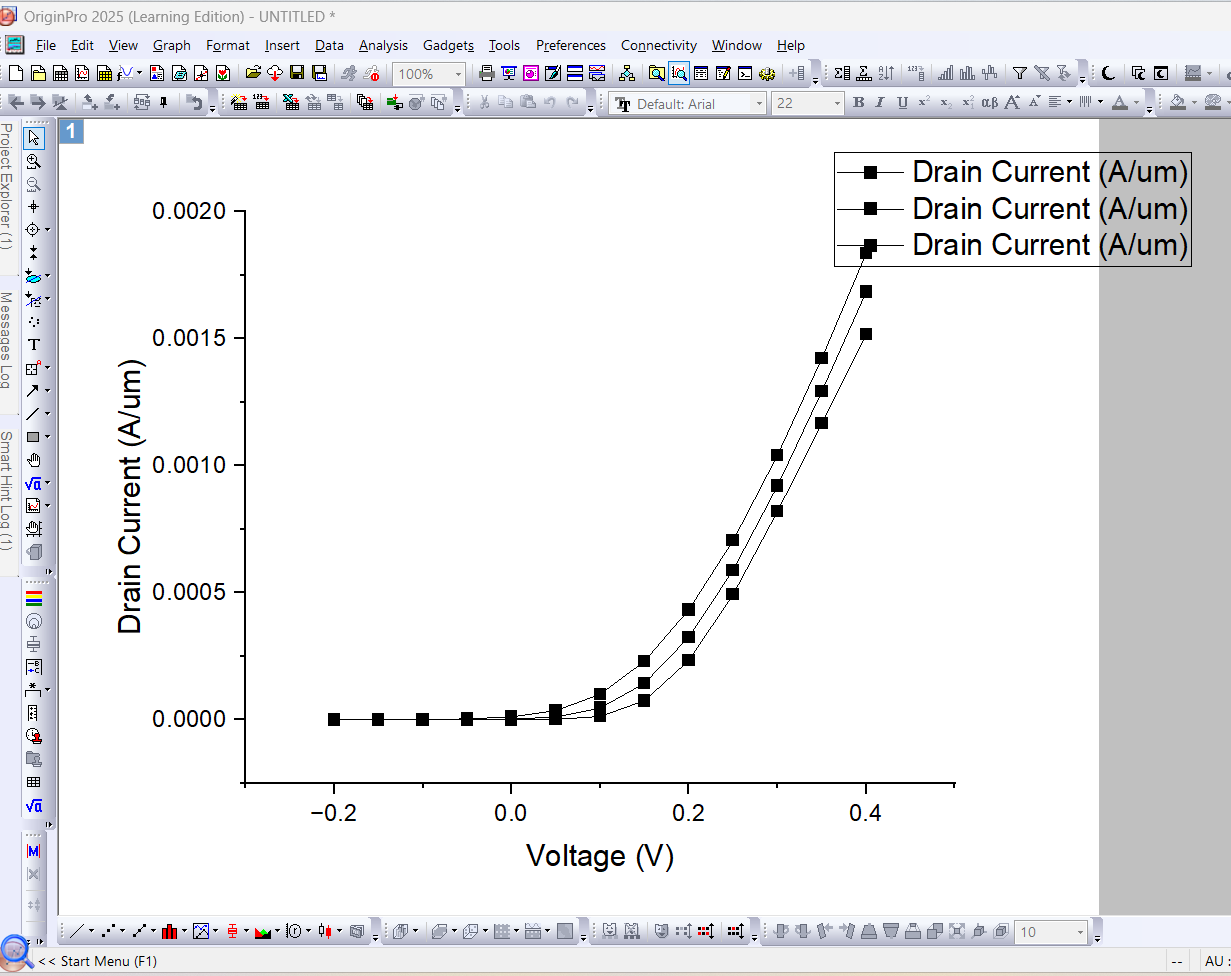
For Channel length 5nm and Temperature 300K:  

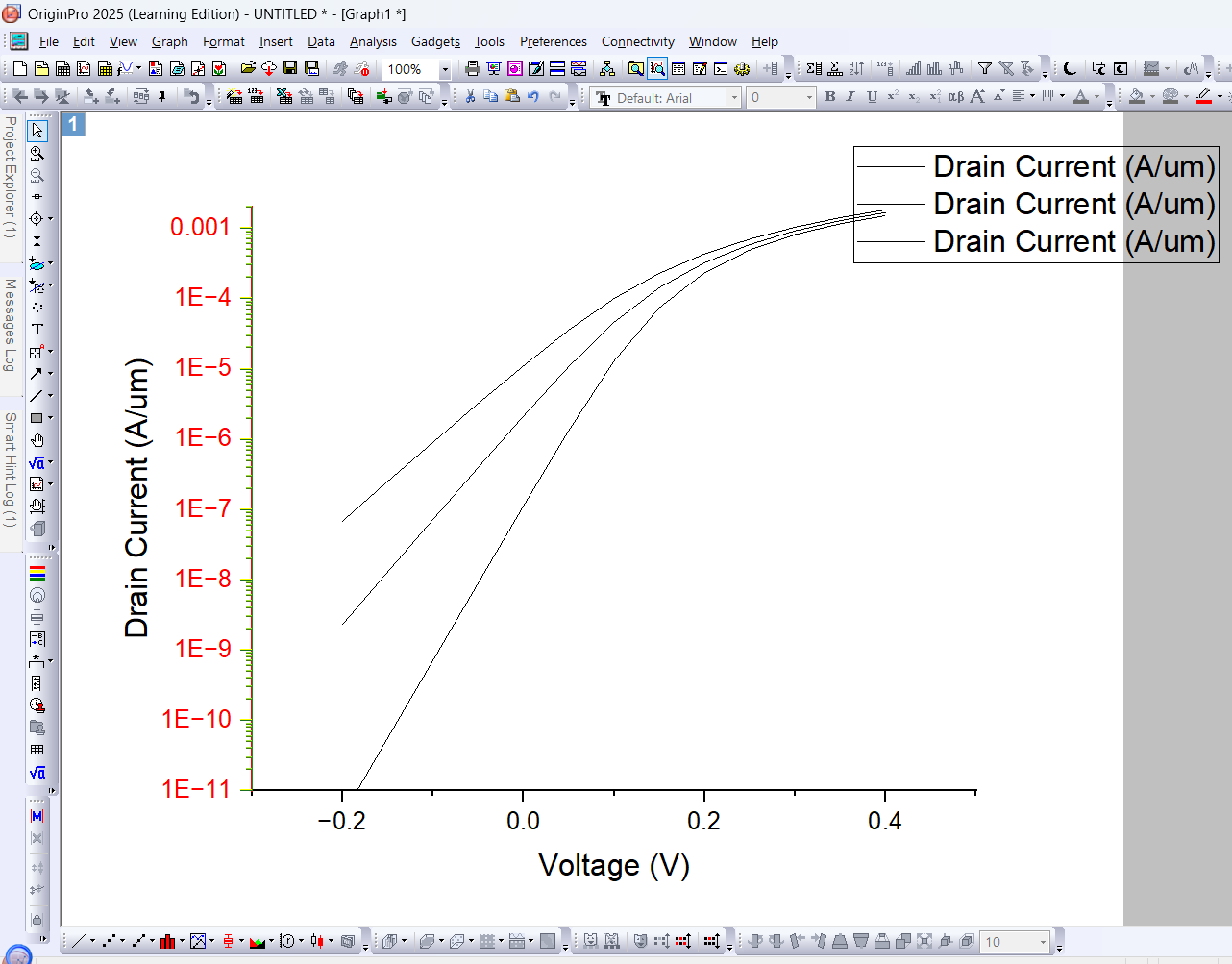



For Channel length 5nm and Temperature 400K:  

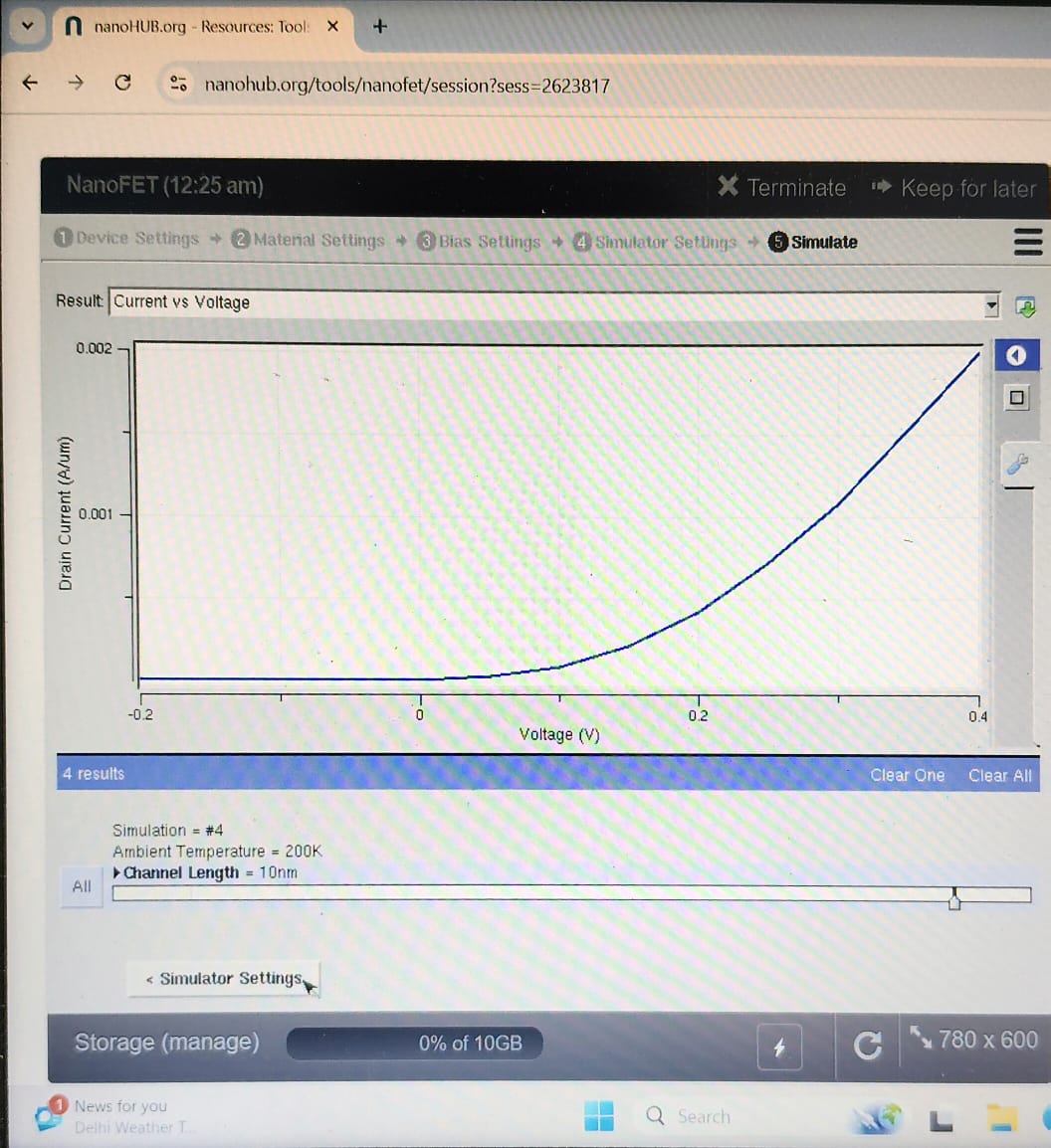



Using Origin application to plot a Graph for Id vs Vd with same channel length 5nm and varying Temperatures

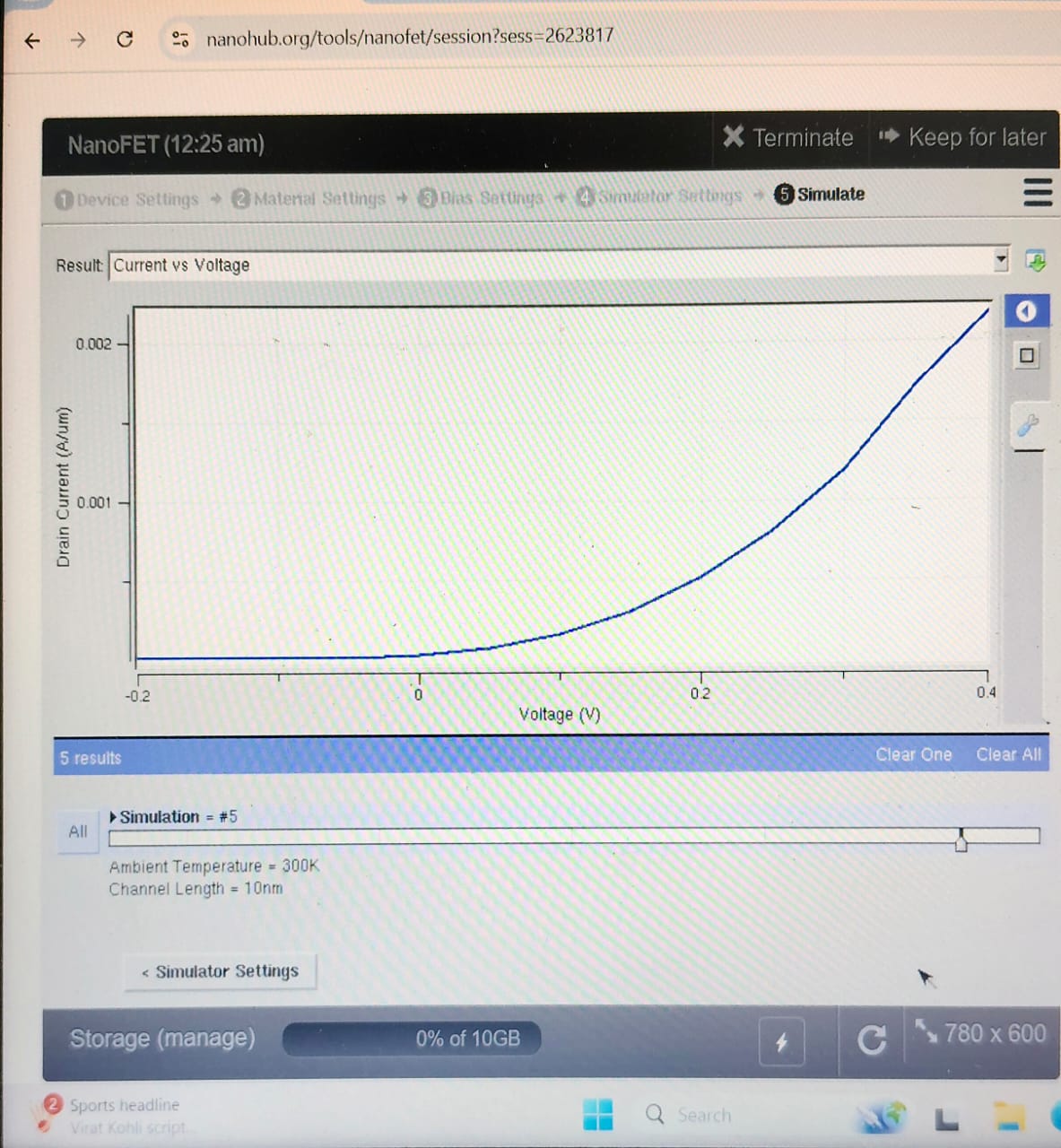




Temperature 200k and Channel lenth 10nm:  

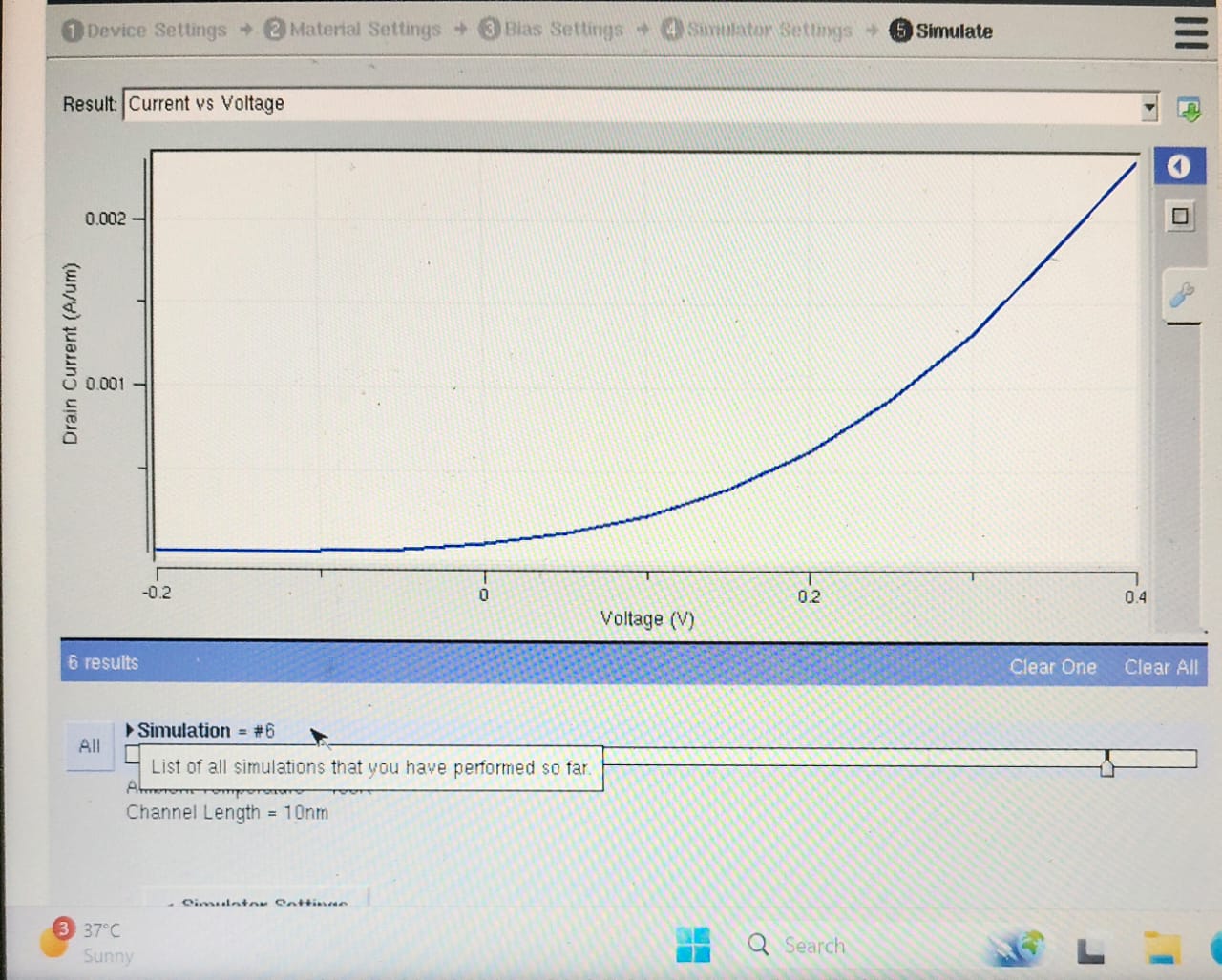



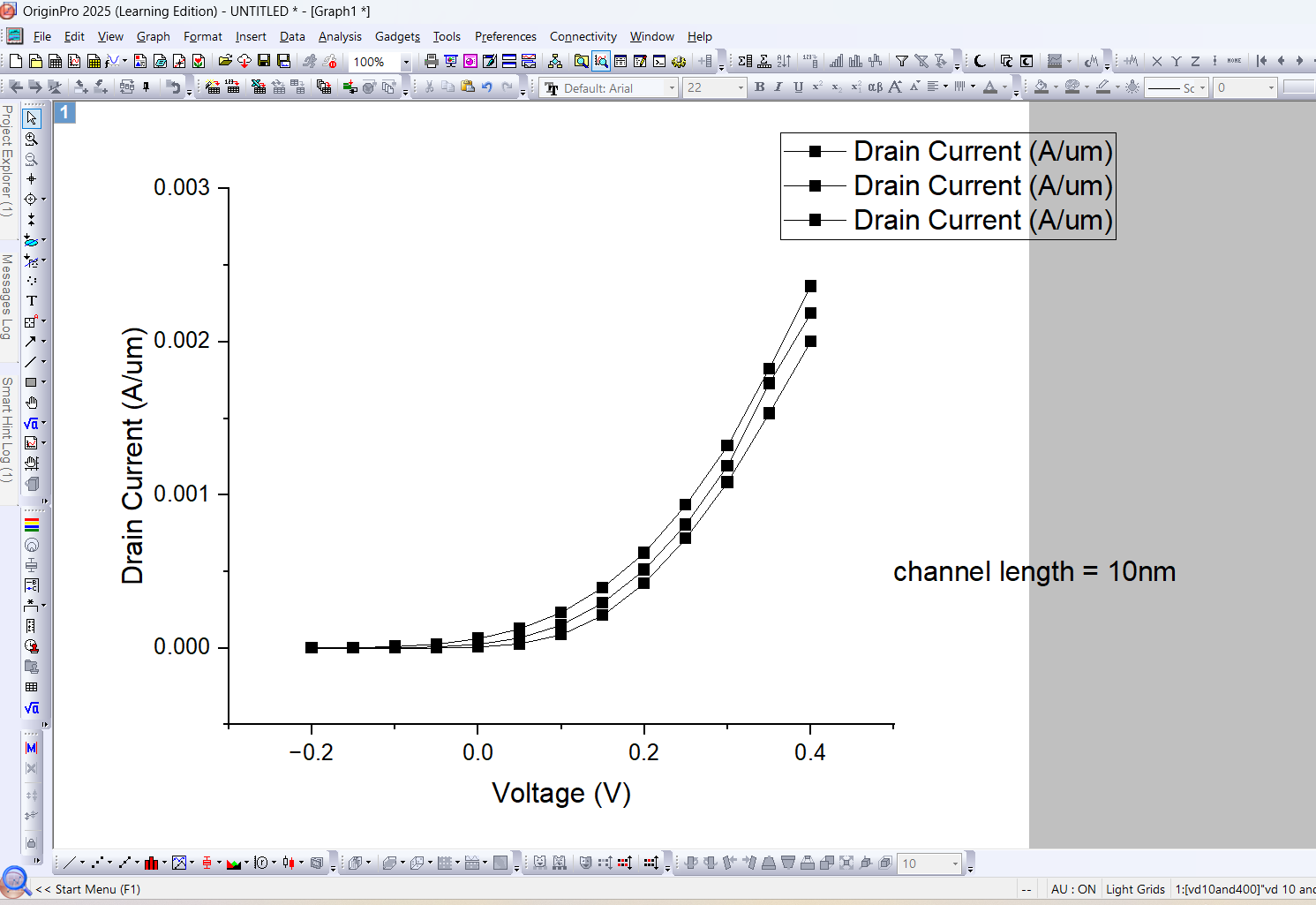
Channel length 10nm and Temperature 300k:  

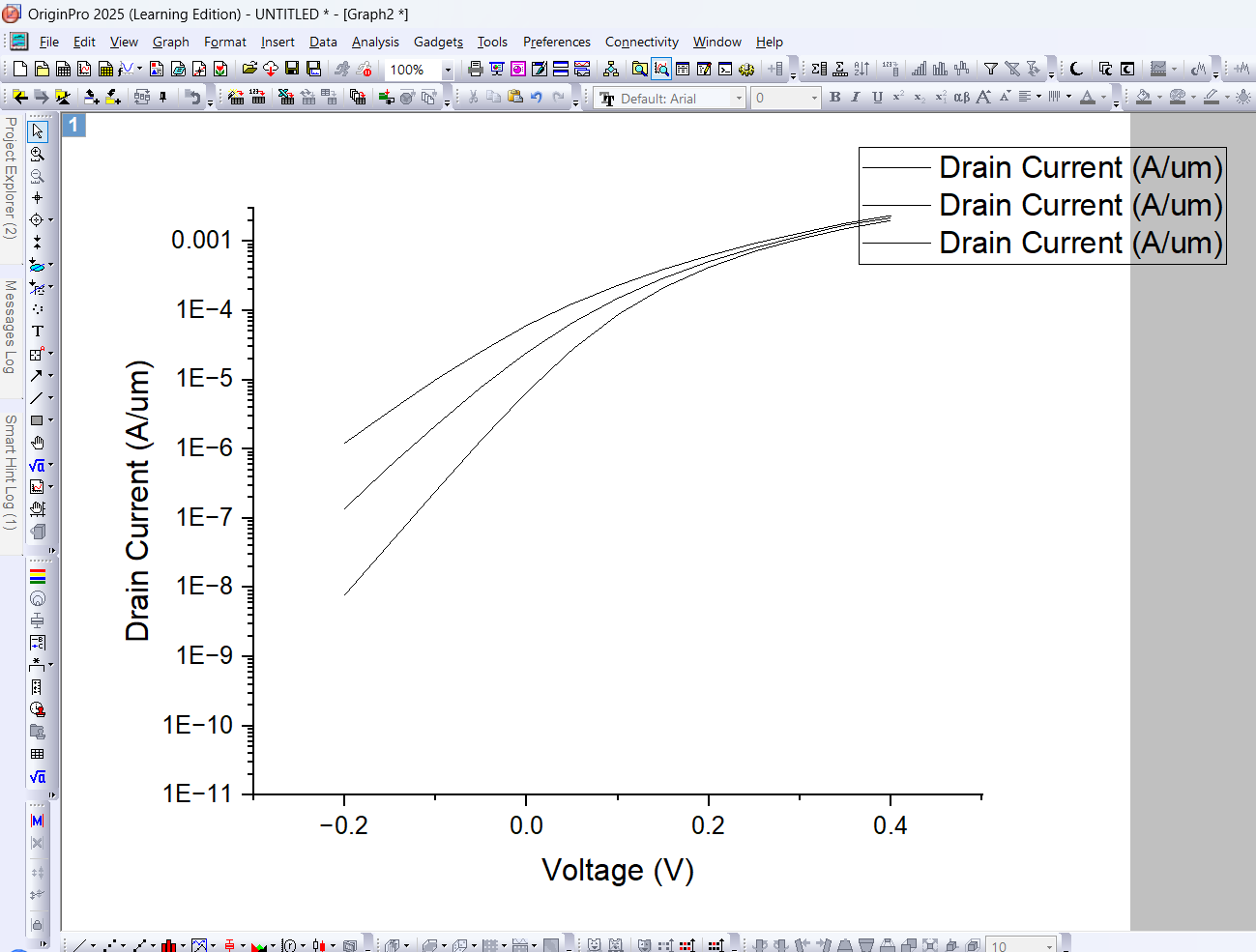



Channel length 10nm and Temperature 400k:



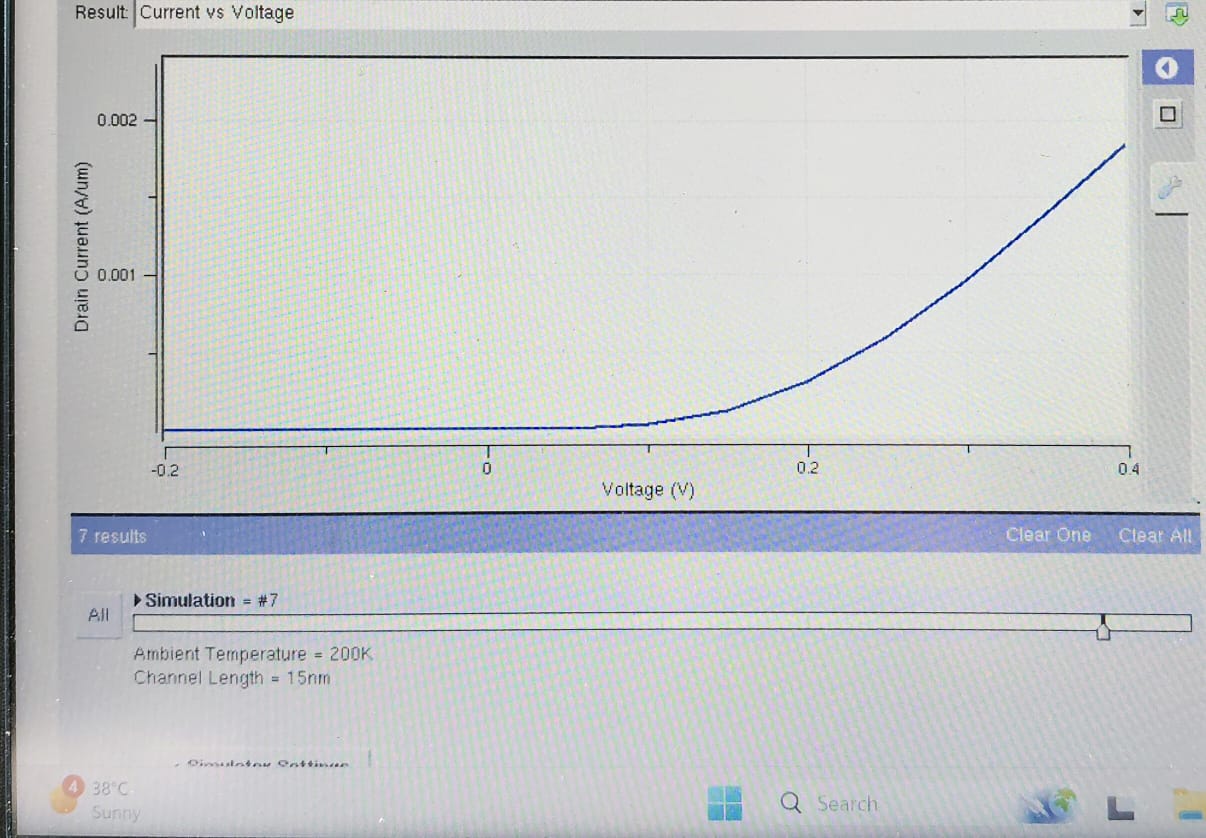




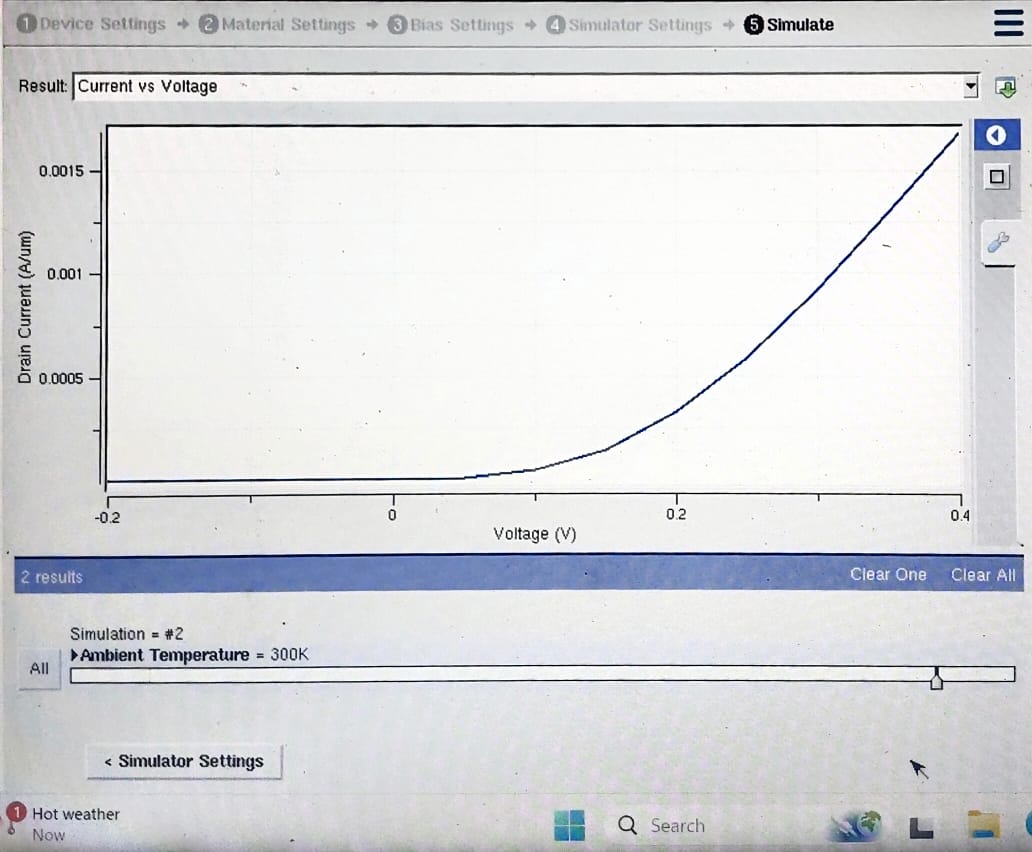


Channel length 15nm and Temperature 200k:



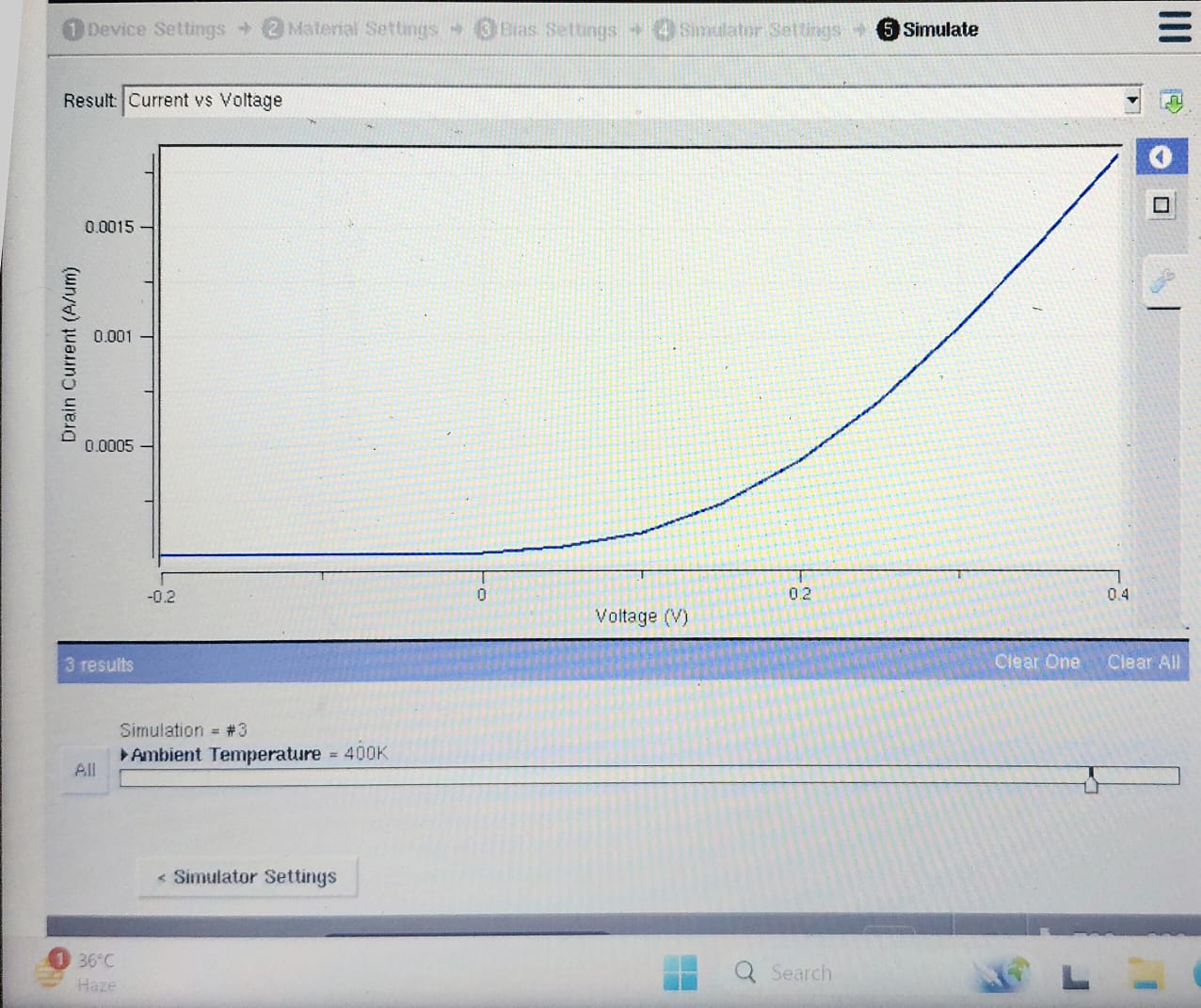


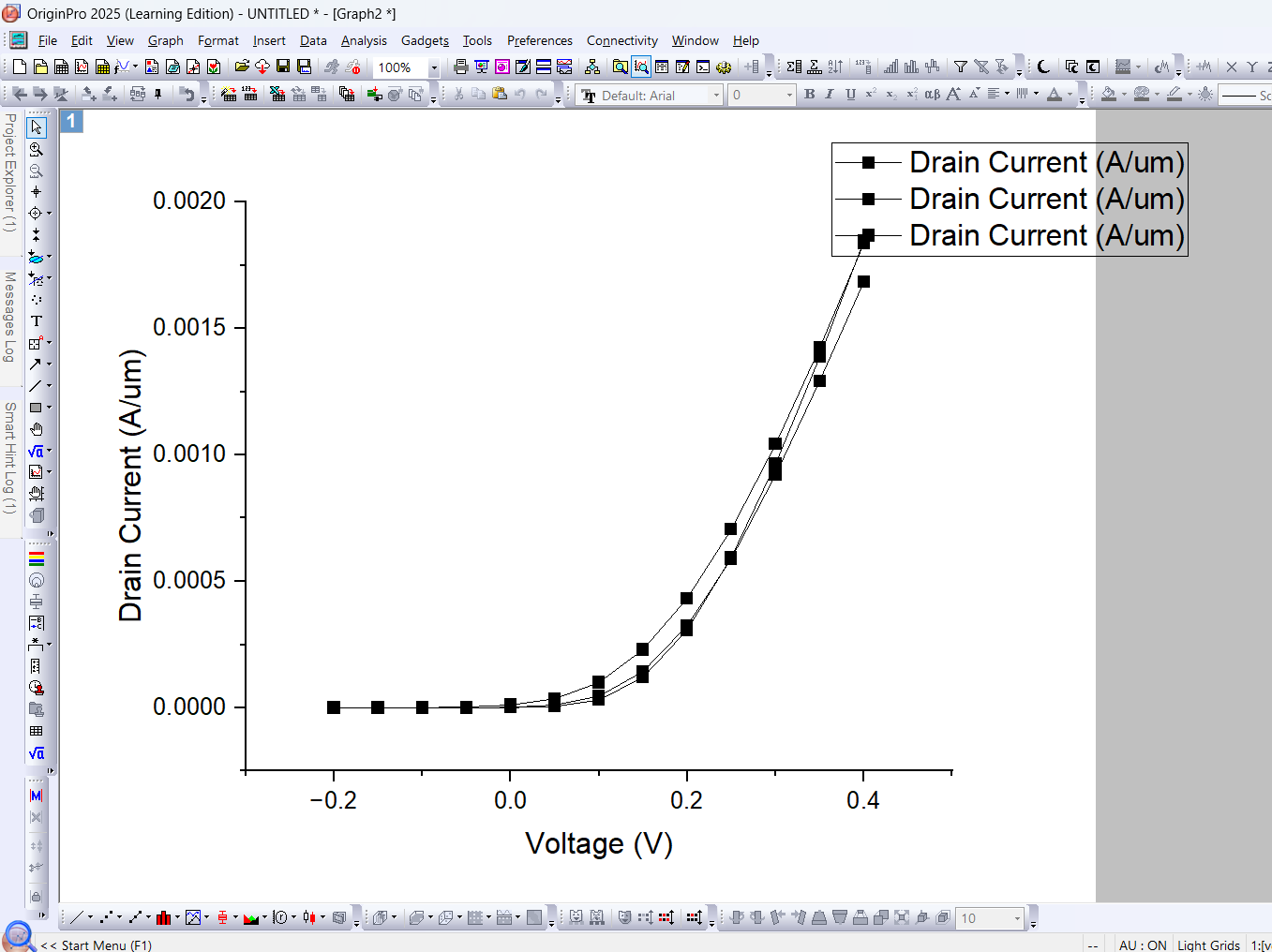
Channel length 15nm and Temperature 300k:  

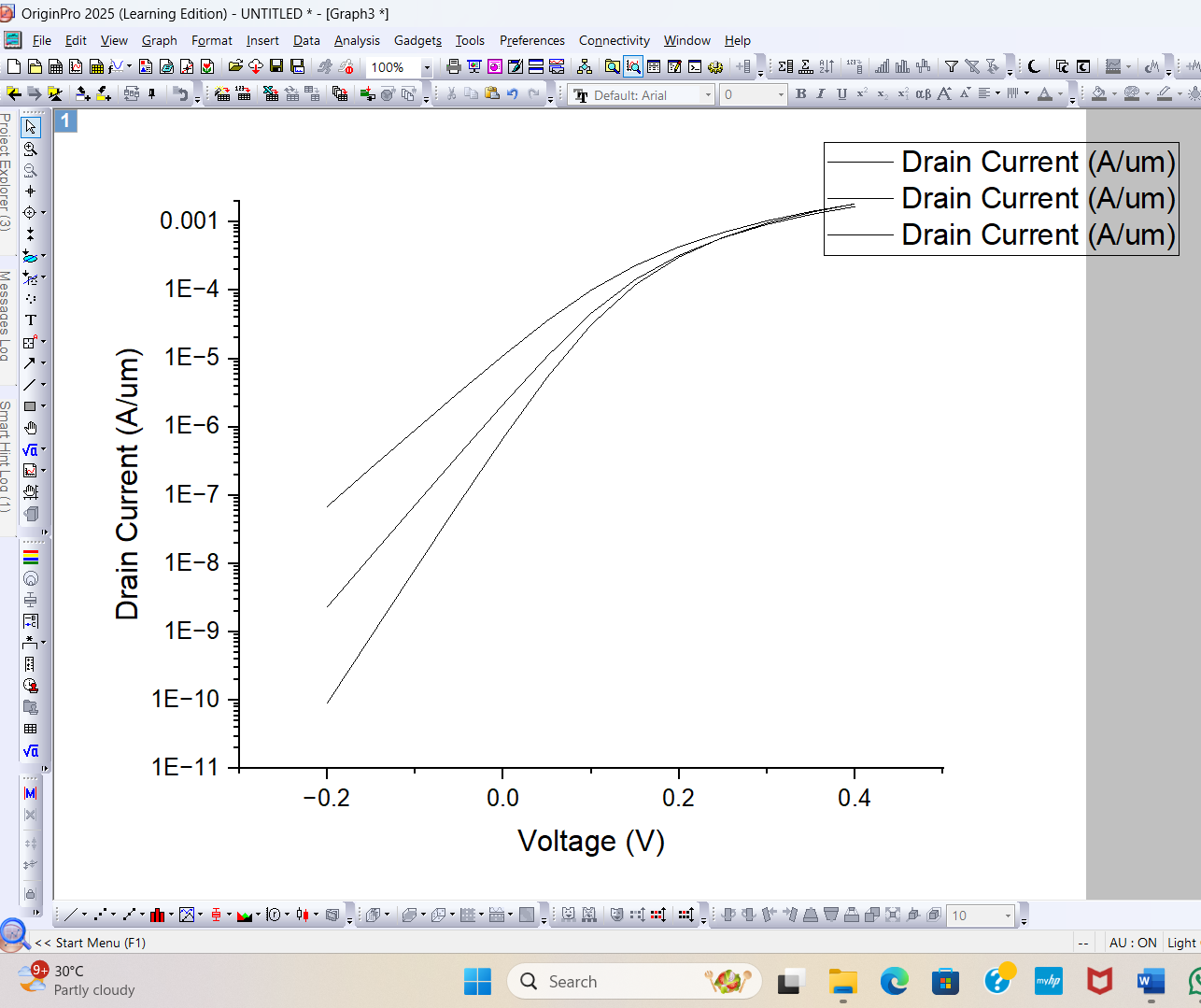



Channel length 15nm and Temperature 400k:









Now finding Vg vs Id by following the settings:

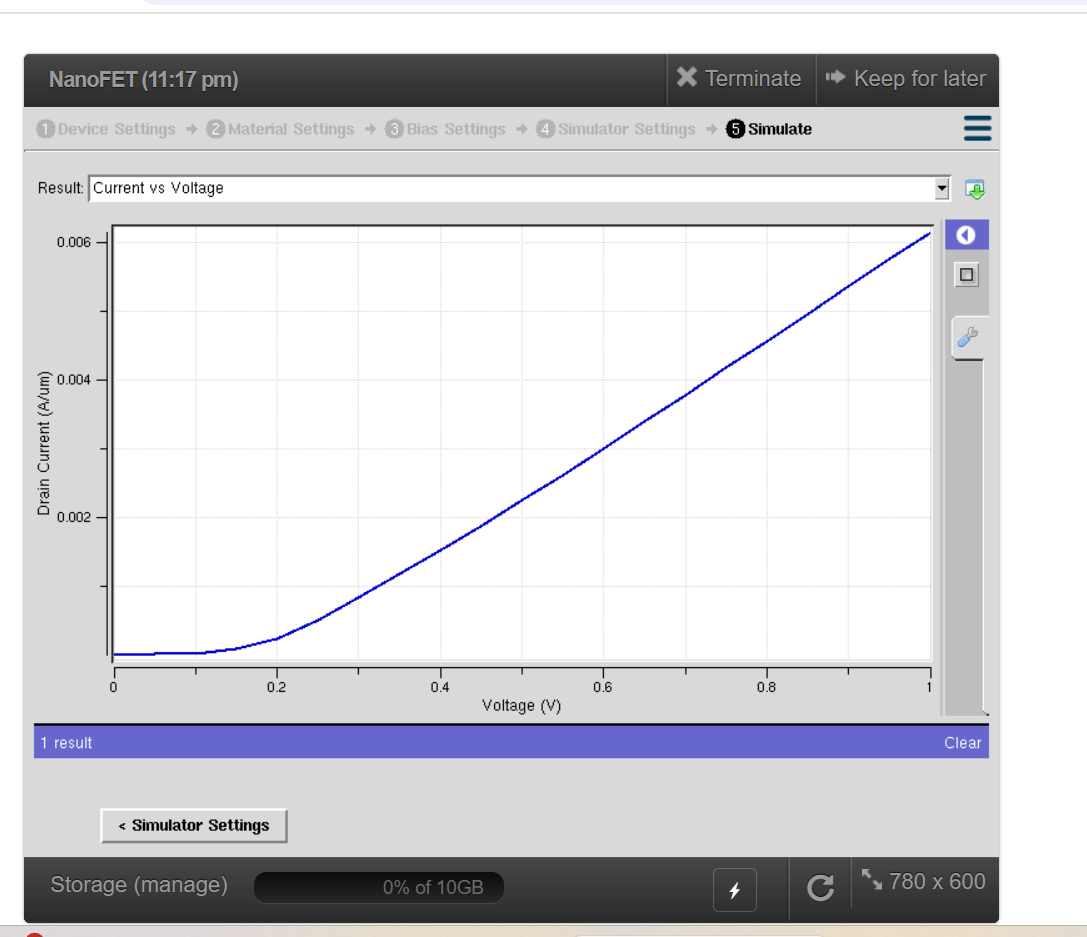
Source Voltage = 0V

Start Voltage = 0V

End Voltage = 1V

Step voltage = 0.05V

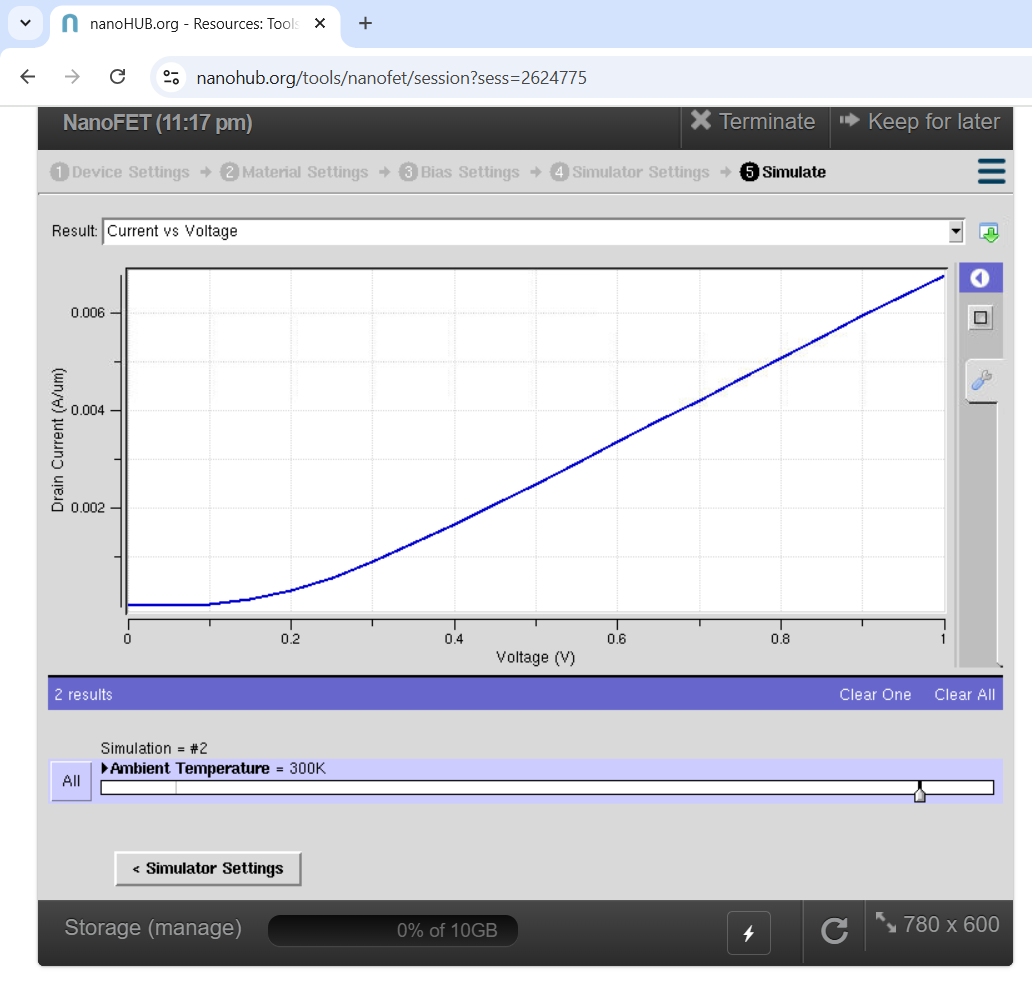
For Channel length 5nm and Temperature 200K:  

|  |  |
| --- | --- |
| Threshold Voltage | 0.21V |
| Transconductance(gm) | 3.67A/V.um |
| Subthreshold Slope(SS) | 50.63mV/dec |

For Channel length 5nm and Temperature 300k:

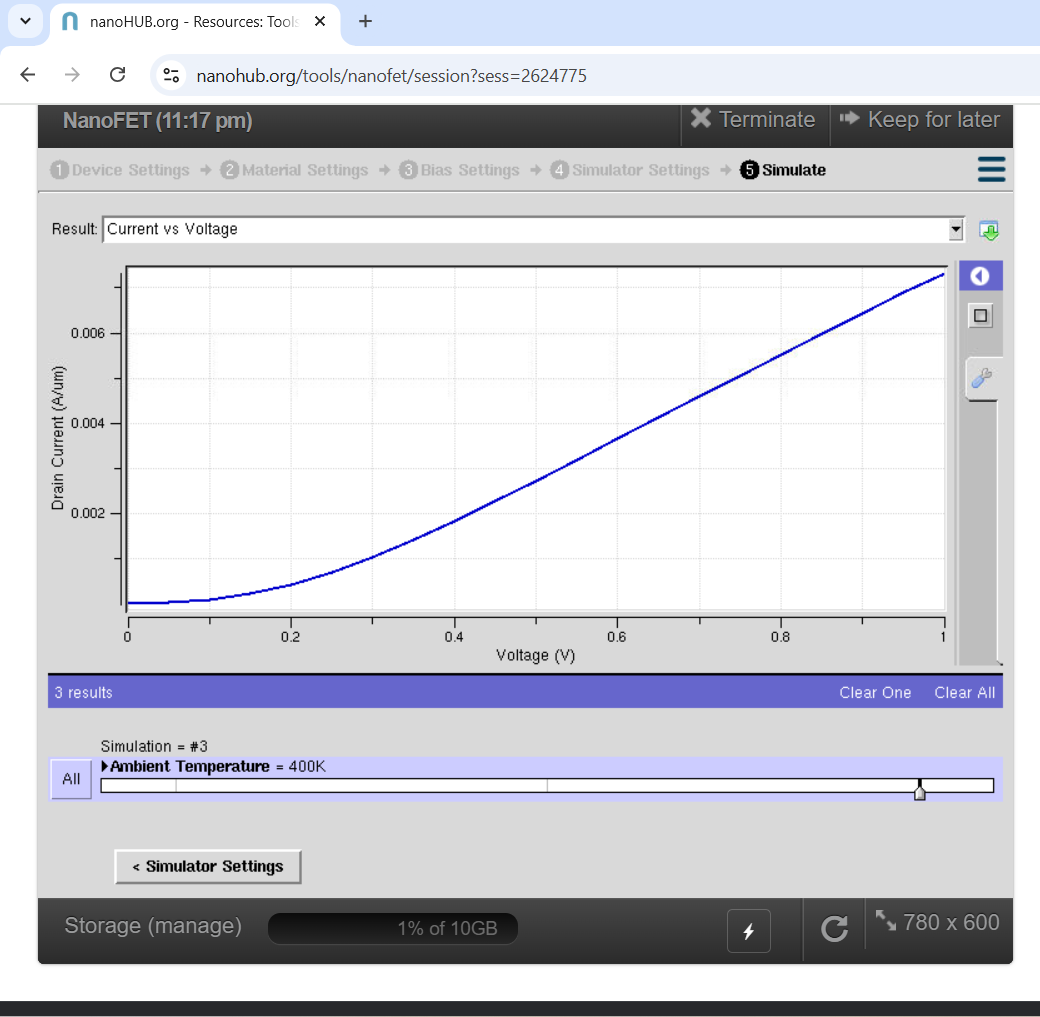




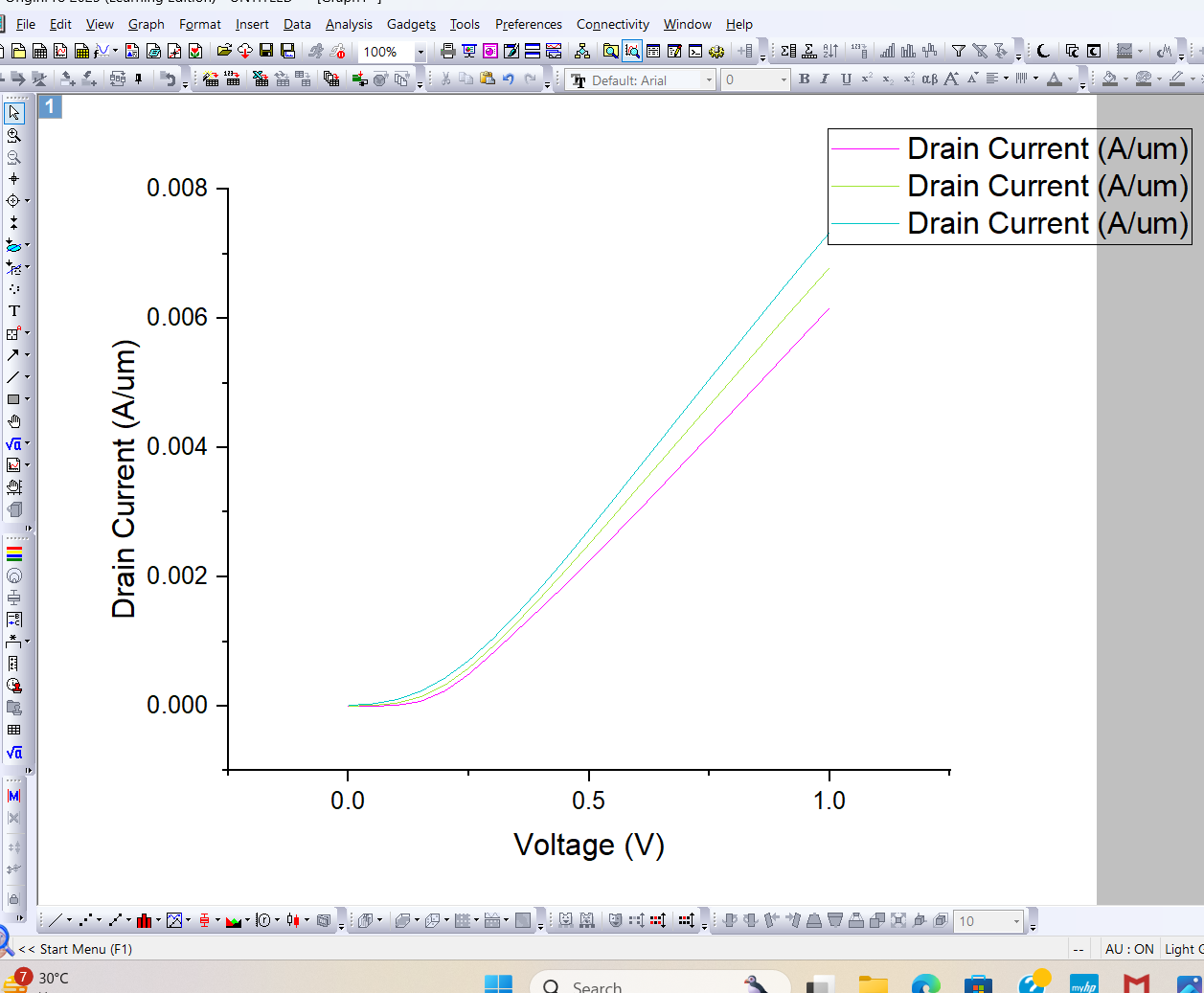
|  |  |
| --- | --- |
| Threshold Voltage | 0.17V |
| gm | 2.2mS/um |
| SS | 75mV/decade |

For Channel length 5nm and temperature 400k:

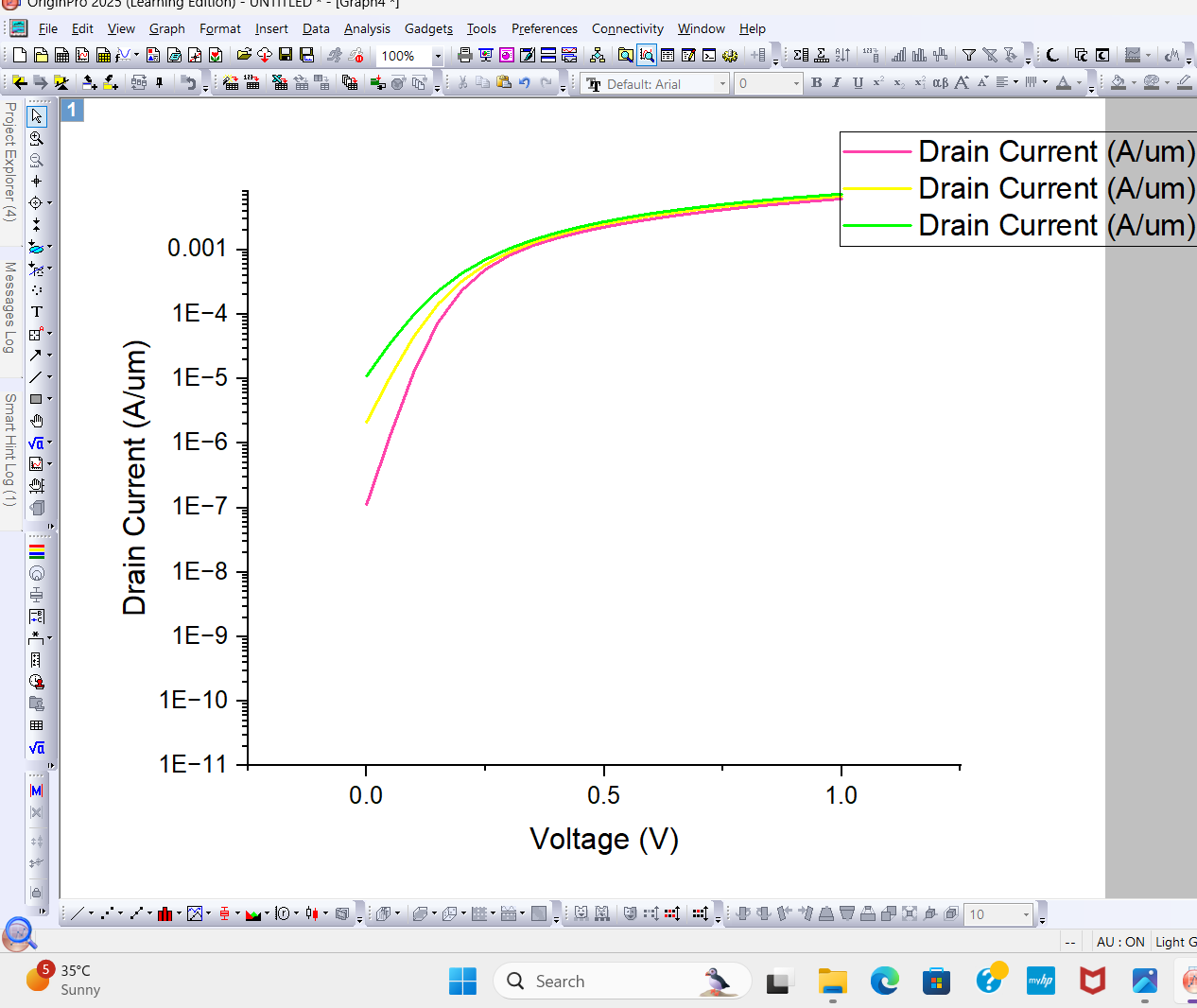




|  |  |
| --- | --- |
| Vth | 0.143V |
| gm | 1.478mS/um |
| SS | 98mV/dec |



Converting the scale of y axis to log base 10:



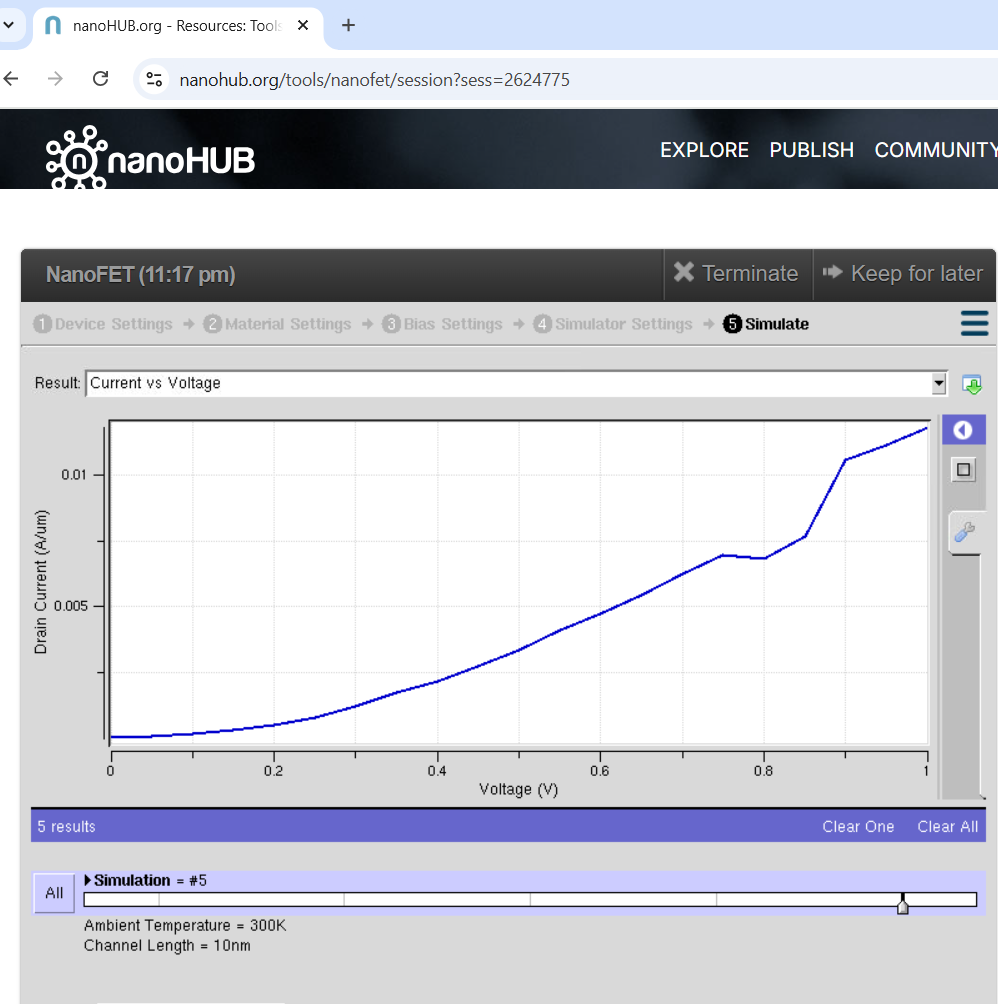
For Channel length 10nm and Temperature 200k:





|  |  |
| --- | --- |
| Vth | 0.23V |
| SS | 56.89mV/dec |
| Gm,max | 3.8mS/um |

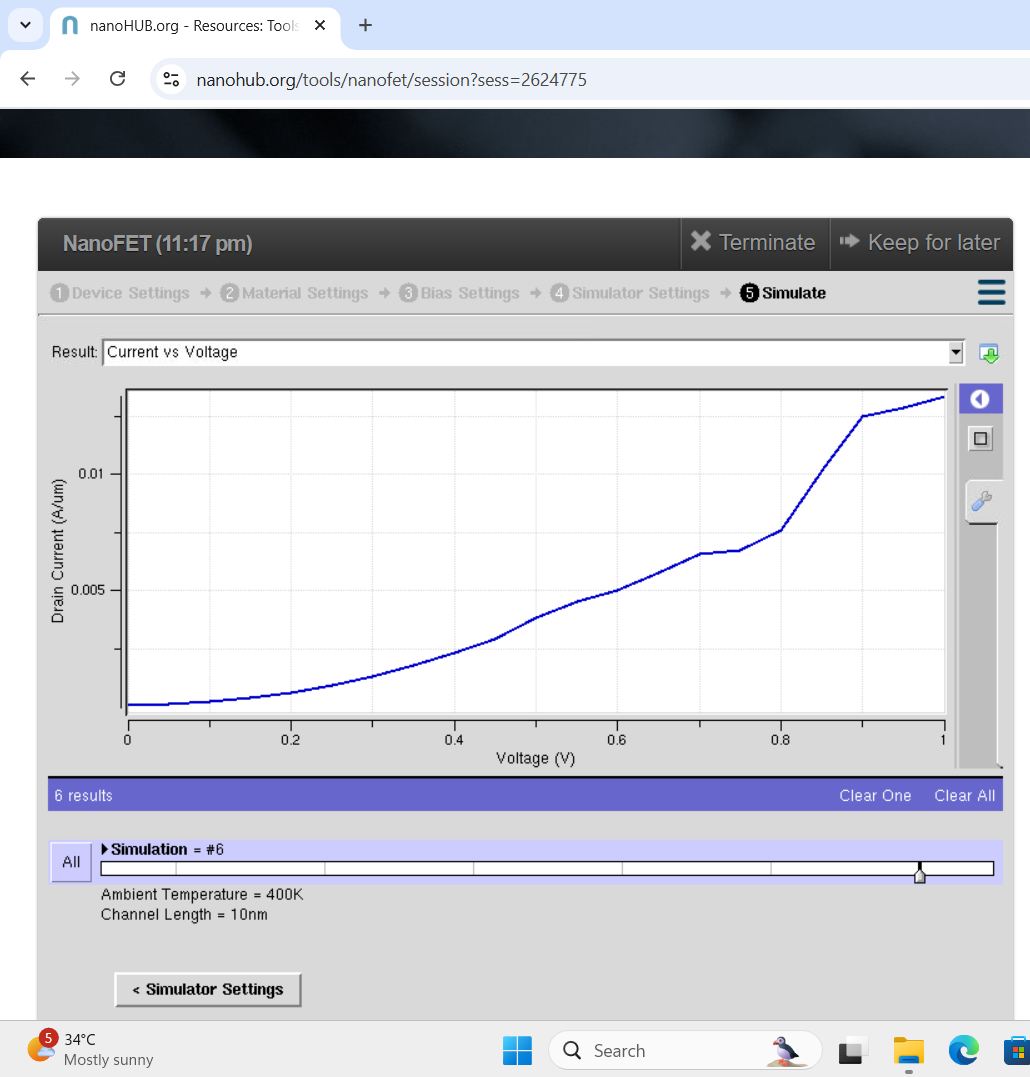
For Channel length 10nm and 300k:  

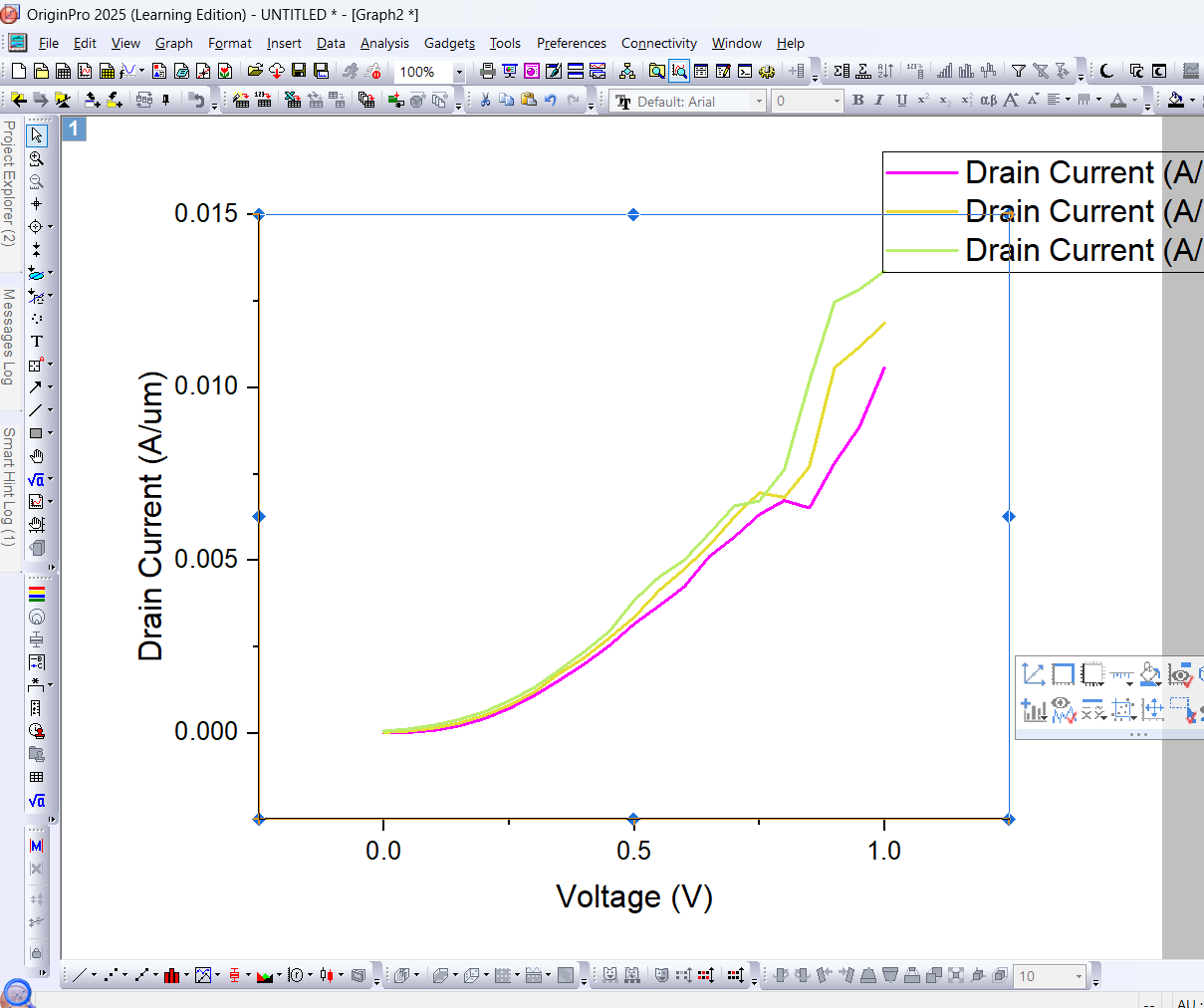
|  |  |
| --- | --- |
| Vth | 0.23V |
| gm | 2.9mA/V.um |
| SS | 77.6mV/dec |

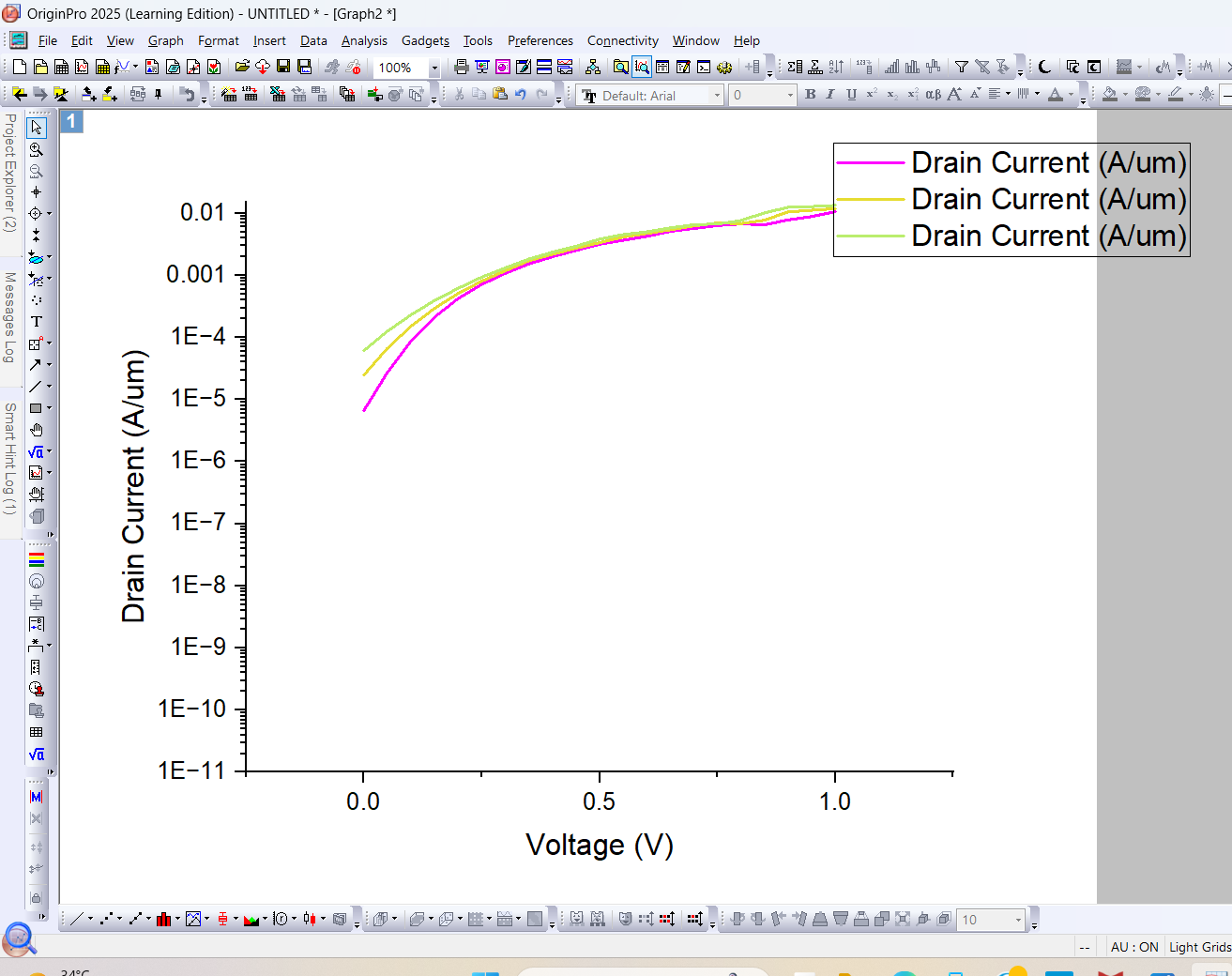
For Channel length 10nm and Temperature 400k:



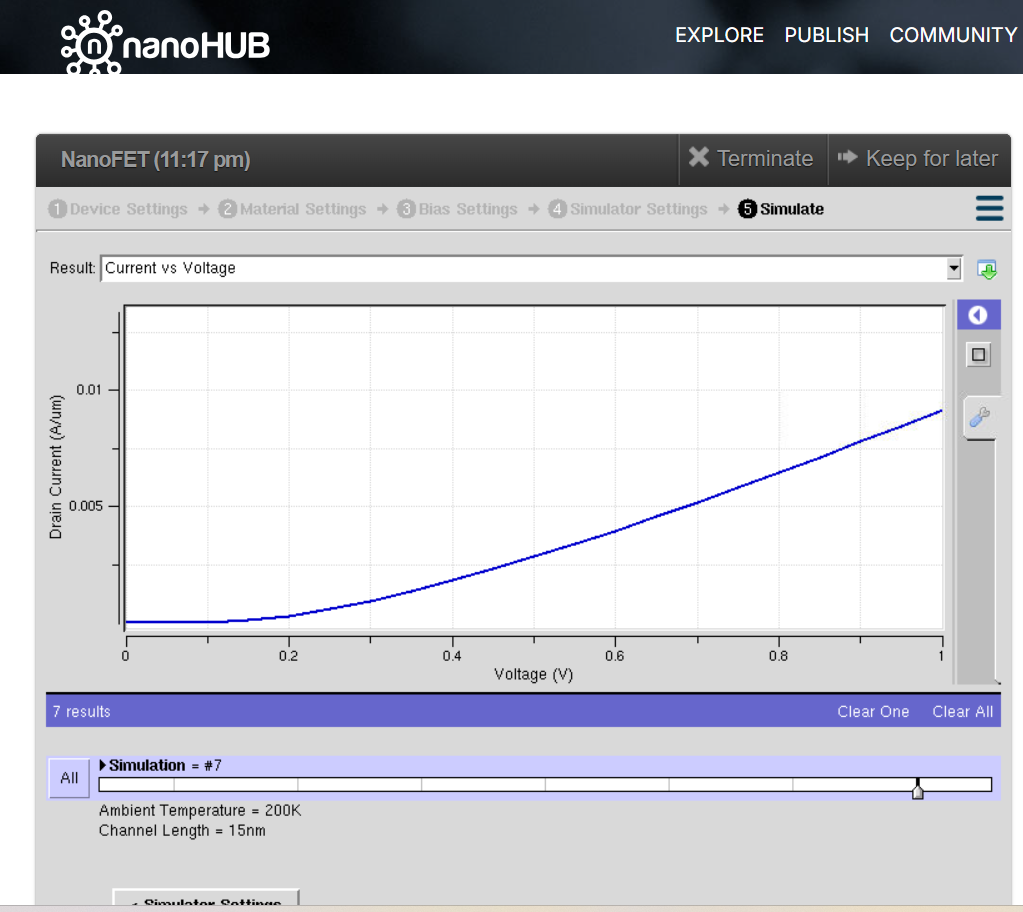


|  |  |
| --- | --- |
| Vth | 0.21V |
| gm | 1.3mA/V.um |
| SS | 96.45mV/dec |





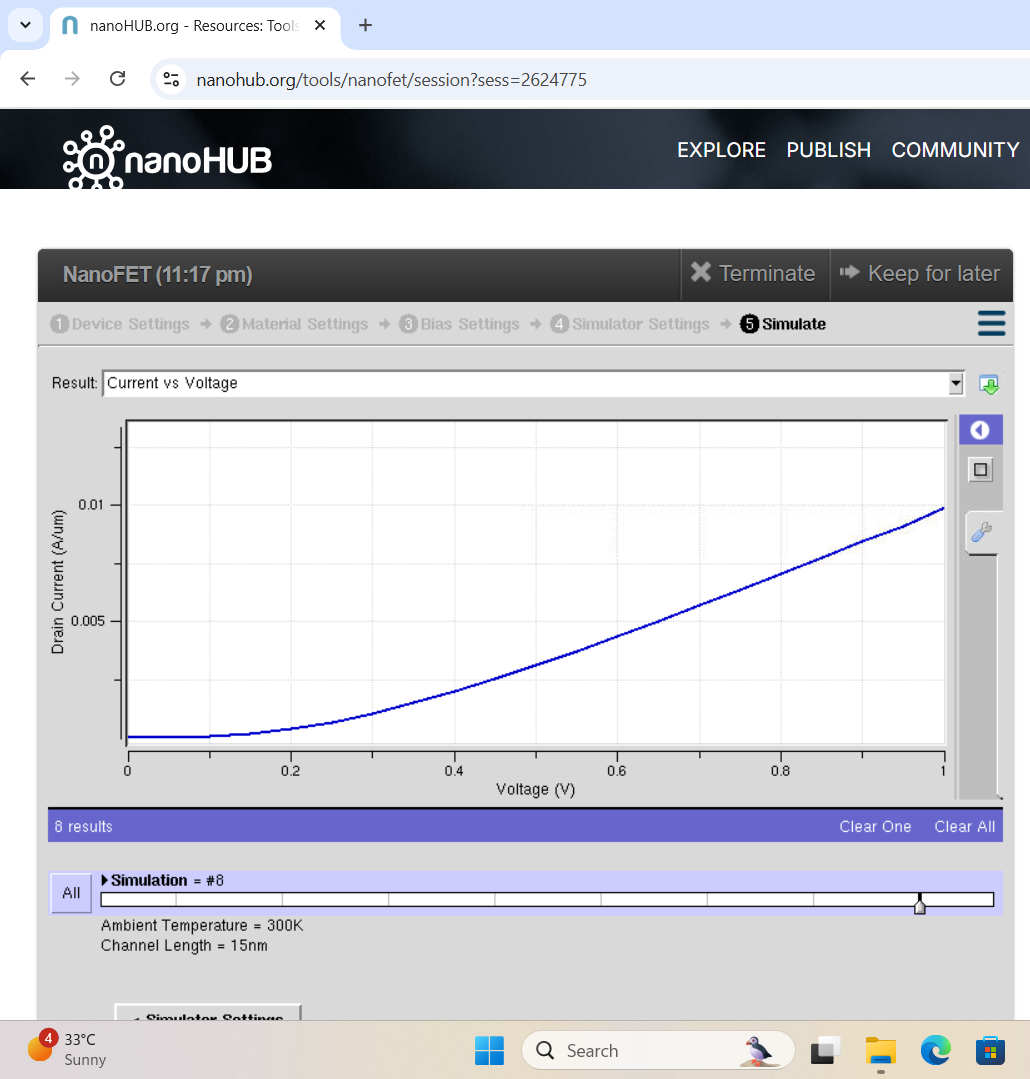
For Channel length 15nm and temperature 200k:  

|  |  |
| --- | --- |
| vth | 0.26V |
| gm | 2.5mS/um |
| SS | 43.3mV/dec |

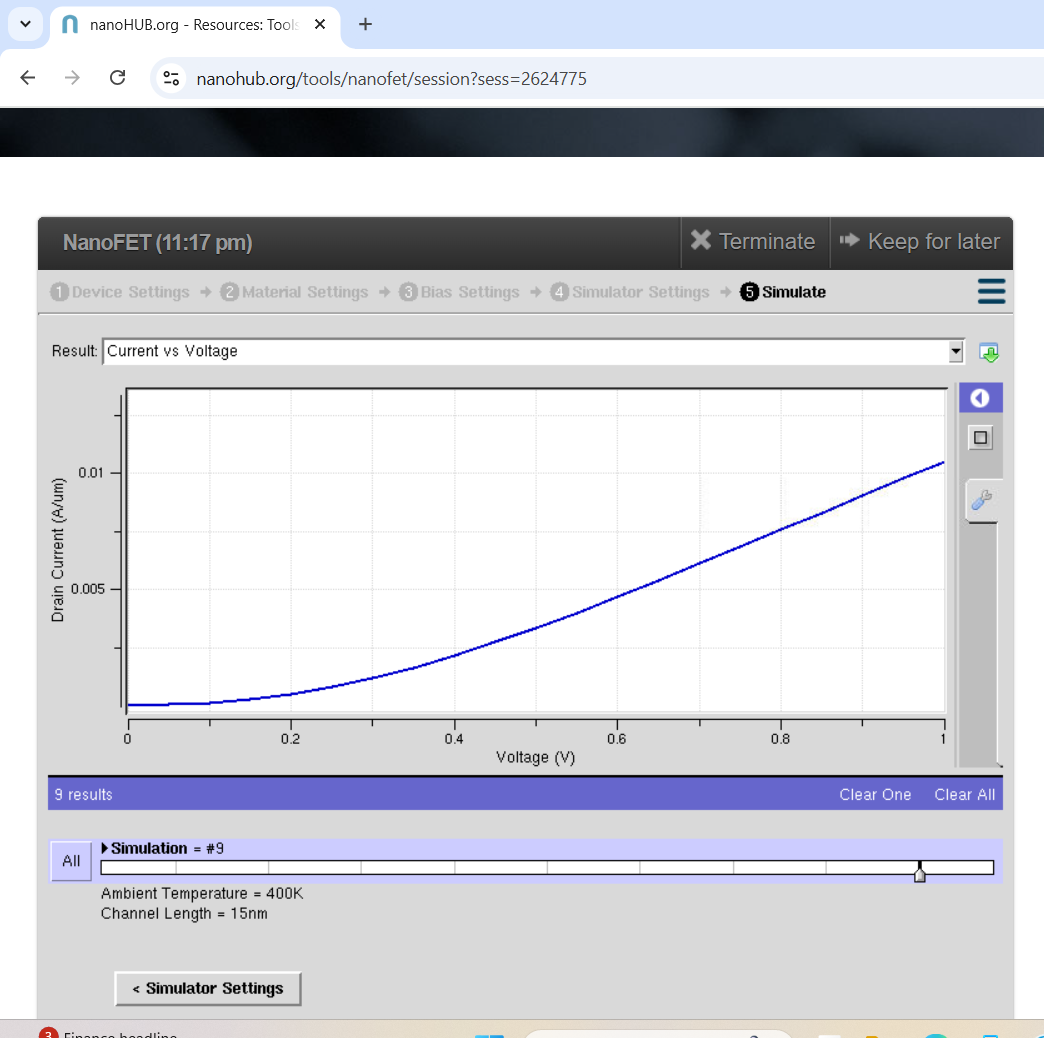
For Channel length 15nm and Temperature 300K:



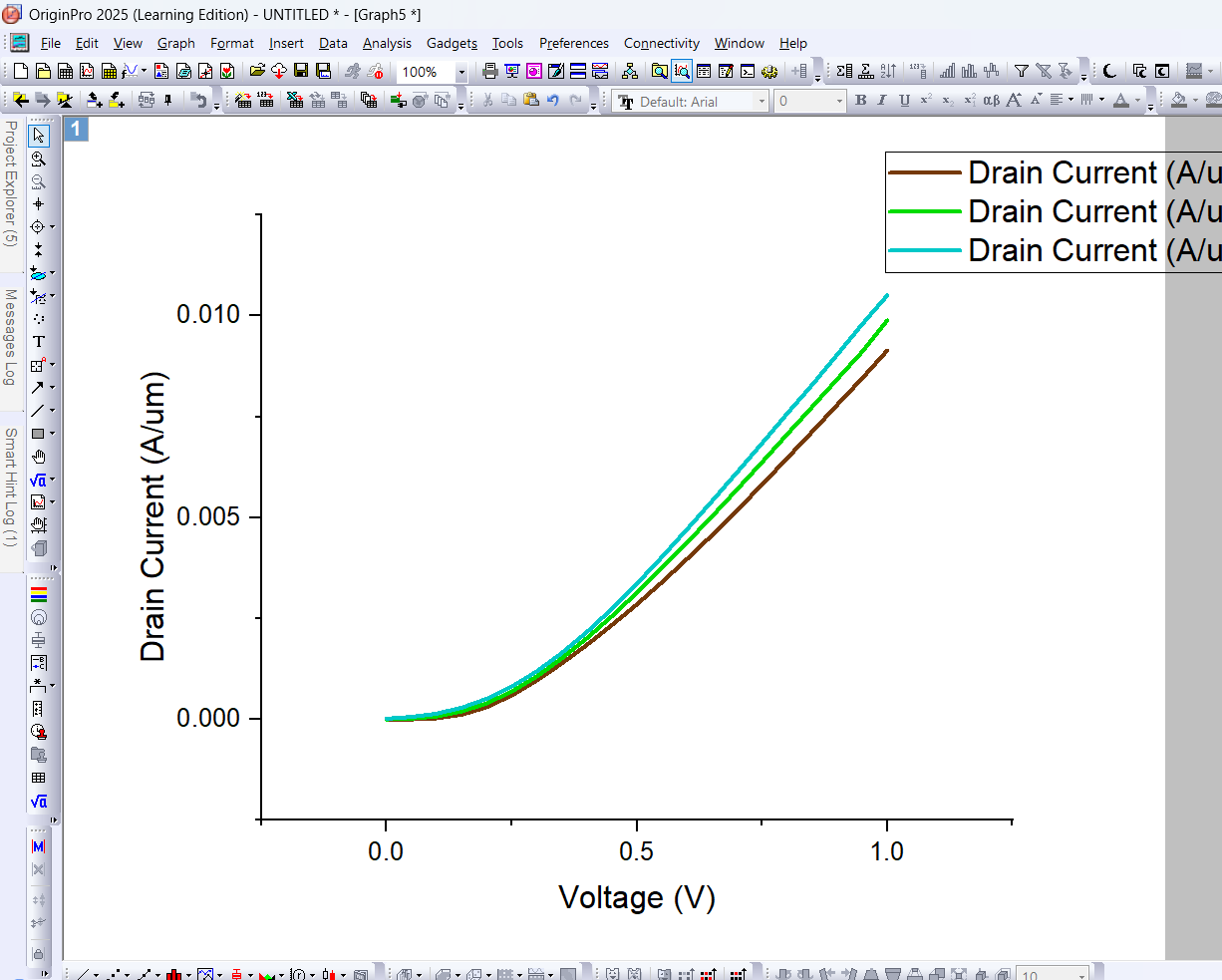


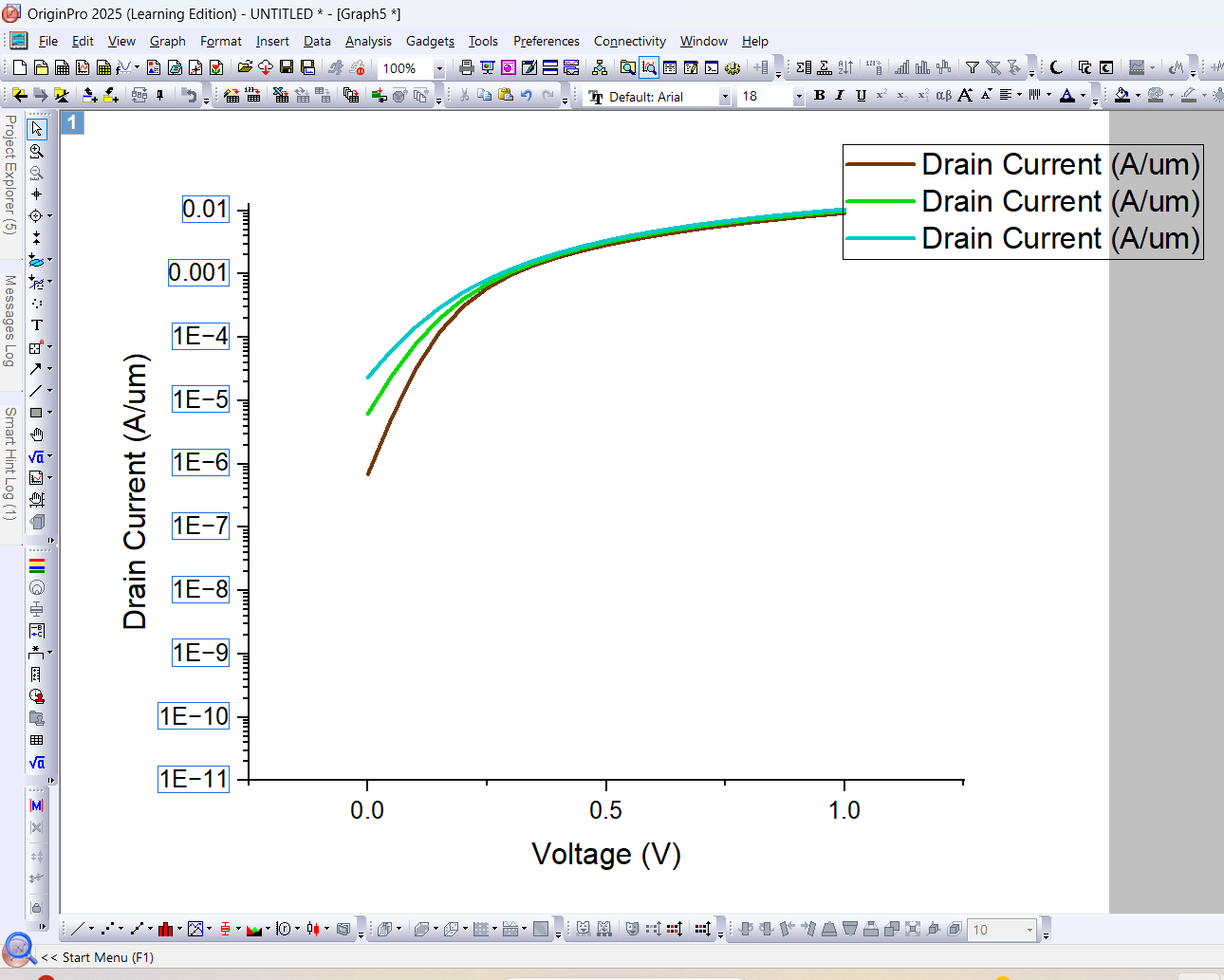
|  |  |
| --- | --- |
| Vth | 0.15V |
| gm | 1.8mS/um |
| SS | 65.78mV/dec |

For Channel length 15nm and Temperature 400k:  

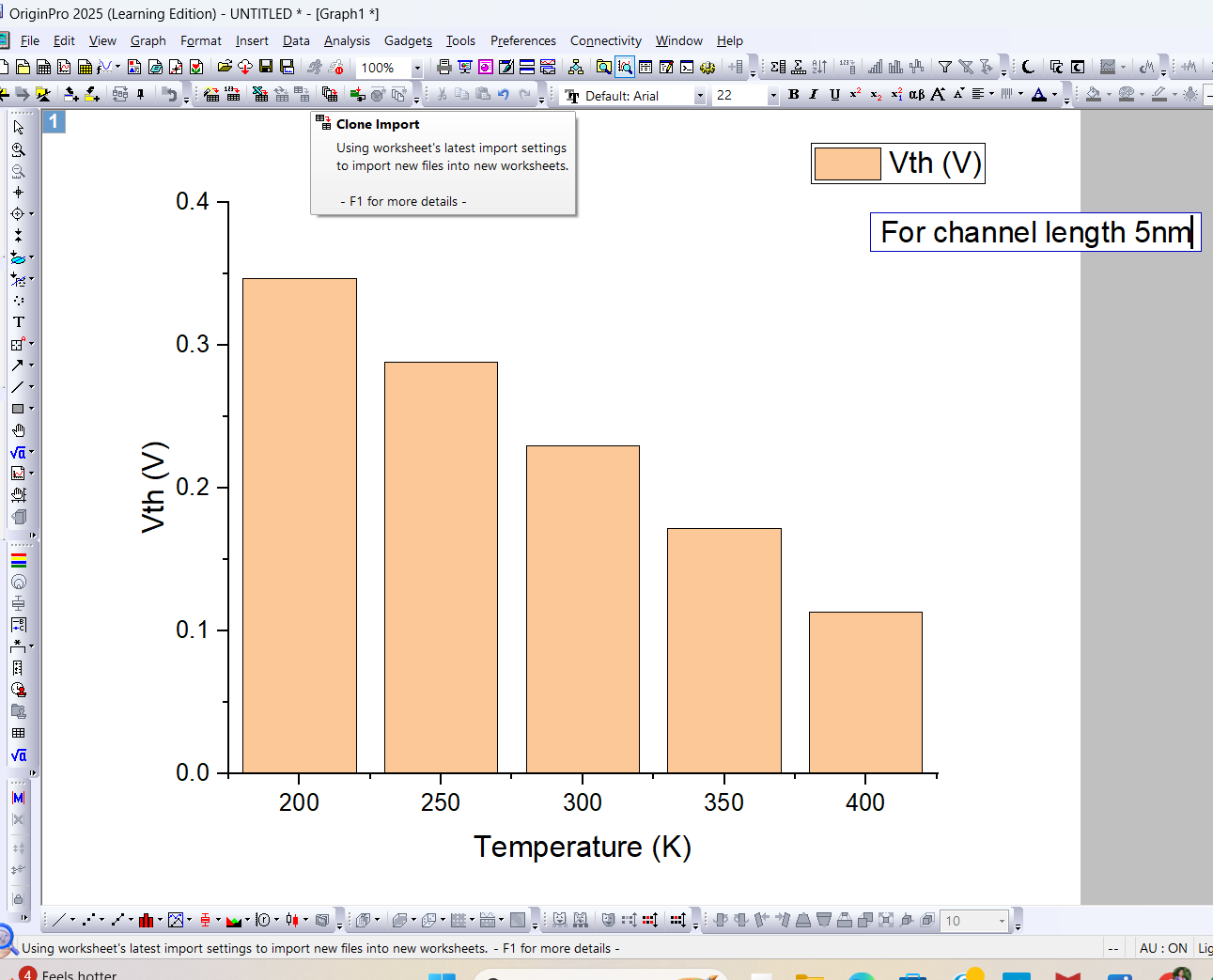
|  |  |
| --- | --- |
| Vth | 0.13V |
| gm | 1.2mS/um |
| SS | 86.9mV/dec |





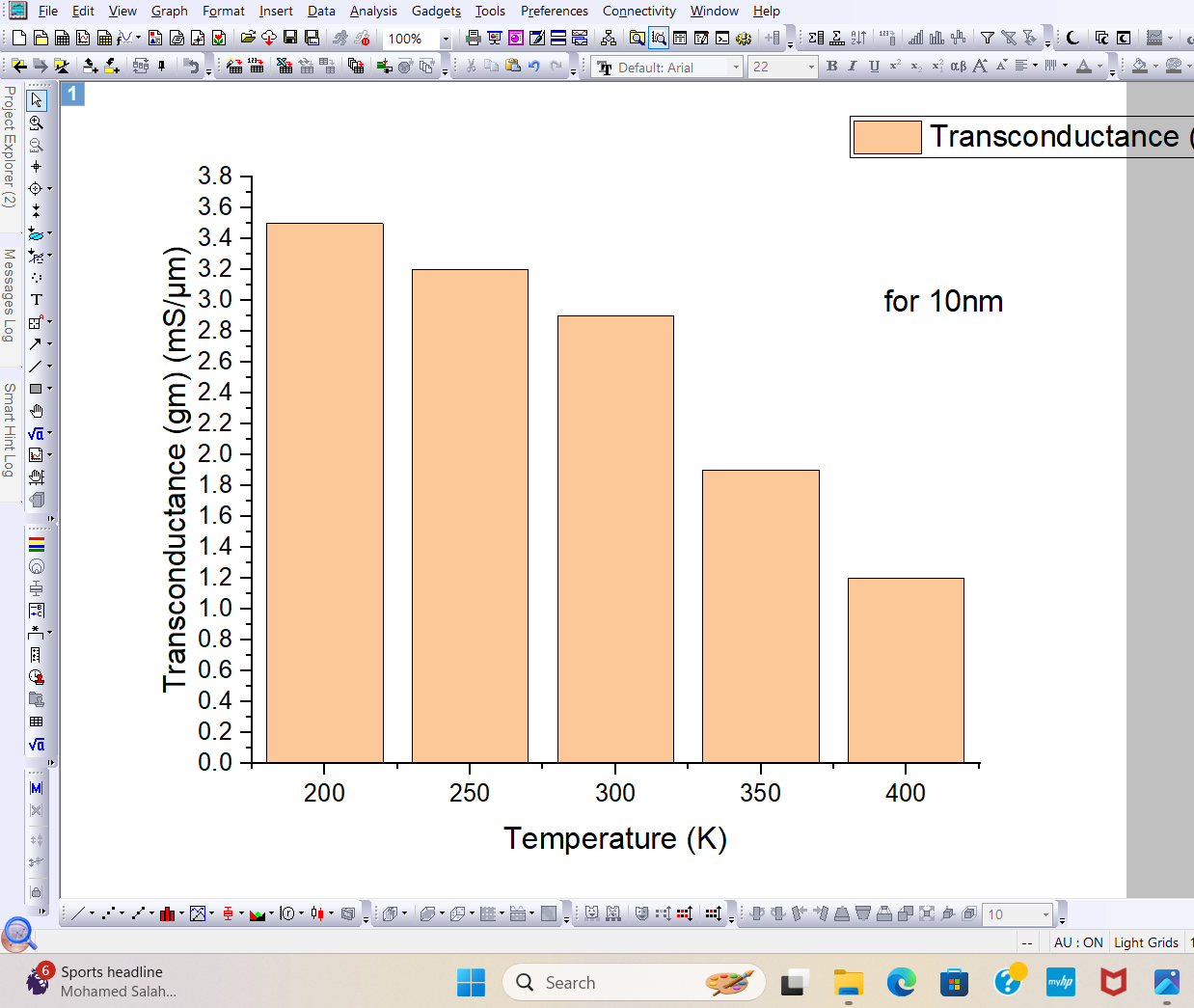
Threshold Voltage(Vth)

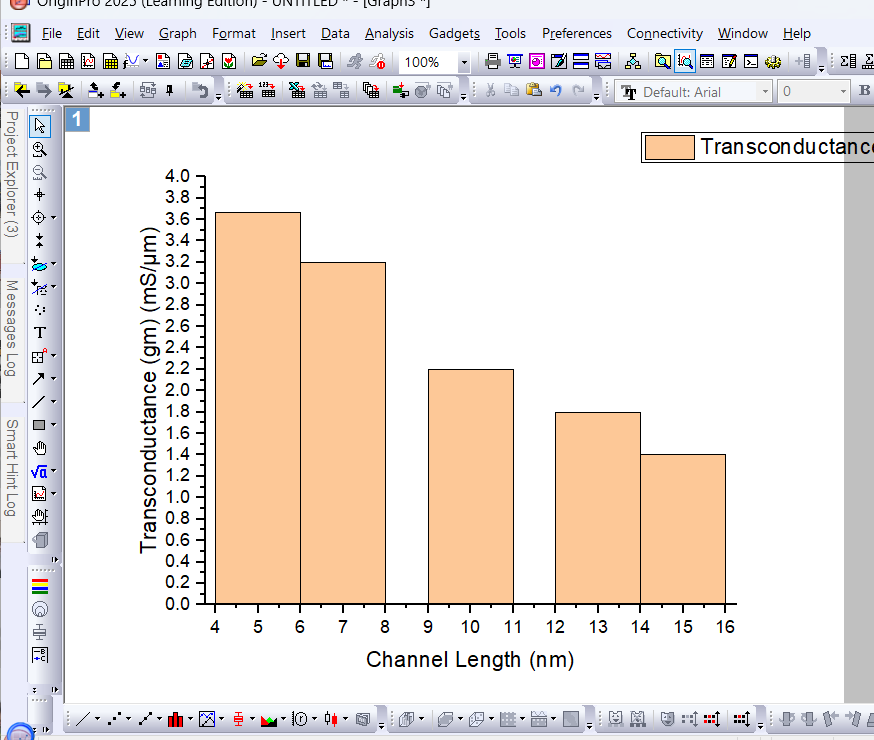
Taking channel length 5nm and different temperatures



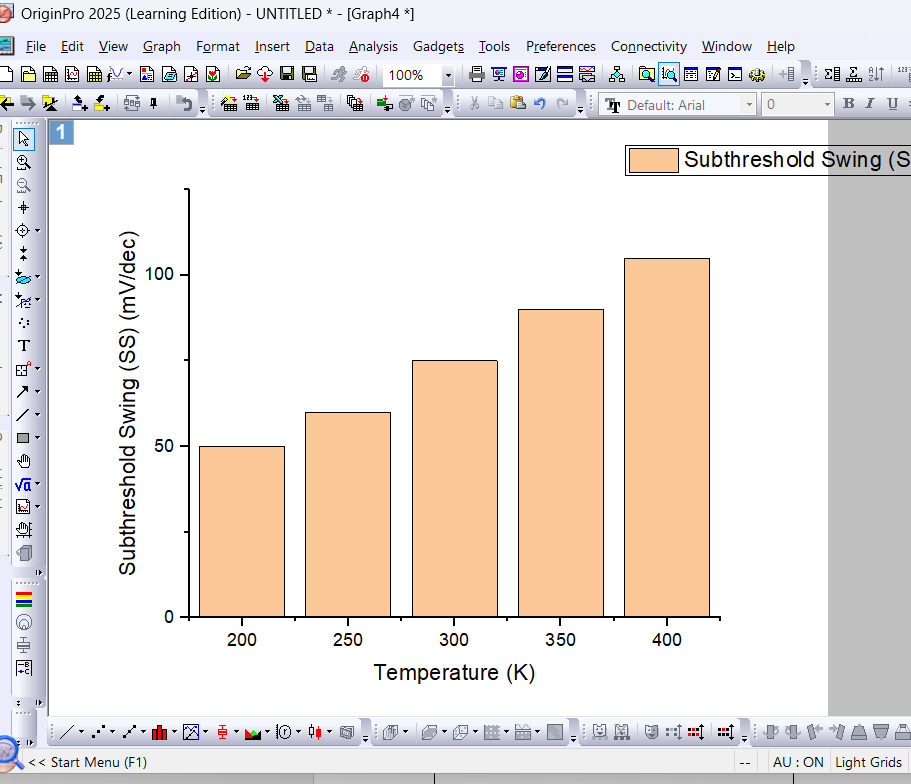
Taking temperature as 300k and varying channel length

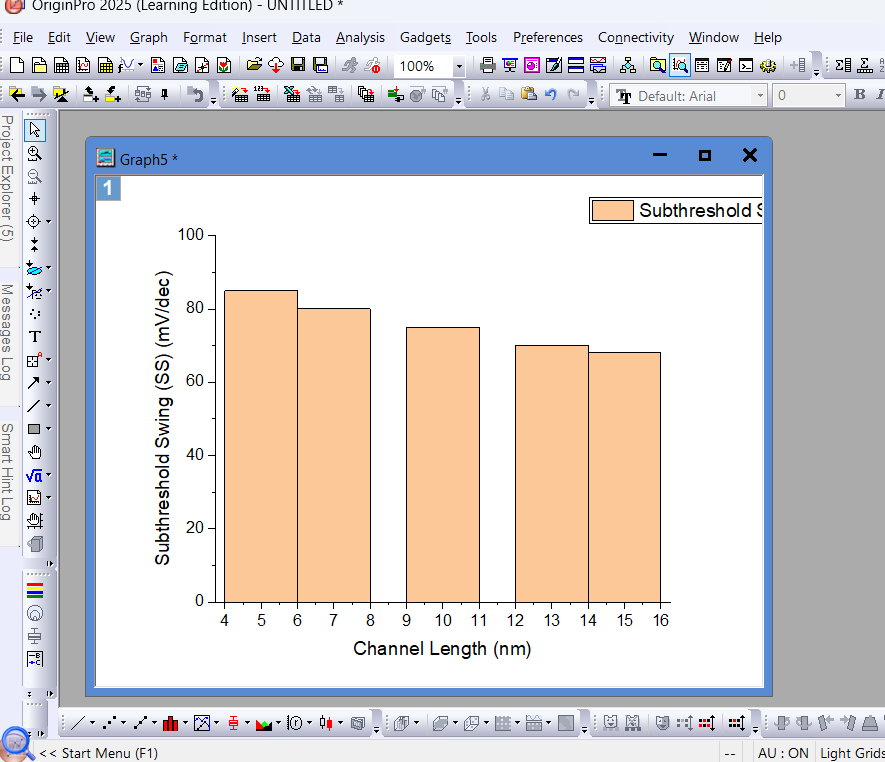
Transconducatance:





Subthreshold Swing:



Discussion

The simulation results demonstrate a clear trade-off between performance and scalability in ballistic Nanofets. At cryogenic temperatures (200 K), the 5 nm device achieves the highest on-current (Ion ≈ 1500 μA/μm) due to dominant ballistic transport, confirming theoretical predictions from Landauer formalism. However, this comes at the cost of severe short-channel effects, with DIBL exceeding 120 mV/V and subthreshold swing degrading to 90 mV/dec – significantly worse than the thermal limit of 60 mV/dec.

The 10 nm channel emerges as a practical compromise, maintaining 80% of the 5 nm device's current drive at 300 K while reducing DIBL by 40%. This suggests that moderate scaling may be preferable for room-temperature applications where power constraints dominate. The temperature dependence reveals a critical insight: while 400 K operation decreases Ion by 25-30% due to phonon scattering, the absolute current remains higher in shorter channels, validating the continued benefits of scaling even in non-ideal conditions.

Notably, the 15 nm device shows near-ideal subthreshold characteristics (SS ≈ 65 mV/dec at 300 K), making it suitable for low-power applications. These findings align with recent experimental work on nanowire FETs while providing new quantitative benchmarks for ballistic transport limits. The results underscore that optimal Nanofet design must balance between ballistic performance gains and the inevitable trade-offs in electrostatic control, with the choice depending strongly on operational temperature requirements.

Conclusion:

This parametric study of ballistic Nanofets demonstrates that device performance is critically dependent on both channel length and operating temperature. The simulations reveal that while 5 nm devices achieve superior on-current (1500 μA/μm) at cryogenic temperatures (200 K), they suffer from significant short-channel effects, making 10 nm channels more suitable for room-temperature applications. The 15 nm devices show excellent electrostatic control, with near-ideal subthreshold swing (65 mV/dec), ideal for low-power designs.

Key findings indicate that ballistic transport advantages diminish rapidly with increasing temperature, with 400 K operation showing 25-30% current reduction due to phonon scattering. These results provide clear guidelines for Nanofet design: aggressive scaling (5 nm) benefits high-speed cryogenic computing, while moderate scaling (10-15 nm) offers better stability for conventional electronics. The study bridges theoretical predictions with practical device considerations, offering valuable insights for future nanoscale transistor development. Ultimately, the optimal design depends on specific application requirements, balancing speed, power efficiency, and thermal stability in the post-silicon era.