Guidelines

- Do **not** write your answers on this sheet. Responses written here will **not** be evaluated. Please use the separate answer sheet provided.
- The attached appendices may assist you with some questions.
- You may use these sheets for rough work.
- Each question is worth 2 points. Total marks: 100 points. If you find any question difficult, proceed to the next one.

Section A: Basic Circuits

A1

Complete the truth table for NAND:

```
A | B | Output (A NAND B)
-------------------------
0 | 0 | ?
0 | 1 | ?
1 | 0 | ?
1 | 1 | ?
```

Write your answer as a four-digit number without spaces — the values from rows 1 to 4 of the truth table. For example, `0000`.

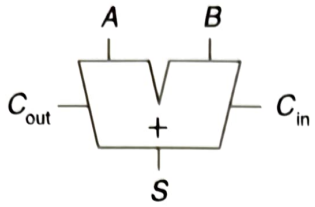
A2

You have built an XOR gate. What is the output of the XOR gate when the inputs are:

```
A = 1, B = 0
```

Provide your answer as a single digit.

A3



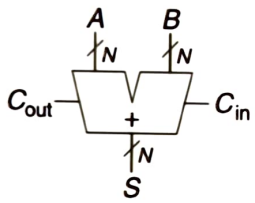
You have built a Full Adder using two Half Adders. Below are the values of the input signals. Calculate the values of the output signals: **Cout=?**, **S=?**.

Unset

A = 0, B = 1, and Cin = 1

Provide your answer as two digits without spaces: the values of **Cout** and **S**.

A4



You have built an 8-bit Adder based on Full Adder logic. If the input values are:

Unset

A = 11111111, B = 11111111

What will the output **S** value be? Provide your answer as 8 digits without spaces.

A5

What is the problem with the Carry Propagate Adder?

A. Cannot perform addition of large numbers
B. Does not support carry propagation
C. Carry propagation is slow
D. Not suitable for operations with negative numbers

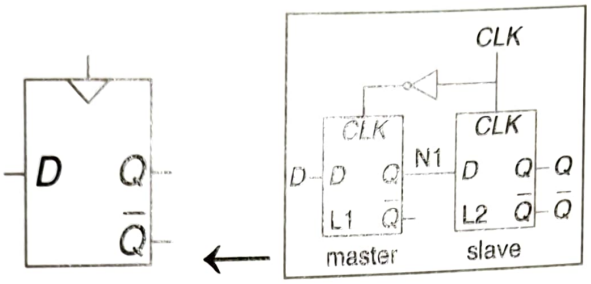
A6

How do I choose the length of one clock cycle?

A. By the time of the slowest component

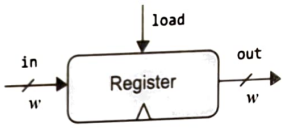
B. By the time of the slowest component sequence
C. By the sum of the times of the top 5 slowest components
D. By the sum of the times of all components in all circuits

A7



You are using a D flip-flop with the following implementation to store a single bit of data.
If the input is `D = 1` and the clock triggers a rising edge, what will the output `Q` be?

A8

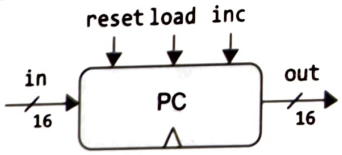


You are using a 16-bit register that initially stores the value `0000000000000000`. After providing a `load` signal of `0` and the input:

Unset
`in = 1010101010101010`

What will the value of the register be?

A9



Assume the PC starts at `0`. After 3 increments, where:
`inc = 1, reset = 0, load = 0, in = 1010101010101010,`
What will the PC value be?
Provide the **decimal** value of the PC as your answer.

A10

Using the ALU designed in you homework, what will the output `out` be when the ALU inputs are:

```
Unset
x = 00..1010, y = 00..0101, zx = 0, nx = 0, zy = 0, ny = 0, f = 1, no = 0
```

Provide the 4 lowest bits of the `out` as your answer. For example: `0000`.

A11

How is subtraction performed in the ALU?

A. Using a reverse propagate adder
B. One of the operands is converted to two's complement
C. Using double addition with overflow
D. Performing an extra subtraction of the operand from zero, then using the result for the original subtraction

A12

What is the difference between Combinational and Sequential logic circuits?

A. The output of a Sequential circuit is affected by both current and previous inputs
B. Combinational circuits must be built using flip-flops.
C. These are just different terms used by engineers and programmers.
D. Combinational circuits can have many inputs and outputs, unlike Sequential circuits.

Section B: Hack Computer

B1

What is the maximum address that can be encoded in a 16-bit A-instruction of a Hack processor?

A. 32767
B. 65535
C. 16384
D. 24576

B2

How will this instruction be presented in memory: `M=A-D` ?

A. 1110000111001000
B. 1111000111001000
C. 1110000111110000
D. 1110110000110000

B3

Write the Hack binary equivalent of the instruction:

Unset
D=A

Write your answer as a machine instruction (16 binary digits). For example:
1010101010101010

B4

In your Hack CPU, what will happen if the A register holds the value 15 and you execute the instruction:

Unset
M=D

Assuming D = 9, what value will be stored in RAM[15] after the instruction executes?

B5

You are given two Hack instructions in binary format. Decode them and provide the corresponding Hack assembly language instructions as your answer:

Unset
0000000000000101
1111110111010000

Provide your answer as two Hack assembly language instructions separated by a comma. For example: M=D,@123

B6

Write the Hack binary equivalent of the jump instruction:

```
Unset
0;JMP
```

B7

What does the following Hack program do:

```
Unset
@31
D=A
@SCREEN
A=D+A
D=A
@R0
M=D
@255
D=A
@R0
A=M
M=D
```

A. Sets pixels 504 to 511 for row 0 to black
B. Sets pixels 496 through 503 for row 0 to black
C. Sets pixel 501 for row 7 to black
D. Sets pixel 506 for row 7 to black

B8

Select the correct statements about the Symbol table:

A. It is used to convert addresses into variable names.
B. It is dynamically built by the processor during program execution.
C. It is dynamically built by the compiler during program translation.
D. It is stored on disk and used by all simultaneously running programs.

B9

Consider the complete Hack assembly program below. What does the assembler do with the labels `(START)` and `(END)`?

```
Unset
(START)
  @10
  D=D+A
  @END
  0;JMP
(END)
```

A. Assigns addresses 0 and 4 to START and END, respectively.
B. Assigns addresses 1 and 3 to START and END, respectively.
C. Assigns addresses 0 and 3 to START and END, respectively.
D. Assigns addresses 0 and 1 to START and END, respectively.

B10

You have the following initial RAM state:

	RAM	
0	3	R0
1	4	R1
2	1	R2
3	2	R3
4	8	R4

A = 4

And you have the following program:

```
Unset
@R1
A=M
D=M
@R0
M=D
```

Provide your answer as comma-separated values of `RAM[0]` and `RAM[1]`. For example: `3,4`

B11

Which of the following statements correctly describes how memory-mapped I/O works?

A. Memory-mapped I/O uses a separate set of specialized instructions to perform input and output operations via dedicated I/O ports.
B. Memory-mapped I/O maps I/O device memory into the same address space as the system's RAM, allowing the CPU to access devices using standard memory instructions.
C. Memory-mapped I/O bypasses the CPU entirely and directly transfers data between devices and main memory.
D. Memory-mapped I/O requires the use of an interrupt driver for every data transfer between the CPU and an I/O device.

Section C: Single/Multi-Cycle Datapath

C1

What is the advantage of a single-cycle processor?
A. Allows the clock cycle to be shorter than that of a multi-cycle processor.
B. Easy to implement.
C. Allows multiple instructions to be executed simultaneously.
D. Uses more than 2 ALUs and three separate memory units for instructions and data.

C2

What is the control unit of a multi-cycle processor?
A. Finite state machine
B. Combinational logic circuit
C. Symbol table
D. Register file

C3

In a multi-cycle processor (with no pipeline), why are additional registers required in the datapath?
A. To store values between clock cycles for the same instruction.
B. These are cache registers used to increase the speed of operation.
C. For parallel execution of several instructions of different types.
D. This is not a required component and may not be used.

C4

Which instruction takes the most cycles to execute in a multi-cycle MIPS processor?
A. Jump (J)
B. Beq (BEQ)
C. Store (SW)

D. Load (LW)

C5

Which of the following statements about pipelining is TRUE?

A. The execution time of one instruction is increased during pipelined execution.
B. Allows up to 5 fewer instruction execution stages compared to a multi-cycle processor.
C. Provides performance gain only in the complete absence of conflicts.
D. This approach can be used only for a single-cycle processor.

C6

What value should the MemWrite control signal have during the fetch instruction stage in a multi-cycle MIPS processor?

C7

How many instructions in a multi-cycle MIPS architecture do not require the Decode stage?

C8

Choose the correct statements:

A. Executing the same single instruction in a pipelined processor takes **more** time than in a non-pipelined processor.
B. Executing the same single instruction in a pipelined processor takes **less** time than in a non-pipelined processor.
C. Executing the same single instruction in a pipelined processor takes the **same** time as in a non-pipelined processor.
D. In a pipelined processor, the execution of a single instruction can take **either more or less time**, but on **average**, the time per instruction is still **less**.

C9

What is the RAW hazard in a pipelined processor?

A. When read and write instructions accidentally swap places due to branch prediction errors.
B. When the processor runs out of empty registers to write during execution.
C. When a subsequent instruction reads a register before a previous instruction writes to it.
D. When a processor's clock speed decreases to wait for a slow read/write memory operation.

C10

Arrange the stages of instruction execution in the pipelined datapath in the correct order. Provide your answer as 5 letters in a row, without spaces or other characters. For example:
ABCDE

A. Decode
B. Memory Read/Write
C. Fetch
D. Execute
E. Register File Writeback

CADBE

Section D: Architectural Enhancements

D1

Which of the following is stored in the stack frame when calling a function in x86 (32-bit) architecture?

A. Amount of available stack memory
B. Function code
C. Function arguments
D. Function name

D2

What is virtual memory?

A. A special type of RAM that is deployed in the cloud and shared between computers.
B. A method of storing memory addresses in a virtual environment, disconnected from physical hardware.
C. A technique where memory is duplicated across multiple processors for faster execution.
D. A memory management technique that gives an application the illusion of having more memory than physically available by using disk storage.

D3

What is paging?

A. A scheduling technique where the CPU alternates between processes to ensure equal execution time.
B. A memory management scheme that divides physical memory into fixed-size blocks and maps them to corresponding blocks in virtual memory.
C. A method of increasing pipelined processor speed by splitting instructions into pages for faster execution.
D. A way to enhance SSD performance by rearranging data into sequential pages.

D4

What is segmentation?

A. A process of splitting the multicycle processor clock cycle into segments to improve instruction throughput.
B. A technique that segments data in the cache for faster retrieval by the processor.
C. A memory management technique that divides memory into variable-sized logical units based on the program's structure.
D. A method of dividing physical memory into fixed-size blocks for easier allocation.

D5

A key characteristic of a Superscalar datapath is:

A. Multiple copies of processing/execution units
B. Use of a conveyor
C. Processing several pieces of data with a single instruction
D. Conveyor registers

D6

Select all correct statements about virtual memory.
Write all the correct answer letters (A, B, C, D) on the answer sheet in alphabetical order.

A. The Memory Management Unit converts the virtual page address to a physical page address.
B. Only a random page size can help to mitigate memory segmentation issues.
C. The virtual address is equal to the physical address as long as the amount of memory used does not exceed the amount of physical memory.
D. The virtual address contains in its structure both the virtual page number and the offset within the physical page.

D7

Segmentation and Paging Comparison
Write all the correct answer letters (A, B, C, D) on the answer sheet in alphabetical order.

A. Segmentation is transparent to the programmer, but Paging is not.
B. Segmentation allows multiple address spaces to exist at once.
C. Both approaches allow the creation of address spaces larger than the physical one.
D. Segmentation was invented to emulate large amounts of virtual RAM.

D8

What is a primary advantage of a Two-way Set Associative Cache compared to a Direct-Mapped Cache?

A. Has fewer collisions
B. Allows to store twice as many cache lines with the same cache size
C. Easier and cheaper to implement
D. Does not require checking for misses when matching a set

Both true

D9

Suppose the access times for the L1 cache, L2 cache, and main memory are 1, 15, and 80 cycles, respectively.
Assume that the L1 and L2 caches have miss rates of 10% and 25%, respectively.
In this case, the average memory access time (in cycles) is:

A. 4.5
B. 42.66
C. 96
D. 22.5

L1H = 0.1
L2H = 0.25
1 + 0.1 (15 + 0.25(80))
15 + 20
1 + 0.1(35)
= 4.5

D10

Which of the following statements about cache write policies is correct?

A. In a write-through cache, data written to a cache block is only updated in the cache and not in main memory.
B. A write-back cache immediately writes any changes to both the cache and main memory simultaneously.
C. In a write-back cache, dirty cache blocks are written back to main memory only when they are evicted from the cache.
D. In a write-through cache, a dirty bit (D) is used to track modified memory blocks that need to be updated in the cache memory.

D11

Which of the following statements best describes how the "best fit" and "first fit" memory allocation algorithms handle fragmentation?

A. The "best fit" algorithm always chooses the largest available memory segment for allocation, resulting in minimal fragmentation.
B. The "first fit" algorithm reduces the chances of fragmentation by ensuring that memory is allocated from the smallest segment available.
C. The "best fit" algorithm tends to create many small, unusable memory segments, leading to increased fragmentation.
D. The "first fit" algorithm results in worse performance than the "best fit" algorithm because it scans the entire memory for the smallest free segment.

D12

In Intel Core i7 processors, privilege levels (or rings) are used to control access to system resources. Which of the following statements is **correct** regarding these protection levels and access control?

A. Any protection level (Ring 0 to Ring 3) can directly call procedures at a lower privilege level using a standard CALL instruction.
B. Attempts to access data at a lower privilege level from a higher privilege level are illegal and cause traps unless a call gate is used to provide controlled access.
C. A call gate is a mechanism that blocks communication within the same level in the Intel Core i7 architecture.
D. Privilege levels in Core i7 allow any ring to directly access data or execute instructions at any other ring without restrictions.

D13

In the context of the ELF (Executable and Linkable Format) file structure, which of the following correctly lists its key components?

A. Header, Program Section, and Debug Table
B. ELF Header, Program Header Table, Section Header Table, and Sections
C. Program Header, Meta Table, and Binary Tree
D. Code Table, Data Table, and Execution Table

D14

What is the difference between Segmentation and Paging?

A. Segmentation is invisible to programmers.
B. The size of segments, unlike pages, can vary.
C. Paging allows the use of any number of linear address spaces.
D. Segments are never unloaded to disk; they always remain in RAM.

D15

Which of the following is a way to resolve control conflicts in a pipeline processor?

A. Pipeline stall
B. Pipeline throttling
C. Random command shuffling
D. Command caching

D16

What is the purpose of the TLB (Translation Lookaside Buffer)?

A. Caches the most commonly used page table entries
B. Caches the most commonly used symbol table entries
C. Stores the last used segment
D. Accelerates runtime translation of programs

D17

Which of the following describes "ABI"?

A. Defines what names should be used in the API.
B. Describes the instruction set supported by the processor.
C. Describes the protocol for hardware-level communication between computer components.
D. Defines how binary modules of a program interact with each other at the machine code level.