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# Battleship



#### Use Case Definition

- Create a RISC-V processor
  - Custom extended ISA for communicating between FPGA boards
- 2 boards will be used
  - Both running the game on the RISC-V
  - Both with their own PPU using VGA to output to two monitors
  - Both handling their own inputs
  - Serial communication between them transmitting game state information
- Custom C implementation of Battleship
  - Add in assembly instructions for custom ISA

#### Motivation

- Use custom processor for a fun, interactive demo

- Demonstrate communication between boards and multiple IOs

- Experience creating an end to end system

### Approach

- Partition design into CPU, PPU, Communication modules
- Design a low latency protocol to synchronize each board's game state
- Utilize FPGA's ability to process different hardware attributes in parallel
- Extend RISC-V ISA with custom instructions to simplify game operation

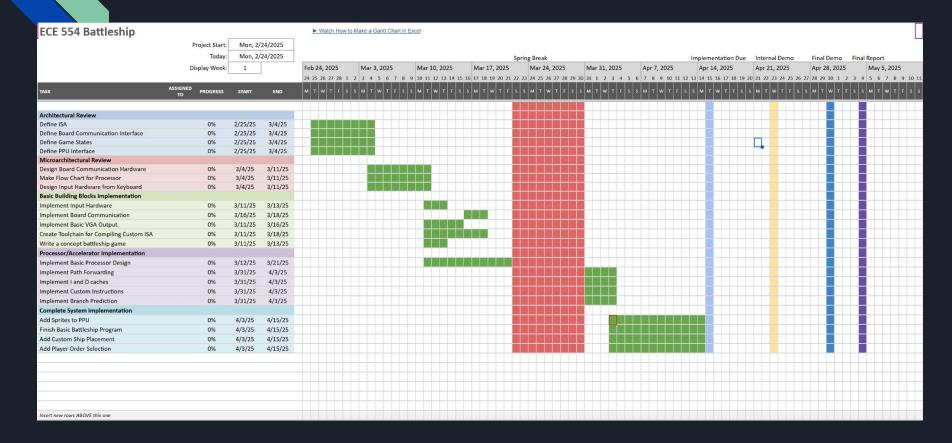
#### Anticipated Challenges

- Complexity with writing the custom C code implementation of Battleship
- Compiling C code with custom ISA
- Setting up communication between boards
- Syncing game states between boards
- Handling video output

#### Risk Management

- Simplifying Game Operation
  - Remove ability for players to place ships at start of game (hard code placement in program)
  - Player selection (hardcode one board as player 1 and player 2)
  - Simplifying video output by removing sprites
- Simplify Input
  - Use onboard keys and switches for input instead of keyboards

#### Milestones and Evaluation



#### Team Responsibilities

Alan: Software, Compiler Toolchain, VGA/PPU, Communication Hardware

Josh: Processor, PPU, Software, Communication Hardware

Jaime: Communication, PPU, Software

Jacob: Processor, System Integration, Verification

Zach: Processor, Software, PPU, Input Hardware

## Questions