PHASE 1: INSTRUCTION FETCH

1) PC is initialized to start at 96. Check cache for addr.

a) Convert PC → bin.

b) Use masks to grab: setIndex, tag (no need for byte offset for address).

c) Go to correct set within cache (via setIndex). Test each block for tag match.

i) If match (V is 1 AND tag match)

1) Load instruction to preIssue buffer.

2) Update LRU

3) Inc PC.

ii) If not match: (V is 0, OR no tag match)

1) Using PC as address, cache goes to that location in memory.

2) Cache loads the aligned block’s equivalent from memory into itself.

3) Cache returns the word (instruction).

4) Update LRU.

5) Inc PC.

Only data memory is in cache?????