Diode/GGNMOS HBM Minimum Width TCAD Simulation Lab5

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ABSTRACT:

In this lab, we utilize all the steps learned in the previous to acquire the optimal design for a Diode. Sentaurus Structure Editor/Device provides us with the 2D imagery and line graph of the TCAD simulation as in Labs 1 and 3. Sentaurus Device can simulate (1) the electrical, thermal, and optical characteristics of various semiconductor devices and (2) 2D, device behavior over a wide range of operating conditions, including mixed-mode circuit simulation. Using the meshing strategies from labs 2 and 4 we can define the max/min meshing sizes to a specific target (a material/device region or a user-defined evaluation window). Compared to labs 2 and 4, where we discovered the electrical and thermal characteristics of Diode and GGNMOS under HBM standard 2KV pulse, we now had to find the minimum width for both to pass HBM 2KV. The range for GGNMOS is 20um-100um, the range for Diode is 10um-20um, and the deviations are 10um for GGNMOS and 1um for Diode. Note: when lattice temp. > 1688, the silicon is melted; simulation will end if temperature failure becomes too high.

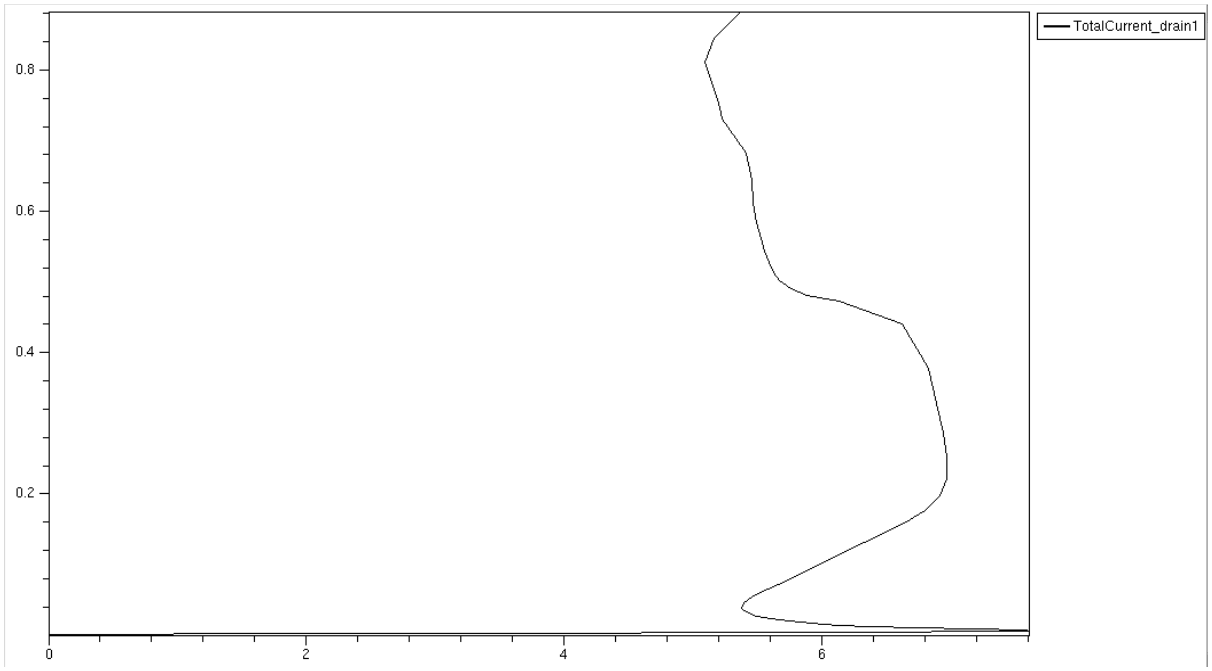
Important Note: if the graph of a new width is similar to the line graph that stops at the highest point (like 20um in GGNMOS) then it fails, due to the 1688 lattice temp. condition. Otherwise, if it curves downward (like 60um in GGNMOS), meaning it doesn't reach the highest temperature, then it passes. If one graph passes and another below it passes, then those above the new width also pass. Implemented sdevice everytime after changing the width/AreaFactor.

Commands:

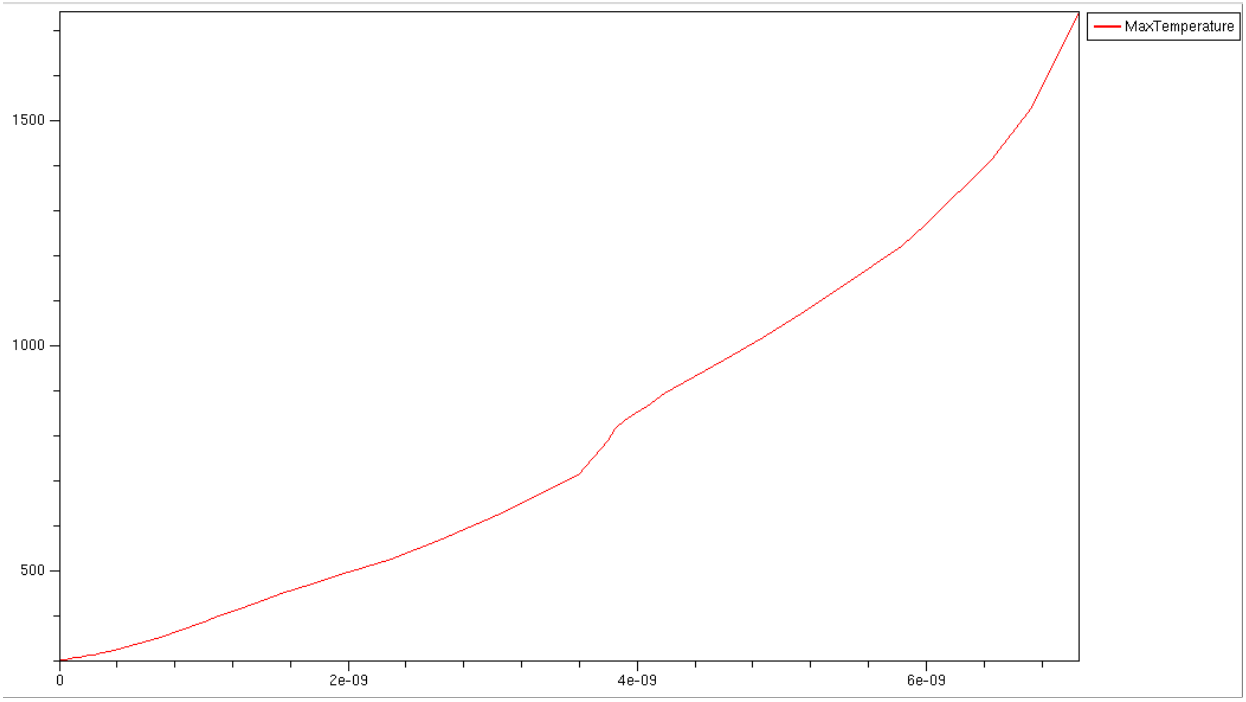
1) bender /home/cemaj/zhill $ mkdir Lab5
2) bender /home/cemaj/zhill $ cd Lab5
3) bender /home/cemaj/zhill/Lab5 $ vim hbm_for_ggnmos18_af.cmd
4) bender /home/cemaj/zhill/Lab5 $ sdevice hbm_for_ggnmos18_af.cmd &
5) bender /home/cemaj/zhill/Lab5 $ inspect
6) bender /home/cemaj/zhill/Lab5 $ vim hbm_for_diode18_af.cmd
7) bender /home/cemaj/zhill/Lab5 $ sdevice hbm_for_diode18_af.cmd &
8) bender /home/cemaj/zhill/Lab5 $ inspect

```
Thermode {
   { name="source1"    temperature=300 surfaceResistance=1e-6}
   { name="source2"    temperature=300 surfaceResistance=1e-6}

   { name="drain1"     temperature=300 surfaceResistance=1e-6}
   { name="drain2"     temperature=300 surfaceResistance=1e-6}

   { name="pwell1"     temperature=300 surfaceResistance=1e-6}
   { name="pwell2"     temperature=300 surfaceResistance=1e-6}

   { name="gate"       temperature=300 surfaceResistance=1e-6}

   { name="substrate"  temperature=300 surfaceResistance=1e-6}
}


Physics(MaterialInterface="Oxide/Silicon") {charge(surfconc=5.e10)}


Physics {
    AreaFactor=20
    Recombination(SRH(DopingDep TempDep) Auger Avalanche(Eparallel))
    Mobility(DopingDep HighFieldSaturation Enormal)
    EffectiveIntrinsicDensity(oldSlotboom)
    Thermodynamic
    AnalTEP
}
```

(a)



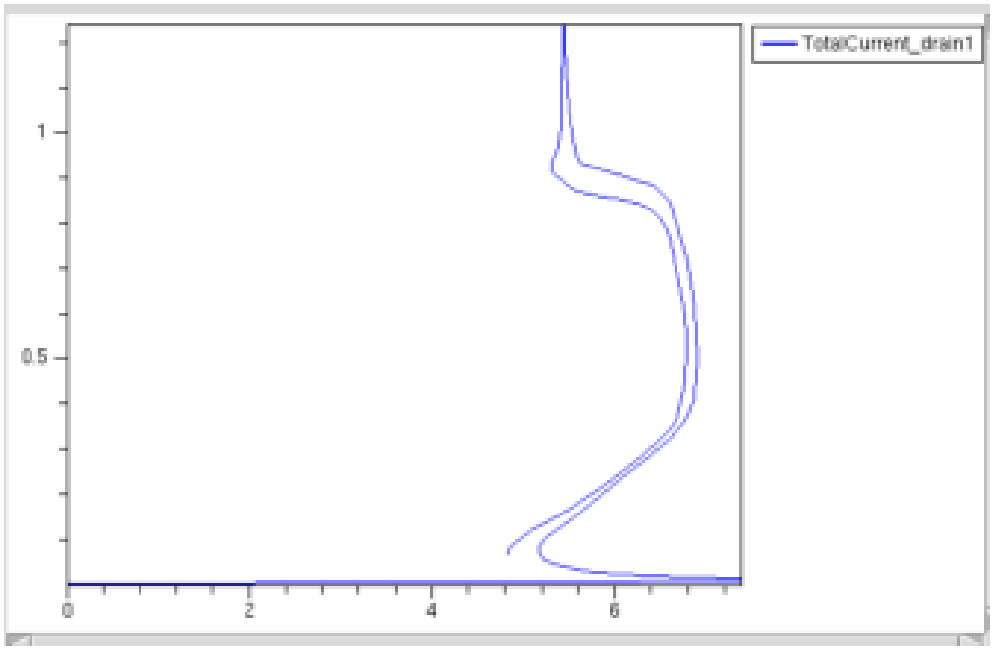
(b)



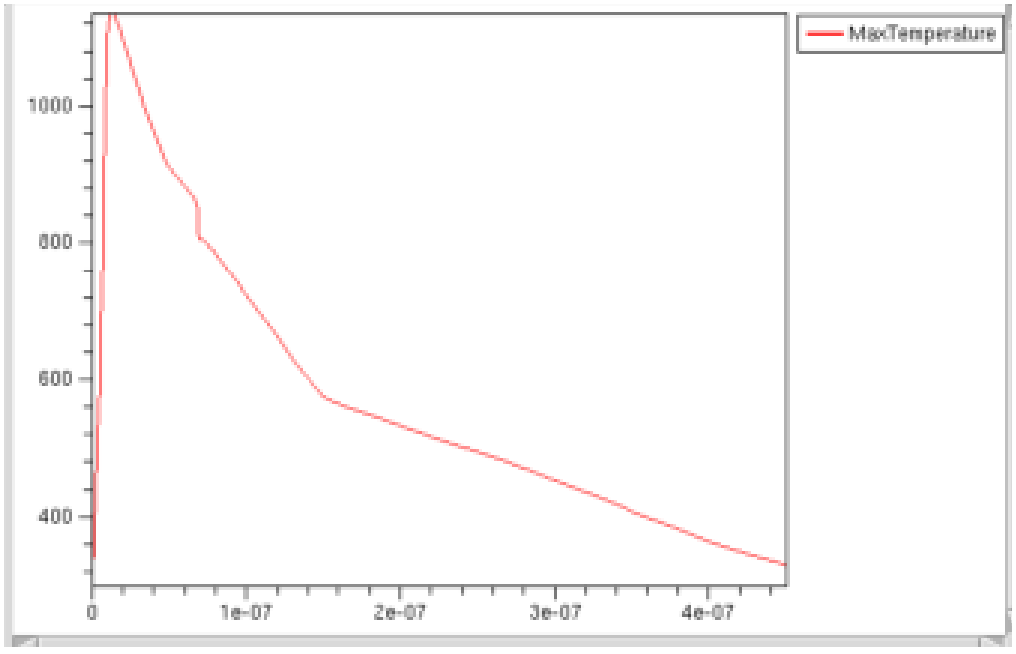
(c)

Figure 1: Width/AreaFactor (GGNMOS) = 20um; no curve

As the I-V curve begins to move upward quite fluently, after remaining constant in the beginning, it eventually reaches the top of the graph where it then stops. This maximum point is above the lattice temperature of 1688 (as seen in Figure 1(c)), i.e. the melting point of the silicon, so this device where width = 20um fails at triggering so we need to increase the width.



(a)



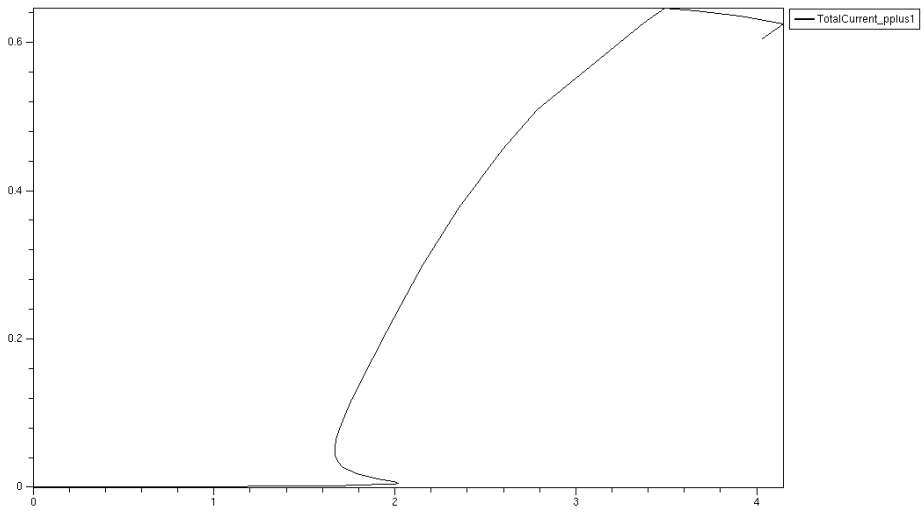
(b)

Figure 2: Width/AreaFactor (GGNMOS) Min. = 40um; similar to curve with 60um (median)

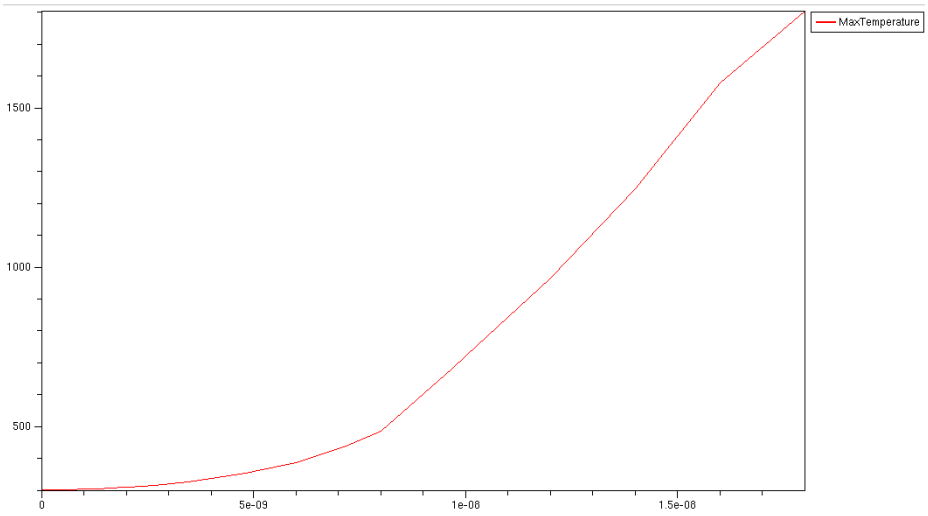
After seeing the device with width = 60um curves downward and it's lattice temperature maximum is less than 1688, we can deduce this device does pass the triggering test but we must go lower to find the best possible solution, i.e. minimum width. Width = 40um is found out to be the minimum width since it's I-V curve is similar to that of width = 60um width = 30um is similar to width = 20um. The I-V, in Figure 2(a), does begin to move upward, slightly differently than in Figure 1(b), but then begins to descend causing the lattice temperature, in Figure 2(b), to descend also.

```
Thermode {
   { name="pplus1"    temperature=300 surfaceResistance=1e-6}
   { name="pplus2"    temperature=300 surfaceResistance=1e-6}

   { name="nplus1"     temperature=300 surfaceResistance=1e-6}
   { name="nplus2"     temperature=300 surfaceResistance=1e-6}

   { name="substrate"  temperature=300 surfaceResistance=1e-6}
}


Physics(MaterialInterface="Oxide/Silicon") {charge(surfconc=5e10)}

Physics {
    AreaFactor=10
    Recombination(SRH(DopingDep TempDep) Auger Avalanche(Eparallel))
    Mobility(DopingDep HighFieldSaturation Enormal)
    EffectiveIntrinsicDensity(oldSlotboom)
    Thermodynamic
    AnalTEP
}
}
```

(a)



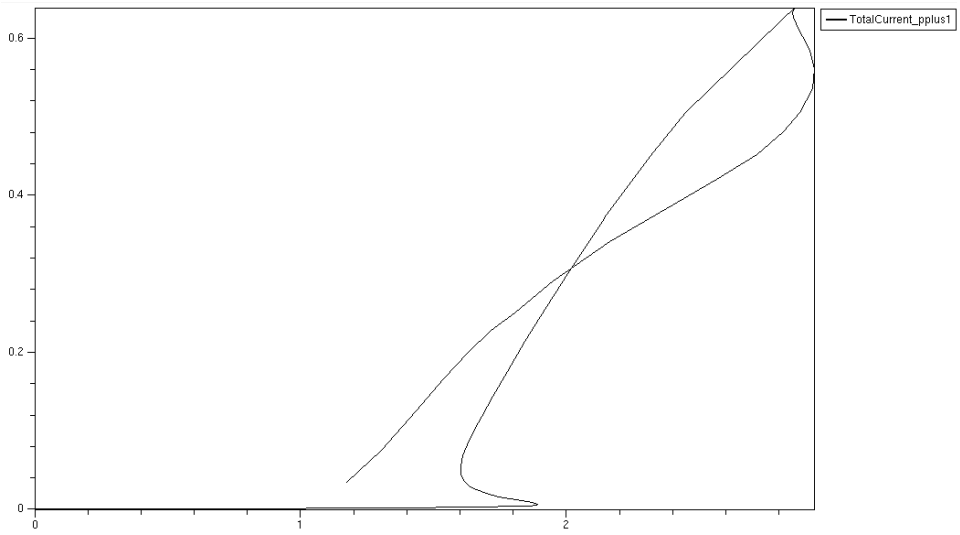
(b)



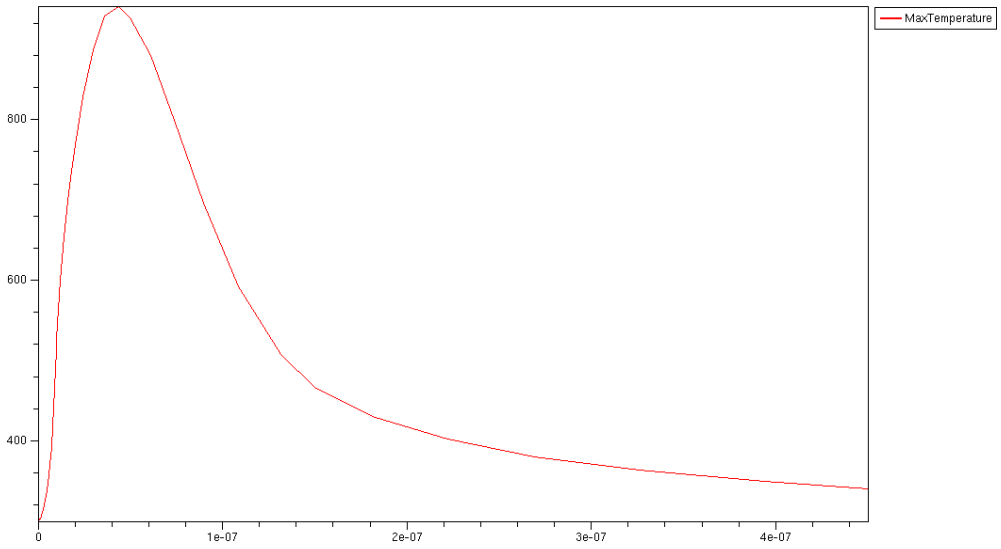
(c)

Figure 3: Width/AreaFactor (Diode) = 10um; curve is visible but still exceeds max temp.

The Diode I-V curve moves less fluently than that of GGNMOS but, even though it curves downward after reaching the top of the graph and changes direction for a bit, it continues to increase in voltage for a majority of the process and decreases in current only slightly. Lattice temperature, again, reaches above 1688 at the end so the width must be increased.



(a)



(b)

Figure 4: Width/AreaFactor (Diode) Min. = 12um; downward as in 15um (median)

The first section of the I-V curve flows similarly to the first half of Figure 3(b) but then begins to decrease in current gain a lot more the moment after the curve reaches the top of the graph. Although the downward curve is moving differently than in Figure 2(a), it is still decreasing the current and voltage values very quickly. As stated earlier, this quick direction change decreases the lattice temperature and stops its maximum point below 1688. Notice how the diode's maximum lattice temperature is lower than that of GGNMOS.