

Design and Optimization of ESD Lateral NPN Device in 14nm FinFET SOI CMOS Technology

Zachary Hill

University of California, Riverside

Tel.: 951-264-3734, email: zhill003@ucr.edu

Abstract: I present the development of the ESD lateral NPN device in 14nm FinFET SOI CMOS technology using body-contact and floating-body approaches. The effects of key design factors on the triggering and ESD performance of LNPN devices are investigated to achieve an optimized design.

I. Introduction

The Diode and Silicon-Controlled Rectifier (SCR) can both offer ESD protection, mostly I/O protection of low-voltage integrated circuits (ICs), in advanced Silicon-on-Insulator (SOI) CMOS technologies. However, these two devices are not suitable for mix-signal or high-voltage ICs due to turn-on voltage for Diode being too low and the holding voltage ($\sim 1.2V$) for SCR can cause I/O latch-up issues. This problem mostly occurs with high voltage and low speed I/O applications in the 45nm SOI technology node [1-2].

A valid solution to this issue would be the usage of NFET-based planar devices. Unfortunately, NFETs formed in the planar region were no longer an option due to a significant loss of silicon from the design's limitations with fin pitch and gate spacing. An alternative device named ESD lateral NPN (LNPN) was developed as an ESD solution for mix-signal/high-voltage circuits in FinFET technology. LNPN can provide direct current conduction path from I/O pad to ground without relying on low power bus resistance to achieve adequate clamping voltage. Even so, LNPN devices should be considered built in the planar region as this

approach shows clear performance benefits involving ESD failure current per device area [3].

Throughout this documentation, I will discuss both the development and performance of the optimized ESD LNPN device by comparing two distinct design approaches: Body-contact and Floating-body. Additionally, there will be clarification on the effects of key design factors (base length, base doping, body resistance, etc.) on triggering and ESD performance.

II. Body-Contact Design

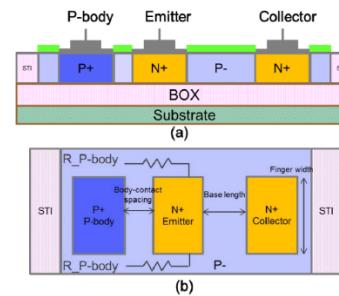


Figure 1: (a) cross-section and (b) top view of ESD SOI lateral NPN device with body-contact design

In Figure 1(a), the cross-section of the body-contact design provides the positions of its three terminals: N+ emitter, N+ collector, and P-body contact with the emitter. The collector will be measured by pulse with rise time = 10ns and pulse width

= 100ns while emitter and P-body terminals are both grounded. Metal wiring connecting P-body and emitter terminals, silicide-blocked region (base length), and finger width are all visible in Figure 1(b). Since the SOI film is considerably thin, the N+ and P+ diffusion can penetrate the P-well region and enter the Buried Oxide (BOX) region just below resulting in a collision of the emitter and collector junctions to form a lateral NPN structure. With N+ and P+ both touching the BOX layer, the P-body resistor, or base resistance of NPN, needs to be formed in the Substrate.

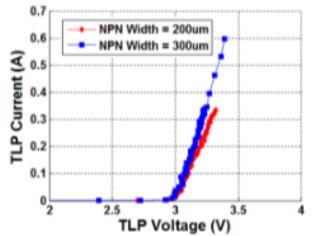


Figure 2: 100ns TLP I-V results of body-contact SOI LNPN devices with width variation

Looking at the 100ns TLP results in Figure 2, there are two NPN Widths used: 200 μm and 300 μm , each with base length = 160nm and finger width = 5 μm . Keep in mind that increasing the total # of fingers will increase the device width. The triggering voltage (the point before current increases) of the LNPN device is ~2.9V. The failure current (last data points in curves, before more leakage appears) increases with larger width. Both lines in Figure 2 curve smoothly, meaning both LNPN devices sustain the TLP current.

The turn-on voltage of LNPN is ~3x higher than the Diode and results in more heat dissipation under the same ESD current. Normalized failure current per width = 1.5~2mA/ μm while the ESD diode, in the planar region, can achieve a failure

rate of 5~6 mA/ μm in the same technology. There is no snapback behavior in either device meaning the risk of latch-up issues for high voltage ESD protection is reduced, unlike a SCR-based solution having a low holding voltage after the snapback.

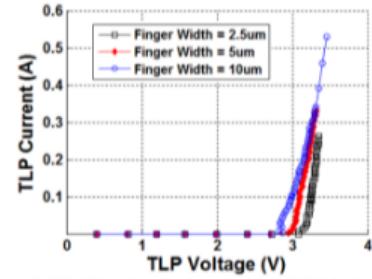


Figure 3: TLP I-V results of body-contact SOI LNPN devices with finger width variation

Looking into Figure 3 you can see 100ns TLP results of body-contact SOI LNPN devices using three finger widths, one of the two design parameters that can affect the ESD performance. Although each finger width is different, the base length (160nm) and device width (200 μm) stays for all devices. The finger width variation affects both trigger voltage and failure current. As seen with the smallest finger width (2.5 μm), trigger voltage increases slightly but the failure current is reduced. This change indicates possible multi-finger triggering issues due to the large number of fingers.

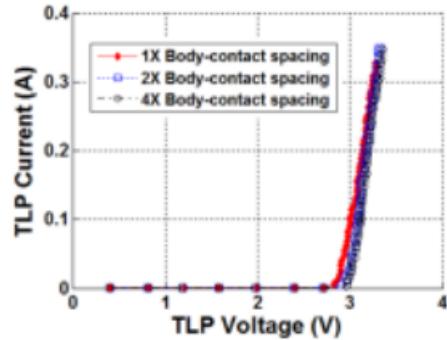


Figure 4: 100ns TLP I-V results of body-contact SOI LNPN devices with body-contact spacing variation

In Figure 4, we have three different body-contact spacings, the distance between P-body contact and N+ emitter terminal and the second design parameter that affects ESD performance. Larger body-contact spacing results in increased bipolar base resistance due to the lack of snapback characteristic. Fortunately, the triggering of body-contact SOI LNPN devices is not sensitive to body-contact spacing. Unlike finger widths in Figure 3, increasing the body-contact spacing likely causes failure current to increase but also, in turn, lowers the devices' area efficiency. Furthermore, decreased body-contact spacing is deemed the optimized design when highest failure current per unit area is concerned.

A lower trigger voltage causes a higher DC leakage while a higher trigger voltage results in more power consumption and reduced ESD performance. Because of this it is sensitive to the NPN device's bipolar characteristics, such as current gain and base resistance. Therefore, we need to understand the NPN base length and base doping, which both affect these bipolar characteristics, in order to properly design trigger voltage and achieve an effective ESD protection for high voltage applications.

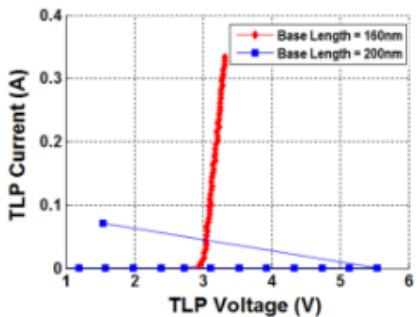


Figure 5: 100ns TLP I-V results of body-contact SOI LNPN devices with base length variation

In Figure 5 above, we have the 100ns TLP results of body-contact SOI LNPN devices with two distinct base lengths (160nm and 200nm) but same width (200μm). Even a small increase in base length causes the triggering to fail because a larger base length results in reduced current gain and the NPN bipolar cannot generate enough base current to initiate the base-emitter junction (BEJ) that turns on the device. This makes base length a characteristic that triggering is sensitive to.

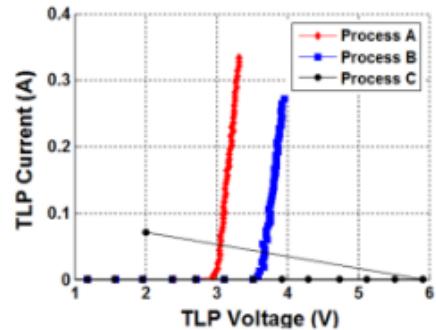


Figure 6: 100ns TLP I-V results of body-contact SOI LNPN devices with P-well implant dosage variation

Another approach that can affect LNPN triggering is process optimization, as shown in Figure 6. In these 100ns TLP results, three process variations (A, B, and C) are provided, each with a device increasing in base doping. You can clearly see the first two sustain the current flow and can still trigger but increasing the TLP voltage causes more heat dissipation which, in turn, slightly reduces the failure current. Since bipolar gain and base resistance, of body-contact LNPN devices, are strongly impacted by base doping, Process C fails to trigger after increasing the dosage even more. This increase makes base resistance too low to produce enough voltage drops across the BEJ to trigger the device.

To better understand their effects on the triggering of LNPN devices, we will use the terms used in Figures 5 and 6 to measure the custom bipolar gain data under DC condition. As shown in Figure 7, current gain drops more significantly for LNPN devices with a larger base length and drops less for those with a smaller base length because of the starting point (current gain for Process A). Those within the dash zone fail to trigger under the 100ns TLP measurements due to them having much reduced current gain. Hence, a small increase in base length or base doping causes bipolar gain and base resistance to significantly decrease causing LNPN devices to fail at triggering.

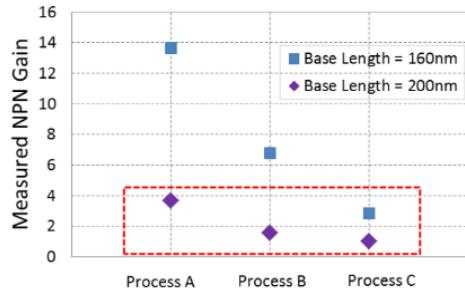


Figure 7: Measured NPN gain under DC condition with base length and P-well implant dosage variation

III. Floating-Body Design

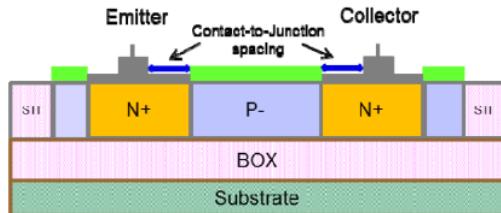


Figure 8: Cross-section of ESD SOI lateral NPN with floating-body design

Knowing a functional LNPN device has a narrow design window for process and dimension variation, we move onto floating-body design to achieve better design flexibility. In the cross-sectional in Figure 8,

P-body contact is ignored leaving N+ emitter (100ns TLP pulses) and N+ collector (grounded) terminals where the TLP I-V characteristics are achieved in the direction of emitter to collector. All other design dimensions are the same as that of body-contact design.

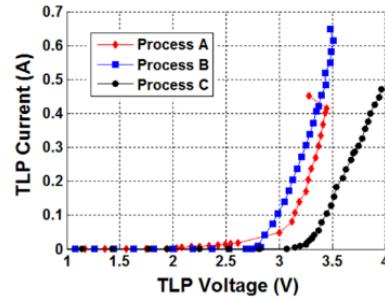


Figure 9: 100ns TLP I-V results of floating-body SOI LNPN devices with P-well implant dosage variation

The 100ns TLP results in Figure 9 use the same base doping processes from Figure 6, only all three devices sustain the TLP current. This difference means triggering is less sensitive to base doping. Because the base region is now floating, base resistance is no longer a key factor in affecting the turn-on of LNPN devices. Process A shows a significantly reduced trigger voltage while that of Process C is higher due to its reduced bipolar gain. However, as we mentioned earlier, higher trigger voltage in Process C results in lower failure current because of the greater power consumption caused by these triggering results.

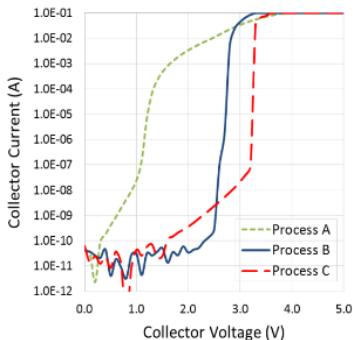


Figure 10: DC measurement results of floating-body SOI LNPN devices with P-well implant dosage variation

Now we review the DC measurement results in Figure 10 and see that Process A has a much reduced static breakdown voltage from the start but the collector current gradually increases shortly after until it passes 3.5V. Although this seems to be the cause of the slow current increase in Process A from Figure 9, there is still an abrupt current increase after breakdown in Process B and C. Even though floating-body design is less sensitive to base doping, Process B is considered the optimum design offering the best ESD performance and lowest leakage current.

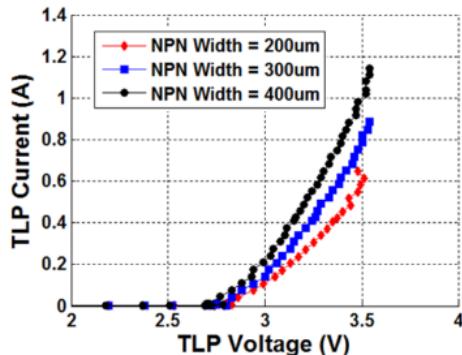


Figure 11: 100ns TLP I-V results of floating-body SOI LNPN devices with width variation

Now let's take a look at three devices each with the same base length (160nm), we'll discuss this later on, and base doping (Process B) but different widths. In Figure 11, there is a consistent current failure rate after each addition of

100 μ m, i.e. current drops by 0.3A after width decreases every 100 μ m (or 3mA/ μ m). This proves the floating-body region performs well at sustaining the current while transitioning to different LNPN devices.

To better grasp this transition between different widths in body-contact and floating-body designs, let's consider the chart in Figure 12. Each device shows a steady increase in capacitance (floating-body => ~0.56fF/ μ m and body-contact => ~0.95fF/ μ m). However, floating-body designs showcase a lower capacitance than the corresponding body-contact design due to the floating base region and base-to-collector and base-to-emitter junction capacitors connected in series.

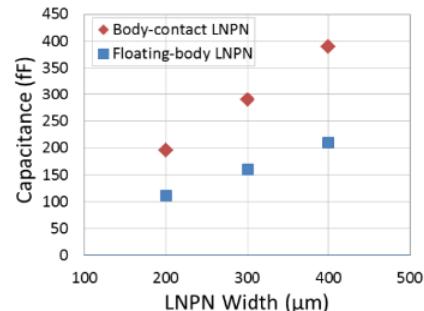


Figure 12: Measured capacitance of floating-body and body-contact SOI LNPN devices with width variation

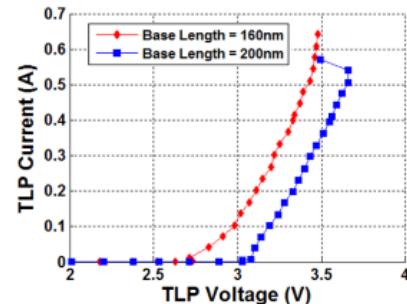


Figure 13: 100ns TLP I-V results of floating-body SOI LNPN devices with base length variation

Although the trigger voltage is much reduced for floating-body devices (2.7V) compared to body-contact (2.9V), we may need to increase it to a certain level. To

determine the correct way to increase in trigger voltage, we can evaluate different base lengths using the 100ns TLP results in Figure 13, each with device width = 200 μ m and process B. Seeing the trigger voltage increase from 2.7V to 3.1V, we can deduce that there are no triggering issues concerning larger base lengths for floating-body LNPN devices, unlike body-contact. However, we again see that failure current has decreased.

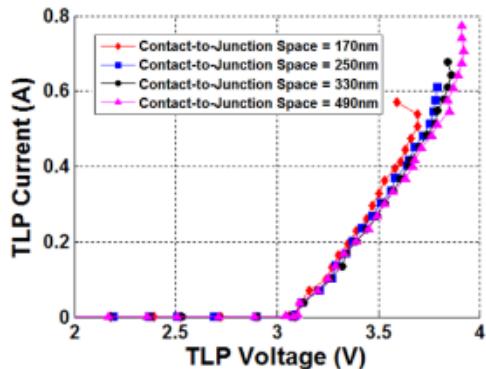


Figure 14: 100ns TLP I-V results of floating-body SOI LNPN devices with contact-to-junction spacing variation

Another design factor that can improve the ESD performance is known as contact-to-junction spacing (CJS), as seen in the cross sectional. Using four different CJS values in Figure 14, each with base length = 200nm and total width = 200 μ m, we find that all these devices can trigger and sustain the current. Keep in mind that larger CJS results in higher contact resistance at the collector and emitter regions and better performing failure current. For example, CJS of 490nm increases the normalized failure current to 3.5~4mA/ μ m. These results occur because the heat generated at the contact is further from the base. However, this larger CJS leads to increased on-resistance and device area. Therefore, it is assumed that the CJS of 250nm is the optimal design.

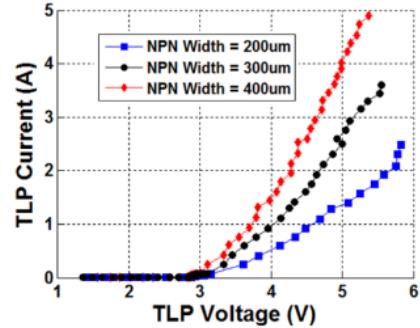


Figure 15: VFTLP results of floating-body SOI LNPN devices with width variation

Lastly, we will measure VERY FAST Transmission Line Pulses (VFTLP) with 1.2ns pulse width and 300ps on-wafer rise time for three devices using the same widths in Figure 11 and base length 200nm. In Figure 15 above, all devices turn on smoothly, sustain the current, and trigger voltage is slightly reduced with increasing width due to the dV/dt effect [4]. We acquire good failure current scaling per width and a normalized failure current of ~12mA/ μ m.

IV. Conclusion

By comparing body-contact and floating-body designs we can deduce a sufficient development for SOI lateral NPN devices.

For body-contact designs, increasing the base length and base doping can significantly decrease bipolar gain and body resistance; both characteristics are highly sensitive in these designs, causing the triggering to fail. The triggering and ESD performance are insensitive to the body-contact spacing due to the LNPN device's non-snapback characteristics. Using the larger finger width, an increased failure current and slightly decreased triggering voltage occur. Body-contact designs have a narrow design window with a normalized failure rate of 1.5~2 mA/ μ m.

Floating-body design contains triggering that is less sensitive to the base doping. Normalized failure current is higher ($2.5\text{--}3 \text{ mA}/\mu\text{m}$) due to the floating body region. Increasing the NPN base length also increases the trigger voltage while larger contact-to-junction spacing improves the failure current. The floating-body design also benefits the LNPN device's capacitance by changing it to $\sim 0.56 \text{ fF}/\mu\text{m}$.

Table 1: Comparison of Diode, SCR and NPN-based ESD solutions for high-voltage I/O protection

	R _{on} ($\Omega\cdot\mu\text{m}$)	I _{fail} per device width ($\text{mA}/\mu\text{m}$)	I _{fail} per device area ($\text{mA}/\mu\text{m}^2$)
Stacked diodes	236	5.5	2.4
Diodes in series with SCR	165	6.2	1.8
Lateral NPN	198	3	2.8

In Table 1, we compare the ESD performances of Diode, SCR and LNPN based solutions for high voltage I/O protection. The LNPN does have the lowest current failure per device width but, in turn, has the highest per layout area. However, the LNPN device saves about 15% to 35% silicon area to achieve the same level of ESD protection (e.g. 1kV HBM) compared to Diode and SCR.

Acknowledgements

This work was modified by Zachary J. Hill, a Computer Engineering student at University of California, Riverside. I would like to thank those at the IBM Microelectronics Division, Semiconductor Research and Development Center, Essex Junction, VT 05452 for completing the previous version of this document.

References

- [1] J. Li, S. Mitra, H. Li, M. Abou-Khalil, K. Chatty and R. Gauthier, "Capacitance Investigation of Diode

and GGNMOS for ESD Protection of High Frequency Circuits in 45nm SOI CMOS Technologies," Proc. EOS/ESD Symp., pp. 1-8, 2008

[2] S. Mitra, R. Gauthier, J. Li, M. Abou-Khalil, C. Putnam, R. Halbach and C. Seguin, "ESD Protection Using Grounded Gate, Gate Non-Silicided (GG-GNS) ESD NFETs in 45nm SOI Technology," Proc. EOS/ESD Symp., pp. 1-7, 2008

[3] J. Li, R. Gauthier, Y. Li and R. Mishra, "ESD Device Performance Analysis in a 14nm FinFET SOI CMOS Technology: Fin-based versus Planar-based," Proc. EOS/ESD Symp., pp. 1-6, 2014

[4] V. Vassilev, G. Groeseneken, M. Steyaert and H. Maes, "Enhanced ESD Protection Robustness of a Lateral NPN Structure in the Advanced CMOS," Proc. IRPS, pp. 605-606, 2004