GGNMOS Process TCAD Simulation

Lab3

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ABSTRACT:

In this lab, we focused on utilizing TCAD and Sentaurus Process to simulate the electrical, thermal, and optical characteristics for the GGNMOS structure, where many widely used process and control commands are utilized. GGNMOS is somewhat similar to the Pplus Nwell Diode from the previous labs, except it consists of a Pwell rather than an Nwell, only two STIs (middle taken out), two Pplus (one on each side) and two Nplus(one on each side the top middle), the Anode/Cathode are replaced with Source/Drain, and a polysilicon gate is in between the Nwells connecting the Source and Drain. The process flow of GGNMOS is calculated as a nominal 0.18um. We also reviewed the graph taken for the Drain as well as the 2D images of a few additions that lead to the creation of the overall GGNMOS.

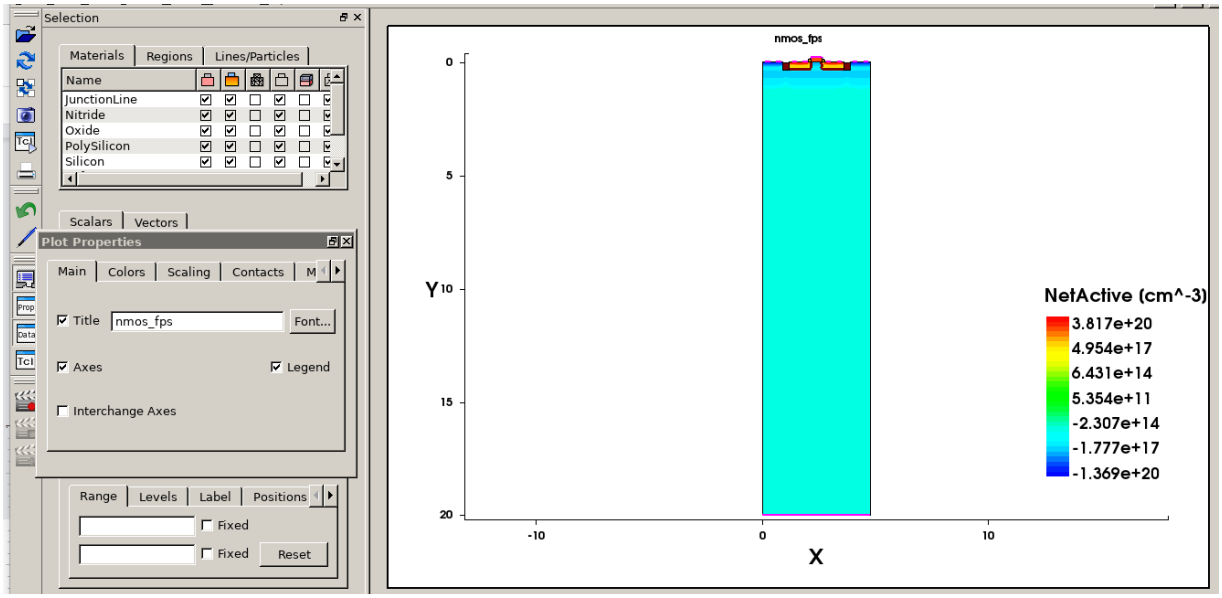
Commands:

1. bender /home/cemaj/zhill $ mkdir Lab3

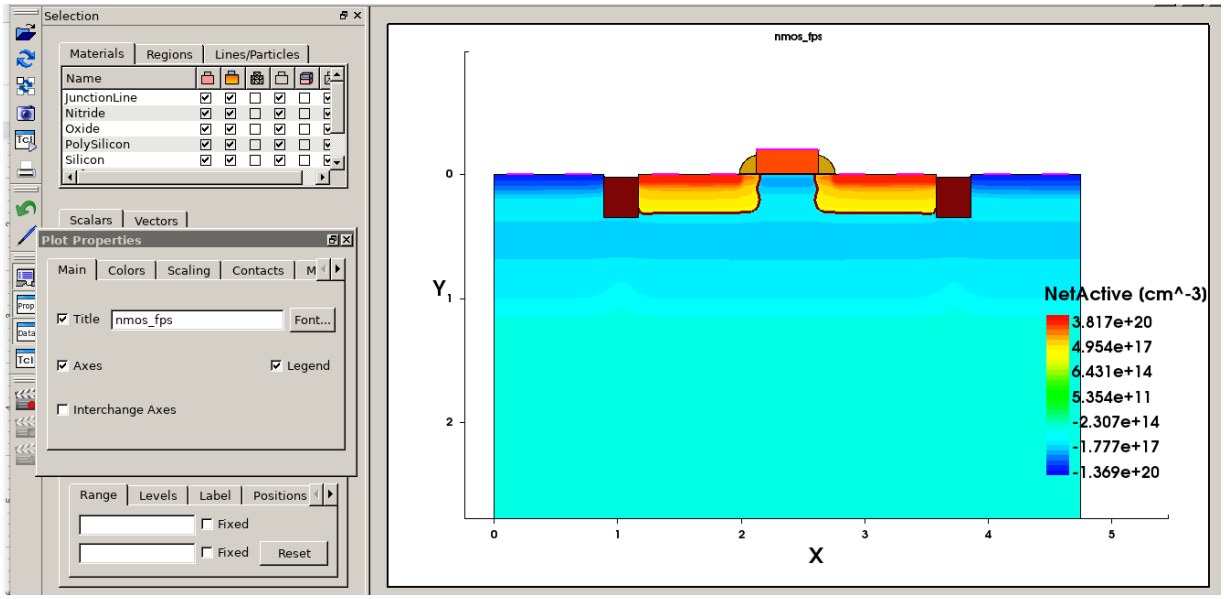
2. bender /home/cemaj/zhill $ cd Lab3

3. bender /home/cemaj/zhill/Lab3 $ sprocess ggnmos_CSMC.cmd &

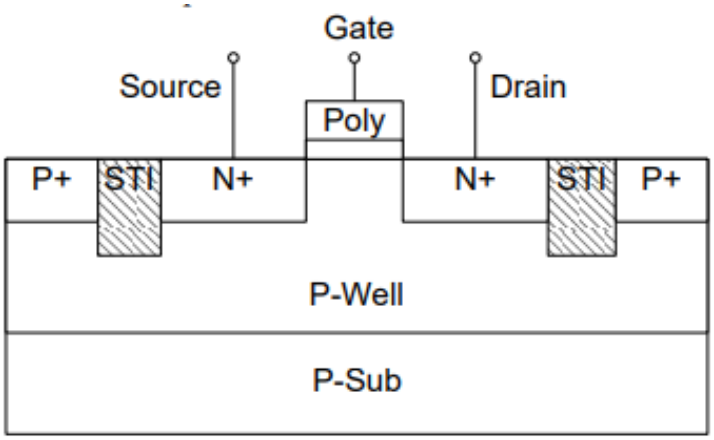
4. bender /home/cemaj/zhill/Lab3 $ svisual &



(a) 2D graph of GGNMOS X-section



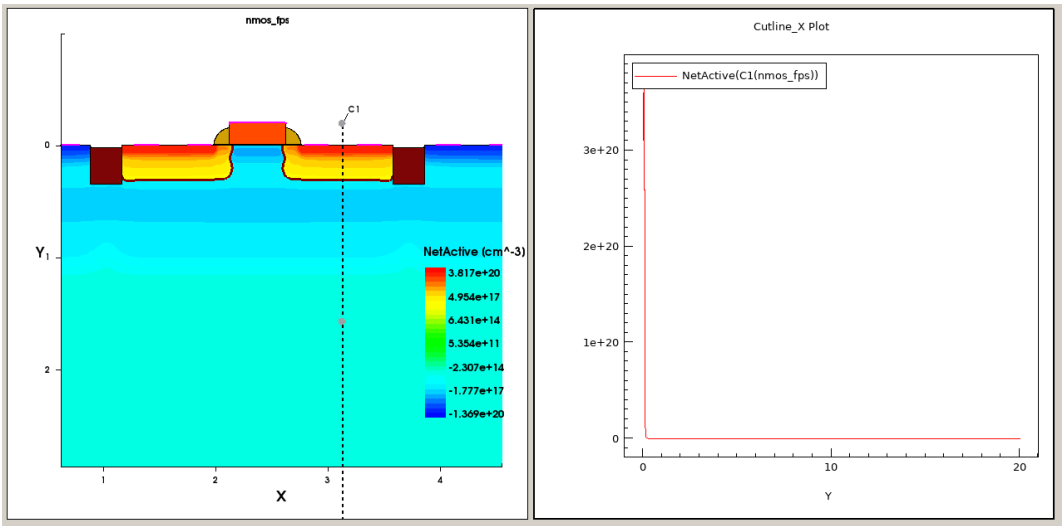
(b) Zoomed-in version of Figure 1(a)



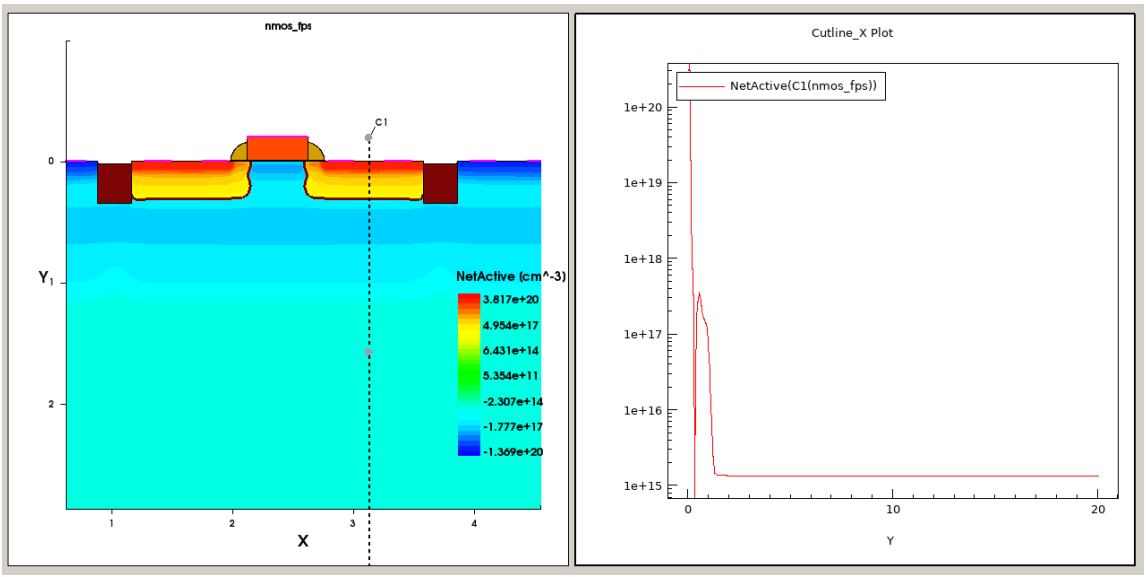
(c) Visual representation of GGNMOS X-section

Figure 1: Images of the final GGNMOS X-section

Each component of the GGNMOS is visible within the 2D graph, including P-sub, P-well, Pplus, Nplus, STI, poly-gate (and the spacer beside it), and Source/Drain. We can clearly see the Pplus regions are the least active then P-well is next least active, along with the contact spot for the polysilicon gate, then P-sub. Nplus regions show most activity, especially at the very top where the Source/Drain connect.



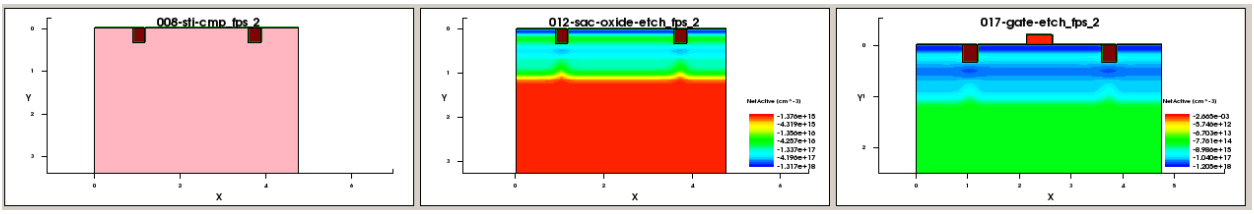
(a) 2D graph before log(y)



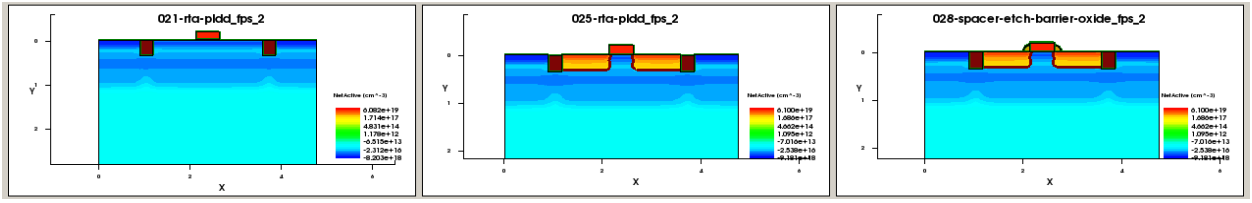
(b) 2D graph after log(y)

Figure 2: Line graph representing the activeness for the Drain

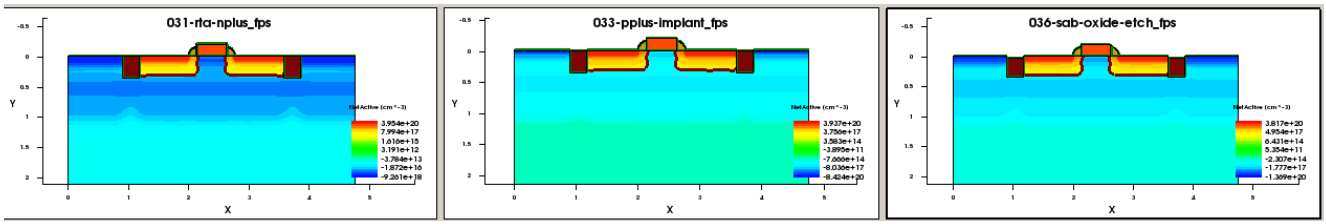
According to Figure 2 (b), the NetActive value begins to gradually decrease after Y=0 but then shoots back up for a short time, until about 1e+17.5, then back down again. Just over 1e+15 the line remains constant at each new value of Y.



(a) STIs are formed; oxidation of SAC around the entire simulation; Gate formed/etched



(b) Rapid thermal annealing (RTA) of PLDD (including after Nplus regions formed); spacer is etched



(c) RTA of Nplus regions; Pplus regions implanted; oxidation of SAB

Figure 3: GGNMOS processing steps simulation results

In the nine processing steps above, we begin to see how the GGNMOS is formed, this is a quick version. The STIs are the first components formed then the entire simulation is oxidized (SAC). Next, the gate is etched followed by multiple processes of rapid thermal annealing, both before and after the Nplus regions are formed, then the spacer is etched on both sides of the gate with an oxidized barrier. RTA of Nplus regions is again implemented to provide the contact spots for Source and Drain. Lastly, the Pplus regions are implanted on the far ends then the whole simulation is once again oxidized, only this time it is (SAB), which can be seen with slightly different colors in P-well and P-sub.