Final Project GGPMOS EE165

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***Abstract*—There is a certain type of Metal Oxide Semiconductor we will analyze and it is called the GGPMOS. In this paper we will explore various aspects of how specifically the GGPMOS is incorporated to be a better performing ESD device.**

***Index Terms*—MOSFET, Nanotech, GGPMOS**

I. INTRODUCTION

A GGPMOS stands for a Grounded Gate P channel Metal Oxide Semiconductor. We used TCAD and the Sentarus Process to simulate electrical, thermal, and optical characteristics of a GGPMOS structure. The process flow of GGPMOS is calculated as a nominal 0.18um. We used svisual to produce the images of structure and we analyzed the steps such as the step that Gate is formed, spacer is formed, and S/D is implanted. These simulations help us with analyzing the etching, deposition, ion implantation, thermal annealing, and oxidation of different structures and we used these techniques to analyze the GGPMOS in this simulation.

The Sentarus Structure editor provides us with a 2D GGPMOS device structure that we then build a mesh. We used svisual to produce the images of structure to see lattice temperature and current density. We simulated this structure under the Human Body Model where we also used streamlining to analyze current flow of the structure. We then graphed the Current v Voltage and the Temperature v Time for the GGPMOS.

II. EXPERIMENT

We used svisual to produce the images of the GGPMOS structure.

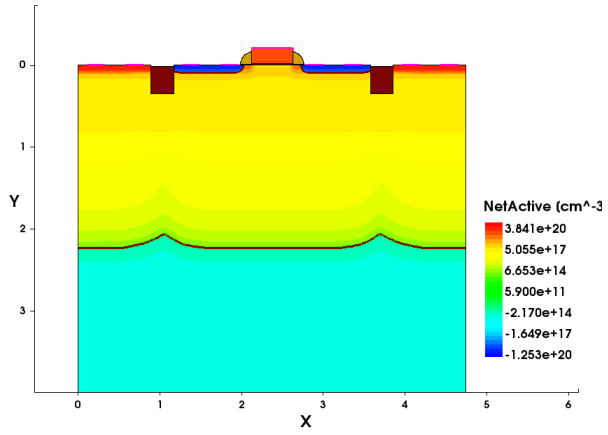


Figure 1: GGPMOS X-section and doping profile

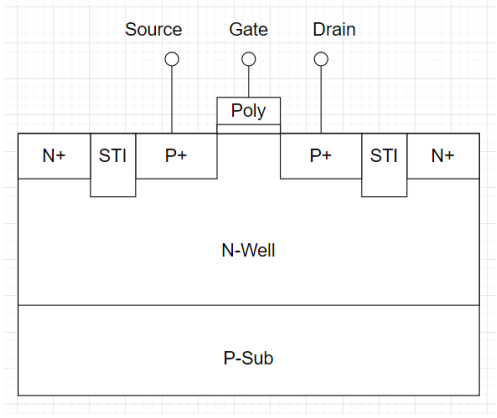


Figure 2: A GGPMOS X-section to compare to our simulation visual in Figure 1

We can clearly see the similarities of the two images in Figure 1 and 2. The poly-gate is formed in the center with the spacer on both sides. There are also two STIs and the P-substrate on the bottom, just like with ggNMOS; however, the source and drain are connected by P+ contacts and ggPMOS contains an N-well. Looking at the doping structure in Figure 1, the N-well has a much higher concentration than the P-substrate and, although the P+ and N+ retain the same concentration, P+ less area space compared to when the N+ contacts are connected to Source/Drain.

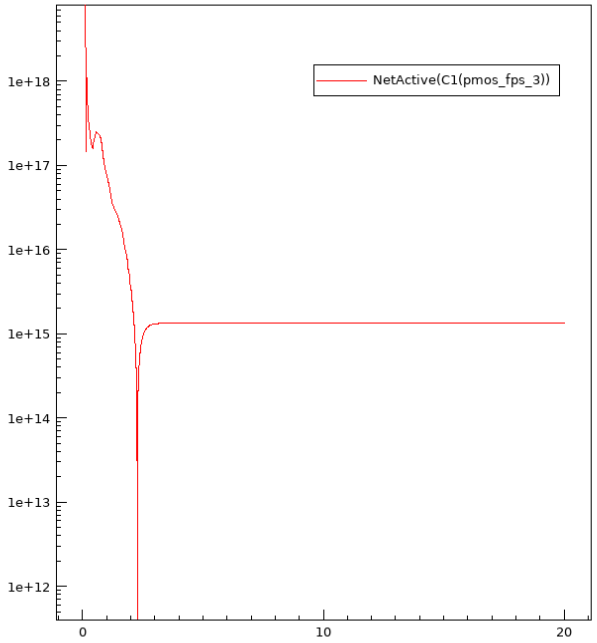
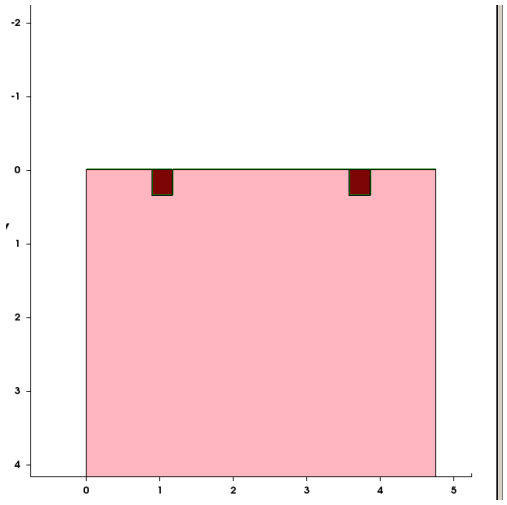
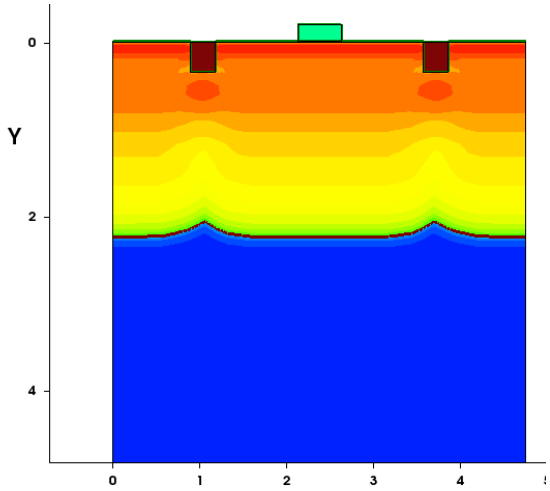


Figure 3: Drain vs. Depth graph along with pmos image (log_y)

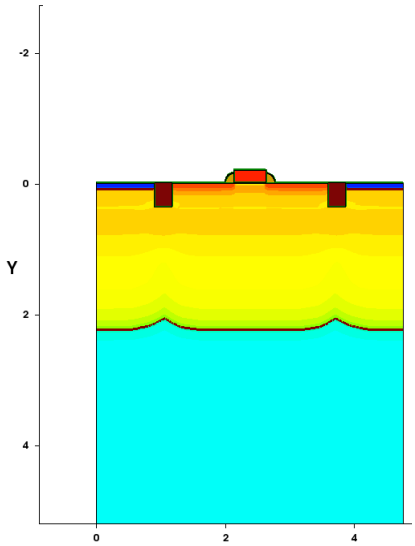
This figure shows the X cut of the middle of the Pplus rain region. The graph illustrates the one dimensional profile of the net-active concentration of the drain vs. depth. Net activation starts out high but begins to decrease significantly by slightly increasing the length of depth. Figure 3 shows the decrease in net activation across drain stops just after X = 2 and begins to increase significantly until it reaches X ~ 3 (Y = 1e+15). Once this depth is reached, concentration remains constant throughout.



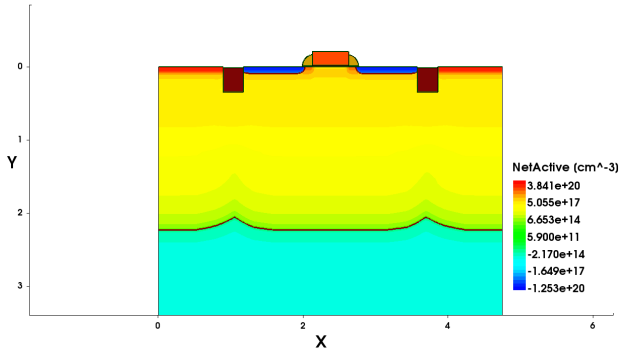
(a)



(b)



(c)



(d)

Figure 4: Steps where Gate is formed, spacer is formed, and S/D is implanted. Illustrates the Gate, spacer, and contact formation and the S/D implantation.

The program starts with Figure 4(a) by creating the dimension of the device as well as masking of both STIs. In Figure 4(b), the entire device is oxidized giving us the net activation for P-substrate, then we build the N-well in the upper region where it is oxidized as well. The gate is constructed in between the source/drain (not yet formed) but remains unoxidized. Before the contacts are formed, the poly-gate is oxidized, as shown in Figure 4(c). Next, the PLDD and NLDD are initialized on their respective sides of each STI, PLDD in the same vicinity as the gate. Note: Rapid Thermal Annealing (RTA) needs to be implemented, after every new implantation involved with creating the P+/N+ regions, in order to heat up the silicon wafer then cools down giving this material the appropriate electrical/physical properties. Spacer is initialized along both sides of the gate to limit the prolongation of the lightly doped extensions under the gate. Figure 4(d) shows the creation of N+ and P+ regions as well as RTA and oxidation of each set. Note: the poly-gate needs to be oxidized again after N+ and P+ regions are completed. Lastly, the Source/Drain contacts are initialized on one of the two P+ regions.

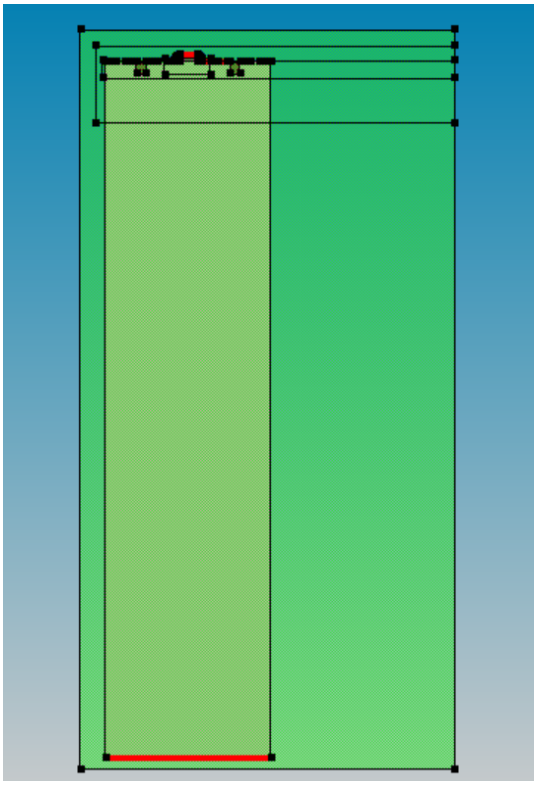
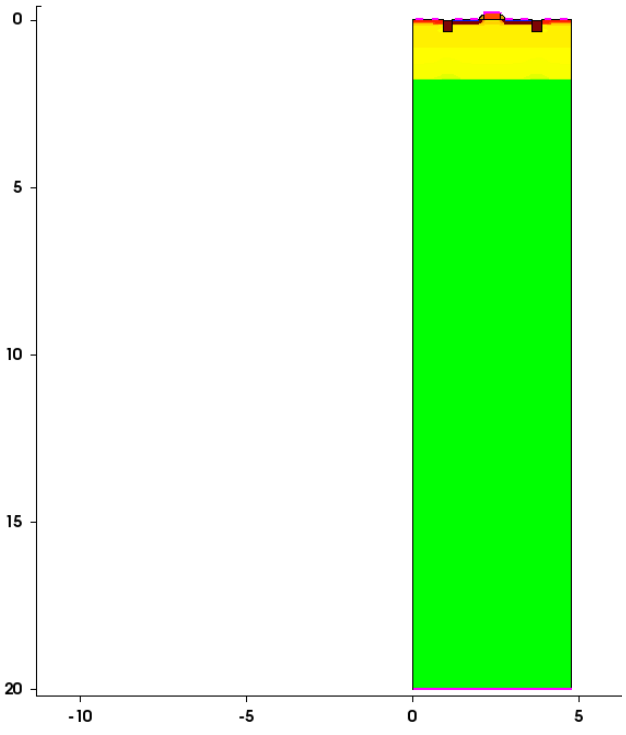


Figure 5: GGPMOS Device structure



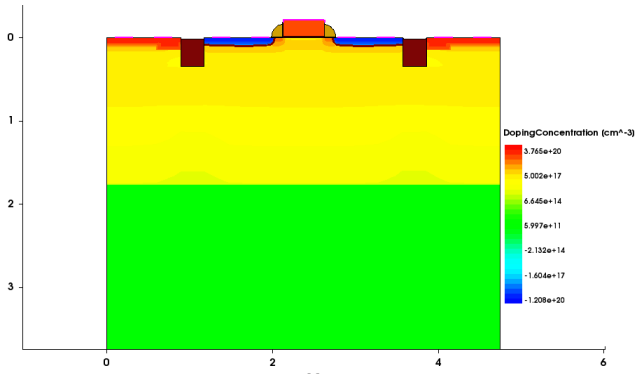


Figure 6: Structure before Mesh is applied

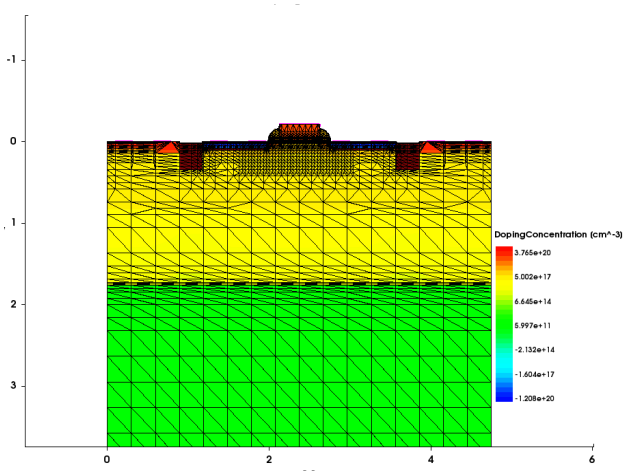


Figure 7: This is the fully meshed GGPMOS Structure

The meshing generation process that we used in this project defines the maximum and minimum meshing sizes to a specific target, which is, in general, a material, or a device region, or a user-defined evaluation window.

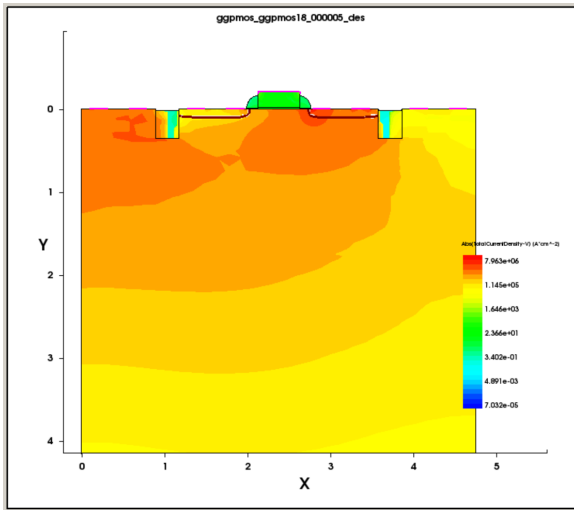


Figure 8: GGPMOS Total Current Density at 10ns

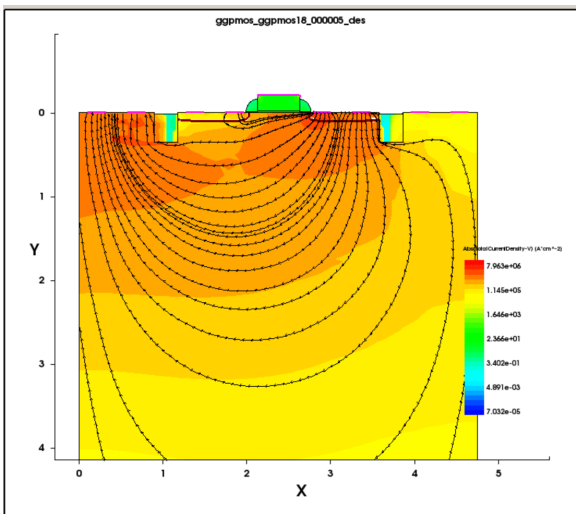


Figure 9: 20 Streamlines applied on the GGPMOS

For this figure, the streamlines represent the current flow. It also shows a color gradient for total current density. Current Density is defined as “the amount of charge per unit time that flows through a unit area of a chosen cross section.” according to Wikipedia.

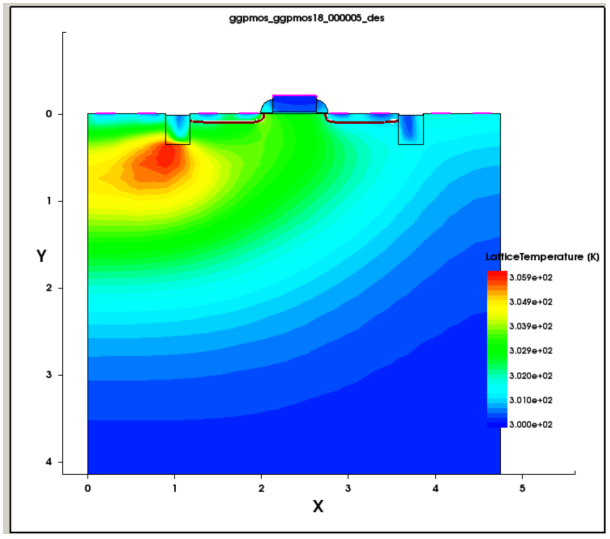


Figure 10: GGPMOS hotspot

This figure shows how we used Sentarus Device to produce an image that illustrates the GGPMOS thermal characteristics by selecting Lattice Temperature. When the lattice temperature is above 1688, the silicon is melted. Simulation will be ended due to high temperature failure.

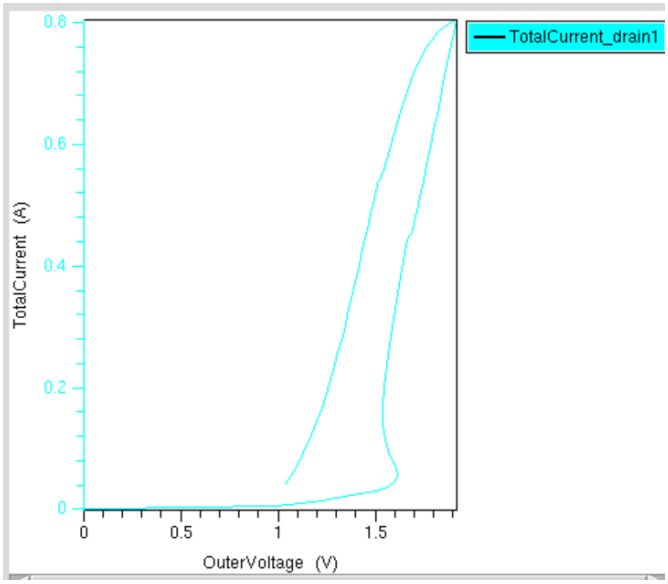


Figure 11: Current vs. Voltage

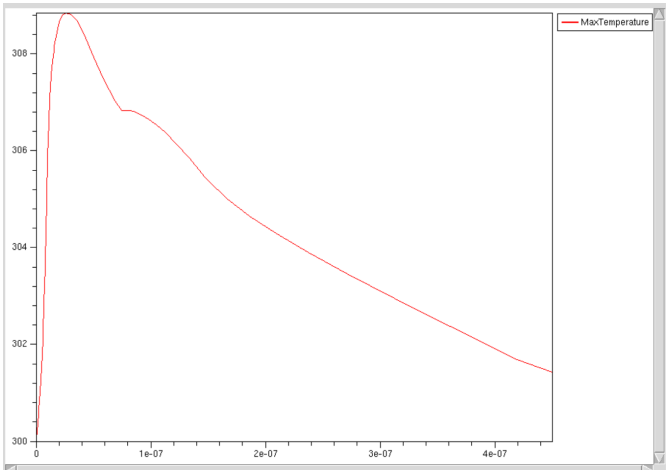


Figure 12: Temperature vs. Time

These graphs show the I-V and temperature results of the simulation of the GGPMOS and it is run with the HBM.

III. Commands

GGPMOS TCAD Simulation

bender /home/eemaj/zhill/Final $ sprocess ggpmos_CSMC.cmd &

bender /home/eemaj/zhill/Final $ svisual &

GGPMOS Mesh TCAD Simulation

bender /home/eemaj/salexander/Final $ sde –l m3d.jrl & -noopenGL

bender /home/eemaj/salexander/Final $ sdevice hbm_for_ggpmos18.cmd &

bender /home/eemaj/salexander/Final $ inspect &

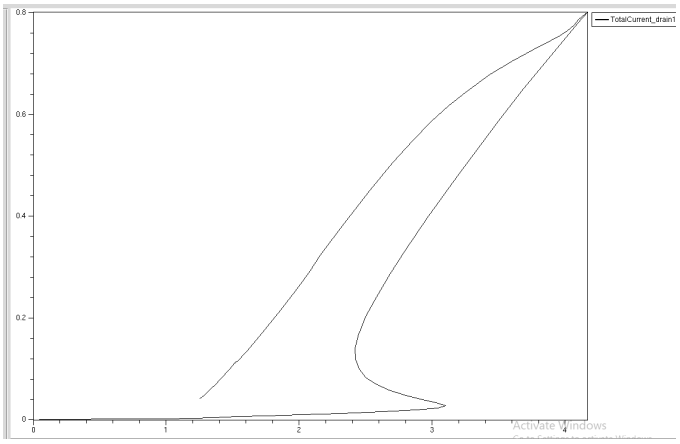
bender /home/eemaj/salexander/Final $ svisual &

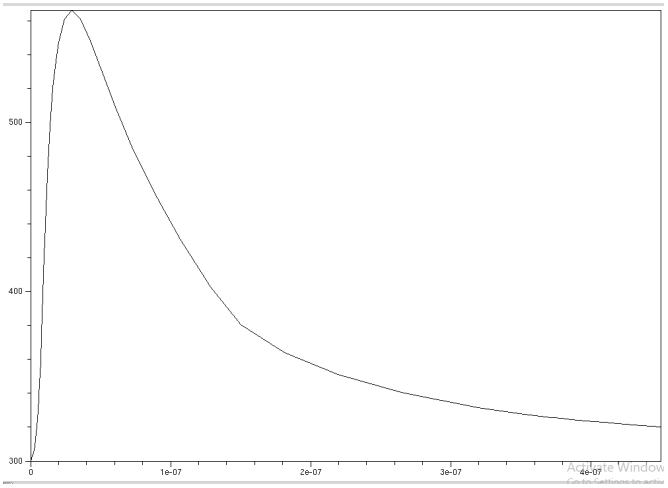
HBM Minimum Width TCAD Simulation

bender /home/eemaj/zhill/Final $ sdevice hbm_for_ggpmos18_af.cmd &

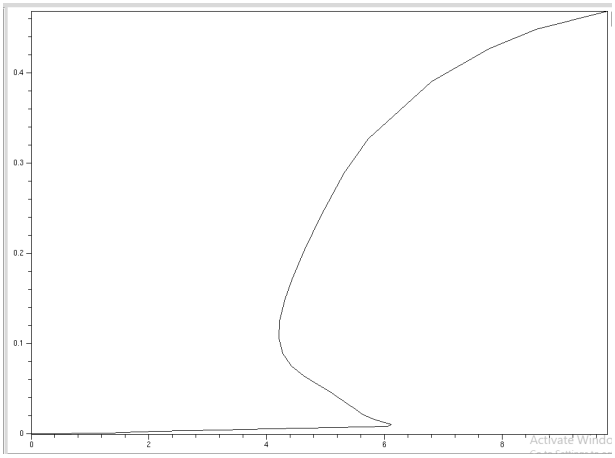
bender /home/eemaj/zhill/Final $ inspect

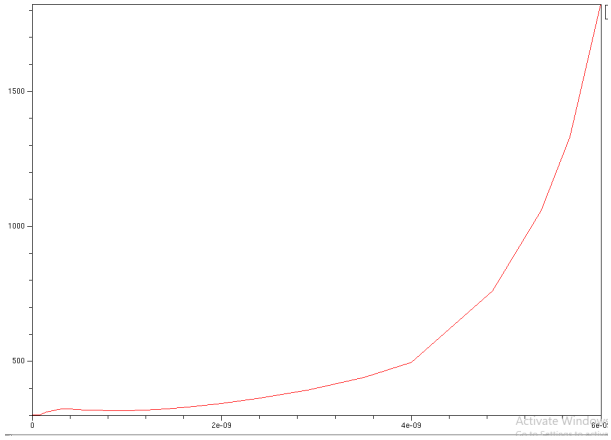
IV. Minimum HBM Width



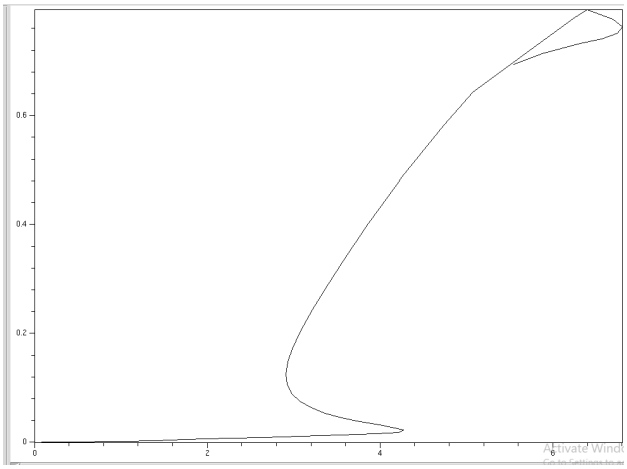


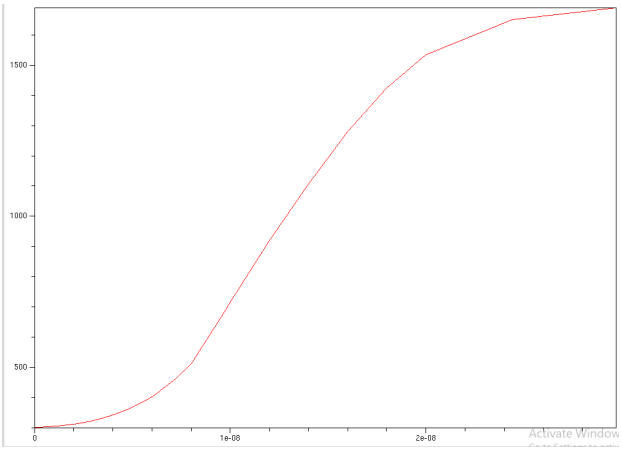
(a)



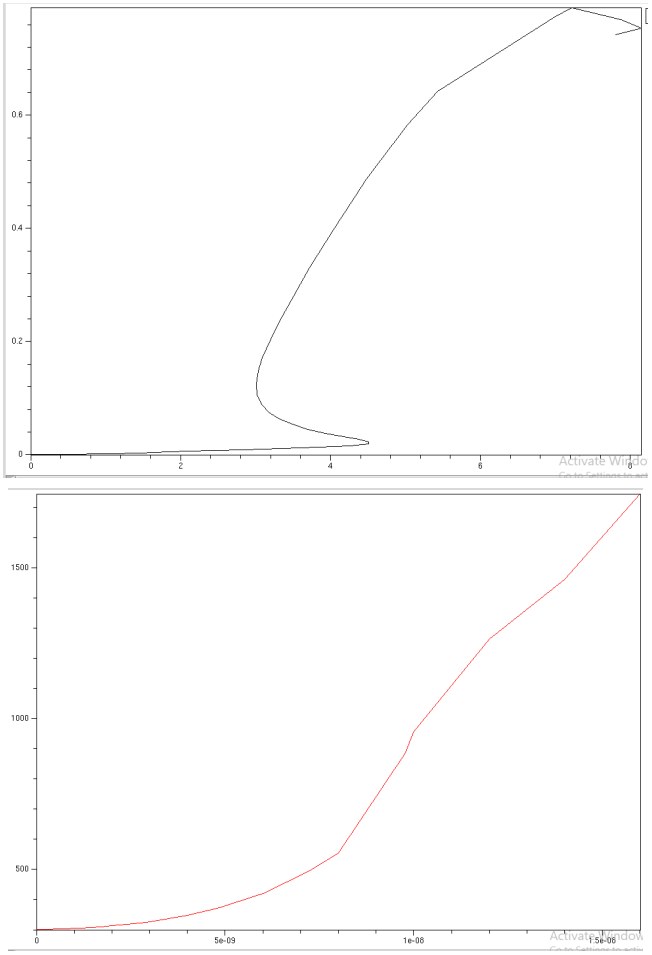


(b)





(c)



(d)

Figure 13. I-V and time vx Tmax results; (a) 10um, (b) 5um, (c) 12um, and (d) 11um

For the current to continuously flow without any leakage, the lattice temperature needs to be less than 1680, otherwise the silicon structure begins to melt. We need to find the lowest possible HBM Width to prevent the silicon from melting but, simultaneously, keep the current increasing at the best possible rate. Looking at Figure 13(a) the current, with HBM width at 20um, continues to flow after reaching the highest point but in Figure 13(b) the opposite occurs when we decrease the width to only 5um, meaning this width does not pass and must be increased. Changing the width to 12um, Figure 13(c), the current flows continuously again and the lattice temperature is < 1680. By decreasing the width by 1um the lattice temperature is now > 1680, as shown in Figure 13(d), making 11um the danger value. This also means 12um is the minimum HBM width for GGPMOS!

V. Bonus Experimentations

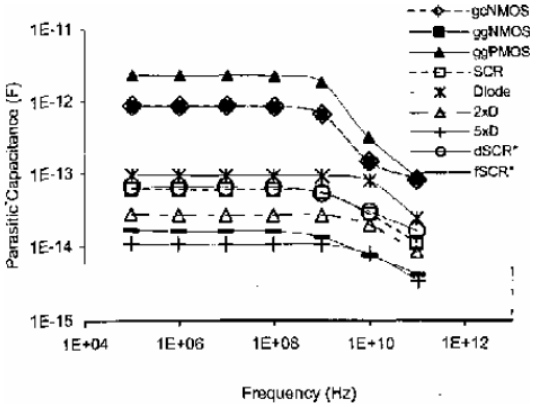


Fig 14.

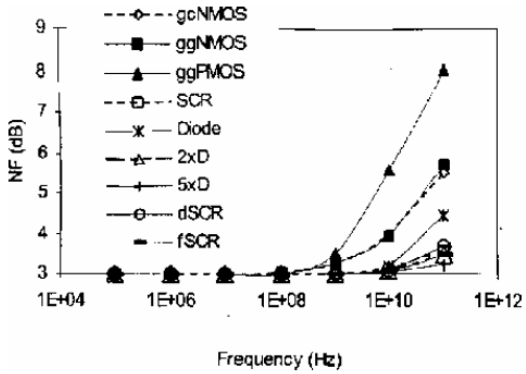


Fig. 15

"It is clearly observed that ggNMOS, gcNMOS & ggPMOS experience much more signal losses compared to diode and SCR type ESD structures." This is what the authors of the paper said about the comparison between ESD structures represented in the graphs.

devices	ggNMOS	ggPMOS	Diode	2xDiode
width (um)	110	238	25	25
R_{ON} (Ω)	4.26	10.53	0.19	0.37
devices	5xDiode	SCR	dSCR	fSCR
width (um)	25	25	36	26
R_{ON} (Ω)	1.01	-	-	-

Table 1 ESD device widths & active discharging resistances.

IV. Conclusion

To conclude, we used the Sentaurus Process to simulate electrical, thermal, and optical characteristics of a GGNMOS structure just like in lab 3 but with different techniques to analyze. The

Sentaurus Structure editor provides us with a 2D GGNMOS device structure that we then build a mesh just like we did in lab 2. We used svisual to produce the images of structure to see lattice temperature and current density. We simulated this structure under the Human Body Model where we also used streamlining to analyze current flow of the structure. We then searched for the minimum to pass by examining the Current vs Voltage curve and the Temperature vs Time curves for both structures.

Acknowledgment

I would like to thank the TA who did an excellent job at teaching us the fundamentals of these procedures. I would like to thank the professor for teaching a great class.

References and Footnotes

[1] Z. Huang, M. Liu, Ming Zhu and Y. Li, "Simulation of the HPM power and pulse width on the influence of ESD protection device," 2016 Progress in Electromagnetic Research Symposium (PIERS), 2016, pp. 2819-2824, doi: 10.1109/PIERS.2016.7735132.

[2] Lo, H. W., and A. Compaan. "Raman measurement of lattice temperature during pulsed laser heating of silicon." Physical Review Letters 44.24 (1980): 1604.

[3] Guang Chen, Haigang Feng and A. Wang, "A systematic study of ESD protection structures for RF ICs," IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 2003, 2003, pp. 347-350, doi: 10.1109/RFIC.2003.1213959.