~~Lab~~ 06 Prelab

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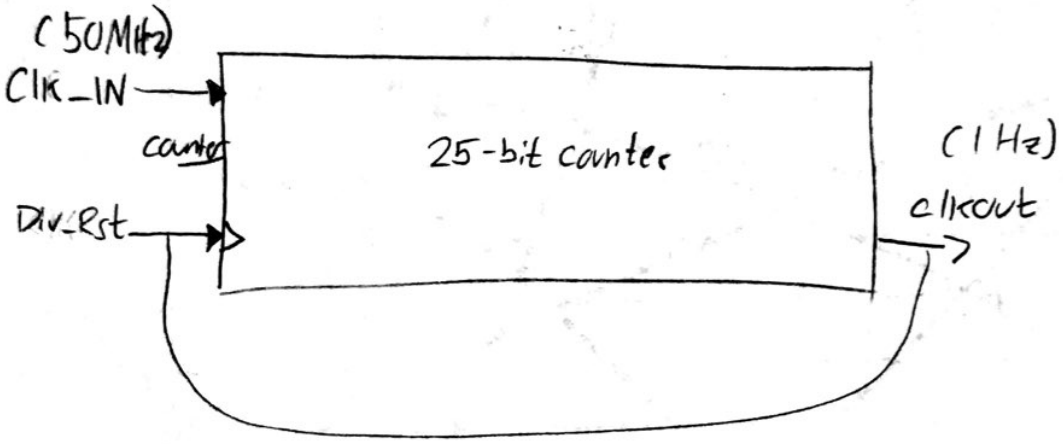
1) 50 MHz

Choosing a counter

$2^{24} = 16,777,216$
$2^{25} = 33,554,432$
$2^{26} = 67,108,864$

But we only need $\frac{50\,MHz}{2} = 25\,MHz$ since always(posedge clk)

We can choose a 25 bit counter and use a "max" value constant of 25,000,000 to get 25MHz. Or rather, choose 24,999,999 or some similar value to avoid an incorrect reset.



PSUEDO CODE

```
module clockDiv(clk, Rst, clkout)
  constants: MAX = 25,000,000
  register: [24:0] counter
  begin

  always at positive edge
    if Rst=1
    counter=0
    clkout=0
    else if counter == 25,000,000
      counter=0; clkout = !clkout
```