Lab 1 – Part 1: Introduction to Verilog Simulation

Starts: August 25, Friday
Demo Due: In-class same day **Report Due:** no report required
Points: 50

Files

Xilinx ISE Simulation Tutorial (written for Version 11)

This semester we have Xilinx ISE Webpack version 14 installed in Room 209. Although the tutorials were written for version 11, there is very little difference between these two versions for our purpose.

Lab Overview:

In this lab, your team will design a library of basic logic gates including a 2-input AND gate, a 2-input OR gate, and an inverter (INV gate). Using these basic components, one can build any combinational logic.

Pre-Lab (required before lab session):

Finish reading the following two documents.

- Xilinx ISE Simulation Tutorial (written for Version 11)

Lab Procedure and Demo:

1. 2-input AND gate ***(20 points)***
    - Follow the Verilog simulation tutorial to design a 2-input AND gate. Test your design exhaustively simulating all possible combinations.
    - Demo to your TA that your AND gate simulation works.
2. 2-input OR gate ***(20 points)***
    - Design a 2-input OR gate. Test your design exhaustively simulating all possible combinations (You have to write your own testbench).
    - Demo to your TA that your OR gate simulation works.
3. INV gate ***(10 points)***
    - Design an inverter (INV gate). Test your design exhaustively simulating all possible combinations (You have to write your own testbench).
    - Demo to your TA that your INV gate simulation works.

Lab Report/Code Requirements

No lab report is required for the first lab. Show your work to your instructor in-class.

Notes:

1. Please save your work on a USB drive, not on network drive.
2. This is a practice lab for your team. However, we want to see rotation of roles in this lab. Each of you needs to design and simulate at least one basic gate in the rotation.
3. When you are ready to demo, signal your TA and show your design and simulation results of each gate. You have this one chance to demo everything to your TA.