Disturbance Observer Based Second Order Sliding Mode Control for DC-DC Buck Converters

Yunfei Yin*, Jianxing Liu*, Sergio Vazquez†, Ligang Wu* and Leopoldo G. Franquelo†,*
*Research Institute of Intelligent Control and Systems, School of Astronautics, Harbin Institute of Technology, Harbin, China 150001. email:yunfeiyin@hit.edu.cn, jx.liu@hit.edu.cn, ligangwu@hit.edu.cn
†Electronic Engineering Department, School of Engineering, Universidad de Sevilla, Seville, Spain 41092. email: sergi@us.es, lgfranquelo@ieee.org

***Abstract*—In this paper, a novel scheme of disturbance observer based second order sliding mode (SOSM) control for DC-DC buck converters is proposed. A cascade-control structure is established to regulate the output voltage and force the inductor current to track its reference, which comprises two control loops. The voltage regulation loop which is based on an SOSM controller combined with extended state observer (ESO) is the external loop. The current tracking loop also accomplished by SOSM controller is the internal loop. The fast motion is dominated by the dynamics of the current tracking loop whereas the slow motion stems from the dynamics of the output voltage. In addition, the load resistance that influences significantly the dynamics of whole system is regarded as the external disturbance in this papper. A disturbance observer, ESO, aims at asymptotically rejecting disturbances to converter. The proposed control strategy is verified using simulation test.**

Keywords: DC-DC Buck Converters; Cascade control; Disturbance Observer; Second Order Sliding Mode.

I. Introduction

The DC-DC converter, also called DC chopper, is the electronic circuit which can convert a source of direct current from one voltage level to the fixed or adjustable one. In the last decades, considerable attention has been paid to the study of this converter due to its numerous applications such as the batteries of mobile phones and computers, LED power sources, switching power supplies and welding power sources, etc. However, because of the uncertainties of power supply and load requirements, in some applications the converter need to promptly regulate the output voltage to the desired values under the conditions of input voltage disturbances and abrupt load variation. Therefore, it is significant to design an efficient control scheme to control the converters [1], [2].

Many control strategies have been proposed to control this converter during the last decades [3]–[5]. At first, the traditional linear controllers have been applied to this converter based on linear model. Due to the design of linear controllers only at a nominal operating point, they can not maintain the smooth output voltage under the parameters uncertainties or load changes [6]. After, a lot of advanced nonlinear control approaches such as sliding mode control (SMC) [4], one-cycle control [7] and fuzzy logical control (FLC) [8], [9] have been adopted to solve this problem. Since DC-DC converter itself is a nonlinear system, these nonlinear control schemes, especially SMC that is less sensitive to parameter uncertainties and disturbance, can effectively and quickly regulate output voltage to its reference. Meanwhile, as the DC-DC converters are the switching devices by nature, it is natural to employ SMC to control the converter.

Generally speaking, there are a couple of approaches for SMC method, direct SMC and indirect SMC, in application to DC/DC converters [10]. The direct SMC as the traditional approach in which the result of the control action directly control the switching semiconductor can cause extremely high switching frequency [11]. This is because the property of SMC which occurs at infinitely high frequency to eliminate deviations from sliding manifold. The high switching frequency not only increase the power loss but also shorten converters' life. To address this problem, indirect SMC method has been put forward, where the result of the control action is first applied to PWM module then to switch device. The advantage of this approach is that it can reduce switching frequency and obtain fixed switching frequency. However, SMC operates at finite frequency, which will lead to chattering around the sliding manifold [12]. The high-order sliding mode (HOSM) method is introduced to deal with this problem in this paper. The HOSM is one of the most promising approach to reduce this undesired chattering effect [13]. It not only guarantees that the first-order time derivative of the sliding variable is continuous, but also preserves the main advantages of robustness and finite-time convergence [14]. In this paper, a super-twisting algorithm (STA) will be designed to control the DC-DC buck converters. Different from other HOSMs, STA does not need the information about derivatives of the sliding variable. STA has been widely employed in various areas such as aircraft [15], power electronics [16], fuel cell power systems [17].

On the other hand, it is worth pointing that most of aforementioned works control the DC-DC buck converter normally based on a single rate-loop control structure. It is generally known that compared with single control structure, cascade structure can achieve more control objectives and has better ability of resisting noise. In this paper, a cascade control structure is proposed to control the DC-DC buck converters, which includes the current tracking loop and voltage regulation loop. The current tracking loop is the internal loop, where an STA controller is employed to force the inductor current towards its desired value, a slowly varying signal generated by the external loop. The voltage regulation loop is the external loop and its control objective is to regulate the

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output voltage. However, the load resistance considered as the external disturbance affects the dynamic features of output voltage directly [18]. Thus a disturbance observer, extended state observer (ESO), is used to estimate the load disturbance aiming at asymptotically rejecting disturbances in this paper. The STA combined with ESO is established for the voltage regulation loop to improve the system performance.

The rest of the paper is organized as follows. Section II outlines the model of DC-DC buck converter, the basic principle of second order sliding mode and the control objectives. The detail of control strategy is presented in Section III. The simulation results are provided and analyzed in Section IV, and there are short concluding remarks in the section V.

II. Problem formulation and preliminaries

A. Model of dc-dc buck converter

Fig. 1 depicts a basic topology of the buck converter, in which v_{in} is the input DC voltage; L is the filter inductor with a parasitic resistance r; C is the output capacitor; R_L is the equivalent load. Then the system dynamics of the buck converter can be expressed as [4],

$$L\frac{di_L}{dt} = -ri_L - v_{out} + uv_{in}, \tag{1}$$

$$C\frac{dv_{out}}{dt} = i_L - \frac{v_{out}}{R_L}, \tag{2}$$

where i_L is the inductor current; v_{out} is the output capacitor DC voltage; u is the control input.

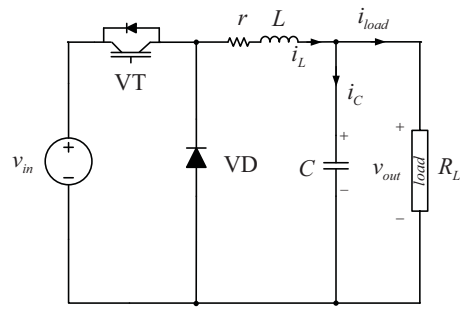

Fig. 1. Synchronous rectifier based on the three-phase two-level power converter

B. Second order sliding mode

Consider a general nonlinear system,

$$\dot{z}(t) = f(t,z) + g(t,x)u(t) \tag{3}$$

$$y = \sigma(t,z), \tag{4}$$

where $z(t) \in \mathbb{R}^n$, $u(t) \in \mathbb{R}^r$ denote the state vector, the control input, respectively; $f(t,z)$ and $g(t,z)$ are smooth uncertain functions; $\sigma(t,z)$ is the sliding variable. Then the first and second derivative of sliding variable $\sigma(t,z)$ are obtained,

$$\dot{\sigma}(t,z) = \frac{\partial}{\partial \mathrm{t}}\sigma(t,z) + \frac{\partial}{\partial z}\sigma(t,z)[f(z,t) + g(z,t)u(t)] \tag{5}$$

$$\begin{aligned}\ddot{\sigma}(t,z) &= \frac{\partial}{\partial \mathrm{t}}\dot{\sigma}(t,z,u) + \frac{\partial}{\partial z}\dot{\sigma}(t,z,u)[f(z,t) + g(z,t)u(t)] \\ &\quad + \frac{\partial}{\partial u}\dot{\sigma}(t,z,u)\dot{u}(t) \\ &= \psi(t,z,u) + \omega(t,z,u)\upsilon(t),\end{aligned} \tag{6}$$

where $\psi(t,z,u)$ and $\omega(t,z,u)$ are bounded unknown functions, and $\upsilon(t) = \dot{u}(t)$. Suppose that $\omega(t,z,u) \neq 0$, i.e., the system (3) has a relative degree one with the sliding variable $\sigma(t,z)$, and that there exist positive constants Ω_m, Ω_M and Ψ, such that

$$\Omega_m < \omega(t,z,u) < \Omega_M, \tag{7}$$

$$-\Psi < \psi(t,z,u) < \Psi. \tag{8}$$

Then from the (7) and (8), one can obtain that the differential inclusion,

$$\ddot{\sigma}(t,x) \in [-\Psi, \Psi] + [\Omega_m, \Omega_M]u(t). \tag{9}$$

The problem of SOSM can be equivalent to, by using a discontinuous control $\upsilon(t)$ on $\ddot{\sigma}(t,z)$, guarantee that the system (6) converge to zero in finite time. There are a lot of algorithms proposed to solve this problem. In this paper, supertwisting algorithm (STA) will be applied to the buck converter. The STA can be designed as follow [19],

$$u(t) = -\mu\left|\sigma(t,z)\right|^{\frac{1}{2}}\operatorname{sign}(\sigma(t,z)) + \int_{t_0}^{t}\upsilon(s)ds \tag{10}$$

$$\upsilon(t) = -\alpha\operatorname{sign}(\sigma(t,z)), \tag{11}$$

where μ and α are the positive constants designed to guarantee that the $\sigma(t,z)$ and $\dot{\sigma}(t,z)$ converge to zero in a finite time. According to [19], the sufficient conditions for finite time ensured that $\sigma(t,z) = \dot{\sigma}(t,z) = 0$ are:

$$\alpha > \frac{\Psi}{\Omega_m}, \mu^2 \geq \frac{4\Psi}{\Omega_m^2}\frac{\Omega_M}{\Omega_m}\frac{\alpha+\Psi}{\alpha-\Psi}. \tag{12}$$

C. Control objectives

The aims of this paper are stated as follows:

- The inductor current i_L should track the reference signal i_L^* calculated in such a way that output DC voltage is driven to a desired value, i.e., $i_L \to i_L^*$.
- The output DC voltage v_{out} should be regulated to a constant reference v_{ref}, i.e., $v_{out} \to v_{ref}$.

III. CONTROL STRATEGIES

In this section, we propose a new control strategy, disturbance observer based second order sliding mode control, for the buck converter based on the cascade control structure, which comprises external loop, voltage regulation loop, and internal loop, current tracking loop. For the external loop, an STA controller plus an extended state observer (ESO) regulate the output voltage to a constant reference, in which the ESO aims at asymptotically rejecting disturbances, load current, to

improve the system performance. For the internal loop, an STA controller is employed to force the inductor current i_L towards its desired value i_L^*, a slowly varying signal generated by the external loop. A schematic block diagram of the control strategies is shown in Fig. 2.

III.A Voltage regulation loop

The voltage regulation loop is the outer loop, and its objective is to regulate the output voltage to a certain desired value. Assuming that the dynamic of inductor current is faster than output voltage dynamic and stable, then its dynamic can be rewritten as,

$$C\frac{dv_{out}}{dt} = i_L^* - i_{load}, \tag{13}$$

where load current $i_{load} = \frac{v_{out}}{R_L}$ considered as an unknown external disturbance in this paper, which is directly affect system performance. Thus, an ESO will be designed to estimate the disturbance aiming at asymptotically decreasing its impact. A linear ESO is presented as follow,

$$C\dot{\hat{v}}_{out} = i_L^* - \hat{i}_{load} + \eta_1 \left(v_{out} - \hat{v}_{out}\right), \tag{14}$$

$$\dot{\hat{i}}_{load} = -\eta_2 \left(v_{out} - \hat{v}_{out}\right), \tag{15}$$

where $\hat{v}_{out}$ and $\hat{i}_{load}$ are the estimation of v_{out} and i_{load}, respectively, and η_1 and η_2 are positive parameters to be designed. Next, we will design the parameters η_1 and η_2 such that the $\hat{i}_{load}$ can asymptotically estimate the i_{load}. Defining the estimation error $\tilde{v}_{out} = v_{out} - \hat{v}_{out}$ and $\tilde{i}_{load} = i_{load} - \hat{i}_{load}$, its dynamics are written as,

$$C\dot{\tilde{v}}_{out} = -\eta_1 \tilde{v}_{out} - \tilde{i}_{load}, \tag{16}$$

$$\dot{\tilde{i}}_{load} = -\eta_2 \tilde{v}_{out} + \dot{i}_{load}. \tag{17}$$

Furthermore, the system (16) and (17), is rewritten as,

$$\dot{\varepsilon}(t) = A\varepsilon(t) + \zeta(t), \tag{18}$$

where $\varepsilon(t) = \begin{bmatrix} \tilde{v}_{out} \\ \tilde{i}_{load} \end{bmatrix}$, $A = \begin{bmatrix} -\frac{\eta_1}{C} & -\frac{1}{C} \\ \frac{\eta_2}{C} & 0 \end{bmatrix}$ and $\phi(t) = \begin{bmatrix} 0 \\ \dot{i}_{load} \end{bmatrix}$. One can select the appropriate parameters η_1 and η_2 to guarantee that matrix A is Hurwitz matrix. Assume that the variation rate of load current $\dot{i}_{load}$ is bound. The solution of (18) is given by,

$$\varepsilon(t) = e^{A(t-t_0)}\varepsilon(t_0) + \int_{t_0}^{t} e^{A(t-t_0)}\zeta(\tau)d\tau, \tag{19}$$

where t_0 is the initial time. It is well known from the result in [20] that $\left\|e^{A(t-t_0)}\right\| \le ce^{\frac{\lambda_{\max}(A)}{2}(t-t_0)}$, where c is a positive constant. One can get that,

$$\begin{aligned} \|\varepsilon(t)\| &= ce^{\frac{\lambda_{\max}(A)}{2}(t-t_0)} \|\varepsilon(t_0)\| + \int_{t_0}^{t} e^{\frac{\lambda_{\max}(A)}{2}(t-t_0)} \\ &\quad \times \|\zeta(\tau)\| d\tau, \\ &\le ce^{\frac{\lambda_{\max}(A)}{2}(t-t_0)} \|\varepsilon(t_0)\| - \frac{2c}{\lambda_{\max}(A)} \sup_{t_0 \le \tau \le t} \|\zeta(\tau)\|. \end{aligned} \tag{20}$$

Thus, it can be concluded that the trajectories of the system (18) are bound in a finite time T_0, i.e., $\|\varepsilon(t)\| \le \epsilon,\ \forall t \ge T_0 > 0$, in which ϵ is a positive constant.

Next, denoting the voltage regulation error $e_v = v_{ref} - v_{out}$, we have

$$C\dot{e}_v(t) = -i_L^* + i_{load}. \tag{21}$$

Based on the estimation of load current $\hat{i}_{load}$ and STA, it yields

$$i_L^* = u_v(e_v) + \hat{i}_{load}, \tag{22}$$

where $u_v(e_v) = \mu_v |\sigma(e_v)|^{\frac{1}{2}} \operatorname{sign}(e_v) + \alpha_v \int_{t_0}^{t} \operatorname{sign}(e_v)ds$, with positive constants μ_v and α_v. Substituting from (22) in (21) gets,

$$C\dot{e}_v(t) = -u_v(e_v) + \tilde{i}_{load}. \tag{23}$$

From the (12) and (20), one can obtain that regulation error e_v converges to 0 if the parameters μ_v and α_v are chosen such that

$$\alpha_v > CH_v, \mu_v^2 \ge 4C^2 H_v \frac{\alpha_v + H_v}{\alpha_v - H_v}, \tag{24}$$

in which H_v is positive constant satisfying $\left\|\dot{\tilde{i}}_{load}\right\| \le H_v$. Fig. 3 shows the structure of voltage regulation loop.

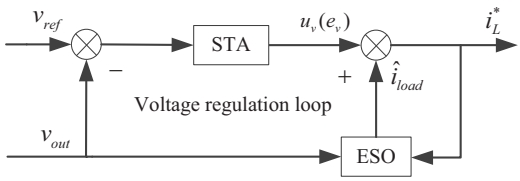

Fig. 3. Voltage regulation loop

III.B Current tracking loop

The STA controller is applied to the current tracking loop which ensure convergence of inductor current i_L to its reference i_L^* calculated from the external loop to regulate output voltage. Define the current tracking error $e_i = i_L^* - i_L$, and from (1) it can be obtained,

$$\dot{e}_i = \dot{i}_L^* + \frac{r}{L}i_L + \frac{v_{out}}{L} - \frac{v_{in}}{L}u. \tag{25}$$

An STA controller is designed to guarantee that current tracking error converges to zero,

$$u = \frac{L}{v_{in}}(u_i(e_i) + \frac{v_{out}}{L} + \frac{r}{L}i_L), \tag{26}$$

where $u_i(e_i) = \mu_i |\sigma(e_i)|^{\frac{1}{2}} \operatorname{sign}(e_i) + \alpha_i \int_{t_0}^{t} \operatorname{sign}(e_i)ds$. Substituting (26) in (25), the following equation is deduced,

$$\dot{e}_i = -u_i(e_i) + \dot{i}_L^*. \tag{27}$$

From the (12) and (27), one can obtain that regulation error e_i converges to 0 if the parameters μ_i and α_i are chosen such that

$$\alpha_i > H_v, \mu_i^2 \ge 4H_i \frac{\alpha_i + H_i}{\alpha_i - H_i}, \tag{28}$$

in which H_i is positive constant satisfying $\left\|\ddot{i}_L^*\right\| \le H_i$. Fig. 4 shows the structure of current tracking loop.

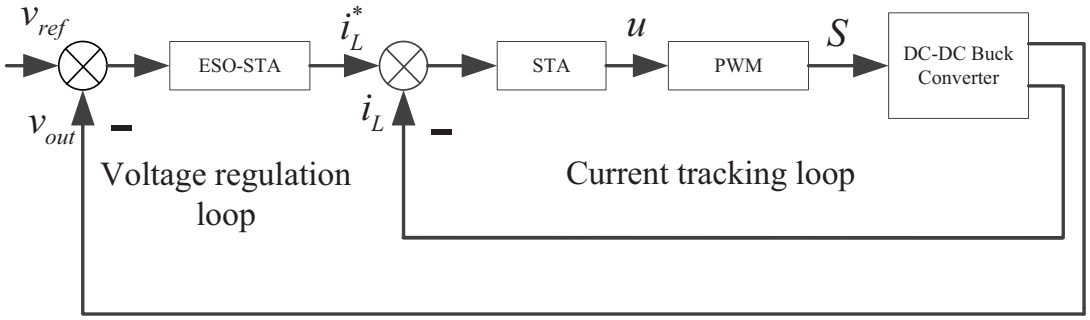

Fig. 2. Proposed cascade control structure

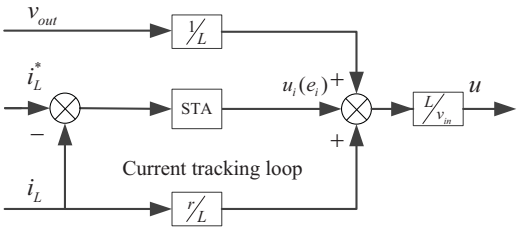

Fig. 4. Current tracking loop

TABLE I
PROPOSED SYSTEM PARAMETERS

Parameter	Value	Description
f	$2{\cdot}10^3$	Switching Rate (Hz)
R_L	$40 \rightarrow 20$	Load Resistance (Ω)
C	4700	Output Capacitor (μF)
L	2	Filter Inductor (mH)
r	0.01	Parasitic resistance (Ω)
v_{in}	$300 \rightarrow 250$	Input Voltage (V)
v_{ref}	$200 \rightarrow 150$	Output Voltage Reference (V)

IV. SIMULATION RESULTS

Two simulation results (PI and the proposed SOSM approach), made by Matlab/Simulink, are shown in this section to validate the effectiveness of the proposed strategy for DC-DC buck converters. The parameters and variables of the simulated system are presented in Table I.

In order to compare the robustness between the PI control and the proposed SOSM approach three simulations have been carried out, including controller against load resistance variation, input voltage variation and reference voltage variation.

TABLE II
SOSM CONTROLLER DESIGN PARAMETERS

Controller	Variable	Value
Internal loop	$(\mu_i,\ \alpha_i)$	$(1.5,\ 10)$
External loop	$(\mu_v,\ \alpha_v)$	$(1{\cdot}10^3,\ 2{\cdot}10^2)$
	(η_1, η_2)	$(39.6,\ 1.65 \cdot 10^3)$

TABLE III
PI CONTROLLER DESIGN PARAMETERS

Controller	Variable	Value
Internal loop	$(K_{ip},\ K_{ii})$	$(2.0{\cdot}10^5,\ 1.0{\cdot}10^6)$
External loop	$(K_{vp},\ K_{vi})$	$(0.8,\ 7)$

A. Against load resistance variation

In this simulation, a load resistance steps at output link (from 40Ω to 20Ω). The parameters of the PI and the proposed SOSM controllers have been shown in Table II and III, respectively. Fig. 5 shows the dynamic of output voltage of the buck converter when the load varies. It can be seen that both strategies can achieve the output voltage regulation. The dynamical characters of the buck converter are excellent and dynamic excess, adjusting time and the ripple of output voltage satisfy all the requirements. However, the dynamic performance of the proposed scheme is better than traditional PI control, especially the transient voltage drop and recovery time. Specifically, for our proposed control scheme, the voltage drop is only 0.05 V, and recover time needs 80 ms after load steps at $t = 0.5$ s, while for PI control, the voltage drop is 5 V, and recover time needs 500 ms after the load is stepped at $t = 0.5$ s. This means that the proposed SOSM controller has a better robustness against load resistance variation.

Fig. 6 presents the trajectories of inductor current along with its reference in the presence of load variation. It is easily remarked that both control law can achieve the inductor current to track its reference signal coming from the external loop. Yet the faster dynamics are achieved with the proposed controller than the PI controller. The dynamic responses of load current and its corresponding estimation are pictured in the Fig. 7, where the ESO can remarkably estimate the load current.

B. Against input voltage variation

In this simulation, the input voltage varies from 300 V to 250 V at 0.5 s. The parameters of the PI and the proposed SOSM controllers are the same as the first simulation. Figs. 8 and 9 show the transient responses of output voltage and inductor current of the buck converter when input voltage varies, respectively. One can see that both strategies can accomplish the voltage regulation and current tracking, and other performance indicators such as dynamic excess, adjusting time and the ripple of output voltage are all in an acceptable range. However, note that the performance of the proposed SOSM controller is obviously better than the PI control, and the input

voltage variation hardly cause damage to the proposed SOSM method.

C. Against reference voltage variation

In this simulation, the reference voltage changes at 0.5 s from 200 V to 150 V. The parameters of the PI and the proposed SOSM controllers are the same as the first simulation. Fig. 10 shows the output voltage of the buck converter when the the reference voltage changes. It can be seen that both strategies can achieve the output voltage regulation, while the the proposed scheme has less dynamics excess and a quicker dynamic response. Specifically, for our proposed control scheme, the voltage drop is only 1 V, and recover time needs 10 ms after the reference voltage steps at $t = 0.5$ s, while for PI control, the voltage drop is 3.5 V, and recover time needs 300 ms. This means that the proposed SOSM controller can quickly regulate the voltage with low overshot. Form the Fig. 11, it can be seen that both control laws can fulfill current tracking, but the PI control has a quicker dynamic response.

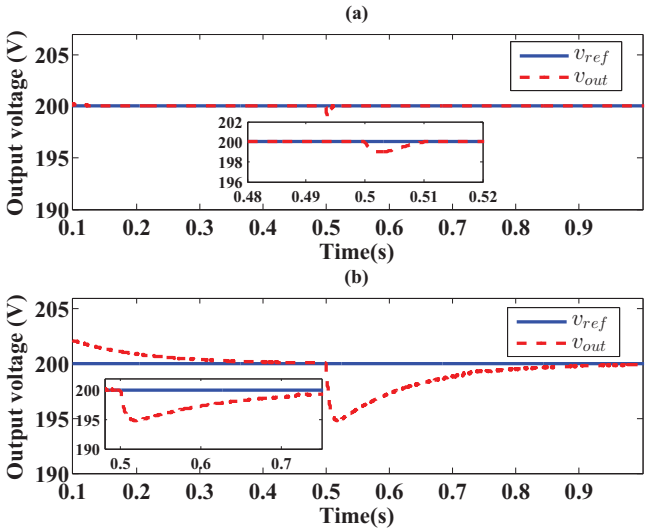

Fig. 5. output voltage (a) SOSM control, (b) PI control.

V. Conclusion

A cascade control strategy for DC-DC buck converters, based on the second order sliding mode control added to extended state observer, has been put forward in this paper. First, the average model of DC-DC buck converter is established. Based on this model, a cascade control scheme containing two control loops, output voltage regulation loop and current tracking loop, is designed to complete the output voltage regulation and inductor current tracking. Three simulations, accomplished under Matlab/Simulink environment, including controller against load resistance variation, input voltage variation and reference voltage variation are provided to show the advantages of the proposed strategy compared with PI control.

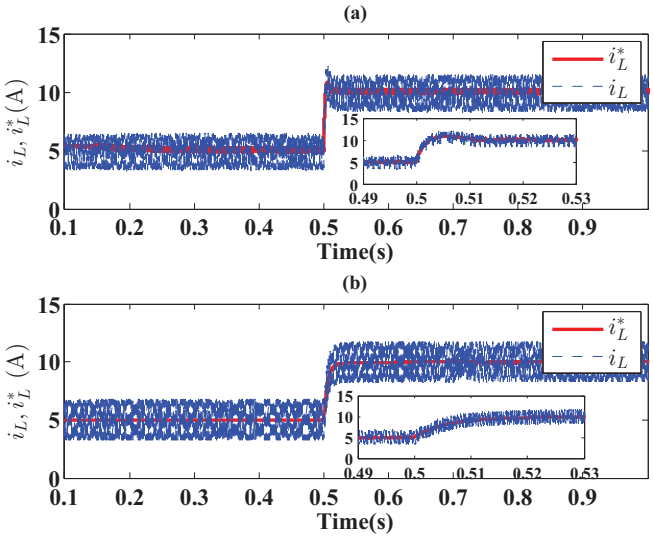

Fig. 6. Curves of i_L and i_L^* (a) SOSM control, (b) PI control.

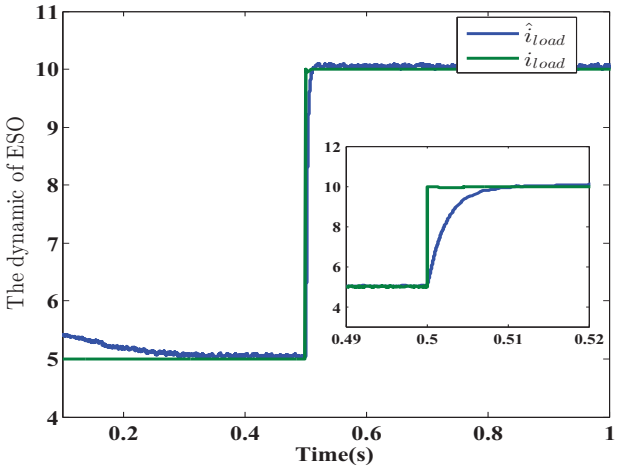

Fig. 7. The dynamic of ESO

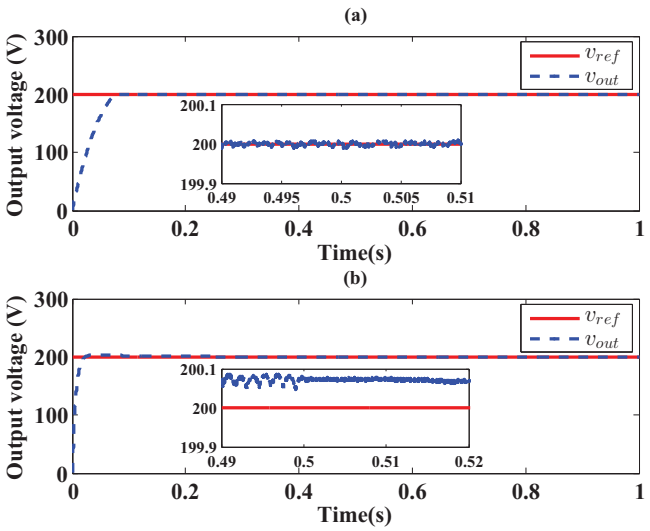

Fig. 8. output voltage (a) SOSM control, (b) PI control.

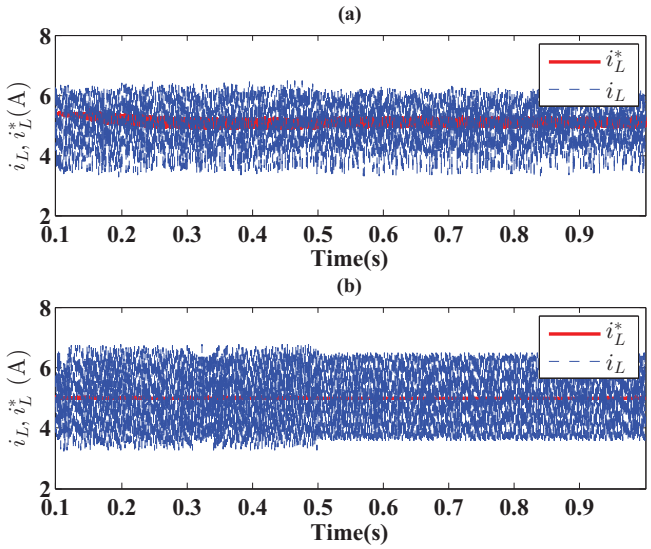

Fig. 9. Curves of i_L and i_L^* (a) SOSM control, (b) PI control.

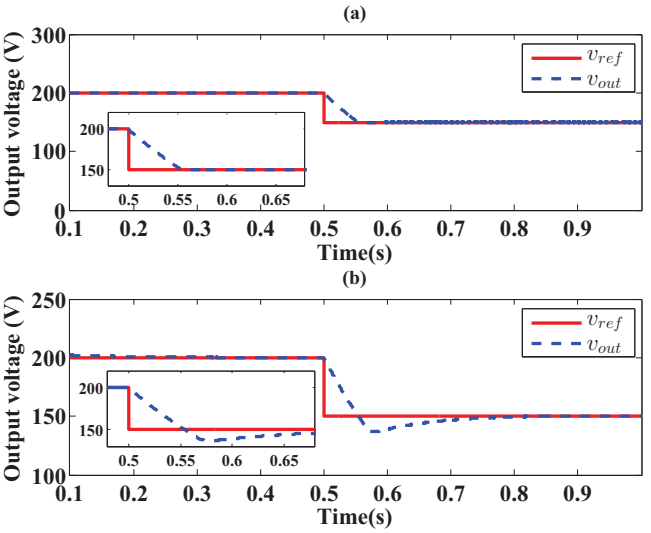

Fig. 10. output voltage (a) SOSM control, (b) PI control.

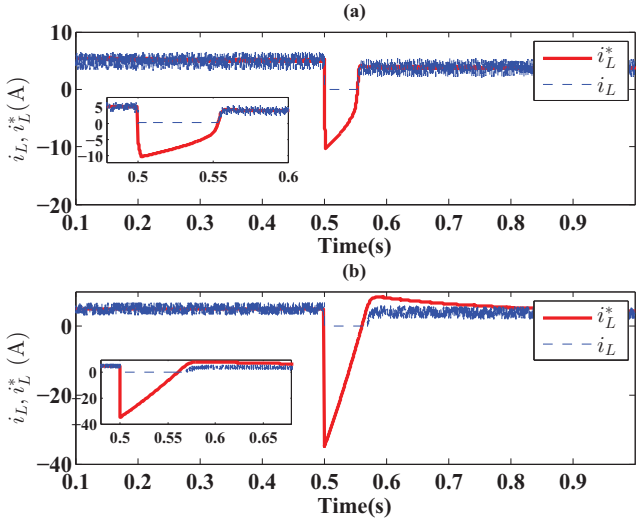

Fig. 11. Curves of i_L and i_L^* (a) SOSM control, (b) PI control.

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