MGC UART Datasheet

Version 1.0
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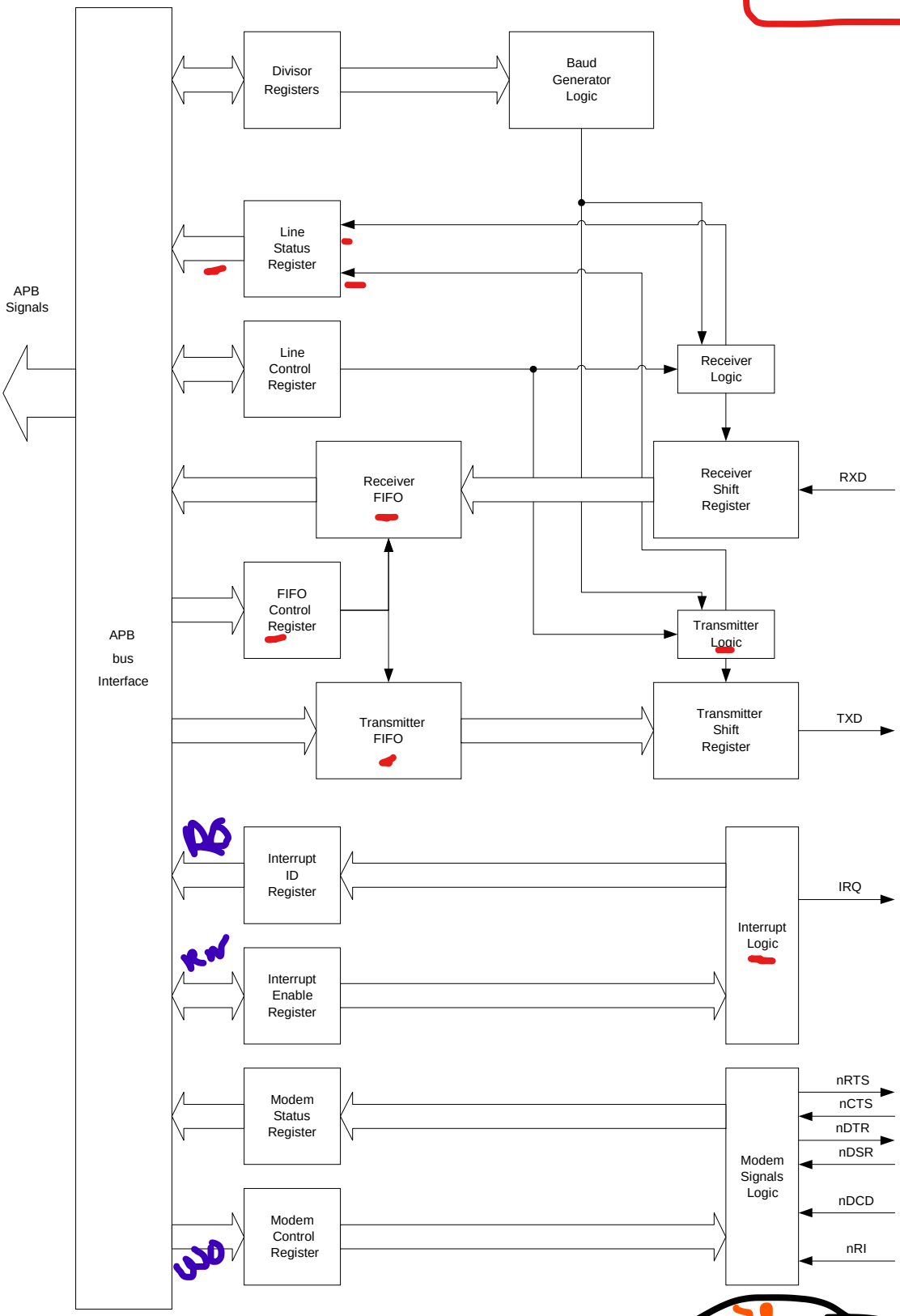
Introduction

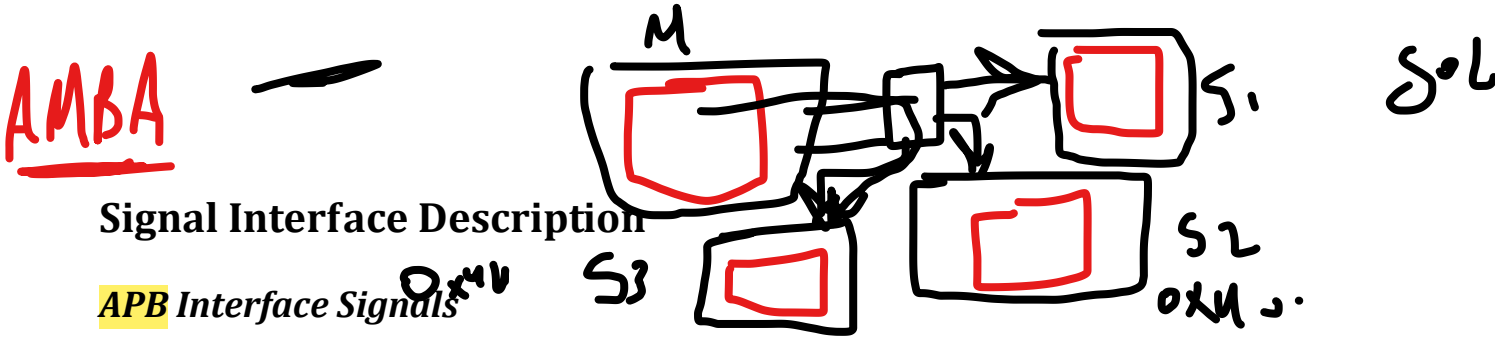
The Mentor Graphics UART is a soft design IP core. It has been designed to be generally compatible with the industry standard 16550A UART, but there are a small number of differences.

Disclaimer

The UART design RTL is supplied on an ‘as is’ basis and is intended to be used with Verification Academy Verification Cookbook verification environments to illustrate different aspects of verification methodology.

Functional Block Diagram





Signal Interface Description

APB Interface Signals

Signal	Width	Direction	Description
PCLK	1	Input	APB bus clock
PRESETn	1	Input	Asynchronous reset
PADDR	32	Input	Address field
PSEL	1	Input	APB peripheral select
PWRITE	1	Input	Write enable
PENABLE	1	Input	Peripheral enable
PWDATA	32	Input	Write data field
PRDATA	32	Output	Read data field
PREADY	1	Output	Peripheral ready
PSLVERR	1	Output	Peripheral slave error

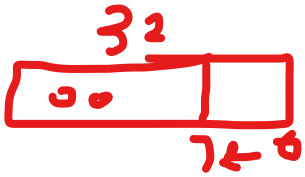
UART Function Signals

Signal	Width	Direction	Description
TXD	1	Output	Serial transmit data output
RXD	1	Input	Serial receive data input
nCTS	1	Input	Not Clear To Send
nDSR	1	Input	Not Data Set Ready
nDCD	1	Input	Not Data Carrier Detect
nRI	1	Input	Not Ring Input
nRTS	1	Output	Not Ready To Send
nDTR	1	Output	Not Data Terminal Ready
nOUT1	1	Output	General purpose output signal 1
nOUT2	1	Output	General purpose output signal 2

Miscellaneous Signals

Signal	Width	Direction	Description
baud_o	1	Output	Baud rate divider output
IRQ	1	Output	Interrupt output

Register Description



Register Summary

The original 16550 8-bit register bit fields are preserved but are mapped into 32 bit slots. The unused, 24 most significant, bits are read back as zeros.

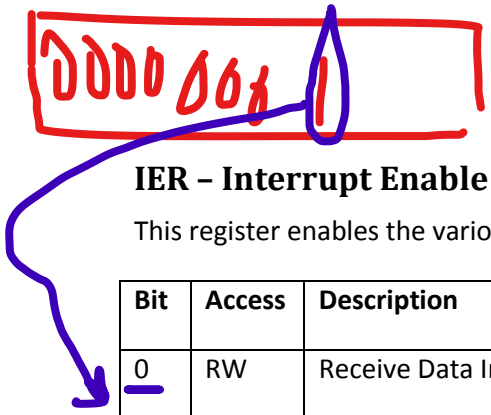
Register	Offset	Width	Access	Description
RXD	0x0	8	RO	Receive FIFO output register
TXD	0x0	8	WO	Transmit FIFO input register
IER	0x4	8	R/W	Interrupt Enable Register
IIR	0x8	8	RO	Interrupt Identification Register
FCR	0x8	8	WO	FIFO Control Register
LCR	0xc	8	R/W	Line Control Register
MCR	0x10	8	R/W	Modem Control Register
LSR	0x14	8	RO	Line Status Register
MSR	0x18	8	RO	Modem Status Register
DIV1	0x1c	8	R/W	16 bit Baud Rate divider – least significant byte
DIV2	0x20	8	R/W	16 bit Baud Rate divider – most significant byte

Detailed Register Descriptions

TXD, RXD - Data buffer registers

Register	Bits	Access	Description
TXD	7:0	WO	Write to the bottom of the Transmit FIFO
RXD	7:0	RO	Read from the top of the Receive FIFO

Reset Value: Undefined



IER – Interrupt Enable Register

This register enables the various interrupts available in the UART.

Bit	Access	Description
0	RW	Receive Data Interrupt enable
1	RW	Transmit Holding Register empty interrupt enable
2	RW	Receive Line Status interrupt enable
3	RW	Modem Status interrupt enable
7:4	RW	Reserved, will always read back as ‘0’

Reset Value: 0x0

Writing a logic ‘1’ to any of these interrupt enable bits will enable the interrupt, and writing a logic ‘0’ will disable the interrupt. After reset all interrupts are disabled.

IIR – Interrupt Identification Register

This read only register is used to identify whether an interrupt is pending, and if so which interrupt.

Bit 0 of the register will read back as a logic '1' if no interrupt is pending, otherwise the UART has an interrupt to be serviced. The valid codes returned in bits 3:0 of the register are described in the following table:

Code	Priority	Interrupt Type	Interrupt Source	Interrupt Reset Control
0x1	-	No interrupt	-	-
0x6	1st	Receive Line Status	Parity, Overrun or Framing errors, or Break Detected	Reading the line status register
0x4	2nd	Receive data available	RX FIFO trigger level reached	RX FIFO drops below the trigger level
0xc	2nd	Receive timeout	At least a character in the RX FIFO, but no character has been received by or read from the RX FIFO for at least 4 character periods	Reading from the receive data register
0x2	3rd	Transmitter Empty	The transmit FIFO and the transmit shift register is empty	Reading the IIR register or writing to the transmit data register
0x0	4th	Modem Status	A change on one of the modem input signals: CTS, DSR, RI or DCD	Reading the modem status register

Bits 7:4 are unused and are always read back as 0xC

Reset Value: 0xC1

FCR – FIFO Control Register

The FIFO Control Register is a write-only register that allows the TX and RX FIFOs to be flushed. It also sets the level of the RX FIFO threshold.

Bit	Access	Description
0	W	Reserved
1	W	If set to logic '1', flushes the content of the RX FIFO, but does not affect the reception of any character that is in progress when the RX FIFO is flushed.
2	W	If set to logic '1', flushes the content of the TX FIFO, but does not affect any in progress transmission.
5:3	W	Reserved
7:6	W	Sets the RX FIFO interrupt threshold: '00' – 1 Character '01' – 4 Characters '10' – 8 Characters '11' – 14 Characters

Reset value: 0xc0

LCR – Line Control Register

The LCR controls the format of the serial characters transmitted and received by the UART.

Bit	Access	Description
1:0	RW	Defines the number of bits per character: ‘00’ – 5 bits ‘01’ – 6 bits ‘10’ – 7 bits ‘11’ – 8 bits
2	RW	Selects the number of stop bits transmitted: ‘0’ – 1 Stop bit ‘1’ – 2 Stop bits for 8,7,6 bit characters, 1.5 stop bits for 5 bit characters **Note:** The receive path only checks for 1 stop bit
3	RW	Parity Enable: ‘0’ – No parity ‘1’ – Parity enabled
4	RW	Even Parity Select: ‘0’ – Odd parity (Parity is set to ensure an odd number of 1’s in the overall character) ‘1’ – Even parity (Parity bit makes an even number of 1’s in the overall character)
5	RW	Stick Parity Select: ‘0’ – Stick parity disabled ‘1’ – The inverse of bit 4 is transmitted as the parity bit
6	RW	Break Control bit ‘0’ – Break disabled ‘1’ – The TX serial data line is forced to logic ‘0’ to indicate a break condition
7	RW	Reserved

Reset Value: 0x3

MCR – Modem Control Register

The MCR register provides the software interface to the modem control lines, it also allows the UART loopback mode to be enabled.

Bit	Access	Description
0	RW	Data Terminal Ready (DTR), the output value is the inverse of the bit value written
1	RW	Request To Send (RTS), the output value is the inverse of the bit value written
2	RW	Out1 – In loopback mode, connected to the Ring Indicator (RI) signal input
3	RW	Out2 – In loopback mode, connected to Data Carrier Detect (DCD) signal input
4	RW	Loopback mode: '0' – Normal mode '1' – Loopback mode enabled In loopback mode, the following loopback internal connections are made: TXD => RXD DTR => DSR RTS => CTS Out1 => RI Out2 => DCD
7:5	RW	Reserved

Reset Value: 0x0

LSR – Line Status Register

The LSR provides status information from the UART receive and transmit channels.

Bit	Access	Description
0	RO	Data Ready (DR) '0' – No characters in the RX FIFO '1' – At least one character in the RX FIFO
1	RO	Overrun Error (OE) The Overrun Error bit is set if a new character is received when the RX FIFO is full. The OE bit is cleared on reading the LSR
2	RO	Parity Error (PE) '1' – The character at the top of the RX FIFO was received with a parity error '0' – No parity error for the character at the top of the RX FIFO The PE bit is cleared on reading the LSR
3	RO	Framing Error (FE) '1' – The character at the top of RX FIFO was received with a framing error '0' – No framing error for the character at the top of the RX FIFO The FE is cleared on reading the LSR
4	RO	Break Interrupt (BI) A break interrupt is detected when the RXD serial input remains at logic '0' for at least one character period, one zero character is loaded into the RX FIFO and a break interrupt is flagged. The BI is cleared on reading the LSR
5	RO	Transmit FIFO empty '1' – The TX FIFO is empty – generates TX empty interrupt '0' – TX FIFO has at least one character in it The bit is cleared when a character is written to the TX FIFO
6	RO	Transmit Empty '1' – Both the transmit shift register and the TX FIFO are empty '0' – TX FIFO has at least one character, or the TX shift register is busy The bit is cleared when a character is written to the TX FIFO
7	RO	FIFO Error '1' – At least one parity error, framing error or break interrupt has been received and are stored in the RX FIFO. The bit is reset on reading the LCR. '0' – No errors

Reset Value: 0x60

MSR – Modem Status Register

The MSR provides status information on the modem input lines, it changes functionality in loopback mode.

Bit	Access	Description
0	RO	Delta Clear To Send (DCTS), set to '1' if the CTS input has changed
1	RO	Delta Data Set Ready (DDSR), set to '1' if the DSR input has changed
2	RO	Trailing Edge of Ring Indicator (TERI), set to '1' on a 1 to 0 transition of the RI input
3	RO	Delta Data Carrier Detect (DDCD), set to '1' if the DCD input has changed
4	RO	Inverse of the CTS input, or RTS in loopback mode
5	RO	Inverse of the DSR input, or DTR in loopback mode
6	RO	Inverse of the RI input, or Out1 in loopback mode
7	RO	Inverse of the DCD input, or Out2 in loopback mode

Reset Value: 0x0

DIV1 – DIVISOR LSB

The UART baud rate divider is implemented as a 16 bit counter which divides down the APB bus clock to arrive at a clock frequency which is 16x the serial data rate. The counter value is loaded via two 8 bit registers, DIV1 and DIV2.

Reading back from these registers will return the baud rate divider, not the current value of the divider counter.

The counter is started, or restarted, when the DIV1 register is written to.

Bit	Access	Description
7:0	RW	Least significant byte of the 16 bit baud rate divisor

Reset value: 0x0

DIV2 – DIVISOR MSB

Bit	Access	Description
7:0	RW	Most significant byte of the 16 bit baud rate divisor

Reset value: 0x0