Dr. Abhishek Kumar
Associate Professor
School of Electronics and Electrical Engineering
Lovely Professional University
abkvjti@gmail.com
9888431215
SCOPUS ID- 6152297700

Area of Research Interest

VLSI Design, Low Power CMOS VLSI Circuit, Hardware Security, Machine Learning, FPGA based System Design

Education

- PhD(Electronics and Electrical Engineering) from Lovely Professional University, CGPA 8.57, 2020
- M.Tech (Electronics Engineering), from VJTI, University of Mumbai, CPI 8.1, 2010
- B.E.(Equivalent)(Electronics and Communication Engineering)from Institution of Engineering(India),CGPA 7.05,2007

Employment Record

- Associate Professor: Lovely Professional University, from August 2020 – onwards
- Assistant Professor, Lovely Professions University, December 2010 –July 2020
- Teaching Assistant, VJTI, University of Mumbai, June 2009 – June 2010

Certification / Accomplishment

- UGC NET (Electronics Science) July 2018
- GATE(EC)-2015, GATE Score-468
- GATE (EC)-2008, percentile 89.35

Software and Programming Skill

- Software Skill- Cadence Tool, Xilinx ISE, Vivado, Modelsim, Microwind, DSCH, Kielμvision, Arduino, Proteus
- Programming Language: VHDL, Verilog, Assembly, Tcl/Tk, Python

Book Publication

[1] S.L.Tripathi, Souvik Ganguli, Abhishek Kumar, Tengiz Magradze , "*Intelligent Green Technologies for Sustainable Smart Cities*" Wiley-Scrivener, In Press
[2] S. L, Tripathi, Abhishek Kumar, Jyotirmaoy Pathak, "*Programming and GUI Fundamentals: TCL–TK for Electronic Design Automation (EDA)*" Wiley-Blackwell, In Press
[3] Abhishek Kumar, S.L. Tripathi, K. Srinivasa Rao, "*Machine Learning Technique for VLSI Chip Design*" Wiley-Scrivener, In Press

Copyright

[1] Logic Gate with Fun using GUI, *Copyright Reg. No. SW-13535/2020,* Copyright Office India
[2] Power Calculation Method of CMOS Circuit, *Copyright Reg No. L-89581/2020*, Copyright Office India
[3] VLSI Lab Manual, *Copyright Reg No L-74179/2018,* Copyright Office India
[4] Laboratory manual ECE 216, *Copyright Reg No L-85680/2019*, Copyright Office India

Patents

[1] Abhishek Kumar, J Pathak, S L Tripathi, "*A system to generate key for hardware authentication*" Application No.201911049739A), ***Reply to FER submitted***, Indian Patent Office on 2nd December 2019
[2] J Pathak, S L Tripathi, Abhishek Kumar, "*A novel obfuscated processor architecture for hardware security and optimization*" (Application No.201911049369A", ***Reply to FER submitted***, Indian Patent Office on 2nd December 2019
[3] Abhishek Kumar, S L Tripathi, "*Power attack resistant masked logic gate*" (Application No.201911053046A), Provisional Patent filed with Indian Patent Office on 20th December 2019
[4] R Sarma, C Bhargava, Abhishek Kumar, J Pathak, P Sharma, A Sachdeva, S Khan "*A rotatable motorbike seat*" (Application No. 201911049793A), Provisional Patent Filed with Indian Patent Office on 3rd December 2019
[5] R Sarma, C Bhargava, Abhishek Kumar, J Pathak, P Sharma, A Sachdeva, S Khan, "*A device to regroove the slipper sole*" (Application No. 201911049976 A), Provisional Patent filed with Indian Patent Office on 4th December 2019
[6] R Sarma, C Bhargava, Abhishek Kumar, J Pathak, P Sharma, A Sachdeva, "*An arm-chair with detachable l-shaped writing desk*" (Application No 201911050035A), Provisional Patent Filed with Indian Patent Office on 4th December 2019

[7] R Sarma, C Bhargava, Abhishek Kumar, J Pathak, P Sharma, A Sachdeva, "*A novel motor vehicle window pane closure detector*" (Application No 201911049749A), Provisional Patent filed with Indian Patent Office on 3rd December 2019

Journal Publication

[1] Abhishek Kumar, NanoSecond Latency Drum Kit**,** *Science, Engineering and Health Studies*, 2021, *Accepted for Publication*, (**Scopus**)

[2] Abhishek Kumar, Degradation of MOS Parameter Due to Bias Instability. *International Journal of Computing and Digital System*, 2021, *Accepted for Publication*, (**Scopus**)

[3] Suman Lata Tripathi, Pooja Pathak, Abhishek Kumar & Sobhit Saxena, "Improved Drain Current with Suppressed Short Channel Effect of p+Pocket Double-Gate MOSFET in Sub-14 nm Technology Node" 2022, https://doi.org/10.1007/s12633-022-01816-2 **(SCIE-IF 2.67)**

[4] Abhishek Kumar, Tripathi S.L, Subramaniam, U, Variability analysis of SBOX with CMOS 45nm technology, *Wireless Personal Communication*, 2021, https://doi.org/10.1007/s11277-021-09377-0 **(SCI-IF 1.671)**

[5] Abhishek Kumar, Srivastava, S., Saxena, S., & Tripathi, S. L., $(Ba/Pb)_xSr_{(1-x)}TiO_3$ based capacitive sensor with $LaNiO_3$ electrode for higher tunability, *Journal of Materials Science: Materials in Electronics*, Vol 31(22), 2020,20387-20399. (**SCI- IF 2.478**)

[6] Abhishek Kumar & Tripathi, S. L., SBOX under PVT variation, *Analog Integrated Circuits and Signal Processing*, Vol 105(1),2020, 73-82 (**SCI-IF 1.337**)

[7] Abhishek Kumar, Tripathi, S. L., & Mishra, R. S., METAPUF: A challenge response pair generator, Periodicals of Engineering and Natural Sciences, Vol 6(2), 2018, 58-63 (**Scopus**)

[8] Abhishek Kumar & Tiwari, K., Wide Tuning Range CMOS VCO, *International Journal of Engineering and Manufacturing*, Vol *7*(5), 2017, 31-38.

[9] Abhishek Kumar, Mishra, R. S.,& Kashwan, K. R, PUF Based challenge Response Pair for Secured Authentication, *International Journal of Control Theory and Applications*, Vol 9(41), 2017, 115-12(**Scopus**)

[10] Tiwari, S. & Abhishek Kumar, 2, 4 Bit Flash ADC using TIQ Comparator, *International Journal of Control Theory and Applications*, Vol 9(11), 2016, 5235-5242. (**Scopus**)

[11] Dayal, M., & Abhishek Kumar, S-Parameter Comparison of Common Source and Common Gate Low Noise Amplifier, *International Journal of Computer Applications*, Vol *120*(19), 2015, 15-18.

[12] Abhishek Kumar, Ultralow power sub-threshold ring oscillator, International *Journal of Applied Engineering Research*, Vol *10*(6), 2015, 14991-14998. (**Scopus**)

[13] Abhishek Kumar, Effect of Body Biasing Over CMOS Inverter, *International Journal of Electronics & Communication Technology*, Vol 4(1-3), 2013, 369-371.

[14] Abhishek Kumar, Memristor: The 4th Circuit Element, *International Journal of Advanced Computer and Mathematical Sciences*, Vol 3(1), 2012, 176-180.

[15] Abhishek Kumar, Leakage current controlling mechanism Using High K Dielectric + Metal Gate, *International Journal of IT & Knowledge Management*, Vol 5(1), 2012, 191-194.

[16] Abhishek Kumar & Wankhede, Y, Need of A Nano-Transistor, *International Journal of Electronics and Electrical Engineering*, Vol 4(3), 2011, 329-335.

[17] Abhishek Kumar ,Wankhede, Y. E., Shinde, P. K.,& Sarwade, N, Design of SDRAM memory controller using VHDL, *International Journal of Computer Science and Application*, Vol 1, 2010, 184-189

Conference Proceedings

[1] Vemula Krishna Chaitanya, Mamidi Sri Harsha, Lanka Maneesh Kumar, Vankadari Rahul, Palem Goutham Kumar Reddy, Abhishek Kumar, Smart Parking Management System, *IOP Conference Series: Earth and Environmental Science*, Jaipur, India, March 18-19, 2021, IOP Publishing

[2] Abhishek Kumar, Tripathi S.L.,& Dhariwal S, Static Timing Analysis of Sequential Circuit with GUI, *6th IEEE International Women in Engineering (WIE) Conference on Electrical and Computer Engineering*(WIECON ECE), Bhuwneshwar, India, December 26, 2020, 312-315, IEEE

[3] Abhishek Kumar & Mishra, R. S, Challenge-Response Pair (CRP) Generator Using Schmitt Trigger Physical Unclonable Function, 11th *International Conference on Advanced Computing and Communication Technologies (ICACCT)*,Panipat, India, February 18, 2018,213-223, Springer

[4] Abhishek Kumar & Tejani, S, S-BOX Architecture, *International Conference on Futuristic Trends in Network and Communication Technologies* (FTNCT), Shimla, India, February 10, 2018,17-27, Springer

[5] Tiwari, S., & Abhishek Kumar, Reconfigurable Flash ADC using TIQ technique, *4th International Conference on Computing Sciences (ICCS)* Phagwara, India, August 31, 2018,204-208. IEEE.

[6] Trivedi, R., Dhariwal, S., & Abhishek Kumar, Comparison of various ATPG techniques to determine Optimal BIST, *International Conference on Intelligent Circuits and Systems* (ICICS), Phagwara, India, April 20, 2018, 93-98, IEEE.

[7] Abhishek Kumar, Mishra, R. S., & Kashwan, K. R, Challenge-response generation using RO-PUF with reduced hardware, *International Conference on Advances in Computing, Communications, and Informatics* (ICACCI), Jaipur, India, September 21, 2016,1305-1308, IEEE.

[8] Naghwal, N. K & Abhishek Kumar, A PN Sequence Generator Using LFSR with Dual Edge Trigger Technique, *MATEC Web of Conferences*, Sangrur, India, May 11, 2016, Vol 57, Article Number 01016, EDP Science.

[9] Tiwari, K.,& Abhishek Kumar, 11GHz CMOS Ring Oscillator, *International Conference on Computing, Communication & Automation* (ICCCA), Noida, India, May 15, 2015, 1280-1283, IEEE.

[10] Sireesha, R., & Abhishek Kumar, Design of low power 0.8 V Flash ADC using TIQ in 90nm technology, *International Conference on Smart Technologies and Management for Computing, Communication, Controls, Energy, and Materials* (ICSTM), Avadi, India, May 6, 2015,406-410, IEEE.

[11] Abhishek Kumar, SRAM Cell Design with Minimum Number of Transistor, *Recent Advances in Engineering and Computational Sciences* (RAECS), Chandigarh, India, March 6, 2014, 1-3, IEEE.

Book Chapter

[1] Abhishek Kumar, CMOS Bootstrap Driver, *Electronic Devices and Circuit Design Challenges and Applications in the Internet of Things*, Apple Academy Press, 2021, 51-68

[2] Abhishek Kumar, VLSI Implementation of Vedic Multiplier, *Design and Deployment of Efficient Energy System*, Wiley Online Library, 2021, 13-28.

[3] Abhishek Kumar, Multiplier for DSP Application in CPS System, *Artificial Intelligence Paradigms for Smart Cyber Physical Systems, IGI Global, 2020,* 229-250.

[4] Abhishek Kumar, Programmable Delay for Nano-devices, Nanotechnology Advances and Real-Life Applications, Taylor & Francis, 2020,295-309.

[5] Abhishek Kumar**,** 40-GHz Inductor less VCO, *AI Techniques for Reliability Prediction for Electronic Components*, IGI Global, 2019, 288-298.

[6] Abhishek Kumar & Tripathi, S. L, Power Analysis to Ensure Secure CMOS Architecture, *Recent Advancement in Electronic Devices, Circuit, and Materials, Nova Science, 2020,*71-86.

[7] Abhishek Kumar & Tripathi, S. L, Current Conveyor Based All-Pass Filter, R*ecent Advancement in Electronic Devices, Circuit, and Materials, Nova Science,2020,*71-86.

[8] Pathak, J., Abhishek Kumar, & Tripathi, S. L, High-Level Transformation Techniques for Designing Reliable and Secure DSP Architectures, *AI Techniques for Reliability Prediction for Electronic Components*, IGI Global, 2019,164-174.

[9] Abhishek Kumar, Pathak, J., & Tripathi, S. L, Frequency-Based RO-PUF, *AI Techniques for Reliability Prediction for Electronic Components, IGI Global, 2019,*252-261

Courses Taught

•Digital VLSI Design •CMOS VLSI Design •Advance Digital System Design •FPGA Prototyping •Digital Electronics •Microprocessor and Microcontroller •Tcl-Tk Scripting •VLSI Design Laboratory with Cadence Tool •IC Technology

PhD Thesis Mentor

Vipin Kumar Sharma, "High Performance and Low Power SRAM using CNTFET Technology" In progress

Workshop/MOOC Attended

[1] AICTE Training and Learning (ATAL) FDP on *Machine Learning Technique in VLSI Design*, 26th –30th July 2021.

[2] Faculty Development Program (FDP) on *Hands-on Project-Based Approach for Biomedical Signal Analysis using MATLAB*, Kakatiya Institute of Technology & Science, 28th Dec 2020- 10th Jan 2021.

[3] AICTE Training and Learning (ATAL) Academy FDP on *Artificial Intelligence*, GSSS Institute of Engineering and Technology for Women, 4th -8th Jan 2021

[4] National Level FDP on *G-Suite & Allied Tools in Education*, Teaching & E-content Development, Sant Gadge Baba Amravati University, 29th June- 4th July 2020.

[5] MOOC course, *AI for Everyone,* Coursera, 8th April 2020

[6] MOOC course, *Getting Started with Go*, Coursera, 1st May 2020

[7] FDP on , *Courseware creation using Moodle for Outcome-based Education*, HRDC Integral University, Lucknow, 8th July 2019 – 5th September 2019

[8] Participation in *Analog, and Digital VLSI Design*, UGC-NRC, SOP, University of Hyderabad, 18th-24th Feb, 2018

[9] MOOC course, *Fundamental of Curriculum in Engineering Education* ,Swayam NITTTR Bhopal, 16th July 2018- 11th Aug 2018

Hands on Training

INUP Hands on Training on 2nd International *Winter School for Graduates on Nanoelectronics*, IIT Bombay, 30th Nov-5th Dec 2009

Professional Enrichment

[1] E-Coach for Entrepreneurship Development Cell, 2020 onwards
[2] Resource person, Workshop on *GUI Development with Tcl/Tk*, 2nd Nov 2020
[3] Resource person, Workshop on *PVT Analysis with Cadence ADE-XL*,14thApril 2018
[4] Resource person, Workshop on *Technology-Driven Circuit Design using Cadence Tool*, 8th April 2017
[5] Editorial Board Member of *Advances in Stem Cell Research*
[6] Reviewer of Peer-Reviewed (SCI, Scopus) Indexed Journal
[7] Program Committee Member and Reviewer for Indexed International Conferences

Personal Information

Permanent Address	S/O Subodh Prasad Singh, Galimpur, Lohchi, Munger, Bihar-811211
Language Known	Hindi, English
Email	abkvjti@gmail.com
Mob	9888431215

Declaration

I hereby declare that all the above information furnished by me in this resume is correct
s **Abhishek Kumar**