YOGESH SHRIVASTAVA

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CAREER OBJECTIVE

As a research-oriented, dedicated, and reliable professional, I would like to impart knowledge to the students in an atmosphere with a scientific temper and expansion of technology as an essential contribution to science and technology.

PERSONAL DETAILS

Fathers Name : N. R. Shrivastava

Mothers Name: Sunita Shrivastava

Date of Birth : 21/06/1986

Address : E4 204 Fortune Kasturi,

Hoshangabad Road, Jatkhedi,

Bhopal, 462026 (M.P.)

EDUCATIONAL QUALIFICATION

Exam Passed	Stream	Board/University/ Institution	Year of Passing	% age marks/ C.G.P.A.
10th	-	M.P. Board	2001	82.8
12th	Physics Chemistry Mathematics	M.P. Board	2003	70.4
B.E.	Electronics and Communication Engineering	R.G.P.V. Bhopal	2007	74.69
M.Tech.	VLSI and Embedded System Design	M.A.N.I.T. Bhopal	2010	8.33 C.G.P.A.
Ph.D.	VLSI design	M.A.N.I.T. Bhopal	Thesis submitted in Dec-2021	-

- Qualified UGC NET Held in June 2012
- Qualified Gate exam held in 2007, 2013, 2014, and 2017.
- Qualified Teachers Eligibility test conducted by RGPV in March 2016

TECHNICAL SKILLS

Software Languages	C, C++.
Hardware languages	VHDL, Verilog
VLSI Tools	H-Spice, P-Spice, Microwind, Cadence

TRAINING DETAILS

- I have completed training of two weeks from **B.S.N.L. SAGAR**.
- Completed a certificate course of four weeks on **VHDL** from **CRISP Bhopal**

PROJECT/THESIS DETAILS

Course Under Project/ Thesis Done	Type of Project Thesis	Name of Project/Thesis	Responsibility
B.E.	Minor Project	Bidirectional Visitors Counter	Circuit Testing on Bread Board and Soldering the Subsystem
B.E.	Major Project	Office Home Security System	Coding
M.Tech.	M.Tech. Thesis	Design of an Efficient Sigma-Delta Modulator	-
Ph.D.	Ph.D. Thesis	Efficient and Reliable Ternary Logic Based Circuits Design	-

LIST OF PUBLICATIONS

Journals

1. **Yogesh Shrivastava,** and Tarun Kumar Gupta, "Design of low-power high-speed CNFET 1-trit unbalanced ternary multiplier," *International Jornal of Numerical Modeling, vol.33, no. 1, Jan./Feb. 2020.*

2. **Yogesh Shrivastava,** and Tarun Kumar Gupta, "Design of High-Speed Low Variation Static Noise Margin Ternary S-RAM Cells," *IEEE Transactions on Device and Materials Reliability*, vol. 21, no. 1, pp. 102-110, March 2021.

3. **Yogesh Shrivastava,** and Tarun Kumar Gupta, "Design of Compact Reliable Energy Efficient Read Disturb Free 17T CNFET Ternary S-RAM Cell," *IEEE Transactions on Device and Materials Reliability*, vol. 21, no. 4, pp. 508-517, December 2021.

4. **Yogesh Shrivastava,** and Tarun Kumar Gupta, " Designing of Low Power High-Speed Noise Immune CNTFET 1-Trit Un-Balanced Ternary Subtractor," *Journal of Circuits, Systems, and Computers, World Scientific*, vol. 31, no. 5, October 2021.

5. **Yogesh Shrivastava**, Lalita Gupta, and J. S. Yadav, "Efficient First-Order Sigma-Delta Modulator," *IJAET Journal of Advanced Engg. Tech*, Vol.I, pp. 99-105, July-Sept, 2010.

Conferences

1. **Yogesh Shrivastava**, and Tarun Kumar Gupta, "Design of Efficient Ternary Subtractor"**,** *International Conference on VLSI Communication and Signal Processing 2019*, Springer.
2. **Yogesh Shrivastava**, Lalita Gupta, and J. S. Yadav, "First and Higher Order Sigma-Delta Modulators with Low Power Consumption," *ConFER 2010 3rd CSI National Conference on Education and Research*, pp. 458-467, Mar 6-7, 2010.
3. **Yogesh Shrivastava**, Lalita Gupta, and J. S. Yadav, "Sigma-Delta Modulator with Feed-Forward Architecture," *NCETEV Conference on Emerging trends in Embedded System and VLSI*, Dec 21-23, 2009.
4. **Yogesh Shrivastava,** Lalita Gupta, and J. S. Yadav, "First Order Sigma-Delta Modulator," *NCVESCOM-2010 National Conference*, pp. 29-31, March 26-27, 2010.

Book Chapter

1. **Yogesh Shrivastava,** and Tarun Kumar Gupta, "Methods to design ternary gates and adders, " *VLSI and Post CMOS Electronic*, Chapter 14, Volume II, IET. (published)

International/National Patent (Granted)

1. Tarun Kumar Gupta, **Yogesh Shrivastava**, Pandey Amit Kumar, Pandey Yudhishthir, and Kori Shiv Prasad, "Design of Efficient Noise Immune Robust Ternary Multiplier" Innovation Patent granted by Australian Government, Patent Number: 2021105714.
2. Tarun Kumar Gupta, Vijayshri Chaurasia, and Yogesh Shrivastava "High-Performance Energy -Efficient Robust Ternary Adder" Innovation Patent granted

by Australian Government, Patent Number: 2021104976.

EXPERIENCE

- Three and a half years of teaching experience at Scope College of Engineering Bhopal.
- One Year teaching experience at Indira Gandhi Government Engineering College Sagar. (Guest Faculty)
- Currently working at Sagar Institute of Science and Technology Ratibadh Bhopal.

EXTRACURRICULAR ACTIVITIES

- Win Vaidik Maths competition at division level in high school.
- Win Judo competition at district level in high school.

I hereby declare that the above written particulars are right to the best of my knowledge and belief.

YOGESH SHRIVASTAVA

Date:

Place: