Dr. Neethu Anna Sabu

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Career Objective

Hard-working person with proven teaching and research skills. Seeking to build on my abilities to fill the faculty role in your esteemed institution and to utilize my skills for the progress of it.

Academic Qualification:

Year	Degree	Institution Name	Mode	% / CGPA
2017-2020	Ph.D (Low Power VLSI Design)	PSNA College of Engineering & Technology, Dindigul, Tamil Nadu (ANNA University, Chennai)	Full-Time	8.5 (Course Work)
2013-2015	M.Tech (VLSI & Embedded Systems)	SCMS School of Engineering & Technology, Ernakulam (Mahatma Gandhi University, Kottayam)	Full-Time	7.75
2008-2012	B.Tech (Electronics& Communication Engineering)	Shahul Hameed Memorial Engineering College, Kollam (Kerala University, Thiruvananthapuram)	Full-Time	7.85
2008	XII (Biology-Maths)	ST. Mary's Residential Central School & Junior College, Alleppey (CBSE)	Full-Time	80
2006	X (All subjects)	ST. Mary's Residential Central School & Junior College, Alleppey (CBSE)	Full-Time	86

Areas of Interest:

- Low power VLSI Designs
- Embedded systems
- Analog and Digital Electronics
- IoT
- Microprocessors and Microcontrollers
- Testing of VLSI Circuits
- Deep Learning

Personal Information:

Date of Birth	26th June 1990
Sex	Female
Father's Name	Sabu Joseph
Mother's Name	Aleyamma Sabu
Mother Tongue	Malayalam
Nationality	Indian
Marital Status	Married
Husband's Name	Anand Abraham
Husband's Occupation	Deputy Manager, IS Audit Section, SBI, Navi Mumbai
Hobbies	Playing Carroms, Cooking and Vegetable Gardening.
Languages Known	English, Malayalam, Hindi and Tamil.

List of Publication:

- Neethu Anna Sabu and K.Batri, "Power and Area Efficient Register Designs involving EHO Algorithm", Circuit World, Emerald Publishers, 10 January 2020. DOI: https://doi.org/10.1108/CW-07-2019-0077. (*SCI and Anna University listed Journal)*
- Neethu Anna Sabu and K.Batri, "Design and Analysis of Power Efficient TG based Dual Edge Triggered Flip-flops with Stacking Technique", Journal of Circuits, Systems and Computers (World Scientific), Vol. 29, No: 8, pp. 1-29, August 2019. DOI: 10.1142/S0218126620501236. *(SCI and Anna University listed Journal)*
- Neethu Anna Sabu and K. Batri, "Review of Low Power Design Techniques for Flip-flops'' in International Journal of Pure and Applied Mathematics (IJPAM), Vol.120, No: 6, June 2018, pp. 1729-1749. *(Scopus Indexed Journal)*
- Neethu Anna Sabu, "Comparison of Latches and Flip-flops in 45 nm Technology'' in

Journal-ICON (Integrating Concepts), Vol.2, Issue 1, January 2017, pp. 7-11.

- Neethu Anna Sabu and Sreeja K.A, "A Low Power Highly Applicable Approach for Caches based on STT-RAM Technology", International Journal of Science and Research (IJSR)", Volume 4, Issue 9, 1325-1327, September 2015.

Experience

SL.No:	Position Held	Name of the Institution	Duration
1	Assistant Professor, Dept. of ECE	Mepco Schlenk Engineering College, Sivakasi,Tamilnadu	18.12.2020 to 30.04.2022
1	Research Scholar, Department of ECE	PSNACET, Dindigul, Tamil Nadu.	15-02-2017 to 30-11-2020
2	Assistant Professor, Department of ECE	St Joseph's College of Engineering & Technology, Palai, Kottayam Dist, Kerala.	01-03-2016 to 31-05-2016

Seminars and Workshops Attended

- Participated in ATAL academy online elementary FDP on Nanodevices and Advanced Nanomaterials, organized by Sikkim Manipal Institute of Technology during 6th -10th December 2021.
- Participated in 40 hour online FDP on ASIC Design Flow-Low Power Perspective, sponsored by Ministry of Electronics & Communication Technology organized by Department of ECE, NITW and E & ICT Academy, NIT Warangal during 1st -10th July 2021.
- Participated in ATAL academy online elementary FDP on Machine Learning Applications in Micro-Nano VLSI Technogies, organized by Department of ECE, BVRIT Hyderabad College of Engineering for Women during 21st -25th June 2021.
- Participated in 2 week online FDP on RISC V-VLSI Implementation flow-RTL2GDS, sponsored by Ministry of Electronics & Communication Technology organized by IIT Guwahati during 27th March -10th April 2021.
- Participated in RSEP-I (Hands on training on Reference Management Tools, Statistical Analysis using R and latex, a three days workshop held in Coimbatore Institute of Technology, Coimbatore from 30th July to August 1, 2018.
- Participated in IEEE sponsored FDP program on Internet of Things: Communication

Technologies held in PSNACET, Dindigul on 27th & 28th April, 2017.

- Participated in two days workshop on Analog & Digital System Design using Cadence Tool held in Thiagarajar College of Engineering, Madurai on 18th & 19th August, 2017.

EDA and Design Tools

- Cadence Virtuoso IC 6.1 Schematic Editor, ADE, Layout Suite and RF Spectre.
- Xilinx ISE 14.7, ModelSim, and Matlab 7.10.
- Magic VLSI Layout Tool, Ngspice and Tanner EDA 16.3.

Research Skills

- Languages – C, C++, Verilog HDL and VHDL.
- Operating Systems – Linux and Windows.

Ongoing Research Work

- Optimization Algorithms
- Magnetic Flip-flops
- FinFet Technology

Subjects Handled

- IoT-Fundamentals & Cloud services
- Artificial Intelligence & Machine learning for Robotics
- Deep learning Techniques for Computer Vision
- Computer Architecture and Parallel Processing
- Linux &Shell Programming

Professional Membership

- ISTE
- IETE

External Excellence & Contributions

- Delivered a guest lecture on the topic "VLSI Design of Advanced Digital Filters" on 18.9.2021 for a two days Technical Seminar on "Recent Advancements in VLSI Signal Processing" in Mepco Schlenk Engineering College, Sivakasi
- Reviewer of the journal "Circuit World"-Emerald Publications from September 2019 to March 2020.
- Reviewer of the journal "International Journal of Electronics"-Taylor & Francis from

June 2021 to present.

- Served as a sub-warden of Ganga hostel (Mepco Schlenk Engineering College Girl's Hostel) for the academic year 2020-2022.
- Placement Faculty Representative, Exam Cell member & NSS in Charge of ECE Department, MSEC, Sivakasi.

Personal Skills

- Winner of Monoact in Kerala State level Sahodaya CBSE Youth Festival, 2007.
- School Kalathilakam of years 2001 to 2004.

References

Dr. K. Batri
Professor and UG Head,
Department of ECE,
PSNA College of Engineering & Technology,
Dindigul-624622
Phone No: 9789680969
Email id: krishnan.batri@gmail.com

Dr. Madhukumar . S
Vice Principal,
St. Joseph's College of Engineering & Technology,
Palai, Kottayam-686579
Phone No: 9495431623
Email id: vp@sjcetpalai.ac.in

Declaration:

I, Neethu Anna Sabu, hereby declare that the information furnished above is true to the best of my knowledge.

Place: Alleppey — Your's sincerely,

Date: — Neethu Anna Sabu