CURRICULUM-VITA

Dr. Neeru Agarwal
E-mail: eng.neeru@gmail.com**,** neeruagarwal@gapp.nthu.edu.tw
Contact: +918218054866, +919456687245
Address: Tower P4, Flat#1222, Ashiana Palm Court, Raj Nagar Extension, Ghaziabad (U.P.)

Objective

Intend to build a career with leading corporate/education hi-tech environment in the area of Microelectronics and VLSI Design with committed & dedicated people and willing to work as a team member in challenging & creative environment

Profile

- *Good understanding of CMOS VLSI design*
- *Good understanding of Display drivers IC Design*
- *Good understanding of semiconductor devices*
- *Good understanding of Data Converters*
- *Good understanding of Mixed Signal Design*
- *Good exposure/experience of M.Tech Programme Leader of ECE/VLSI/EST/WC*

Software Skills

- *Windows, UNIX, Linux*
- *Cadence Virtuoso*
- *HSPICE, LAKER*
- *Mentor Graphics, ELDO Design Architect-IC*
- *Tanner Tools (L-Edit, S-Edit, LVS, T-SPICE)*
- *MATLAB*

Personal Strength:

- *Goal Oriented*
- *Able to work hard in any environment*
- *To handle challenging tasks*

Current Status

Recently completed Ph.D in IC Design, December (2021) from National Tsing Hua University, Taiwan.

Teaching Experience

12 years (12 years Educational, Administrative and Management experience at various positions + 1 year Industry exposure).

Scholastic Background

Doctorate	Ph.D in IC Design from National Tsing Hua University, Taiwan, (Session-2016-2021)
Post Graduation	M.Tech (Microelectronics) from UCIM, Panjab University, Chandigarh. (69%), (Session- 2006-2008)
	M.Sc.(Specialisation in Electronics) from Rohilkhand University, Bareilly (64.75%), (Session- 1998-2000)
Graduation	B.Sc. (PCM), from M.J.P Rohilkhand University (69%), (Session- 1995-1998)

Work Experience	
Ph.D	IC Design from National Tsing Hua University, Taiwan, (2016-2021)
Industry Experience	Worked as trainee in TYRAFOS Technology Company, Ltd. Taiwan, February 2020-January 2021.
Name of Institution	Amity University, Noida Sector 125
Designation	Assistant Professor-II, ASET, Electronics and Communication Engineering Department, Amity University, Noida
Duration	9th September 2008- 31March 2016
Name of Institution	R.S.M. Degree College, Dhampur (U.P)
Designation	Lecturer
Duration	1st August 2004 to 30th June 2006
Designation	Lecturer
Employer	R.S.M. Degree College, Dhampur (U.P)
Duration	6th August 2002 to 30th June 2004

Additional Institutional Responsibility

- Organizing secretary of International conference VMN 2012
- M.Tech Program Leader
- Exam Evaluation Coordinator
- Admission Board Panel Exposure for B.Tech and M.Tech Program

Ph.D Project

1# Title: "A Compact High-Performance 10-bit 30-Channel OLED Driver Using Switched Capacitor Circuit for High-Linearity Application"

- This work proposes a new OLED column driver architecture with 10-bit segmented DAC and switched capacitor multiply by two circuit application. A 30-channel 10-bit switched capacitor driver chip prototype is implemented in 0.18-µm CMOS technology. In this architecture the achieved output range is 1.5-4.8 V for an input range of 1.5-3.15 V, which is suitable for OLED driver with different colors. In the segmented DAC, 6-bit coarse DAC and 4-bit fine DAC are used for the input voltage range 1.5-3.15 V. The new architecture drastically reduces the number of switches and complex metal routing which results in reduced power consumption and good settling time. In the proposed OLED driver, no extra buffer is required as switched capacitor operational amplifier is applying for the same purpose with a gain of more than one. This high-resolution design with small die area also improves the linearity and uniformity with low power consumption. The post simulated results show that the OLED driver exhibits the maximum DNL and INL of 0.03 LSB and -0.06 LSB, respectively, with an LSB voltage of 3 mV. The one-channel area is 0.586 mm ×0.017 mm and the settling time is 4.25 µs for 30 kΩ and 30 pF driving load**.**

2# Title: "A Chopper-Embedded BGR Composite Noise Reduction Circuit for Clock Generator"

- A chopper-embedded bandgap reference (BGR) scheme is designed using 0.18 µm CMOS technology for low-frequency noise suppression for the clock generator application. As biasing circuitry produces significant flicker noise, along with thermal noise from passive components, the proposed low-noise chopper-stabilized BGR circuit was designed and implemented for a wide range of temperature from -40 to 125 ℃, including a startup and self-biasing circuit to reduce critical low-frequency noise from the bias circuitry and op amp input offset voltage. The BGR circuit generated a reference voltage of 1.25 V for a supply voltage range of 2.5–3.3 V. The gain of the implemented BGR operational transconductance amplifier is 84.1 dB. The low-frequency flicker noise was reduced from 1.5 to 0.4 µV/sqrt(Hz) at 1 KHz, with the proposed chopping scheme in the bandgap. A reduction in the flicker noise, from 181.3 to 10.26 mV/sqrt(Hz) at 100 KHz, was observed with the filter.

3# **Title: "ISFET Array Chip Characterization & Implementation using 0.18 µm CMOS Technology for Integrated Sensor Application"**

- An Ion Sensitive Field Effect Transistor (ISFET) array chip is implemented in 0.18µm TSMC CMOS 1P6M technology. It comprises n-ISFET and p-ISFET for characterization towards sensor application. NMOS and PMOS ISFET are fabricated in regular dimension (< 8 µm) compatible with standard NMOS and PMOS dimension. A chip is fabricated with 18 NMOS ISFETs cell and 18 PMOS ISFETs cell of different dimensions for the characterization and to observe the possible effect of scalability. Each cell also has two folded NMOS and PMOS ISFET of standard dimension, unlike very large dimension (>200 µm). We are using metal 1 to metal 6 and via together on the gate area to make extended/floating gate for the

electrochemical sensing of ISFET. These metals are electrically floating with intermediate dielectric. These different sizes floating gate ISFETs provide different sensing area and the passivation Si_3N_4 layer is used for the pH sensing without any extra post processing measures. The different values of gate reference voltage are applied and sweep V_{DS} to measure I_D and observe the ISFET sensitivity, performance in 0.18 μm technology with submicron effects. The measured characterization results propose ISFET a promising sensing device for handheld and remote field application. ISFET chip dimension is 1179 μm × 1185 μm.

M.Tech Project

Title: ''Design of 12 bit Pipeline Analog to Digital Converter using 0.35μm TSMC technology''

- This work presents a new architecture with reduced circuit components and completes circuit realization of its individual circuit blocks. This new architecture applies an indigenous gain stage for multiply by two function particularly used for the subtraction and amplification block. Hence in this block, we are using merely a single operational amplifier for multiplication as well as amplification. Gain stage is used for multiply-by-two function required in high-resolution Pipeline analog-to-digital (A/D) converters. The beauty of this architecture is that it is designed without using digital to analog converter (DAC) & digital correction logic. Here, we are successfully converting the analog value in to corresponding digital output. There may be less power dissipation because this Pipeline ADC needs only one additional operational amplifier and a comparator compare to traditional one Pipeline A/D architecture.

Supervisor: Dr. S.C Bose, Scientist G, IC Design Group, Central Electronics Engineering Research Institute, Pillani (Rajasthan)

Place: Central Electronics Engineering Research Institute, Pillani (Rajasthan)

Area of Interest

Analog CMOS Design, Analog Electronics-I, Analog Electronics-II, Basic Electronics, Semiconductor Devices Physics, Digital Electronics, VLSI Technology & Fabrication, Packaging & Testing.

Projects / Training

IMS Workshop on VLSI Design & Technology at University Centre of Instrumentation and Microelectronics, Punjab University, Chandigarh, 2006.

Conferences/ Workshop

- Attended and presented a research paper in IEEE TENCON 2009 Conference, (Emerging Technologies for Sustainable Development), Singapore.
- Organizing Secretary of International Conference VLSI, MEMS & NEMS, (VMN 2012), ECE Department, ASET, Amity University, Sector 125, Noida, India.
- IEEE SSCS Delhi Chapter 1-day "Workshop on Analog/Digital PLLs and VCO Based ADCs" lead by IEEE-SSCS Distinguished Lecturer Dr. Michael H. Perrott, Silicon Laboratories, Greater Boston Area, USA on 2nd of December 2013 at ST Microelectronics Gr. NOIDA sponsored by IEEE-SSCS, ST Microelectronics, Freescale Semiconductor, Agilent Technologies, Synopsys and IIT Delhi, India.
- IEEE SSCS Delhi Chapter Seminar on todays challenges in Analog & Mixed Signal Design and Test, High Performance Computer Architecture on 21st June 2013 at ST Microelectronics Greater Noida, India.
- IEEE Solid State Circuits and Systems, Delhi Chapter Lecture Series July 2012 @ ST Microelectronics Greater Noida, India.
- IMS National Conference 2007 on Trends in VLSI Design & Embedded System held at Panjab Engineering College, Chandigarh, India.

Seminars:

- National Seminar attended on MEMS, Micro sensors, Smart Materials, Structures and Systems on 16-17 November at CEERI Pillani.
- Seminar Delivered on Mentor Graphics, VLSI Design.
- Seminar Delivered on Data Converters and their application.
- Seminar Delivered on Sample and Hold and their application.
- Seminar Delivered on Introduction to Op Amp.
- Seminar Delivered on Digital Electronics (Flip Flop, Counters etc)

Personal Details

Gender	Female
Marital Status	Single
Date of Birth	June 13, 1979
Father's Name	Shri N. M. Agarwal
Language Known	English, Hindi
Contact No.	+918218054866, +919456687245

References:

#Prof. Dinesh Kumar
Vice Chancellor, Gurugram University, Gurugram, India
Former-Vice Chancellor, J.C. Bose University of Science and Technology, YMCA, Faridabad.
E-mail: dineshelectronics@gmail.com

#Dr. J.N. Roy
Visiting Professor, IIT Kharagpur, Joint faculty in ATDC (Advance Technology Development Centre) & SESE (School of Energy Science & Engineering).
Ex- Senior Vice President (R&D), Solar Semiconductor Pvt. Ltd.
#8-2-608/1/4, Naim Chambers Road No.10, Banjara Hills
Hyderabad-500034
Email: jatinroy2000@yahoo.co.in

 # Dr. S. C. Bose
Former-Senior Scientist, IC Design Lab
Central Electronics Engineering Research Institute of Pillani, Rajasthan
Email: bose.ceeri@gmail.com

#Deep Sehgal
Scientist/Engineer- 'SF' Head, VLSI Design Division
Semiconductor Complex Laboratory' (SCL), Mohali, Chandigarh
Email: sehgal@sclchd.co.in

Paper Published

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1. *Neeru Agarwal*, Neeraj Agarwal, Chih Wen Lu "**A Compact High-Performance 10-bit 30-Channel OLED Driver Using Switched Capacitor Circuit for High-Linearity Application**" Journal of Circuit Systems and Computers, Vol. 31, No.01, 2250013, 2022.

2. *Neeru Agarwal*, Neeraj Agarwal, Chih Wen Lu, Masahito Oh-e "**A Chopper-Embedded BGR Composite Noise Reduction Circuit for Clock Generator" Electronics**, 2021, 10(18), 2257.

3. Neeraj Agarwal, *Neeru Agarwal*, Chih Wen Lu, Masahito Oh-e "**A 33 MHz Fast-Locking PLL with Programmable VCO and Automatic Band Selection for Clock Generator Application**" Electronics, 2021,10(14),1743.

4. *Neeru Agarwal*, B. Prasad, S. C. Bose, Nirmaljit Sharma "**Design & Simulation of Successive Approximation Analog To Digital Converter using asynchronous control logic**" **International IEEE Symposium on Next-Generation Electronics (ISNE 2016)**. This conference will be held at National Tsing Hua University in Hsinchu, Taiwan from May 4th to 6th 2016.

5. Neeraj Agarwal, *Neeru Agarwal*, Manish Sharma "**Design A Test Chip To Find Out Mixed Signal Interference With Broad Range Instrumentation Amplifier**" **International** IEEE Symposium on Next-Generation Electronics (ISNE 2016). This conference will be held at National Tsing Hua University in Hsinchu, Taiwan from May 4th to 6th 2016.

6. *Neeru Agarwal*, B. Prasad, S. C. Bose, Neeraj Agarwal**,** "**Design & Simulation of low power Analog To Digital Converter for medical applications**" Journal, Romania Annals. Computer Science Series Vol. XII, tome 12, fasc. 2. 2014 (ISSN: 2065-7471).

7. Neeraj Agarwal, J. N. Roy, Deep Sehgal, *Neeru Agarwal* "**Design of Noise Injector using Instrumentation amplifier for high efficiency sensor applications** " Journal, Romania Annals. Computer Science Series Vol. XII, tome 12, fasc. 2. 2014 (ISSN: 2065-7471).

8. *Neeru Agarwal* "**Design & Simulation of a novel 12 bit Pipelined Analog to Digital Converter with Simplified functional blocks modules using 0.35µ tsmc technology**" IEEE TENCON 2009 Singapore, 23 - 26 November 2009.

9. *Neeru Agarwal* "**Design and simulation of Low power double tail comparator**" National Conference on Advanced Research & Innovation in Science and Technology (ARISE -15) May 2015, India.

10. *Neeru Agarwal* " **Design and simulation of Sample and Hold circuit using 0.35µ tsmc technology for A/D Converter application**" National Conference on Advanced Research &Innovation in Science and Technology (ARISE -14) May 2014, India.

11. *Neeru Agarwal* "**Design & Simulation of 12 bit Shift Register with reduced complexity for A/D Converter application"** International conference VMN 2012, 24-45th January 2012, India.

12. Neeraj Agarwal, *Neeru Agarwal* "**Design of broad range Instrumentation amplifier to find out mixed signal interference using 0.8µ Nwell Psub CMOS technology** " International conference 'SPVL-2010' on Emerging trends in Signal processing and VLSI design during 11-13th of June 2010, Hyderabad-A.P-(India).

13. *Neeru Agarwal*, Neeraj Agarwal "**Design & Simulation of Low Power Design Strategy for Pipelined A/D Converter with Low INL, DNL**" International conference 'SPVL-2010' on Emerging trends in Signal processing and VLSI design during 11-13th of June 2010, Hyderabad-A.P-(India).

14. *Neeru Agarwal*, S. C. Bose, Anil Saini, Neeraj Agarwal "**A new approach for Designing Subtraction and Amplification block with reduced circuit complexity using 0.35µ TSMC technology for A/D converter application**" Silver Jubilee Conference on "Communication Technologies and VLSI Design" to be held at VIT University, Tamil Naidu, India 2009.

15. *Neeru Agarwal*, S. C. Bose, Anil Saini, Neeraj Agarwal "**Design & Simulation of 12 bit Pipelined Analog to Digital Converter with improved Cascading Technique using 0.35µ TSMC Technology**" International Conference on Wireless Networks & Embedded Systems (WECON-2009).

16. *Neeru Agarwal*, S. C. Bose **"Design & Simulation of High Gain Operational Amplifier for 12 bit Pipelined Analog to Digital Converter using reduced complexity Algorithm** International joint journal conferences in Computer, Electronics, and Electrical CEE 2009 (ACEEE).

(NEERU AGARWAL)