CURRICULUM-VITA

Dr. Neeraj Agarwal
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Objective

Intend to build a career with leading corporate/education hi-tech environment in the area of Microelectronics and VLSI Design with committed & dedicated people and willing to work as a team member in challenging & creative environment.

Profile

- *Good understanding of CMOS VLSI design*
- *Good understanding of Semiconductor devices*
- *Good understanding of Display driver IC design*
- *Sound Knowledge of full custom layout*
- *Good understanding of Data Converters*
- *Good understanding of Mixed Signal Design*
- *Good understanding of Latch up and IO Circuit*

Software Skills

- *Windows, UNIX, Linux*
- *Cadence Virtuoso*
- *HSPICE, LAKER*
- *MENTOR GRAPHICS, ELDO DESIGN ARCHITECT*
- *Tanner Tools (L-Edit, S-Edit, LVS, T-SPICE)*

Personal Strength:

- *Goal Oriented, Dedicated team player*
- *Able to work hard in any environment*
- *To handle Challenging tasks*

Current Status

Recently completed Ph.D in IC Design, December (2021) from National Tsing Hua University, Taiwan.

Teaching Experience

14 years (14 years teaching experience at various positions + 2 year Industry exposure).

Scholastic Background

Doctorate	PhD in IC Design from National Tsing Hua University, Taiwan, (Session-2016-2021)
Post Graduation	MTech. (Microelectronics) from UCIM, Panjab University, Chandigarh. (**77%)**, (Session- 2006-2008)
	One Year Post Graduation in Nanotechnology (Session 2005-2006)
	M.Phill (Instrumentation) from IIT Roorkee, Roorkee (**78.60 %**, Session- 2001-2002)
	M.Sc.(Specialization in Electronics) from H.N.B University, Srinagar (Uttarakhand) **(64.33%), (**Session- 1996-1998)
Graduation	B.Sc. (PCM), from M.J.P Rohilkhand university Bareilly (**63%,** Session-1993-1996)

Work Experience:

Ph.D	IC Design from National Tsing Hua University, Taiwan, (2016-2021)
Industry Experience	Worked as trainee in TYRAFOS Technology Company, Ltd. Taiwan, Feb 2020- Jan 2021
Duration	From 1 August 2012 to 31 March 2016
Designation	Associate Professor & Head
Name of Institution	Teerthanker Mahaveer University, Moradabad
Duration	From 11 August 2009 to 31 July 2012
Designation	Associate Professor & Head
Name of Institution	Institute of Technology & Management, Meerut
Duration	From 1 March 2009 to 10th August 2009
Designation	Assit. Professor & Head
Name of Institution	Dr. K.N.Modi Institute of Engg. & Technology,

	Modinagar
Duration	From 06 Oct 2008 to 28 Feb 2009
Designation	Assit. Professor
Name of Institution	Echelon Institute of Technology, Faridabad
Duration	1 Aug 2002 – 30 Jun 2005
Designation	Lecturer
Name of Institution	R.S.M. College, Dhampur (U.P)
Duration	15 July 1998 – 31 July 2001
Designation	Lecturer
Name of Institution	R.S.M. College, Dhampur (U.P)

Additional Institutional Responsibility

- Organized National Conference NCFTEC-2013, ARISE-14,15
- Worked on NAAC Complaisance
- Exposure to Exam Evaluation Coordinator
- Exposure to establish lab and course curriculum updation

Ph.D Project

1# Title: "A 10-bit 20 Channel LCD Column Driver using Compact DAC"

- A 20-channel liquid crystal display (LCD) driver architecture is implemented with 0.18 µm CMOS technology. This work presents a novel design of a 10-bit compact and high resolution two stage DAC to improve the linearity and uniformity of each channel performance. A complete column driver including compact DAC, low power buffer, global R-string and multiplexing circuit design is implemented and layout of this 20-channel 10-bit LCD driver is generated by using 0.18 µm CMOS technology. All circuit blocks of the proposed LCD column driver were simulated using the EDA tool HSPICE and layout generation by Laker. This work also realizes high performance class AB low power operational amplifier with a gain of 140 dB for proposed LCD driver. The 10-bit compact LCD driver has 1.4 mV LSB and output voltage 1.7 V is achieved for the input range of 0.25V–1.7V. The experimental results exhibit maximum differential nonlinearity (DNL) and integral nonlinearity (INL) of 0.065 LSB and -0.12 LSB, respectively. One channel area is 951.69 µm × 17.8 µm and settling time is 5.65 µs for the 20 kΩ and 20 pF driving load.

2# Title: "A 33 MHz Fast-Locking PLL with Programmable VCO and Automatic Band Selection for Clock Generator Application"

- This work presents a prototype of an auto-ranging phase-locked loop (PLL) with low jitter noise over a wide operating frequency range using the multiband programmable voltage-controlled oscillator (VCO) gain stage with automatic band selection. We successfully reduce the VCO gain (Kvco) and retain the desired frequency band. The proposed PLL comprises a prescaler, phase frequency detector (PFD), charge pump (CP), programmable VCO and automatic

band selection circuit. The PLL prototype with all sub blocks was implemented using the TSMC 0.18 μm 1P6M process. Contrary to conventional PLL architectures, the proposed architecture incorporates a real time check and automatic band selection circuit in the secondary loop. To maintain a low Kvco and fast locking, the automatic frequency band selection circuit also has two indigenous, most probable voltage levels. The proposed architecture provides the flexibility of not only band hopping but also band twisting to obtain an optimized Kvco for the desired output range, with the minimum jitter and spurs. The proposed programmable VCO was designed using a voltage-to-current-converter circuit and current DAC followed by a four-stage differential ring oscillator with a cross-coupled pair. The VCO frequency output range is 150–400 MHz, while the input frequency is 25 MHz.

3# **"ISFET Array Chip Characterization & Implementation using 0.18 μm CMOS Technology for Integrated Sensor Application"**

- An Ion Sensitive Field Effect Transistor (ISFET) array chip is implemented in 0.18μm TSMC CMOS 1P6M technology. It comprises n-ISFET and p-ISFET for characterization towards sensor application. NMOS and PMOS ISFET are fabricated in regular dimension (< 8 μm) compatible with standard NMOS and PMOS dimension. A chip is fabricated with 18 NMOS ISFETs cell and 18 PMOS ISFETs cell of different dimensions for the characterization and to observe the possible effect of scalability. Each cell also has two folded NMOS and PMOS ISFET of standard dimension, unlike very large dimension (>200 μm). We are using metal 1 to metal 6 and via together on the gate area to make extended/floating gate for the electrochemical sensing of ISFET. These metals are electrically floating with intermediate dielectric. These different sizes floating gate ISFETs provide different sensing area and the passivation Si_3N_4 layer is used for the pH sensing without any extra post processing measures. The different values of gate reference voltage are applied and sweep V_{DS} to measure I_D and observe the ISFET sensitivity, performance in 0.18 μm technology with submicron effects. The measured characterization results propose ISFET a promising sensing device for handheld and remote field application. ISFET chip dimension is 1179 μm × 1185 μm.

M.Tech Project

Title: "Mixed Signal Interference-Analysis, Measurement & Reduction Techniques"

Mixed Signal Interference- The design of system on a single chip (SOC) where several circuits of entirely different nature, operating modes & functionality are integrated on the same substrate at short distances to one another and when we put these analog & digital circuit on the same chip which is increasingly the case in modern VLSI and if a minute fraction of digital swing is coupled to sensitive analog nodes the result can be disastrous for the affected analog circuit

Object- A test chip to find out various aspects of MSI was planned in 0.8 µm (NWell PSub) 5V double poly double metal CMOS technology. Basic aim of the chip was to find out magnitude of interference happening when analog and digital circuit placed nearby on a common substrate.

Supervisor: Dr. J. N .Roy, Scientist/Engineer-'G' & Deep Sehgal, Sr. Scientist, SCL, Mohali, (Punjab).

M. Phill (Project)

Title: "To design and fabricate a precise rotational system for ion exchange columns".

Supervisor: Dr. K. Chandra, Prof & Head Institute Instrumentation center, IIT Roorkee, Uttrakhand

Area of Interest

Semiconductor Devices Physics, Basic Electronics, Analog Electronics, Analog & Mixed Signal Design, VLSI Technology & Fabrication, Digital Electronics, Packaging & Testing.

Conference/Workshop

- Convener of National Conference Advance Research & Innovation in Science & Engineering (ARISE-15), April 30, 2015, College of Engineering, ECE Department, Teerthanker Mahaveer University, Moradabad, India.
- Convener of National Conference Advance Research & Innovation in Science & Engineering (ARISE-14), May 11, 2014, College of Engineering, ECE Department, Teerthanker Mahaveer University, Moradabad, India.
- Convener of National Conference NCFTEC-2013, May 17, 2015, College of Engineering, ECE Department, Teerthanker Mahaveer University, Moradabad, India.
- IEEE SSCS Delhi Chapter 1-day "Workshop on Analog/Digital PLLs and VCO Based ADCs" lead by IEEE-SSCS Distinguished Lecturer Dr. Michael H. Perrott, Silicon Laboratories, Greater Boston Area, USA on 2nd of December 2013 at ST Microelectronics Gr. NOIDA sponsored by IEEE-SSCS, STMicroelectronics, Freescale Semiconductor, Agilent Technologies, Synopsys and IIT Delhi, India.
- IEEE SSCS Delhi Chapter Seminar on today's challenges in Analog & Mixed Signal Design and Test, High Performance Computer Architecture on 21st June 2013 at ST Microelectronics Gr. NOIDA, India.

- IEEE Solid State Circuits and Systems, Delhi Chapter Lecture Series July 2012 @ ST Microelectronics Greater Noida, India.

- IMS Workshop on VLSI Design & Technology at University Centre of Instrumentation and Microelectronics, Panjab University, Chandigarh, India.

- IMS National Conference 2007 on Trends in VLSI Design & Embedded System held at Panjab Engineering College, Chandigarh, India.

Personal Details

Gender	Male
Marital Status	Single
Date of Birth	April 4 1977
Father's Name	Shri N. M. Agarwal
Language Known	English, Hindi

References:

#Prof. Dinesh Kumar
Vice Chancellor, Gurugram University, Gurugram, India
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#Dr. J.N. Roy
Visiting Professor, IIT Kharagpur, Joint faculty in ATDC (Advance Technology Development Centre) & SESE (School of Energy Science & Engineering).
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#Deep Sehgal
Scientist/Engineer- 'SF' Head, VLSI Design Division
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Paper Published

1. *Neeraj Agarwal*, Neeru Agarwal, Chih Wen Lu, Masahito Oh-e "**A 33 MHz Fast-Locking PLL with Programmable VCO and Automatic Band Selection for Clock Generator Application**" Electronics, 2021,10(14),1743.

2. Neeru Agarwal, *Neeraj Agarwal*, Chih Wen Lu "**A Compact High-Performance 10-bit 30-Channel OLED Driver Using Switched Capacitor Circuit for High-Linearity Application**" Journal of Circuit Systems and Computers, Vol.31, No.01, 2250013, 2022.

3. Neeru Agarwal, *Neeraj Agarwal*, Chih Wen Lu, Masahito Oh-e "**A Chopper-Embedded BGR Composite Noise Reduction Circuit for Clock Generator**" Electronics, 2021, 10(18), 2257.

4. *Neeraj Agarwal*, Neeru Agarwal, Manish Sharma "**Design A Test Chip To Find Out Mixed Signal Interference With Broad Range Instrumentation Amplifier**" International IEEE Symposium on Next-Generation Electronics (ISNE 2016). This conference will be held at National Tsing Hua University in Hsinchu, Taiwan from May 4th to 6th 2016.

5. *Neeraj Agarwal*, J.N. Roy, Deep Sehgal, Neeru Agarwal "**Design of Noise Injector using Instrumentation amplifier for high efficiency sensor applications**" Journal, Romania Annals. Computer Science Series Vol. XII, tome 12, fasc. 2. 2014 (ISSN: 2065-7471).

6. Neeru Agarwal, B. Prasad, S. C. Bose, *Neeraj Agarwal***,** "**Design & Simulation of low power Analog To Digital Converter for medical applications**" Journal, Romania Annals. Computer Science Series Vol. XII, tome 12, fasc. 2. 2014 (ISSN: 2065-7471).

7. *Neeraj Agarwal* "**A Review And Comparative Study Of Different Soft Error Tolerant SRAM Cells " National conference 'ARISE-14'** on Advance Research and Innovation in Science & Technology during 17th of May 2014, India.

8. *Neeraj Agarwal* "**Design Of High Gain Cascode Amplifier Using 65 nm technology** " National conference 'ARISE-14' on Advance Research and Innovation in Science & Technology during 17th of May 2014, India.

9. *Neeraj Agarwal* "**Low Power Analysis of Multi-Stage Operational Amplifier using 45nm technology** " National conference 'NCFTEC-13' on Future Trends in Electronics and Communication during 11th of May 2013, India.

10. *Neeraj Agarwal* "**Design & Optimization of Operational Transconductance Amplifier for Ultra Low Power Applications using 32nm CMOS technology**" National conference 'NCFTEC-13' on Future Trends in Electronics and Communication during 11th of May 2013, India.

11. *Neeraj Agarwal*, Neeru Agarwal "**Design of broad range Instrumentation amplifier to find out mixed signal interference using 0.8µ Nwell Psub CMOS technology** " International conference 'SPVL-2010' on Emerging trends in Signal processing and VLSI design during 11-13th of June 2010, Hyderabad-A.P-(India).

12. Neeru Agarwal, *Neeraj Agarwal* "**Design & Simulation of Low Power Design Strategy for Pipelined A/D Converter with Low INL, DNL** " International conference 'SPVL-2010' on Emerging trends in Signal processing and VLSI design during 11-13th of June 2010, Hyderabad-A.P-(India).

13. Neeru Agarwal, S. C. Bose, Anil Saini, *Neeraj Agarwal* "**A new approach for Designing Subtraction and Amplification block with reduced circuit complexity using 0.35µ tsmc technology for A/D converter application** " Silver Jubilee Conference on "Communication Technologies and VLSI Design" to be held at VIT University, Tamilnadu, India 2009.

14. Neeru Agarwal, S. C. Bose, Anil Saini, *Neeraj Agarwal* " **Design & Simulation of 12 bit Pipelined Analog to Digital Converter with improved Cascading Technique using 0.35µ tsmc Technology** " International Conference on Wireless Networks & Embedded Systems (WECON-2009).

Date: 20 January 2022
Place: Ghaziabad

(NEERAJ AGARWAL)