RESUME

Dr. Vishnu Annarao Suryawanshi
Sr.No. 172/9 Aishwarya Greens
Building A1 Flat No-301. Near Old Power House Bhekrainagar Pune-412308
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Google Scholar Id: https://scholar.google.com/citations?user=7hdhACsAAAAJ&hl=en
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Objective:

Intent to build a career with leading corporate of hi-tech environment with committed & dedicated people, which will help me to explore myself fully and realize my potential. Willing to work as a key player in challenging & creative environment looking for the position, where I can continuously learn and contribute my knowledge experience for the society, from where I got lot of things.

Publications:--

JOURNAL

Vishnu suryawanshi, Sachin Ahankari, Dr.G.C.Manna "A REVIEW OF SOME POPULAR HARDWARE IMPLEMENTATION TECHNIQUES IMPLEMENTED ON ADVANCED ENCRYPTION STANDARD" International Journal Of Advance Research In Science And Engineering http://www.ijarse.com IJARSE, Vol. No.2, Issue No.10, October 2013 2319- 8354(E)

V. A. Suryawanshi G.C.Manna Dr.S.S Dorale "Optimized AES Algorithm Using Cyclic Shift Method for Mix-Column and Design Trade in Shift Rows" Institute of Engineers Pune.

V. A. Suryawanshi, G. C. Manna and Dr.S.S. Dorale "Modified Logic Parallel Pipelined Architecture for Enhanced Throughput of Advanced Encryption Standard" CiiT International Journal of Wireless Communication, Vol 6, No 09, October - December 2014 325 0974-9756/CIIT–IJ-5522/05/$20/

V. A. Suryawanshi, G. C. Manna and Dr.S.S. Dorale "Compact and High Speed Hardware Implementation of the Block- Cipher Clefia" International Journal of Computer Applications (0975 – 8887) Volume 133 – No.8, January 2016.

CONFERENCE

VA Suryawanshi and G.C. Manna "Compact Hardware Implementation for Advanced Encryption Standard using Feedback Method" Proceedings of National Conference on Trends in Signal Processing & Communication (TSPC'14) ISBN: 978-93-83842-40-7

V.A.Suryawanshi and G.C. Manna "Area-High Speed Design Trade-Offs for Advanced Encryption Standard Cipher Engine" 2015 International Conference on Nascent Technologies in the Engineering Field (ICNTE-2015 978-1-4799-7263-0/15/2015 IEEE.

- Written a chapter on "Cryptographic Algorithms for Next Generation wireless networks Security for "Next Generation Wireless Network IGI Publications Scoups Indexed.

Other Platforms:

Programming Language	: Python, SQR, R, C,C++,VHDL and Verilog
Software Packages	: Multi-sim, Model Sim, Ltspice
Operating System	: MS-Dos, Windows 95/98/2000.
Application S/W and Tools	: Xilinx, Sci Lab,MATLAB,
TESTING.	

Work Experience

- Working as a Asst. Proff in MIT College of Railway Engineering and Research Barshi since (**from 11 July 2019 to till date**)
- Worked as a Asst. Proff. in G.H.Raisoni Institute of Engineering and Technology Pune. (From **2 July 2009** t**o 27 Aug 2018**).
- Worked as Asst. proff. in Arkay college of Engineering & Technology, Bodhan Dist Nizamabad.(A.P).Over more than 3 years (From **5th August 2005 to 29 June2009**)
- Worked as a Asst. proff. in Srinivasa college of Engineering ,Banaswada Dist Nizamabad over more than 3 years (From **24th September 2002 to 4th August 2005**) (A.P)
- Worked as a Asst. proff. in Dr. V.R.K. College of Engineering & Technology, Jagtiyal Dist Karimnagar A.P. over more than 1 and half year (From **06 April 2001 to 14th September 2002**)
- Worked as lecturer in Puranmal Lahoti Govt. Polytechnic College Latur (MS) for 1 year.
- Nodal Centre Co-ordinator for Virtual Lab under NMEICT (Govt College of Engg Pune)

Subject Taught:

- CS (Control system)
- VLSI (Very Large Scale Integration)
- BEE (Basic Electronics Engineering)
- RM (Research Methodology for M.E.)
- Machine Learning
- Data Mining
- Data Science

Educational Profile:

- **Ph.D (Network Security)** from Rashtra Sant Tukdoji Maharaj Nagpur University Nagpur.
- **M.Tech. (VLSI SYSTEM DESIGN)-[2007-2009]** from Nimra College Of Engineering and Technology Vijaywada under Jawaharlal Nehru Technological University Hyderabad With 70.71%.
- **B.E.(ELECTRONICS)** from Shri Tulaja Bhavani College Of Engineering Tulajapur. Dist-Osmanabad (M.S.) under Dr. Babasaheb Ambedkar Marathwada University, Aurangabad. with 63.93%.(M.S.)
- **H.S.C** From Maharashtra State Board Of Aurangabad with 66.66%, Dayanand Science College, Latur-413531(M.S)
- **S.S.C** From Maharashtra State Board Of Aurangabad with 75.14%, Shri Lokmanya Vidyalaya Panchincholi, Tq-Nilanga, Dist-Latur (M.S)

Workshops/Seminars Conducted and Attended:

- Conducted as a NATIONAL LEVEL WORKSHOP ON VLSI SYSTEM DESIGN in Arkay College of engineering and technology, Bodhan. Dist Nizamabad (A.P.)
- Attended a workshop on ISTE Approved Short Term Training Program (STTP) On "RECENT TRENDS IN ADVANCED IMAGE PROCESSING" In G.H.R.C.E.M. Pune.
- Participated One Day Workshop on "Syllabus Detailing of SE (ELEX/ETC) SEM-II Subjects (2008Course)" organized by S.G.R.E.F.S Ahmednagar And by University of Pune.
- Participated One Day Workshop on „MODIFIED TEACHING METHODOLOGIES OF BASIC ELECTRONICS ENGINEERING For F.E(2008Course) & HANDS-ON EXPERIENCE OF ONLINE EXAMINATION" Organized by Vidya Pratishthan"s college of Engineering, Baramati. And University of Pune.
- Attended a one month course for ELITE PROGRAM "Leveraging Technology for Effective Teaching in the Classroom and Beyond" Sponsored by the Department of Information Technology, Govt. of India .Organized by "INTERNATIONAL INSTITUTE OF INFORMATION TECHNOLOGY" Bangalore.
- Participated One Day Workshop on "Syllabus Detailing of TE (ELEX/ETC) SEM-I Subjects (2008Course)" organized by MMIT Lohgaon Pune and University of Pune.
- Attended Short Term Training Program (STTP) On "VLSI SIGNAL PROCESSING" In IIT Khargapur. (17 Dec to 23 Dec-2010).
- Conducted workshops on "ANALOG ELECTRONICS" and "CONTROL SYSTEM" under NMEICT by MHRD Govt Of India and IIT Kharagpur as a workshop co-ordinator.
- Attended a workshop on "Research Planning and Technical Paper Writing" conducted by Dept of electronics, university of Pune and Fergusson college and speed

Personal Details:

Date of Birth	: 10-07-76.
Marital Status	: Married.
Languages known	: English, Hindi, Marathi.Telgu
Address for Correspondence	: At. Kalandi Post. kelgaon. Tq. Nilanga.Dist :Latur(413521)

Dr.Vishnu Suryawanshi