Pankaj Bhagawat
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Education:

- ***Ph.D.** in **Electrical and Computer Engineering*** **Dec, 2011**
  Texas A&M University, College Station, U.S.A.
  Dissertation: Hardware Accelerator for MIMO Wireless Systems.
  Degree Plan GPA: 3.54/4.00
  Overall GPA: 3.54/4.00
- ***M.S.** in **Electrical and Computer Engineering*** **Aug, 2003**
  Texas A&M University, College Station, U.S.A.
  Thesis: Design of a Robust Parameter Estimator for Nominally Laplacian Noise.
  Degree Plan GPA: 3.75/4.00
  Overall GPA: 3.42/4.00
- ***B.E.** in **Electronics & Communication Engineering*** **May, 2000**
  National Institute of Technology, Trichy, India.
  GPA: 69%
  Project: VLSI Implementation of Discrete Cosine Transform
- ***High School in Science(12th)*** **May, 1995**
  Kendriya Vidyalaya, Ambernath, India.
  Mathematics: 99% **Physics:** 97% **Chemistry:** 95%
  Overall: 82%
- ***High School in Science(10th)*** **May, 1995**
  Kendriya Vidyalaya, Ambernath, India.
  Mathematics: 95% **science:** 85%
  Overall: 76%

Date of Birth: 9-11-1977

Courses supervised as a teaching assistant:

Electronic devices and circuits, Circuit Analysis, Digital Electronics, Computer Organization.

Research Interests:

Hardware/Algorithm co-design, Multiple Antenna Systems, Application Specific Processor Architecture.

Teaching Interests:

VLSI design, Digital logic design, VLSI signal processing, Computer organization, Digital signal processing.

Professional Experience:

- ***Self Employed, Ambernath, India.*** ***Dec 2013 – Present***
  Worked on trading stocks and other financial instruments. Traded mostly on short term (swing trading) basis. Developed knowledge and further interest in entrepreneur-ship.
- ***Senior Engineer, Qualcomm Inc, San Diego, USA.*** ***Oct 2011 – Oct 2013***
  Responsible for hardware verification of an instruction for the software defined radio. The instruction is used to generate soft information for 2x2 MIMO system. Also, responsible for verifying and assembly programming of Qualcomm's massively parallel vector baseband processor. Programmed the processor for noise estimation and channel estimation task of the receiver.
- ***Doctoral Research under Prof. Gwan Choi, Texas A&M University, USA.*** ***Aug 2003- May 2011***
  My research work focuses on developing high throughput, configurable VLSI architectures/designs for detectors used in MIMO wireless systems. Practical issues including real time configurability, energy/area efficiency, throughput, and the error rate performance of the detector hardware are addressed. Micro-architectural techniques such as pipelining, parallel processing, and clock gating are explored to improve the hardware efficiency.

  Highly pipelined systolic-like architectures are developed to compute both hard and soft estimates. The detector architectures can be configured in real-time to support multiple modulation schemes (QPSK, 16-QAM, and 64-QAM). The

architectures also support variable numbers of antennas (2x2, 3x3, and 4x4). The error rate performance, throughput, and energy consumption of the detector architectures is thoroughly analyzed. Architectural space exploration is also done to optimize the area and power consumption of the detector under throughput constraints, for the 802.11n standard. Algorithmic approximations are developed, and tradeoff analyses between energy/area efficiency of the hardware and error rate performance are conducted.

- ***Engineering Intern, Qualcomm Inc, San Diego, USA*** ***Feb-July, 2005***
  - Power consumption profiles of Qualcomm's WCDMA/HSDPA chipsets.
    - Measured and reported power consumption profiles of various subsystems of the chipset such as RF, baseband modem components and display.
    - Debugged issues related to power consumption and battery life of cell phones.
    - Set up test environment by creating and executing test scenarios.

- ***Graduate Teaching Assistant, Texas A&M University, USA*** ***Aug 2003- May 2011***
  - Conducted laboratory sessions, weekly laboratory lectures, assisting students and grading lab assignments. The courses taught included Electronic Devices and Circuits, Circuit Analysis, Digital Electronics, System-Design in LabView, Computer organization. Also, mentored one M.S. and one Ph.D. student in my research group.

- ***Research Intern, Inter University Centre for Astronomy and Astrophysics (IUCAA), Pune, India***
  May- July, 1999
  - Designed an innovative algorithm (based on edge detection) to detect clouds in images captured by a CCD camera. (Under Distinguished Prof. Shyam Tandon.)

Publications:

Peer Reviewed Conference Articles (Over 100 paper citations and 6 patent citations)

- *"Energy-Efficient MIMO Detection Using Unequal Error Protection for Embedded Joint Decoding System", Yang,* ***Bhagawat****, Choi, IEEE Design Automation Conference (DAC), 2011. (****Acceptance Rate: 22.6%)***
- *"Systolic Like Soft-Detection Architecture for 4x4 64-QAM MIMO System",* ***Bhagawat****, Dash, Choi. Design Automation and Test in Europe (DATE), April, 2009, Nice, France. (****Acceptance Rate:23.42%)***
- *"Array Like Runtime Reconfigurable MIMO Detectors for 802.11n WLAN: A Design Case Study",* ***Bhagawat****, Dash, Choi. IEEE Asia and South Pacific Design Automation Conference (ASPDAC), Jan, 2009, Yokohama, Japan. (Presented) (****Acceptance Rate: 33%)***
- *"High Performance On-The-Fly Reconfigurable MIMO Detector",* ***Bhagawat****, Dash, Choi. IEEE Asilomar Conference on Signals, Systems, and Computers, Oct, 2008, Monterey. (Presented)*
- *"Dynamically Reconfigurable Soft MIMO Detector",* ***Bhagawat****, Dash, Choi. IEEE International Conference on Computer Design (ICCD), Oct, Lake Tahoe, 2008. (Presented) (****Acceptance Rate: 34%)***
- *"Architecture for Reconfigurable MIMO Detector and its FPGA Implementation",* ***Bhagawat****, Dash, Choi. IEEE International Conference on Electronic Circuits and Systems (ICECS), 2008.*
- *"VLSI Implementation of a Staggered Sphere Decoder Design for MIMO Detection",* ***Bhagawat****, Ekambavanan, Choi, Khatri. Forty Fifth Annual Allerton Conference, 2007. (Presented)*
- *"An FPGA Implementation of Dirty Paper Precoder",* ***Bhagawat****, Wang, Uppal, Choi, Xiong, Yeary. IEEE International Conference on Communications (ICC), 2007. (Presented) (****Acceptance Rate: 37.8%)***
- *"A High-Speed Fully Programmable VLSI Decoder for Regular Low Density Parity Check (LDPC) Codes", Kim, Jayakumar,* ***Bhagawat****, Selvarathinam, Choi, Khatri. IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP), 2006.*
- *"FPGA Based Implementation of Decoder for Array LDPC Codes",* ***Bhagawat****, Uppal, Choi. IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP), 2005.*
- *"An Efficient Implementation of IS-95 CDMA Reverse Link Transceiver: A Codesign approach", Raman,* ***Bhagawat****, Mahapatra. International Conference on Signal Processing, Robotics and Automation, 2002.*

Academic Projects:

- Simulated ZF, Sphere Detector, and K-Best algorithms for MIMO detection under block and fast fading.
- Implemented a MIPS micro-processor in Verilog.

Relevant Skills:

- Competent in deriving micro-architectural specifications, RTL design, cycle accurate modeling, low power techniques, and hardware/software implementation trade-offs.
- Digital communications and signal processing concepts.
- MIMO systems, LDPC.
- Familiar with the LTE standard.
- Understanding of ASIC design flow.
- **Programming Languages** : Matlab, assembly programming, C++.
- **HDL** : Verilog.
- **Simulators** : ModelSim.
- **Design Tools** : Synopsys Design Compiler.
- **FPGA** : Xilinx ISE.

Professional Activities:

- Reviewed for IEEE Transactions on Very Large Scale Integration (TVLSI)
- Reviewed for IEEE Transactions on Signal Processing (TSP)
- Reviewed for IEEE Transactions on Communications (TCOM)
- Reviewed for IEEE International Conference on Communications (ICC)
- Reviewed for IEEE International Symposium on Circuits and Systems (ISCAS)

Honors:

- Recipient of departmental scholarship for the year 2000-2001 (Dept. of ECE, TAMU).
- First prize in hardware design contest at Probe 2000 (A National Level Technical Symposium in India).
- Top 1% in the country in National Level Science Talent Exam.
- Certificates of merit at National Mathematics Olympiad contests.
- Top 1% in the state in National Physics Olympiad.
- Top 0.1% of the country in mathematics exam (high school) conducted by C.B.S.E.

Relevant Courses:

- Introduction to VLSI Design
- VLSI Circuit Design
- Advanced VLSI System Design
- Advanced Logic Design
- Hardware-Software Co-Design for Embedded Systems
- Digital Signal Processing
- Wireless Communications
- Probability and Random Processes
- Error Control Coding
- Analysis of Algorithms