Divyanshi Yadav

Contact Details
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Curriculum Vitae

- **Objective**: To acquire an academic position lecturing and teaching courses in the Electronics field, To see every student succeed. My key goal is to assist in helping students achieve their academic goals. I am ready to start an entry-level position in a college environment and expand my teaching skills. Enthusiastic and ready to help the whole community develop personal and professional skills as well as work on my own.

Education Qualification:

Degree	College	Stream	Percentage /CGPA
MTech (2021)	Thapar Institute of Engineering andTechnology, Patiala	VLSI Design	7.89
BTech (2016)	College of Engineering Roorkee	Applied Electronics and Instrumentation	72%
Senior Secondary (2012)	Heliger Borden Education Centre	Science	62%
Secondary (2010)	St. Anthony Sr Sec School	Science	86%

Work Experience:

- Worked as an R&D intern with Nokia Solutions & Networks for a period of 11 months (August 2020 – July 2021).
- Worked on Testing & Automation profile
- Worked as an apprentice in Havells India Pvt. Ltd. (February 2018 – August 2019)

Software Skills:

Operating Systems	GNU/Linux, Windows 95/98/ME/2000/XP

Hardware Description Languages	Verilog, VHDL
Internet	HTML
Software Tools	Microsoft Office, Microsoft Word
Electronics Tools	Pyxis
Scripting Language	Python

Relevant Courses Attended:

1. Analog Circuit Design
2. Digital VLSI Design
3. Physical Design Automation
4. Digital Electronics
5. Analog Electronics
6. Electronics Devices and Circuits
7. Control Systems
8. Signals and System

Projects:

1: Designed a Low Power Configurable Adder for Approximate Applications.

Faculty Name: Dr. Bharat Garg Team Size 3

Abstract: The project aims to propose a carry maskable error whose accuracy can be configured at run time.

Technologies used: VHDL

2: Designed a wide swing cascode current mirror and high output resistance to meet given specifications.

Faculty Name: Dr. Anil Singh Team Size 2

Abstract: The project aims to design a wide-swing, current reference to be used as a biasing circuit.

3: Designed a Secure Hash Algorithm-1 using Verilog.

Faculty Name: Dr. Bharat Garg

Abstract: Secure hash Algorithms, also known as SHA, are a family of cryptographic functions designed to keep data secured.

4: Designing a dynamic comparator for 6-bit FLASH ADC, for a power budget of 2mW. (ongoing)

Faculty Name: Dr. Anil Singh Team Size 2

Extra-Curricular Activities:

• Participated in Expressions 12-The Linguistic Committee in College

• Active member of 'PANKHURI'(NGO) during College Tenure

• Coordinator of "ECO CLUB" (COER) during College Tenure

• Participated in NATIONAL CONFERENCE on "ETEST-2014" at college. • Coordinated various events in "HARITIMA" (college fest) in 2013, 14& 15.

Personal profile:

- Date of Birth: 29 January 1996
- Father's Name: Mr. Ravindra Singh Yadav
- Mother's Name: Mrs. Mamata Yadav
- Marital Status: Married
- Husband's Name: Mr. Gaurav Yadav
- Permanent Address: 18 MIG Ist Mahabalipuram, panki road, kalyanpur, Kanpur (U.P)
- Current Address: 1501 Lush Meadows Sector 11, Kharghar (Maharashtra)
- Strengths: Hard Work, Quick Learner, Optimistic, Adaptive, Good team player
- Hobbies: Reading Books, Movies, Crafts, Calligraphy.

Note: All information furnished above is true to the best of my knowledge.
