ANURAG CHILWIRWAR

VLSI design and Verification Trainee Engineer

A budding professional completed Mtech in VLSI design from NIT Jalandhar looking forward to an opportunity in a renowned organization where I can utilize my expertise and skills and also for the advancement in terms of knowledge acquisition and career development. I have good leadership skills and team management. Hardworking and avoid procrastination. I am a trainee at Maven Silicon that can be an advantage.My aim is to benefit the organization to achieve it goals by my technical skills and knowledge

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EDUCATION

MASTER OF TECHNOLOGY in VLSI Design
Dr BR Ambedkar National Institute OF technology Jalandhar Punjab

07/2019 - 10/2021 *7.67*

Thesis and paper

- Design of Fault tolerant XOR gate using Quantum dots cellular automata and analysis.
- International conference IMRSE 2021 publised paper on "Design of digital circuits using QCA""

BACHELOR OF ENGINEERING
Government College Of engineering Jalgaon Maharashtra

07/2013 - 07/2017 *6.89*

project

- Internet of things based home sensing station

Intermediate
Nagpur

07/2011 - 05/2013 *69%*

SSC
Maharashtra state board

06/2010 - 05/2011 *86%*

PROJECTS

Design of FIFO using verilog HDL and 16*8 syncronous dual port RAM

Vending machine using verilog HDL

- The vending machine was based on FSM .The design was tested using testbench.The objective of the project was to design a real life time design using verilog HDL

Design of FSM using verilog HDL

- FSM was designed using mealey machine usind parameter.The objective was to oberve the working of FSM by degining the various states as parameter

1x3 Router design using verilog HDL

- Designed RTL of various blocks of router that is FSM,FIFO,REGISTER SYNCHRONISERand top level block.The RTL design was also stimulated using test bench.The router accepts 8 bit data and transfer the packets to one of the destination.The tools used were modelsim,Questasim and Quartus prime.The objective of the project was routing of packets.

SKILLS

RISC V ,Verification,VERILOG,System, Verilog,VHDL,FPGA,RTL,Physical design flow,Layout design,low power VLSI design

C programming,Python,PERL,Comprehensive understanding of CMOS Technology,Basic Knowledge of Physical design flow and IC design

VLSI,CMOS,ASIC flow,RTL DESIGN,Digital design,Static time analysis(STA),IC Fabrication,

QCAD DESIGNER,TCAD,embedded systems

hands-on experience with softwares such as cadence VIRTUOSO,IC LAYOUT,LT SPICE,ANALOG CIRCUIT,glade IC layout editor,Model sim ,xilinix ISE

Relevant Coursework : IC Fabrication,Digital Integrated Circuit,Digital Electronics,Low power VLSI DesignNano Electronics,Fundamental of Semiconductor

CERTIFICATES

Online internship in VLSI covering Analog and Digital flow

Jointly organized by NIT Calicut and NIELIT. Certificate no.OLC0828

BSNL INTERNSHIP at RTTC Nagpur

INTERESTS

VLSI design | Verification

Physical design flow,Chip design,IC Fabrication and design,Physical layout

To work in VLSI Industry

ASIC,Analog Circuits