A Modified PLL for Single-Phase Voltage System

Md. Zahid Hasan, Istiaq Firoz Shiam, Tasnim Tabassum & Md. Shamim Reza
Department of Electrical and Electronic Engineering
Bangladesh University of Engineering and Technology, Dhaka 1205, Bangladesh

Introduction

- Phase locked loop (PLL) is a control system that generates an output signal whose phase is related to the phase input signal.

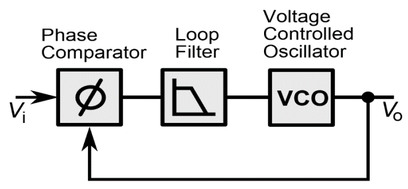
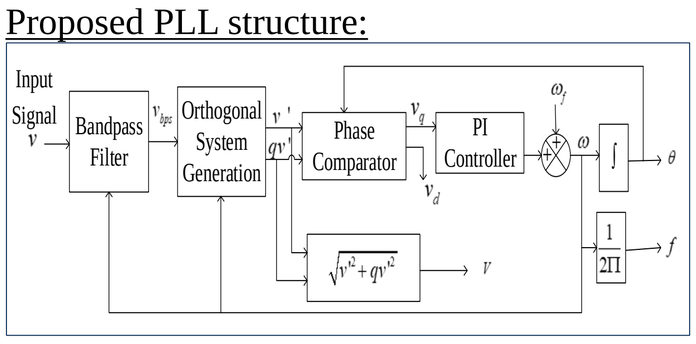


Fig.1. Basic structure of PLL

Proposed PLL structure:



- The proposed PLL offers a modified orthogonal system generation based on second order generalized integrator(SOGI) to generate - in phase component (v') & 90º shifted quadrature component (qv').

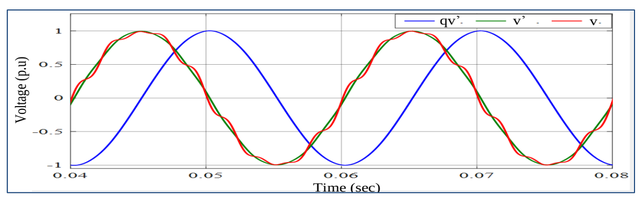


Fig.2. Input distorted signal and orthogonal signals

- For harmonics suppression a band pass filter is utilized [1].
- A phase comparator is used and only (qv') component is tuned through PI controller to achieve almost zero phase difference.

Methods and Structures

Step by step working procedure of the system-

❖ Removing harmonics from input voltage by BPF [1] $H(z)=\frac{v_{BPF}}{v}=\frac{1-\alpha}{2}\frac{1-z^{-2}}{1-\beta(1+\alpha)z^{-1}+\alpha z^{-2}}$

❖ Orthogonal component generation by SOGI[2]

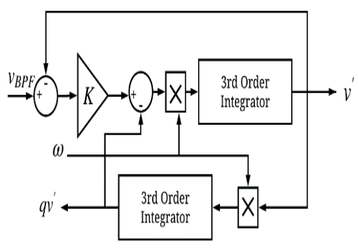


Fig.3. Second Order Generalized Integrator

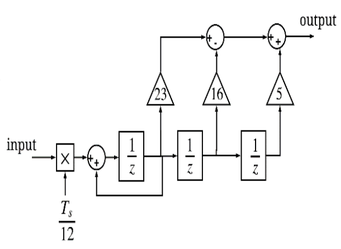


Fig.4. Third order integrator

❖ dq component generation by phase comparator[3]

❖ Tuning q component by PI controller[4]

❖ Output phase, frequency and voltage amplitude determination

➢ Transfer function of 3rd order integrator[2] is- $\frac{T_s}{12}\frac{23z^{-1}-16z^{-2}+5z^{-3}}{1-z^{-1}}$

➢ The output voltage is calculated using the formula as V= $\sqrt{v'^2+qv'^2}$

Simulation Results

The performances tested by Simulink-

❖ Steady state 50% DC offset and harmonics
❖ Frequency step and harmonics
❖ Frequency ramp and harmonics
❖ Voltage swell and harmonics
❖ Voltage sag and harmonics
❖ Noise and harmonics

Simulation Parameters	
Input voltage amplitude	1V
Input voltage type	Sine wave
Fundamental frequency	50Hz
Total harmonic distortion	10%

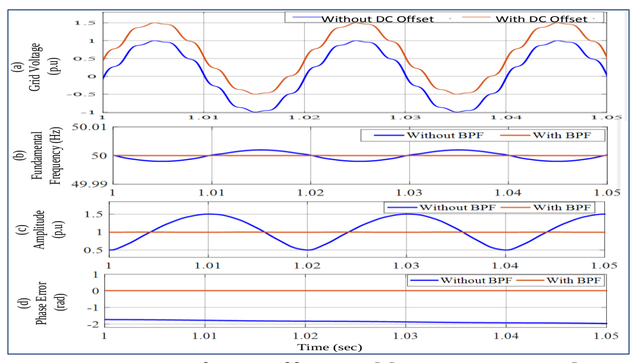


Fig.5. Output of DC offset and harmonics condition

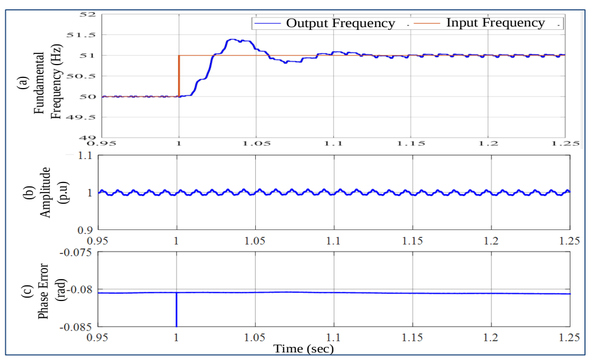


Fig.6. Output of Frequency step and harmonics

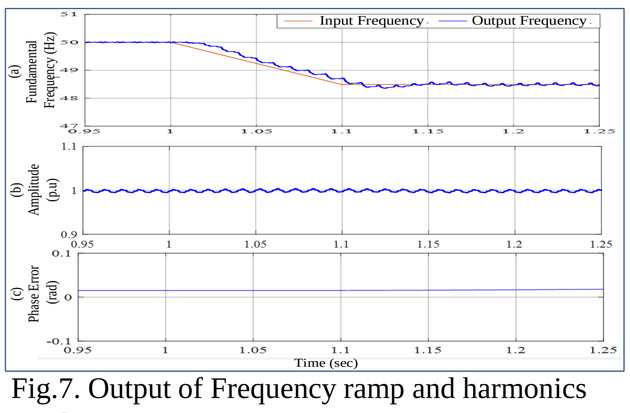


Fig.7. Output of Frequency ramp and harmonics condition

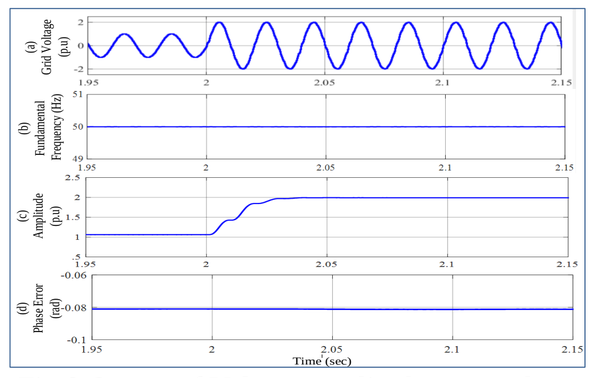


Fig.8.Output of Voltage amplitude step and harmonics condition

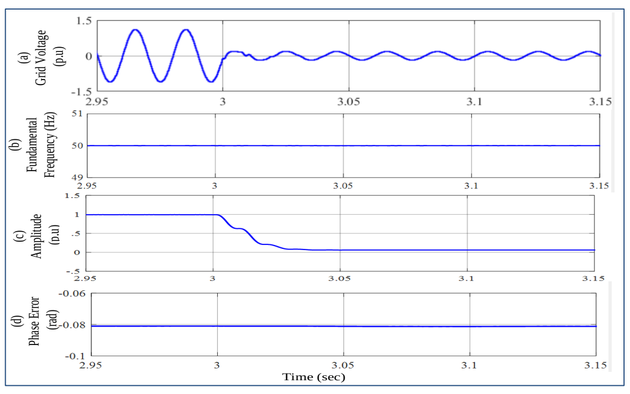


Fig.9.Output of Voltage sag and harmonics condition

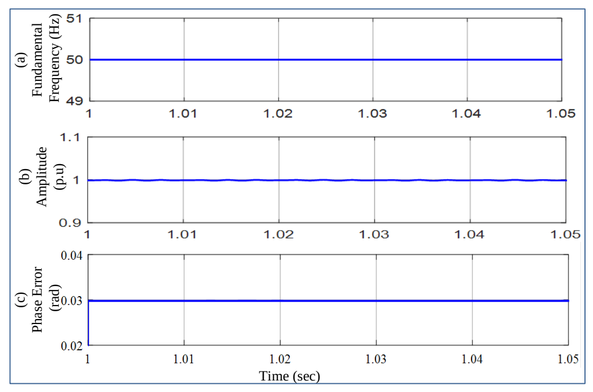
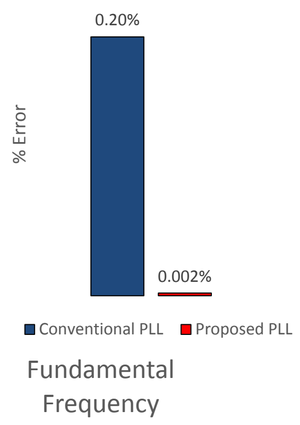


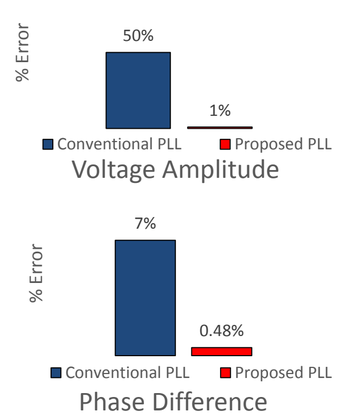
Fig.10. Noise and harmonics condition

Result Analysis

% Error comparison of conventional PLL and proposed PLL structure under 0.5 pu DC offset and harmonics conditions:

% of error under 0.5 pu DC offset and harmonics condition in-	Conventional PLL structure	Proposed PLL structure
Output frequency	0.2%	0.002%
Voltage amplitude	50%	1%
Phase difference	7%	0.48%





Future work

➢ The digital PLLs are constructed at the expense of high power consumption. Further works should be carried out to reduce the power consumption.
➢ More simplified integrator should be used to alleviate complicacy of the system.

Conclusion

❖ Though utilizing SOGI structure may introduce complexity to the basic PLL method but it can successfully suppress the DC offset.
❖ This PLL method provides better response to frequency ramp, amplitude step, voltage sag and so on.
❖ The proposed PLL structure is an improved version of conventional PLL structure.

Acknowledgements

Dr. Md. Shamim Reza
Associate Professor
Department of Electrical and Electronic Engineering
Bangladesh University of Engineering and Technology
Email: shamim_reza@eee.buet.ac.bd

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