Zahra Ebrahimi

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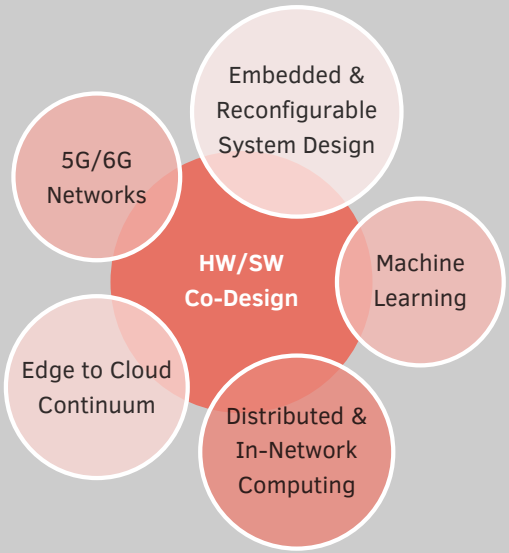
Cfaed-Processor Design

Google Scholar

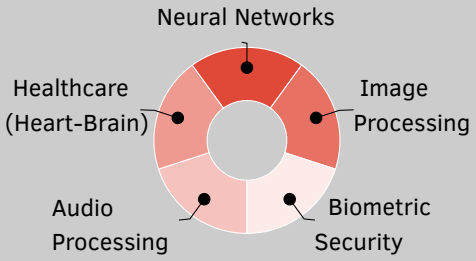
Linkedin

Github

Research Skills and Interest



Application Domain Expertise



Work Experience

Research Associate, Ruhr University Bochum (X-ReAp, DFG Grant). 2024–2026
Targeting sustainability, I optimize the energy-efficiency of emerging applications (including generative AI models). Targeting high-performance/real-time processing, I also design various optimization techniques for a HW/SW co-design approach.

AI Founder Researcher, Acatech (GREEN-DNN, BMVD Grant). Feb to Nov 2025
Performance- and energy-efficient deployment of AI models for distributed & in-network computing.

Project Manager, Cfaed, TU Dresden (X-DNet, BMBF Grant). 2022–2025
Industry project with **Huawei**: optimizing performance & energy-efficiency of 5G/6G applications (audio-processing, NNs) for distributed & in-network computing.

Research Associate, Cfaed, TU Dresden. 2018–2024
I worked on two projects: Re-Learning (ESF Grant) and ReAp (DFG Grant). I designed energy-efficient reconfigurable and self-adaptive accelerators for image processing, healthcare, and ML applications.

Research Assistant, DSN LAB, Sharif University of Technology. 2012–2018
I optimized the performance and energy of embedded processors and FPGAs, using various circuit- and architecture-level techniques.

Honors and Awards

◇ Winner of **€125.000 AI Founder Fellowship**, acatech (Mission KI Program) 2025
◇ **1st Place, AI programming Hackathon**, AI Grid Summer School 2024
◇ **2nd Place**, in Science Slam Pitching, AI Grid Contest 2024
◇ Winner of **€100.000 Grant**, BMBF (Software Campus Program) 2022
◇ **2nd Place**, TUD Imaging Science Contest, among 300+ images 2021
◇ **Ranked 17th** (top 0.002%) Among 11,000+ BSc. Students,
Annual Nationwide Universities Entrance Exam for Master of Science, Iran 2013
◇ Accepted in **National Mathematics Olympiad** for High School Students, Iran 2007

Education

◇ **PhD** in Computer Science, Cfaed, TU Dresden 2021–2025
. Thesis: "Design of Sustainable and High-Throughput Reconfigurable Systems Through Cross-Layer Approximation of Accelerators and Applications"

◇ **MSc** in Computer Science, Sharif University of Technology **(GPA: 1.4)** 2016
. Thesis: "A Power-Efficient Architecture for FPGAs Using Reconfigurable Hard Logic Design in Dark Silicon Era" **(Grade 1.0)**

◇ **BSc** in Computer Engineering, Sharif University of Technology 2013
. Thesis: "An Energy-Efficient Architecture for Reconfigurable Devices" **(Grade 1.0)**

◇ Abitur: Iran National Organization for Development of Exceptional Talents 2009

Certificates

◇ **Industry Workshops**: Entrepreneurship in AI (K.I.E.Z.), Innovation Management (Huawei), Effective Leadership Communication (ZEISS), Leading Diverse Teams and Promoting Potential (Volkswagen), Culture, sustainability and decision making (Huawei), Insights Discovery to Understand Yourself and Others (Merck KGaA), Strategic Workshop Facilitator (Software AG). Leadership competence (Holtzbrinck), Eco-Tech: Decoding IT's Impact on a Sustainable Future (iversity).

◇ **University & Academic Workshops**: Advanced Project Management with Digital Tools, Leadership/Supervision, Intercultural/Supportive Communication & Conflict Resolution, Professional Networking, Mental Health & Power Abuse in Academia, Negotiating Skill, Good Scientific Practice, Female Empowerment, Elevator Pitch.

Zahra Ebrahimi

Programming Languages

- C/C++ ●●●●●
- Python ●●●●○
- MATLAB ●●●●○
- Verilog/VHDL ●●●●○
- Bash Scripting ●●●○○

Software & Hardware Tools

Software

Visual Studio | MATLAB | Eclipse | PyTorch | TensorFlow | NumPy | Linux (Ubuntu, Red Hat, NixOs), macOS

Hardware

HSpice | Xilinx Vivado Design Suite | High Level Synthesis (Xilinx Vitis) | Synopsys Design Compiler | Xilinx ISE | Verilog to Routing (VTR) | Cadence Innovus | Altera Quartus | SoC Encounter | ModelSim | ABC Logic Synthesis, Formal Verification

Languages

- German (A2) ●●○○○
- English (TOEFL 98) ●●●●○
- Turkish ●●○○○
- Arabic ●●○○○
- Persian ●●●●●

References

Prof. Akash Kumar
@ Ruhr University Bochum
akash.kumar@rub.de

Patent, Book, and Publications

◇ **US Patent Invention**: *"Programmable Logic Design"*. 2017

◇ **Book Chapter**: *"Introduction to Emerging SRAM-based FPGA Architectures in Dark Silicon Era"*, Elsevier's Advances in Computers. 2018

◇ **Journal Papers**

- *"X-DINC: Energy Optimization for Distributed and In-Network AI Acceleration in 5G/6G Networks"*, submitted to Future Generation Computer Systems (FGCS).
- *"RAPID: Approximate Pipelined Soft Multipliers and Dividers for High Throughput and Energy Efficiency"*, IEEE TCAD. 2023
- *"Plasticine: Cross-layer Approximation Methodology for Multi-kernel Applications via High-throughput, Energy-efficient SIMD Multiplier-divider"*, ACM TODAES. 2022
- *"An Efficient SRAM-based Reconfigurable Architecture for Embedded Processors"*, IEEE TCAD. 2018
- *"PEAF: A Power-Efficient Architecture for SRAM-Based FPGAs Using Reconfigurable Hard Logic Design in Dark Silicon Era"*, IEEE TC. 2017

◇ **Conference Papers**

- *"BioCare: Energy-Efficient Bio-Signal Processing at Edge"*, IEEE ISCAS. 2021
- *"LeAp: Leading-one Detection-based Softcore Approximate Multipliers with Tunable Accuracy"*, ACM/IEEE ASP-DAC. 2020
- *"SIMDive: Approximate SIMD Soft Multiplier-Divider for FPGAs with Tunable Accuracy"*, ACM GLSVLSI. 2020
- *"Toward Dark Silicon Era in FPGAs via Hard Logic Design"*, IEEE FPL. 2014

Teaching & Supervision

◇ **PhD/Master Student, SHK/WHK Supervision**, 2019-25

- Maryam Eslami, PhD Thesis (5G/6G, Machine Learning)
- Dennis Klar, Master Project (Iris Recognition, Object Tracking)
- Yifan Yang, Master Thesis (Parallel Computing)
- Muhammad Zaid, WHK Student Job (NN-based Image Processing)
- Mohammad Aasim Ekhtiyar, Master Thesis (Heart Monitoring at Edge)

◇ **University Teaching Assistant**

Embedded Hardware Systems Design, Reconfigurable Computing, Advanced VLSI Design, Scientific and Technical Presentation, Digital Electronics, Digital System Design, Numerical Methods and Analysis, Signals and Systems.

Extra-Curricular Activities

◇ Elected as **AI Grid** member for participation in AI-related activities 2023–25

◇ **Professional Reviewer** in IEEE TCAD Journal 2024

◇ **Executive Assistant** in IEEE/CSI Conferences

. Computer Architecture and Digital Systems (CADS) 2015

. Real-Time and Embedded Systems and Technologies (RTEST) 2015

◇ Demonstration at Dresdner Lange Nacht der Wissenschaften, TU Dresden

. Accelerating Real-Time Object Tracking Application on Intel Board 2019