Microcontrôleurs & Applications
Watchdog Timer

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Sources de Réinitialisation

- 4 Sources de RESET sur le LPC23xx
  - **Power On Reset (POR)**
  - **External Reset (Broche Reset) (EXTR)**
  - **Watchdog Timer (WDTR)**
  - **Brown out Detection (BODR)**

Table 11. Reset Source Identification register (RSID - address 0xE01F C180) bit description

Bit	Symbol	Description	Reset value
0	POR	Assertion of the POR signal sets this bit, and clears all of the other bits in this register. But if another Reset signal (e.g., External Reset) remains asserted after the POR signal is negated, then its bit is set. This bit is not affected by any of the other sources of Reset.	See text
1	EXTR	Assertion of the $\overline{\text{RESET}}$ signal sets this bit. This bit is cleared by POR, but is not affected by WDT or BOD reset.	See text
2	WDTR	This bit is set when the Watchdog Timer times out and the WDTRESET bit in the Watchdog Mode Register is 1. It is cleared by any of the other sources of Reset.	See text
3	BODR	This bit is set when the 3.3 V power reaches a level below 2.6 V.	See text

Brown Out Detection

- Lorsque la tension d'alimentation descend en dessous de 2,95V, une interruption Brown Out est déclenchée par le circuit de détection

- Lorsque la tension d'alimentation descend en dessous de 2,65V, un reset Brown Out est déclenché par le circuit de détection pour éviter des erreurs de lecture mémoire et protéger la mémoire flash

WatchDog Timer

- But:
  - **Provoquer un reset du µC après un certain délai lorsqu'une erreur irrécupérable s'est produite**

- Fonctionnement:
  - **Timer chargé à une valeur initiale**
  - **Décrémentation périodique**
  - **Provoque un Reset système lorsque sa valeur passe en dessous de 0**

Registres du WatchDog Timer

Table 436. Watchdog register map

Name	Description	Access	Reset Value[1]	Address
WDMOD	Watchdog mode register. This register contains the basic mode and status of the Watchdog Timer.	R/W	0	0xE000 0000
WDTC	Watchdog timer constant register. This register determines the time-out value.	R/W	0xFF	0xE000 0004
WDFEED	Watchdog feed sequence register. Writing 0xAA followed by 0x55 to this register reloads the Watchdog timer with the value contained in WDTC.	WO	NA	0xE000 0008
WDTV	Watchdog timer value register. This register reads out the current value of the Watchdog timer.	RO	0xFF	0xE000 000C
WDCLKSEL	Watchdog clock source selection register.	R/W	0	0xE000 0010

Registre WDMOD

- Registre WatchDog MODe

Table 438: Watchdog Mode register (WDMOD - address 0xE000 0000) bit description

Bit	Symbol	Description	Reset Value
0	WDEN	WDEN Watchdog interrupt enable bit (Set Only).	0
1	WDRESET	WDRESET Watchdog reset enable bit (Set Only).	0
2	WDTOF	WDTOF Watchdog time-out flag.	0 (Only after external reset)
3	WDINT	WDINT Watchdog interrupt flag (Read Only).	0
7:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

- Les bits WDEN et WDRESET ne peuvent pas être remis à 0 de façon logicielle
  - **Il faut passer par un reset externe ou un reset provoqué par le Watchdog Timer**

Registre WDMOD

- Registre WatchDog MODe

Table 438: Watchdog Mode register (WDMOD - address 0xE000 0000) bit description

Bit	Symbol	Description	Reset Value
0	WDEN	WDEN Watchdog interrupt enable bit (Set Only).	0
1	WDRESET	WDRESET Watchdog reset enable bit (Set Only).	0
2	WDTOF	WDTOF Watchdog time-out flag.	0 (Only after external reset)
3	WDINT	WDINT Watchdog interrupt flag (Read Only).	0
7:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

- Le drapeau WDTOF doit être remis à 0 de façon logicielle
- Le drapeau WDINT est remis à 0 de façon matérielle

Registre WDMOD

- Modes de fonctionnement

Table 437. Watchdog operating modes selection

WDEN	WDRESET	Mode of Operation
0	X (0 or 1)	Debug/Operate without the Watchdog running.
1	0	Watchdog interrupt mode: debug with the Watchdog interrupt but no WDRESET enabled. When this mode is selected, a watchdog counter underflow will set the WDINT flag and the Watchdog interrupt request will be generated.
1	1	Watchdog reset mode: operate with the Watchdog interrupt and WDRESET enabled. When this mode is selected, a watchdog counter underflow will reset the microcontroller. Although the Watchdog interrupt is also enabled in this case (WDEN = 1) it will not be recognized since the watchdog reset will clear the WDINT flag.

Registre WDTC

- Registre WatchDog Timer Constant
  - **Valeur de réinitialisation du WatchDog**

Table 439: Watchdog Constant register (WDTC - address 0xE000 0004) bit description

Bit	Symbol	Description	Reset Value
31:0	Count	Watchdog time-out interval.	0x0000 00FF

Registre WDFEED

- Registre WatchDog Feed
  - Registre de commande du WatchDog Timer
    - Démarrage
    - Réinitialisation

Table 440: Watchdog Feed Register (WDFEED - address 0xE000 0008) bit description

Bit	Symbol	Description	Reset Value
7:0	Feed	Feed value should be 0xAA followed by 0x55.	NA

Registre WDFEED

- Registre WatchDog Feed
  - Registre de commande du WatchDog Timer
    - Démarrage

Table 440: Watchdog Feed Register (WDFEED - address 0xE000 0008) bit description

Bit	Symbol	Description	Reset Value
7:0	Feed	Feed value should be 0xAA followed by 0x55.	NA

  - Si le WatchDog est à l'arrêt
  - Si WDEN est à 1
  - L'écriture successive de 0xAA puis 0x55 dans WDFEED démarre le WatchDog

Registre WDFEED

- Registre WatchDog Feed
  - Registre de commande du WatchDog Timer
    - Réinitialisation

Table 440: Watchdog Feed Register (WDFEED - address 0xE000 0008) bit description

Bit	Symbol	Description	Reset Value
7:0	Feed	Feed value should be 0xAA followed by 0x55.	NA

  - Si le WatchDog est en marche
  - L'écriture successive de 0xAA puis 0x55 dans WDFEED réinitialise le WatchDog à la valeur de WDTC

Registre WDFEED

- Registre WatchDog Feed
  - Registre de commande du WatchDog Timer
    - Réinitialisation

Table 440: Watchdog Feed Register (WDFEED - address 0xE000 0008) bit description

Bit	Symbol	Description	Reset Value
7:0	Feed	Feed value should be 0xAA followed by 0x55.	NA

  - L'écriture de 0xAA puis d'une valeur AUTRE que 0x55 provoque un reset

Registre WDCLKSEL

- Registre Sélection de l'Horloge

Table 442: Watchdog Timer Clock Source Selection register (WDCLKSEL - address 0xE000 0010) bit description

Bit	Symbol	Value	Description	Reset Value
1:0	WDSEL		These bits select the clock source for the Watchdog timer as described below. **Warning:** Improper setting of this value may result in incorrect operation of the Watchdog timer, which could adversely affect system operation.	0
		00	Selects the Internal RC oscillator as the Watchdog clock source (default).	
		01	Selects the APB peripheral clock (PCLK) as the Watchdog clock source.	
		10	Selects the RTC oscillator as the Watchdog clock source.	
		11	Reserved	
31:2	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Période du WatchDog Timer

- Formule Générale
  - $T_{WDCLK} \times WDTC \times 4$
  - Par défaut, WDTC ≥ 0xFF
    - $T_{WDCLK} \times 256 \times 4$
    - $T_{WDCLK} \times 2^{32} \times 4$
  - Si WDCLKSEL = 01 avec F(CCLK)=12 MHz
  - Quel est le temps d'attente?

Exemple

- Fonction INIT du WDTimer
- Fonction FEED du WDTimer
- Fonction Interruption

Exemple

- Fonction INIT du WDTimer

```
void WDTInit( void )
{
  wdt_counter = 0;

  WDTC = WDT_FEED_VALUE;

// WDMOD = WDEN | WDRESET; // Mode Reset
  WDMOD = WDEN;           // Mode Interrupt

  WDFEED = 0xAA;          /* Feeding sequence */
  WDFEED = 0x55;
}
```

Exemple

- Fonction FEED du WDTimer

```
void WDTFeed( void )
{
  WDFEED = 0xAA;              /* Feeding sequence */
  WDFEED = 0x55;
}
```

Fonction Interruption du WDTimer

```
void WDTHandler(void) __irq
{
  WDMOD &= ~WDTOF;  /* clear the time-out flag */

   wdt_counter++;
   VICVectAddr = 0;  /* Acknowledge Interrupt */
}
```

Exemple

- Fonction main()

```
int main (void)
{
   WDTInit(); VICIntEnable=1; VICVectAddr0=...;

   while( 1 )
   {
      // Do Task…
      WDTFeed();      /* Feed the watchdog timer */
    }
   }
   return 0;
}
```