Microcontrôleurs & Applications
Power Management

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Systèmes Electroniques Actuels

- Systèmes complexes
  - **Multiplicité des fonctionnalités**
  - **Systèmes embarqués**
    - Alimentation sur batterie / pile
    - Green Electronics / Green Computing
- La consommation devient un enjeu de plus en plus important
- C'est un critère de performance pour bon nombre de systèmes et d'applications

Consommation

- L'estimation, la réduction, l'optimisation de la consommation est actuellement une problématique majeure du monde de l'électronique

- La réduction de la consommation permet de:
  - **Prolonger la durée de vie des batteries**
  - **Baisser la température du système**
  - **Limiter ou éviter l'utilisation de techniques de refroidissement**
  - **Supprimer l'électronique gérant les systèmes de refroidissement**

Consommation

- Il y a deux types de consommation d'énergie
  - **Consommation statique**
  - **Consommation dynamique**
    - En CMOS: correspond aux transistors qui changent d'état
    - $P \approx C \cdot V^2 \cdot f$
      - C: capacité totale des transistors en commutation
      - V: Tension d'alimentation
      - F: Fréquence de fonctionnement
- La réduction de la consommation peut être envisagée au niveau:
  - **Technologique**
  - **Circuit**
  - **Système**

Réduction de la Consommation

- $P \approx C \cdot V^2 \cdot f$

- Dynamic Voltage Scaling
  - **Réduction de la tension d'alimentation**
  - **Allongement des temps de commutation des transistors du circuit**
  - **Diminution de la fréquence de fonctionnement**
  - **Réduction de la puissance consommée**

Réduction de la Consommation

- $P \approx C \cdot V^2 \cdot f$
- Dynamic Frequency Scaling
  - **Réduction de la fréquence de fonctionnement**
  - **Réduction de la puissance consommée**
- Dynamic Frequency & Voltage Scaling sont utilisés conjointement pour optimiser la consommation d'un système en fonction de la charge de traitement qu'il a à exécuter

Dynamic Power Management

- Pour un processeur:
  - **Consiste à ralentir**
    - En contrôlant la tension ou la fréquence
  - **ou arrêter**
    - De façon permanente ou temporaire
  - **Le cœur**
  - **Et/ou les périphériques**

DPM et LPC2378

- 4 modes de consommation
  - **Normal**
  - **Idle**
  - **Sleep**
  - **Power Down**

- Activité des périphériques
  - **Possibilité d'activer ou désactiver les périphériques**

Mode IDLE

- Mode VEILLE

- Arrêt de l'horloge du cœur du processeur
  - **Le contenu de la mémoire et des registres est conservé**

- Les périphériques restent actifs
  - **Une interruption permet de réveiller le cœur**
  - **Les interruptions doivent être autorisées avant de rentrer dans ce mode**

Mode SLEEP

- Mode SOMMEIL
- Les horloges du cœur et des périphériques sont désactivés
  - **Le contenu de la RAM est conservé**
  - **Mémoire FLASH activée**
- Un Reset ou une interruption ne nécessitant pas d'horloge permet de sortir de ce mode

Mode POWER DOWN

- Mode ARRET

- Les horloges du cœur et des périphériques sont désactivés
  - **Le contenu de la RAM est conservé**
  - **La Flash est désactivée**

- Une interruption spécifiée à l'avance permet de sortir de ce mode

Registre PCON

- Contrôle de la Consommation

Bit	Symbol	Description	Reset value
0	PM0 (IDL)	Power mode control bit 0. See text and table below for details.	0
1	PM1 (PD)	Power mode control bit 1. See text and table below for details.	0
2	BODPDM	Brown-Out Power Down Mode. When BODPDM is 1, the Brown-Out Detect circuitry will turn off when chip Power Down mode is entered, resulting in a further reduction in power usage. However, the possibility of using Brown-Out Detect as a wakeup source from Power Down mode will be lost. When 0, the Brown-Out Detect function remains active during Power Down mode. See the System Control Block chapter for details of Brown-Out detection.	0
3	BOGD	Brown-Out Global Disable. When BOGD is 1, the Brown-Out Detect circuitry is fully disabled at all times, and does not consume power. When 0, the Brown-Out Detect circuitry is enabled. See the System Control Block chapter for details of Brown-Out detection.	0

Registre PCON

- Contrôle de la Consommation

4	BORD	Brown-Out Reset Disable. When BORD is 1, the second stage of low voltage detection (2.6 V) will not cause a chip reset. When BORD is 0, the reset is enabled. The first stage of low voltage detection (2.9 V) Brown-Out interrupt is not affected. See the System Control Block chapter for details of Brown-Out detection.	0
6:3	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
7	PM2	Power mode control bit 2. See text and table below for details.	0

Sélection du mode

Table 41. Encoding of reduced power modes

PM2, PM1, PM0	Description
000	Normal operation
001	Idle mode. Causes the processor clock to be stopped, while on-chip peripherals remain active. Any enabled interrupt from a peripheral or an external interrupt source will cause the processor to resume execution. See text for details.
101	Sleep mode. This mode is similar to Power Down mode (the oscillator and all on-chip clocks are stopped), but the Flash memory is left in Standby mode. This allows a more rapid wakeup than Power Down mode because the Flash reference voltage regulator start-up time is not needed. See text for details.
010	Power Down mode. Causes the oscillator and all on-chip clocks to be stopped. A wakeup condition from an external interrupt can cause the oscillator to re-start, the PD bit to be cleared, and the processor to resume execution. See text for details.
110	Reserved.
Others	Reserved, not currently used.

Réveil du Processeur

- En mode POWER DOWN
  - **Registre INTWAKE**
    - Réveil par EINT, GPIO, CAN, etc…
      - Périphériques accédant aux broches d'E/S

Table 42. Interrupt Wakeup register (INTWAKE - address 0xE01F C144) bit description

Bit	Symbol	Description	Reset value
0	EXTWAKE0	When one, assertion of $\overline{\text{EINT0}}$ will wake up the processor from Power Down mode.	0
1	EXTWAKE1	When one, assertion of $\overline{\text{EINT1}}$ will wake up the processor from Power Down mode.	0
2	EXTWAKE2	When one, assertion of $\overline{\text{EINT2}}$ will wake up the processor from Power Down mode.	0
3	EXTWAKE3	When one, assertion of $\overline{\text{EINT3}}$ will wake up the processor from Power Down mode.	0

- Réveillent le processeur si la fonction est validée

Registre INTWAKE (suite)

Bit	Symbol	Description	Reset value
4	ETHWAKE	When one, assertion of the Wake-up on LAN interrupt (WakeupInt) of the Ethernet block will wake up the processor from Power Down mode.	0
5	USBWAKE	When one, activity on the USB bus will wake up the processor from Power Down mode. Any change of state on the USB data pins will cause a wakeup when this bit is set. For details on the relationship of USB to Power Down Mode and wakeup, see the relevant USB chapter(s).	0
6	CANWAKE	When one, activity of the CAN bus will wake up the processor from Power Down mode. Any change of state on the CAN receive pins will cause a wakeup when this bit is set.	0
7	GPIOWAKE	When one, specified activity on GPIO pins enabled for wakeup will wake up the processor from Power Down mode. See the GPIO chapter for details.	0
13:8	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
14	BODWAKE	When one, Brown-Out Detect interrupt will wake up the processor from Power Down mode. **Note:** since there is a delay before execution begins, there is no guarantee that execution will resume before $V_{DD(3V3)}$ has fallen below the lower BOD threshold, which prevents execution. If execution does resume, there is no guarantee of how long the processor will continue execution before the lower BOD threshold terminates execution. These issues depend on the slope of the decline of $V_{DD(3V3)}$. High decoupling capacitance (between $V_{DD(3V3)}$ and ground) in the vicinity of the LPC2300 will improve the likelihood that software will be able to do what needs to be done when power is in the process of being lost.	0
15	RTCWAKE	When one, assertion of an RTC interrupt will wake up the processor from Power Down mode.	0

Activation des Périphériques

- Registre PCONP
  - Permet d'activer/désactiver les horloges des périphériques du microcontrôleur
  - A l'initialisation, certains périphériques sont activés
    - GPIO
    - EINT
    - Timer0,1)
  - D'autres ne le sont pas
    - Timer 2,3
    - ADC
    - CAN

Activation des Périphériques

- Registre PCONP
  - Pour activer un périphérique
    - Il faut écrire 1 sur le bit correspondant de PCONP
  - Pour désactiver un périphérique
    - Il faut écrire 0 sur le bit correspondant de PCONP
  - Si un périphérique est désactivé, les opérations de lecture/écriture sur les registres de ce périphérique n'ont aucun effet
  - Si un périphérique n'est pas activé
    - Il ne consomme pas
    - Optimisation de la consommation

Registre PCONP

Table 43. Power Control for Peripherals register (PCONP - address 0xE01F C0C4) bit description

Bit	Symbol	Description	Reset value
0	-	Unused, always 0.	0
1	PCTIM0	Timer/Counter 0 power/clock control bit.	1
2	PCTIM1	Timer/Counter 1 power/clock control bit.	1
3	PCUART0	UART0 power/clock control bit.	1
4	PCUART1	UART1 power/clock control bit.	1
5	-	Unused, always 0.	1
6	PCPWM1	PWM1power/clock control bit.	1
7	PCI2C0	The I^2C0 interface power/clock control bit.	1
8	PCSPI	The SPI interface power/clock control bit.	1
9	PCRTC	The RTC power/clock control bit.	1
10	PCSSP1	The SSP 1 interface power/clock control bit.	1
11	PCEMC	External Memory Controller	1
12	PCAD	A/D converter (ADC) power/clock control bit. **Note:** Clear the PDN bit in the AD0CR before clearing this bit, and set this bit before setting PDN.	0
13	PCAN1	CAN Controller 1 power/clock control bit.	0
14	PCAN2	CAN Controller 2 power/clock control bit.	0

Registre PCONP

19	PCI2C1	The I^2C1 interface power/clock control bit.	1
20	-	Unused, always 0	0
21	PCSSP0	The SSP0 interface power/clock control bit.	1
22	PCTIM2	Timer 2 power/clock control bit.	0
23	PCTIM3	Timer 3 power/clock control bit.	0
24	PCUART2	UART 2 power/clock control bit.	0
25	PCUART3	UART 3 power/clock control bit.	0
26	PCI2C2	I^2S interface 2 power/clock control bit.	1
27	PCI2S	I^2S interface power/clock control bit.	0
28	PCSDC	SD card interface power/clock control bit.	0
29	PCGPDMA	GP DMA function power/clock control bit.	0
30	PCENET	Ethernet block power/clock control bit.	0
31	PCUSB	USB interface power/clock control bit.	0

Horloges Cœur et Périphériques

- Horloge Cœur: CCLK
- Horloge Périphérique PCLK
  - Il est possible de configurer le rapport entre PCLK et CCLK pour chaque périphérique
  - Registres PCLKSEL0 et PCLKSEL1

Table 38. Peripheral Clock Selection register bit values

PCLKSEL0 and PCLKSEL1 individual peripheral's clock select options	Function	Reset value
00	PCLK_xyz = CCLK/4	00
01	PCLK_xyz = CCLK[1]	
10	PCLK_xyz = CCLK/2	
11	Peripheral's clock is selected to PCLK_xyz = HCLK/8 except for CAN1, CAN2, and CAN filtering when '11' selects PCLK_xyz = HCLK/6.	

Horloges Cœur et Périphériques

Table 36. Peripheral Clock Selection register 0 (PCLKSEL0 - address 0xE01F C1A8) bit description

Bit	Symbol	Description	Reset value
1:0	PCLK_WDT	Peripheral clock selection for WDT.	00
3:2	PCLK_TIMER0	Peripheral clock selection for TIMER0.	00
5:4	PCLK_TIMER1	Peripheral clock selection for TIMER1.	00
7:6	PCLK_UART0	Peripheral clock selection for UART0.	00
9:8	PCLK_UART1	Peripheral clock selection for UART1.	00
11:10	-	Unused, always read as 0.	00
13:12	PCLK_PWM1	Peripheral clock selection for PWM1.	00
15:14	PCLK_I2C0	Peripheral clock selection for I2C0.	00
17:16	PCLK_SPI	Peripheral clock selection for SPI.	00
19:18	PCLK_RTC[1]	Peripheral clock selection for RTC.	00
21:20	PCLK_SSP1	Peripheral clock selection for SSP1.	00
23:22	PCLK_DAC	Peripheral clock selection for DAC.	00
25:24	PCLK_ADC	Peripheral clock selection for ADC.	00
27:26	PCLK_CAN1	Peripheral clock selection for CAN1.	00
29:28	PCLK_CAN2	Peripheral clock selection for CAN2.	00
31:30	PCLK_ACF	Peripheral clock selection for CAN filtering.	00

Horloges Cœur et Périphériques

Table 37. Peripheral Clock Selection register 1 (PCLKSEL1 - address 0xE01F C1AC) bit description

Bit	Symbol	Description	Reset value
1:0	PCLK_BAT_RAM	Peripheral clock selection for the battery supported RAM.	00
3:2	PCLK_GPIO	Peripheral clock selection for GPIOs.	00
5:4	PCLK_PCB	Peripheral clock selection for the Pin Connect block.	00
7:6	PCLK_I2C1	Peripheral clock selection for I2C1.	00
9:8	-	Unused, always read as 0.	00
11:10	PCLK_SSP0	Peripheral clock selection for SSP0.	00
13:12	PCLK_TIMER2	Peripheral clock selection for TIMER2.	00
15:14	PCLK_TIMER3	Peripheral clock selection for TIMER3.	00
17:16	PCLK_UART2	Peripheral clock selection for UART2.	00
19:18	PCLK_UART3	Peripheral clock selection for UART3.	00
21:20	PCLK_I2C2	Peripheral clock selection for I2C2.	00
23:22	PCLK_I2S	Peripheral clock selection for I2S.	00
25:24	PCLK_MCI	Peripheral clock selection for MCI.	00
27:26	-	Unused, always read as 0.	00
29:28	PCLK_SYSCON	Peripheral clock selection for the System Control block.	00
31:30	-	Unused, always read as 0.	00

Horloges Cœur et Périphériques

- Courant d'alimentation Icc, Vcc = 3,3 V, T = 25°C
- Mode Actif :
  - **Aucun périphérique actif**
    - Icc typ @ CCLK = 10 MHz : 15 mA
    - Icc typ @ CCLK = 72 MHz : 63 mA
  - **Tous périphériques actifs, PCLK = CCLK / 8**
    - Icc typ @ CCLK = 10 MHz : 21 mA
    - Icc typ @ CCLK = 72 MHz : 92 mA
  - **Tous périphériques actifs, PCLK = CCLK**
    - ! Icc typ @ CCLK = 10 MHz : 27 mA
    - ! Icc typ @ CCLK = 72 MHz : 125 mA
- Mode Power-down :
  - **Ipd typ = 150 µA**
- Sauvegarde batterie :
  - **Ipd max = 20 µA**

Source: Philips, LPC2378 Data Sheet, Rev 02, 27 Mars 2007

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