– if the EMC_Reset_Disable = 1 (see Section 3–7 “Other system controls and status flags”), they retain their values for external memory interface
– else if the EMC_Reset_Disable = 0, they are reset to '0'.

6.1 Pin Function Select register 0 (PINSEL0 - 0xE002 C000)

The PINSEL0 register controls the functions of the pins as per the settings listed in Table 9–84. The direction control bit in the IO0DIR register (or the FIO0DIR register if the enhanced GPIO function is selected for port 0) is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically.

Table 84. Pin function select register 0 (PINSEL0 - address 0xE002 C000) bit description

PINSEL0	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P0.0	GPIO Port 0.0	RD1	TXD3	SDA1	00
3:2	P0.1	GPIO Port 0.1	TD1	RXD3	SCL1	00
5:4	P0.2	GPIO Port 0.2	TXD0	Reserved	Reserved	00
7:6	P0.3	GPIO Port 0.3	RXD0	Reserved	Reserved	00
9:8	P0.4	GPIO Port 0.4	I2SRX_CLK	RD2	CAP2.0	00
11:10	P0.5	GPIO Port 0.5	I2SRX_WS	TD2	CAP2.1	00
13:12	P0.6	GPIO Port 0.6	I2SRX_SDA	SSEL1	MAT2.0	00
15:14	P0.7	GPIO Port 0.7	I2STX_CLK	SCK1	MAT2.1	00
17:16	P0.8	GPIO Port 0.8	I2STX_WS	MISO1	MAT2.2	00
19:18	P0.9	GPIO Port 0.9	I2STX_SDA	MOSI1	MAT2.3	00
21:20	P0.10	GPIO Port 0.10	TXD2	SDA2	MAT3.0	00
23:22	P0.11	GPIO Port 0.11	RXD2	SCL2	MAT3.1	00
25:24[1]	P0.12	GPIO Port 0.12	Reserved	MISO1	AD0.6	00
27:26[1]	P0.13	GPIO Port 0.13	$\overline{\text{U2UP\_LED}}$	MOSI1	AD0.7	00
29:28[1]	P0.14	GPIO Port 0.14	$\overline{\text{U2CONNECT}}$	Reserved	SSEL1	00
31:30	P0.15	GPIO Port 0.15	TXD1	SCK0	SCK	00

[1] LPC2378 only. These bits are reserved for LPC2364/66/68.

6.2 Pin Function Select Register 1 (PINSEL1 - 0xE002 C004)

The PINSEL1 register controls the functions of the pins as per the settings listed in Table 9–85. The direction control bit in the IO0DIR (or the FIO0DIR register if the enhanced GPIO function is selected for port 0) register is effective only when the GPIO function is selected for a pin. For other functions direction is controlled automatically.

Table 85. Pin function select register 1 (PINSEL1 - address 0xE002 C004) bit description

PINSEL1	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P0.16	GPIO Port 0.16	RXD1	SSEL0	SSEL	00
3:2	P0.17	GPIO Port 0.17	CTS1	MISO0	MISO	00
5:4	P0.18	GPIO Port 0.18	DCD1	MOSI0	MOSI	00
7:6	P0.19	GPIO Port 0.19	DSR1	MCICLK	SDA1	00
9:8	P0.20	GPIO Port 0.20	DTR1	MCICMD	SCL1	00

Table 85. Pin function select register 1 (PINSEL1 - address 0xE002 C004) bit description

PINSEL1	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
11:10	P0.21	GPIO Port 0.21	RI1	MCIPWR	RD1	00
13:12	P0.22	GPIO Port 0.22	RTS1	MCIDAT0	TD1	00
15:14	P0.23	GPIO Port 0.23	AD0.0	I2SRX_CLK	CAP3.0	00
17:16	P0.24	GPIO Port 0.24	AD0.1	I2SRX_WS	CAP3.1	00
19:18	P0.25	GPIO Port 0.25	AD0.2	I2SRX_SDA	TXD3	00
21:20	P0.26	GPIO Port 0.26	AD0.3	AOUT	RXD3	00
23:22	P0.27	GPIO Port 0.27	SDA0	Reserved	Reserved	00
25:24	P0.28	GPIO Port 0.28	SCL0	Reserved	Reserved	00
27:26	P0.29	GPIO Port 0.29	U1D+	Reserved	Reserved	00
29:28	P0.30	GPIO Port 0.30	U1D−	Reserved	Reserved	00
31:30[1]	P0.31	GPIO Port 0.31	U2D+	Reserved	Reserved	00

[1] LPC2378 only. These bits are reserved for LPC2364/66/68.

6.3 Pin Function Select register 2 (PINSEL2 - 0xE002 C008)

The PINSEL2 register controls the functions of the pins as per the settings listed in Table 9–86. The direction control bit in the IO1DIR register (or the FIO1DIR register if the enhanced GPIO function is selected for port 1) is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically.

Table 86. Pin function select register 2 (PINSEL2 - address 0xE002 C008) bit description

PINSEL2	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P1.0	GPIO Port 1.0	ENET_TXD0	Reserved	Reserved	00
3:2	P1.1	GPIO Port 1.1	ENET_TXD1	Reserved	Reserved	00
5:4	P1.2	Reserved	Reserved	Reserved	Reserved	00
7:6	P1.3	Reserved	Reserved	Reserved	Reserved	00
9:8	P1.4	GPIO Port 1.4	ENET_TX_EN	Reserved	Reserved	00
11:10	P1.5	Reserved	Reserved	Reserved	Reserved	00
13:12	P1.6	Reserved	Reserved	Reserved	Reserved	00
15:14	P1.7	Reserved	Reserved	Reserved	Reserved	00
17:16	P1.8	GPIO Port 1.8	ENET_CRS	Reserved	Reserved	00
19:18	P1.9	GPIO Port 1.9	ENET_RXD0	Reserved	Reserved	00
21:20	P1.10	GPIO Port 1.10	ENET_RXD1	Reserved	Reserved	00
23:22	P1.11	Reserved	Reserved	Reserved	Reserved	00
25:24	P1.12	Reserved	Reserved	Reserved	Reserved	00
27:26	P1.13	Reserved	Reserved	Reserved	Reserved	00
29:28	P1.14	GPIO Port 1.14	ENET_RX_ER	Reserved	Reserved	00
31:30	P1.15	GPIO Port 1.15	ENET_REF_CLK	Reserved	Reserved	00

6.4 Pin Function Select Register 3 (PINSEL3 - 0xE002 C00C)

The PINSEL3 register controls the functions of the pins as per the settings listed in Table 9–87. The direction control bit in the IO1DIR register (or the FIO1DIR register if the enhanced GPIO function is selected for port 1) is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically.

Table 87. Pin function select register 3 (PINSEL3 - address 0xE002 C00C) bit description

PINSEL3	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P1.16	GPIO Port 1.16	ENET_MDC	Reserved	Reserved	00
3:2	P1.17	GPIO Port 1.17	ENET_MDIO	Reserved	Reserved	00
5:4	P1.18	GPIO Port 1.18	$\overline{\text{U1UP\_LED}}$	PWM1.1	CAP1.0	00
7:6	P1.19	GPIO Port 1.19	Reserved	Reserved	CAP1.1	00
9:8	P1.20	GPIO Port 1.20	Reserved	PWM1.2	SCK0	00
11:10	P1.21	GPIO Port 1.21	Reserved	PWM1.3	SSEL0	00
13:12	P1.22	GPIO Port 1.22	Reserved	Reserved	MAT1.0	00
15:14	P1.23	GPIO Port 1.23	Reserved	PWM1.4	MISO0	00
17:16	P1.24	GPIO Port 1.24	Reserved	PWM1.5	MOSI0	00
19:18	P1.25	GPIO Port 1.25	Reserved	Reserved	MAT1.1	00
21:20	P1.26	GPIO Port 1.26	Reserved	PWM1.6	CAP0.0	00
23:22	P1.27	GPIO Port 1.27	Reserved	Reserved	CAP0.1	00
25:24	P1.28	GPIO Port 1.28	Reserved	PCAP1.0	MAT0.0	00
27:26	P1.29	GPIO Port 1.29	Reserved	PCAP1.1	MAT0.1	00
29:28	P1.30	GPIO Port 1.30	Reserved	V_{BUS}	AD0.4	00
31:30	P1.31	GPIO Port 1.31	Reserved	SCK1	AD0.5	00

6.5 Pin Function Select Register 4 (PINSEL4 - 0xE002 C010)

The PINSEL4 register controls the functions of the pins as per the settings listed in Table 9–88. The direction control bit in the FIO2DIR register is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically.

Table 88. Pin function select register 4 (PINSEL4 - address 0xE002 C010) bit description

PINSEL4	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P2.0	GPIO Port 2.0	PWM1.1	TXD1	TRACECLK[1]	00
3:2	P2.1	GPIO Port 2.1	PWM1.2	RXD1	PIPESTAT0[1]	00
5:4	P2.2	GPIO Port 2.2	PWM1.3	CTS1	PIPESTAT1[1]	00
7:6	P2.3	GPIO Port 2.3	PWM1.4	DCD1	PIPESTAT2[1]	00
9:8	P2.4	GPIO Port 2.4	PWM1.5	DSR1	TRACESYNC[1]	00
11:10	P2.5	GPIO Port 2.5	PWM1.6	DTR1	TRACEPKT0[1]	00
13:12	P2.6	GPIO Port 2.6	PCAP1.0	RI1	TRACEPKT1[1]	00
15:14	P2.7	GPIO Port 2.7	RD2	RTS1	TRACEPKT2[1]	00
17:16	P2.8	GPIO Port 2.8	TD2	TXD2	TRACEPKT3[1]	00
19:18	P2.9	GPIO Port 2.9	$\overline{\text{U1CONNECT}}$	RXD2	EXTIN0[1]	00

Table 88. Pin function select register 4 (PINSEL4 - address 0xE002 C010) bit description

PINSEL4	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
21:20	P2.10	GPIO Port 2.10	$\overline{\text{EINT0}}$	Reserved	Reserved	00
23:22	P2.11	GPIO Port 2.11	$\overline{\text{EINT1}}$	MCIDAT1	I2STX_CLK	00
25:24	P2.12	GPIO Port 2.12	$\overline{\text{EINT2}}$	MCIDAT2	I2STX_WS	00
27:26	P2.13	GPIO Port 2.13	$\overline{\text{EINT3}}$	MCIDAT3	I2STX_SDA	00
29:28	P2.14	Reserved	Reserved	Reserved	Reserved	00
31:30	P2.15	Reserved	Reserved	Reserved	Reserved	00

[1] See Section 9–6.11 “Pin Function Select Register 10 (PINSEL10 - 0xE002 C028)”for details on using the ETM functionality.

6.6 Pin Function Select Register 5 (PINSEL5 - 0xE002 C014)

The PINSEL5 register controls the functions of the pins as per the settings listed in Table 9–89. The direction control bit in the FIO2DIR register is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically.

Table 89. Pin function select register 5 (PINSEL5 - address 0xE002 C014) bit description

PINSEL5	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P2.16	Reserved	Reserved	Reserved	Reserved	00
3:2	P2.17	Reserved	Reserved	Reserved	Reserved	00
5:4	P2.18	Reserved	Reserved	Reserved	Reserved	00
7:6	P2.19	Reserved	Reserved	Reserved	Reserved	00
9:8	P2.20	Reserved	Reserved	Reserved	Reserved	00
11:10	P2.21	Reserved	Reserved	Reserved	Reserved	00
13:12	P2.22	Reserved	Reserved	Reserved	Reserved	00
15:14	P2.23	Reserved	Reserved	Reserved	Reserved	00
17:16	P2.24	Reserved	Reserved	Reserved	Reserved	00
19:18	P2.25	Reserved	Reserved	Reserved	Reserved	00
21:20	P2.26	Reserved	Reserved	Reserved	Reserved	00
23:22	P2.27	Reserved	Reserved	Reserved	Reserved	00
25:24	P2.28	Reserved	Reserved	Reserved	Reserved	00
27:26	P2.29	Reserved	Reserved	Reserved	Reserved	00
29:28	P2.30	Reserved	Reserved	Reserved	Reserved	00
31:30	P2.31	Reserved	Reserved	Reserved	Reserved	00

6.7 Pin Function Select Register 6 (PINSEL6 - 0xE002 C018)

The PINSEL6 register controls the functions of the pins as per the settings listed in Table 9–90. The direction control bit in the FIO3DIR register is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically.

Table 90. Pin function select register 6 (PINSEL6 - address 0xE002 C018) bit description

PINSEL6	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0[1]	P3.0	GPIO Port 3.0	D0	Reserved	Reserved	00
3:2[1]	P3.1	GPIO Port 3.1	D1	Reserved	Reserved	00
5:4[1]	P3.2	GPIO Port 3.2	D2	Reserved	Reserved	00
7:6[1]	P3.3	GPIO Port 3.3	D3	Reserved	Reserved	00
9:8[1]	P3.4	GPIO Port 3.4	D4	Reserved	Reserved	00
11:10[1]	P3.5	GPIO Port 3.5	D5	Reserved	Reserved	00
13:12[1]	P3.6	GPIO Port 3.6	D6	Reserved	Reserved	00
15:14[1]	P3.7	GPIO Port 3.7	D7	Reserved	Reserved	00
17:16	P3.8	Reserved	Reserved	Reserved	Reserved	00
19:18	P3.9	Reserved	Reserved	Reserved	Reserved	00
21:20	P3.10	Reserved	Reserved	Reserved	Reserved	00
23:22	P3.11	Reserved	Reserved	Reserved	Reserved	00
25:24	P3.12	Reserved	Reserved	Reserved	Reserved	00
27:26	P3.13	Reserved	Reserved	Reserved	Reserved	00
29:28	P3.14	Reserved	Reserved	Reserved	Reserved	00
31:30	P3.15	Reserved	Reserved	Reserved	Reserved	00

[1] LPC2378 only. These bits are reserved for LPC2364/66/68.

6.8 Pin Function Select Register 7 (PINSEL7 - 0xE002 C01C)

The PINSEL7 register controls the functions of the pins as per the settings listed in Table 9–91. The direction control bit in the FIO3DIR register is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically.

Table 91. Pin function select register 7 (PINSEL7 - address 0xE002 C01C) bit description

PINSEL7	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0	P3.16	Reserved	Reserved	Reserved	Reserved	00
3:2	P3.17	Reserved	Reserved	Reserved	Reserved	00
5:4	P3.18	Reserved	Reserved	Reserved	Reserved	00
7:6	P3.19	Reserved	Reserved	Reserved	Reserved	00
9:8	P3.20	Reserved	Reserved	Reserved	Reserved	00
11:10	P3.21	Reserved	Reserved	Reserved	Reserved	00
13:12	P3.22	Reserved	Reserved	Reserved	Reserved	00
15:14[1]	P3.23	GPIO Port 3.23	Reserved	CAP0.0	PCAP1.0	00
17:16[1]	P3.24	GPIO Port 3.24	Reserved	CAP0.1	PWM1.1	00
19:18	P3.25	GPIO Port 3.25	Reserved	MAT0.0	PWM1.2	00
21:20	P3.26	GPIO Port 3.26	Reserved	MAT0.1	PWM1.3	00
23:22	P3.27	Reserved	Reserved	Reserved	Reserved	00
25:24	P3.28	Reserved	Reserved	Reserved	Reserved	00

Table 91. Pin function select register 7 (PINSEL7 - address 0xE002 C01C) bit description

PINSEL7	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
27:26	P3.29	Reserved	Reserved	Reserved	Reserved	00
29:28	P3.30	Reserved	Reserved	Reserved	Reserved	00
31:30	P3.31	Reserved	Reserved	Reserved	Reserved	00

[1] LPC2378 only. These bits are reserved for LPC2364/66/68.

6.9 Pin Function Select Register 8 (PINSEL8 - 0xE002 C020)

The PINSEL8 register controls the functions of the pins as per the settings listed in Table 9–92. The direction control bit in the FIO4DIR register is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically.

Table 92. Pin function select register 8 (PINSEL8 - address 0xE002 C020) bit description

PINSEL8	Pin name	Function when 00	Function when 01	Function when 10	Function when 11	Reset value
1:0[1]	P4.0	GPIO Port 4.0	A0	Reserved	Reserved	00
3:2[1]	P4.1	GPIO Port 4.1	A1	Reserved	Reserved	00
5:4[1]	P4.2	GPIO Port 4.2	A2	Reserved	Reserved	00
7:6[1]	P4.3	GPIO Port 4.3	A3	Reserved	Reserved	00
9:8[1]	P4.4	GPIO Port 4.4	A4	Reserved	Reserved	00
11:10[1]	P4.5	GPIO Port 4.5	A5	Reserved	Reserved	00
13:12[1]	P4.6	GPIO Port 4.6	A6	Reserved	Reserved	00
15:14[1]	P4.7	GPIO Port 4.7	A7	Reserved	Reserved	00
17:16[1]	P4.8	GPIO Port 4.8	A8	Reserved	Reserved	00
19:18[1]	P4.9	GPIO Port 4.9	A9	Reserved	Reserved	00
21:20[1]	P4.10	GPIO Port 4.10	A10	Reserved	Reserved	00
23:22[1]	P4.11	GPIO Port 4.11	A11	Reserved	Reserved	00
25:24[1]	P4.12	GPIO Port 4.12	A12	Reserved	Reserved	00
27:26[1]	P4.13	GPIO Port 4.13	A13	Reserved	Reserved	00
29:28[1]	P4.14	GPIO Port 4.14	A14	Reserved	Reserved	00
31:30[1]	P4.15	GPIO Port 4.15	A15	Reserved	Reserved	00

[1] LPC2378 only. These bits are reserved for LPC2364/66/68.

6.10 Pin Function Select Register 9 (PINSEL9 - 0xE002 C024)

The PINSEL9 register controls the functions of the pins as per the settings listed in Table 9–93. The direction control bit in the FIO4DIR register is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically.