– if the EMC_Reset_Disable = 1 ( see Section 3–7 “Other system controls and status flags”), they retain their values for external memory interface
– else if the EMC_Reset_Disable = 0, they are reset to '0'.

## 6.1 Pin Function Select register 0 (PINSEL0 - 0xE002 C000)

The PINSEL0 register controls the functions of the pins as per the settings listed in Table 9–84. The direction control bit in the IO0DIR register (or the FIO0DIR register if the enhanced GPIO function is selected for port 0) is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically.

**Table 84. Pin function select register 0 (PINSEL0 - address 0xE002 C000) bit description**

| PINSEL0 | Pin name | Function when 00 | Function when 01 | Function when 10 | Function when 11 | Reset value |
|---|---|---|---|---|---|---|
| 1:0 | P0.0 | GPIO Port 0.0 | RD1 | TXD3 | SDA1 | 00 |
| 3:2 | P0.1 | GPIO Port 0.1 | TD1 | RXD3 | SCL1 | 00 |
| 5:4 | P0.2 | GPIO Port 0.2 | TXD0 | Reserved | Reserved | 00 |
| 7:6 | P0.3 | GPIO Port 0.3 | RXD0 | Reserved | Reserved | 00 |
| 9:8 | P0.4 | GPIO Port 0.4 | I2SRX_CLK | RD2 | CAP2.0 | 00 |
| 11:10 | P0.5 | GPIO Port 0.5 | I2SRX_WS | TD2 | CAP2.1 | 00 |
| 13:12 | P0.6 | GPIO Port 0.6 | I2SRX_SDA | SSEL1 | MAT2.0 | 00 |
| 15:14 | P0.7 | GPIO Port 0.7 | I2STX_CLK | SCK1 | MAT2.1 | 00 |
| 17:16 | P0.8 | GPIO Port 0.8 | I2STX_WS | MISO1 | MAT2.2 | 00 |
| 19:18 | P0.9 | GPIO Port 0.9 | I2STX_SDA | MOSI1 | MAT2.3 | 00 |
| 21:20 | P0.10 | GPIO Port 0.10 | TXD2 | SDA2 | MAT3.0 | 00 |
| 23:22 | P0.11 | GPIO Port 0.11 | RXD2 | SCL2 | MAT3.1 | 00 |
| 25:24[1] | P0.12 | GPIO Port 0.12 | Reserved | MISO1 | AD0.6 | 00 |
| 27:26[1] | P0.13 | GPIO Port 0.13 | $\overline{\text{U2UP\_LED}}$ | MOSI1 | AD0.7 | 00 |
| 29:28[1] | P0.14 | GPIO Port 0.14 | $\overline{\text{U2CONNECT}}$ | Reserved | SSEL1 | 00 |
| 31:30 | P0.15 | GPIO Port 0.15 | TXD1 | SCK0 | SCK | 00 |

[1] LPC2378 only. These bits are reserved for LPC2364/66/68.

## 6.2 Pin Function Select Register 1 (PINSEL1 - 0xE002 C004)

The PINSEL1 register controls the functions of the pins as per the settings listed in Table 9–85. The direction control bit in the IO0DIR (or the FIO0DIR register if the enhanced GPIO function is selected for port 0) register is effective only when the GPIO function is selected for a pin. For other functions direction is controlled automatically.

**Table 85. Pin function select register 1 (PINSEL1 - address 0xE002 C004) bit description**

| PINSEL1 | Pin name | Function when 00 | Function when 01 | Function when 10 | Function when 11 | Reset value |
|---|---|---|---|---|---|---|
| 1:0 | P0.16 | GPIO Port 0.16 | RXD1 | SSEL0 | SSEL | 00 |
| 3:2 | P0.17 | GPIO Port 0.17 | CTS1 | MISO0 | MISO | 00 |
| 5:4 | P0.18 | GPIO Port 0.18 | DCD1 | MOSI0 | MOSI | 00 |
| 7:6 | P0.19 | GPIO Port 0.19 | DSR1 | MCICLK | SDA1 | 00 |
| 9:8 | P0.20 | GPIO Port 0.20 | DTR1 | MCICMD | SCL1 | 00 |

Table 85. Pin function select register 1 (PINSEL1 - address 0xE002 C004) bit description

| PINSEL1 | Pin name | Function when 00 | Function when 01 | Function when 10 | Function when 11 | Reset value |
|---|---|---|---|---|---|---|
| 11:10 | P0.21 | GPIO Port 0.21 | RI1 | MCIPWR | RD1 | 00 |
| 13:12 | P0.22 | GPIO Port 0.22 | RTS1 | MCIDAT0 | TD1 | 00 |
| 15:14 | P0.23 | GPIO Port 0.23 | AD0.0 | I2SRX_CLK | CAP3.0 | 00 |
| 17:16 | P0.24 | GPIO Port 0.24 | AD0.1 | I2SRX_WS | CAP3.1 | 00 |
| 19:18 | P0.25 | GPIO Port 0.25 | AD0.2 | I2SRX_SDA | TXD3 | 00 |
| 21:20 | P0.26 | GPIO Port 0.26 | AD0.3 | AOUT | RXD3 | 00 |
| 23:22 | P0.27 | GPIO Port 0.27 | SDA0 | Reserved | Reserved | 00 |
| 25:24 | P0.28 | GPIO Port 0.28 | SCL0 | Reserved | Reserved | 00 |
| 27:26 | P0.29 | GPIO Port 0.29 | U1D+ | Reserved | Reserved | 00 |
| 29:28 | P0.30 | GPIO Port 0.30 | U1D− | Reserved | Reserved | 00 |
| 31:30[1] | P0.31 | GPIO Port 0.31 | U2D+ | Reserved | Reserved | 00 |

[1] LPC2378 only. These bits are reserved for LPC2364/66/68.

## 6.3 Pin Function Select register 2 (PINSEL2 - 0xE002 C008)

The PINSEL2 register controls the functions of the pins as per the settings listed in Table 9–86. The direction control bit in the IO1DIR register (or the FIO1DIR register if the enhanced GPIO function is selected for port 1) is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically.

Table 86. Pin function select register 2 (PINSEL2 - address 0xE002 C008) bit description

| PINSEL2 | Pin name | Function when 00 | Function when 01 | Function when 10 | Function when 11 | Reset value |
|---|---|---|---|---|---|---|
| 1:0 | P1.0 | GPIO Port 1.0 | ENET_TXD0 | Reserved | Reserved | 00 |
| 3:2 | P1.1 | GPIO Port 1.1 | ENET_TXD1 | Reserved | Reserved | 00 |
| 5:4 | P1.2 | Reserved | Reserved | Reserved | Reserved | 00 |
| 7:6 | P1.3 | Reserved | Reserved | Reserved | Reserved | 00 |
| 9:8 | P1.4 | GPIO Port 1.4 | ENET_TX_EN | Reserved | Reserved | 00 |
| 11:10 | P1.5 | Reserved | Reserved | Reserved | Reserved | 00 |
| 13:12 | P1.6 | Reserved | Reserved | Reserved | Reserved | 00 |
| 15:14 | P1.7 | Reserved | Reserved | Reserved | Reserved | 00 |
| 17:16 | P1.8 | GPIO Port 1.8 | ENET_CRS | Reserved | Reserved | 00 |
| 19:18 | P1.9 | GPIO Port 1.9 | ENET_RXD0 | Reserved | Reserved | 00 |
| 21:20 | P1.10 | GPIO Port 1.10 | ENET_RXD1 | Reserved | Reserved | 00 |
| 23:22 | P1.11 | Reserved | Reserved | Reserved | Reserved | 00 |
| 25:24 | P1.12 | Reserved | Reserved | Reserved | Reserved | 00 |
| 27:26 | P1.13 | Reserved | Reserved | Reserved | Reserved | 00 |
| 29:28 | P1.14 | GPIO Port 1.14 | ENET_RX_ER | Reserved | Reserved | 00 |
| 31:30 | P1.15 | GPIO Port 1.15 | ENET_REF_CLK | Reserved | Reserved | 00 |

## 6.4 Pin Function Select Register 3 (PINSEL3 - 0xE002 C00C)

The PINSEL3 register controls the functions of the pins as per the settings listed in Table 9–87. The direction control bit in the IO1DIR register (or the FIO1DIR register if the enhanced GPIO function is selected for port 1) is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically.

**Table 87. Pin function select register 3 (PINSEL3 - address 0xE002 C00C) bit description**

| PINSEL3 | Pin name | Function when 00 | Function when 01 | Function when 10 | Function when 11 | Reset value |
|---|---|---|---|---|---|---|
| 1:0 | P1.16 | GPIO Port 1.16 | ENET_MDC | Reserved | Reserved | 00 |
| 3:2 | P1.17 | GPIO Port 1.17 | ENET_MDIO | Reserved | Reserved | 00 |
| 5:4 | P1.18 | GPIO Port 1.18 | $\overline{\text{U1UP\_LED}}$ | PWM1.1 | CAP1.0 | 00 |
| 7:6 | P1.19 | GPIO Port 1.19 | Reserved | Reserved | CAP1.1 | 00 |
| 9:8 | P1.20 | GPIO Port 1.20 | Reserved | PWM1.2 | SCK0 | 00 |
| 11:10 | P1.21 | GPIO Port 1.21 | Reserved | PWM1.3 | SSEL0 | 00 |
| 13:12 | P1.22 | GPIO Port 1.22 | Reserved | Reserved | MAT1.0 | 00 |
| 15:14 | P1.23 | GPIO Port 1.23 | Reserved | PWM1.4 | MISO0 | 00 |
| 17:16 | P1.24 | GPIO Port 1.24 | Reserved | PWM1.5 | MOSI0 | 00 |
| 19:18 | P1.25 | GPIO Port 1.25 | Reserved | Reserved | MAT1.1 | 00 |
| 21:20 | P1.26 | GPIO Port 1.26 | Reserved | PWM1.6 | CAP0.0 | 00 |
| 23:22 | P1.27 | GPIO Port 1.27 | Reserved | Reserved | CAP0.1 | 00 |
| 25:24 | P1.28 | GPIO Port 1.28 | Reserved | PCAP1.0 | MAT0.0 | 00 |
| 27:26 | P1.29 | GPIO Port 1.29 | Reserved | PCAP1.1 | MAT0.1 | 00 |
| 29:28 | P1.30 | GPIO Port 1.30 | Reserved | $V_{BUS}$ | AD0.4 | 00 |
| 31:30 | P1.31 | GPIO Port 1.31 | Reserved | SCK1 | AD0.5 | 00 |

## 6.5 Pin Function Select Register 4 (PINSEL4 - 0xE002 C010)

The PINSEL4 register controls the functions of the pins as per the settings listed in Table 9–88. The direction control bit in the FIO2DIR register is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically.

**Table 88. Pin function select register 4 (PINSEL4 - address 0xE002 C010) bit description**

| PINSEL4 | Pin name | Function when 00 | Function when 01 | Function when 10 | Function when 11 | Reset value |
|---|---|---|---|---|---|---|
| 1:0 | P2.0 | GPIO Port 2.0 | PWM1.1 | TXD1 | TRACECLK[1] | 00 |
| 3:2 | P2.1 | GPIO Port 2.1 | PWM1.2 | RXD1 | PIPESTAT0[1] | 00 |
| 5:4 | P2.2 | GPIO Port 2.2 | PWM1.3 | CTS1 | PIPESTAT1[1] | 00 |
| 7:6 | P2.3 | GPIO Port 2.3 | PWM1.4 | DCD1 | PIPESTAT2[1] | 00 |
| 9:8 | P2.4 | GPIO Port 2.4 | PWM1.5 | DSR1 | TRACESYNC[1] | 00 |
| 11:10 | P2.5 | GPIO Port 2.5 | PWM1.6 | DTR1 | TRACEPKT0[1] | 00 |
| 13:12 | P2.6 | GPIO Port 2.6 | PCAP1.0 | RI1 | TRACEPKT1[1] | 00 |
| 15:14 | P2.7 | GPIO Port 2.7 | RD2 | RTS1 | TRACEPKT2[1] | 00 |
| 17:16 | P2.8 | GPIO Port 2.8 | TD2 | TXD2 | TRACEPKT3[1] | 00 |
| 19:18 | P2.9 | GPIO Port 2.9 | $\overline{\text{U1CONNECT}}$ | RXD2 | EXTIN0[1] | 00 |

Table 88. Pin function select register 4 (PINSEL4 - address 0xE002 C010) bit description

| PINSEL4 | Pin name | Function when 00 | Function when 01 | Function when 10 | Function when 11 | Reset value |
|---|---|---|---|---|---|---|
| 21:20 | P2.10 | GPIO Port 2.10 | $\overline{\text{EINT0}}$ | Reserved | Reserved | 00 |
| 23:22 | P2.11 | GPIO Port 2.11 | $\overline{\text{EINT1}}$ | MCIDAT1 | I2STX_CLK | 00 |
| 25:24 | P2.12 | GPIO Port 2.12 | $\overline{\text{EINT2}}$ | MCIDAT2 | I2STX_WS | 00 |
| 27:26 | P2.13 | GPIO Port 2.13 | $\overline{\text{EINT3}}$ | MCIDAT3 | I2STX_SDA | 00 |
| 29:28 | P2.14 | Reserved | Reserved | Reserved | Reserved | 00 |
| 31:30 | P2.15 | Reserved | Reserved | Reserved | Reserved | 00 |

[1] See Section 9–6.11 “Pin Function Select Register 10 (PINSEL10 - 0xE002 C028)”for details on using the ETM functionality.

## 6.6 Pin Function Select Register 5 (PINSEL5 - 0xE002 C014)

The PINSEL5 register controls the functions of the pins as per the settings listed in Table 9–89. The direction control bit in the FIO2DIR register is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically.

Table 89. Pin function select register 5 (PINSEL5 - address 0xE002 C014) bit description

| PINSEL5 | Pin name | Function when 00 | Function when 01 | Function when 10 | Function when 11 | Reset value |
|---|---|---|---|---|---|---|
| 1:0 | P2.16 | Reserved | Reserved | Reserved | Reserved | 00 |
| 3:2 | P2.17 | Reserved | Reserved | Reserved | Reserved | 00 |
| 5:4 | P2.18 | Reserved | Reserved | Reserved | Reserved | 00 |
| 7:6 | P2.19 | Reserved | Reserved | Reserved | Reserved | 00 |
| 9:8 | P2.20 | Reserved | Reserved | Reserved | Reserved | 00 |
| 11:10 | P2.21 | Reserved | Reserved | Reserved | Reserved | 00 |
| 13:12 | P2.22 | Reserved | Reserved | Reserved | Reserved | 00 |
| 15:14 | P2.23 | Reserved | Reserved | Reserved | Reserved | 00 |
| 17:16 | P2.24 | Reserved | Reserved | Reserved | Reserved | 00 |
| 19:18 | P2.25 | Reserved | Reserved | Reserved | Reserved | 00 |
| 21:20 | P2.26 | Reserved | Reserved | Reserved | Reserved | 00 |
| 23:22 | P2.27 | Reserved | Reserved | Reserved | Reserved | 00 |
| 25:24 | P2.28 | Reserved | Reserved | Reserved | Reserved | 00 |
| 27:26 | P2.29 | Reserved | Reserved | Reserved | Reserved | 00 |
| 29:28 | P2.30 | Reserved | Reserved | Reserved | Reserved | 00 |
| 31:30 | P2.31 | Reserved | Reserved | Reserved | Reserved | 00 |

## 6.7 Pin Function Select Register 6 (PINSEL6 - 0xE002 C018)

The PINSEL6 register controls the functions of the pins as per the settings listed in Table 9–90. The direction control bit in the FIO3DIR register is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically.

Table 90. Pin function select register 6 (PINSEL6 - address 0xE002 C018) bit description

| PINSEL6 | Pin name | Function when 00 | Function when 01 | Function when 10 | Function when 11 | Reset value |
|---|---|---|---|---|---|---|
| 1:0[1] | P3.0 | GPIO Port 3.0 | D0 | Reserved | Reserved | 00 |
| 3:2[1] | P3.1 | GPIO Port 3.1 | D1 | Reserved | Reserved | 00 |
| 5:4[1] | P3.2 | GPIO Port 3.2 | D2 | Reserved | Reserved | 00 |
| 7:6[1] | P3.3 | GPIO Port 3.3 | D3 | Reserved | Reserved | 00 |
| 9:8[1] | P3.4 | GPIO Port 3.4 | D4 | Reserved | Reserved | 00 |
| 11:10[1] | P3.5 | GPIO Port 3.5 | D5 | Reserved | Reserved | 00 |
| 13:12[1] | P3.6 | GPIO Port 3.6 | D6 | Reserved | Reserved | 00 |
| 15:14[1] | P3.7 | GPIO Port 3.7 | D7 | Reserved | Reserved | 00 |
| 17:16 | P3.8 | Reserved | Reserved | Reserved | Reserved | 00 |
| 19:18 | P3.9 | Reserved | Reserved | Reserved | Reserved | 00 |
| 21:20 | P3.10 | Reserved | Reserved | Reserved | Reserved | 00 |
| 23:22 | P3.11 | Reserved | Reserved | Reserved | Reserved | 00 |
| 25:24 | P3.12 | Reserved | Reserved | Reserved | Reserved | 00 |
| 27:26 | P3.13 | Reserved | Reserved | Reserved | Reserved | 00 |
| 29:28 | P3.14 | Reserved | Reserved | Reserved | Reserved | 00 |
| 31:30 | P3.15 | Reserved | Reserved | Reserved | Reserved | 00 |

[1] LPC2378 only. These bits are reserved for LPC2364/66/68.

## 6.8 Pin Function Select Register 7 (PINSEL7 - 0xE002 C01C)

The PINSEL7 register controls the functions of the pins as per the settings listed in Table 9–91. The direction control bit in the FIO3DIR register is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically.

Table 91. Pin function select register 7 (PINSEL7 - address 0xE002 C01C) bit description

| PINSEL7 | Pin name | Function when 00 | Function when 01 | Function when 10 | Function when 11 | Reset value |
|---|---|---|---|---|---|---|
| 1:0 | P3.16 | Reserved | Reserved | Reserved | Reserved | 00 |
| 3:2 | P3.17 | Reserved | Reserved | Reserved | Reserved | 00 |
| 5:4 | P3.18 | Reserved | Reserved | Reserved | Reserved | 00 |
| 7:6 | P3.19 | Reserved | Reserved | Reserved | Reserved | 00 |
| 9:8 | P3.20 | Reserved | Reserved | Reserved | Reserved | 00 |
| 11:10 | P3.21 | Reserved | Reserved | Reserved | Reserved | 00 |
| 13:12 | P3.22 | Reserved | Reserved | Reserved | Reserved | 00 |
| 15:14[1] | P3.23 | GPIO Port 3.23 | Reserved | CAP0.0 | PCAP1.0 | 00 |
| 17:16[1] | P3.24 | GPIO Port 3.24 | Reserved | CAP0.1 | PWM1.1 | 00 |
| 19:18 | P3.25 | GPIO Port 3.25 | Reserved | MAT0.0 | PWM1.2 | 00 |
| 21:20 | P3.26 | GPIO Port 3.26 | Reserved | MAT0.1 | PWM1.3 | 00 |
| 23:22 | P3.27 | Reserved | Reserved | Reserved | Reserved | 00 |
| 25:24 | P3.28 | Reserved | Reserved | Reserved | Reserved | 00 |

Table 91. Pin function select register 7 (PINSEL7 - address 0xE002 C01C) bit description

| PINSEL7 | Pin name | Function when 00 | Function when 01 | Function when 10 | Function when 11 | Reset value |
|---|---|---|---|---|---|---|
| 27:26 | P3.29 | Reserved | Reserved | Reserved | Reserved | 00 |
| 29:28 | P3.30 | Reserved | Reserved | Reserved | Reserved | 00 |
| 31:30 | P3.31 | Reserved | Reserved | Reserved | Reserved | 00 |

[1] LPC2378 only. These bits are reserved for LPC2364/66/68.

## 6.9 Pin Function Select Register 8 (PINSEL8 - 0xE002 C020)

The PINSEL8 register controls the functions of the pins as per the settings listed in Table 9–92. The direction control bit in the FIO4DIR register is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically.

Table 92. Pin function select register 8 (PINSEL8 - address 0xE002 C020) bit description

| PINSEL8 | Pin name | Function when 00 | Function when 01 | Function when 10 | Function when 11 | Reset value |
|---|---|---|---|---|---|---|
| 1:0[1] | P4.0 | GPIO Port 4.0 | A0 | Reserved | Reserved | 00 |
| 3:2[1] | P4.1 | GPIO Port 4.1 | A1 | Reserved | Reserved | 00 |
| 5:4[1] | P4.2 | GPIO Port 4.2 | A2 | Reserved | Reserved | 00 |
| 7:6[1] | P4.3 | GPIO Port 4.3 | A3 | Reserved | Reserved | 00 |
| 9:8[1] | P4.4 | GPIO Port 4.4 | A4 | Reserved | Reserved | 00 |
| 11:10[1] | P4.5 | GPIO Port 4.5 | A5 | Reserved | Reserved | 00 |
| 13:12[1] | P4.6 | GPIO Port 4.6 | A6 | Reserved | Reserved | 00 |
| 15:14[1] | P4.7 | GPIO Port 4.7 | A7 | Reserved | Reserved | 00 |
| 17:16[1] | P4.8 | GPIO Port 4.8 | A8 | Reserved | Reserved | 00 |
| 19:18[1] | P4.9 | GPIO Port 4.9 | A9 | Reserved | Reserved | 00 |
| 21:20[1] | P4.10 | GPIO Port 4.10 | A10 | Reserved | Reserved | 00 |
| 23:22[1] | P4.11 | GPIO Port 4.11 | A11 | Reserved | Reserved | 00 |
| 25:24[1] | P4.12 | GPIO Port 4.12 | A12 | Reserved | Reserved | 00 |
| 27:26[1] | P4.13 | GPIO Port 4.13 | A13 | Reserved | Reserved | 00 |
| 29:28[1] | P4.14 | GPIO Port 4.14 | A14 | Reserved | Reserved | 00 |
| 31:30[1] | P4.15 | GPIO Port 4.15 | A15 | Reserved | Reserved | 00 |

[1] LPC2378 only. These bits are reserved for LPC2364/66/68.

## 6.10 Pin Function Select Register 9 (PINSEL9 - 0xE002 C024)

The PINSEL9 register controls the functions of the pins as per the settings listed in Table 9–93. The direction control bit in the FIO4DIR register is effective only when the GPIO function is selected for a pin. For other functions, direction is controlled automatically.

| N° Canal | Masque Hexa | Source |
|---|---|---|
| 0 | 0x00000001 | Watchdog Timer |
| 1 | 0x00000002 | Reserved for software interrupts only |
| 2 | 0x00000004 | ARM Core Embedded ICE, DbgCommRx |
| 3 | 0x00000008 | ARM Core Embedded ICE, DbgCommTx |
| 4 | 0x00000010 | TIMER0 |
| 5 | 0x00000020 | TIMER1 |
| 6 | 0x00000040 | UART0 |
| 7 | 0x00000080 | UART1 |
| 8 | 0x00000100 | PWM1 |
| 9 | 0x00000200 | I2C0 |
| 10 | 0x00000400 | SPI0, SSP0 |
| 11 | 0x00000800 | SSP1 |
| 12 | 0x00001000 | PLL |
| 13 | 0x00002000 | RTC |
| 14 | 0x00004000 | External Interrupt 0 |
| 15 | 0x00008000 | External Interrupt 1 |
| 16 | 0x00010000 | External Interrupt 2 |
| 17 | 0x00020000 | External Interrupt 3 |
| 18 | 0x00040000 | A/D Converter |
| 19 | 0x00080000 | I2C1 |
| 20 | 0x00100000 | Brown Out Detect |
| 21 | 0x00200000 | Ethernet |
| 22 | 0x00400000 | USB |
| 23 | 0x00800000 | CAN |
| 24 | 0x01000000 | SD / MMC |
| 25 | 0x02000000 | GP DMA |
| 26 | 0x04000000 | Timer 2 |
| 27 | 0x08000000 | Timer 3 |
| 28 | 0x10000000 | UART 2 |
| 29 | 0x20000000 | UART 3 |
| 30 | 0x40000000 | I2C2 |
| 31 | 0x80000000 | I2S |

## 3. Registre EXTMODE

| Bits | Fonction | Bit à 0 | Bit à 1 | Reset |
|---|---|---|---|---|
| 0 | EXTMODE0 | Niveau | Front | 0 |
| 1 | EXTMODE1 | Niveau | Front | 0 |
| 2 | EXTMODE2 | Niveau | Front | 0 |
| 3 | EXTMODE3 | Niveau | Front | 0 |
| 7:4 | Réservé | - | - | N/A |



## 4. Registre EXTPOLAR

| Bits | Fonction | Bit à 0 | Bit à 1 | Reset |
|---|---|---|---|---|
| 0 | EXTPOLAR0 | Niveau bas ou Front Descendant selon EXTMODE | Niveau haut ou Front Montant selon EXTMODE | 0 |
| 1 | EXTPOLAR1 | | | 0 |
| 2 | EXTPOLAR2 | | | 0 |
| 3 | EXTPOLAR3 | | | 0 |
| 7:4 | Réservé | - | - | N/A |



## 5. Registre d'interruptions EXTINT

| Bits | Fonction | Description | | Reset |
|---|---|---|---|---|
| 0 | EINT0 | Mis à 1 lorsque EINTx est sélectionnée et : Niveau actif détecté Ou Front attendu détecté. Mis à 0 si on écrit 1, sauf quand broche à 1 et sensible à 1 niveau. | | 0 |
| 1 | EINT1 | | | 0 |
| 2 | EINT2 | | | 0 |
| 3 | EINT3 | | | 0 |
| 7:4 | Réservé | - | - | N/A |

This bit is cleared by writing a one to it, except in level sensitive mode when the pin is in its active state



## 6. Broches associés

- P2.10 EINT0 Bar
- P2.11 EINT1 Bar
- P2.12 EINT2 Bar
- P2.13 EINT3 Bar

# Actions définies par TyMCR

| Bit # | Description | Reset |
|---|---|---|
| 0 | Demande d'interruption MR0 si match TyMR0 (si bit à 1) | 0 |
| 1 | Mise à 0 de Ty si match TyMR0 (si bit à 1) | 0 |
| 2 | Arrêt de Ty si match TyMR0 (si bit à 1) | 0 |
| 3 | Demande d'interruption MR1 si match TyMR1 (si bit à 1) | 0 |
| 4 | Mise à 0 de Ty si match TyMR1 (si bit à 1) | 0 |
| 5 | Arrêt de Ty si match TyMR1 (si bit à 1) | 0 |



# Actions définies par TyMCR (bis)

| Bit # | Description | Reset |
|---|---|---|
| 6 | Demande d'interruption MR2 si match TyMR2 (si bit à 1) | 0 |
| 7 | Mise à 0 de Ty si match TyMR2 (si bit à 1) | 0 |
| 8 | Arrêt de Ty si match TyMR2 (si bit à 1) | 0 |
| 9 | Demande d'interruption MR3 si match TyMR3 (si bit à 1) | 0 |
| 10 | Mise à 0 de Ty si match TyMR3 (si bit à 1) | 0 |
| 11 | Arrêt de Ty si match TyMR3 (si bit à 1) | 0 |



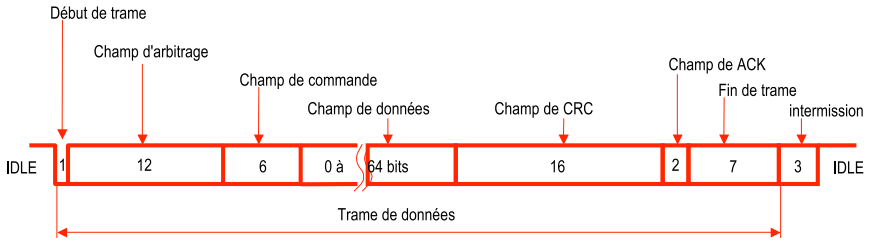
# Demande d'interruptions de match pour Ty : TyIR Interrupt Request

| Bit # | Description | Reset |
|---|---|---|
| 0 | Demande d'interruption de Match TyMR0 | 0 |
| 1 | Demande d'interruption de Match TyMR1 | 0 |
| 2 | Demande d'interruption de Match TyMR2 | 0 |
| 3 | Demande d'interruption de Match TyMR3 | 0 |

Quand le drapeau vaut 1, l'interruption est demandée.
Quand le drapeau vaut 0, l'interruption n'est pas demandée.

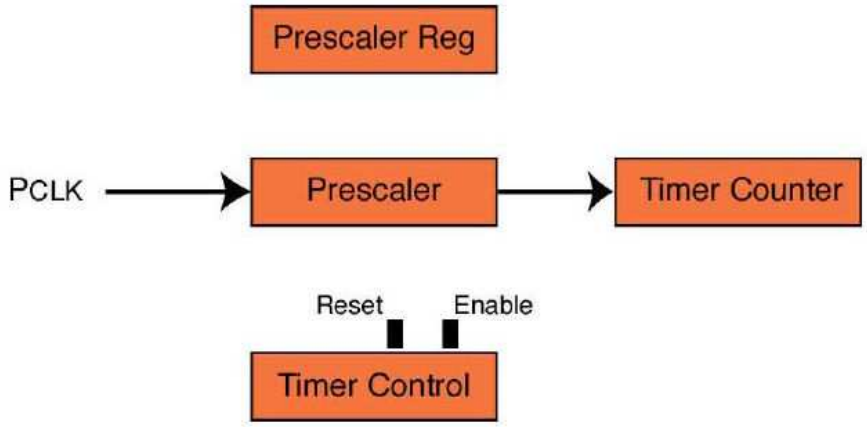


# Trame de données



# Architecture – Timers LPC2378

- Registres Correspondants
  - Timer Counter : TxTC (Lecture seule)
  - Prescaler : TxPC (Lecture seule)
  - Prescaler Register : TxPR
  - x = 0,1,2 ou 3






# Registre de Commande

- Registre TxTCR (x=0,1,2 ou 3)
  - Bit 0: Démarrage/Arrêt du Compteur
  - Bit 1: Reset du Compteur

Table 430: Timer Control Register (TCR, TIMERn: TnTCR - addresses 0xE000 4004, 0xE000 8004, 0xE007 0004, 0xE007 4004) bit description

| Bit | Symbol | Description | Reset Value |
|---|---|---|---|
| 0 | Counter Enable | When one, the Timer Counter and Prescale Counter are enabled for counting. When zero, the counters are disabled. | 0 |
| 1 | Counter Reset | When one, the Timer Counter and the Prescale Counter are synchronously reset on the next positive edge of PCLK. The counters remain reset until TCR[1] is returned to zero. | 0 |

# Match (Comparaison)

- Chaque Timer possède 4 Match Register
  - TxMR0, TxMR1, TxMR2, TxMR3

- A chaque incrémentation du Timer Tx, le contenu de TxTC est comparé aux Match Registers
  - Si les deux valeurs sont égales, une action peut alors être entreprise

**Table 485: PWM Timer Control Register (PWM1TCR address 0xE001 8004) bit description**

| Bit | Symbol | Value | Description | Reset Value |
|---|---|---|---|---|
| 0 | Counter Enable | 1 | The PWM Timer Counter and PWM Prescale Counter are enabled for counting. | 0 |
| | | 0 | The counters are disabled. | |
| 1 | Counter Reset | 1 | The PWM Timer Counter and the PWM Prescale Counter are synchronously reset on the next positive edge of PCLK. The counters remain reset until this bit is returned to zero. | 0 |
| | | 0 | Clear reset. | |
| 2 | - | | Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined. | NA |
| 3 | PWM Enable | 1 | PWM mode is enabled (counter resets to 1). PWM mode causes the shadow registers to operate in connection with the Match registers. A program write to a Match register will not have an effect on the Match result until the corresponding bit in PWMLER has been set, followed by the occurrence of a PWM Match 0 event. Note that the PWM Match register that determines the PWM rate (PWM Match Register 0 - MR0) must be set up prior to the PWM being enabled. Otherwise a Match event will not occur to cause shadow register contents to become effective. | 0 |
| | | 0 | Timer mode is enabled (counter resets to 0). | |
| 7:4 | - | | Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined. | NA |

**Table 484: PWM Interrupt Register (PWM1IR - address 0xE001 8000) bit description**

| Bit | Symbol | Description | Reset Value |
|---|---|---|---|
| 0 | PWMMR0 Interrupt | Interrupt flag for PWM match channel 0. | 0 |
| 1 | PWMMR1 Interrupt | Interrupt flag for PWM match channel 1. | 0 |
| 2 | PWMMR2 Interrupt | Interrupt flag for PWM match channel 2. | 0 |
| 3 | PWMMR3 Interrupt | Interrupt flag for PWM match channel 3. | 0 |
| 4 | PWMCAP0 Interrupt | Interrupt flag for capture input 0 | 0 |
| 5 | PWMCAP1 Interrupt | Interrupt flag for capture input 1. | 0 |
| 7:6 | - | Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined. | NA |
| 8 | PWMMR4 Interrupt | Interrupt flag for PWM match channel 4. | 0 |
| 9 | PWMMR5 Interrupt | Interrupt flag for PWM match channel 5. | 0 |
| 10 | PWMMR6 Interrupt | Interrupt flag for PWM match channel 6. | 0 |
| 15:11 | - | Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined. | NA |

**Table 487: Match Control Register (PWM1MCR - address 0xE000 8014) bit description**

| Bit | Symbol | Value | Description | Reset Value |
|---|---|---|---|---|
| 0 | PWMMR0I | 1 | Interrupt on PWMMR0: an interrupt is generated when PWMMR0 matches the value in the PWMTC. | 0 |
| | | 0 | This interrupt is disabled. | |
| 1 | PWMMR0R | 1 | Reset on PWMMR0: the PWMTC will be reset if PWMMR0 matches it. | 0 |
| | | 0 | This feature is disabled. | |
| 2 | PWMMR0S | 1 | Stop on PWMMR0: the PWMTC and PWMPC will be stopped and PWMTCR[0] will be set to 0 if PWMMR0 matches the PWMTC. | 0 |
| | | 0 | This feature is disabled | |
| 3 | PWMMR1I | 1 | Interrupt on PWMMR1: an interrupt is generated when PWMMR1 matches the value in the PWMTC. | 0 |
| | | 0 | This interrupt is disabled. | |
| 4 | PWMMR1R | 1 | Reset on PWMMR1: the PWMTC will be reset if PWMMR1 matches it. | 0 |
| | | 0 | This feature is disabled. | |
| 5 | PWMMR1S | 1 | Stop on PWMMR1: the PWMTC and PWMPC will be stopped and PWMTCR[0] will be set to 0 if PWMMR1 matches the PWMTC. | 0 |
| | | 0 | This feature is disabled. | |

**Table 487: Match Control Register (PWM1MCR - address 0xE000 8014) bit description**

| Bit | Symbol | Value | Description | Reset Value |
|---|---|---|---|---|
| 6 | PWMMR2I | 1 | Interrupt on PWMMR2: an interrupt is generated when PWMMR2 matches the value in the PWMTC. | 0 |
| | | 0 | This interrupt is disabled. | |
| 7 | PWMMR2R | 1 | Reset on PWMMR2: the PWMTC will be reset if PWMMR2 matches it. | 0 |
| | | 0 | This feature is disabled. | |
| 8 | PWMMR2S | 1 | Stop on PWMMR2: the PWMTC and PWMPC will be stopped and PWMTCR[0] will be set to 0 if PWMMR2 matches the PWMTC. | 0 |
| | | 0 | This feature is disabled | |
| 9 | PWMMR3I | 1 | Interrupt on PWMMR3: an interrupt is generated when PWMMR3 matches the value in the PWMTC. | 0 |
| | | 0 | This interrupt is disabled. | |
| 10 | PWMMR3R | 1 | Reset on PWMMR3: the PWMTC will be reset if PWMMR3 matches it. | 0 |
| | | 0 | This feature is disabled | |
| 11 | PWMMR3S | 1 | Stop on PWMMR3: The PWMTC and PWMPC will be stopped and PWMTCR[0] will be set to 0 if PWMMR3 matches the PWMTC. | 0 |
| | | 0 | This feature is disabled | |
| 12 | PWMMR4I | 1 | Interrupt on PWMMR4: An interrupt is generated when PWMMR4 matches the value in the PWMTC. | 0 |
| | | 0 | This interrupt is disabled. | |
| 13 | PWMMR4R | 1 | Reset on PWMMR4: the PWMTC will be reset if PWMMR4 matches it. | 0 |
| | | 0 | This feature is disabled. | |
| 14 | PWMMR4S | 1 | Stop on PWMMR4: the PWMTC and PWMPC will be stopped and PWMTCR[0] will be set to 0 if PWMMR4 matches the PWMTC. | 0 |
| | | 0 | This feature is disabled | |
| 15 | PWMMR5I | 1 | Interrupt on PWMMR5: An interrupt is generated when PWMMR5 matches the value in the PWMTC. | 0 |
| | | 0 | This interrupt is disabled. | |
| 16 | PWMMR5R | 1 | Reset on PWMMR5: the PWMTC will be reset if PWMMR5 matches it. | 0 |
| | | 0 | This feature is disabled. | |

**Table 489: PWM Control Registers (PWM1PCR - address 0xE001 804C) bit description**

| Bit | Symbol | Value | Description | Reset Value |
|---|---|---|---|---|
| 1:0 | Unused | | Unused, always zero. | NA |
| 2 | PWMSEL2 | 1 | Selects double edge controlled mode for the PWM2 output. | 0 |
| | | 0 | Selects single edge controlled mode for PWM2. | |
| 3 | PWMSEL3 | 1 | Selects double edge controlled mode for the PWM3 output. | 0 |
| | | 0 | Selects single edge controlled mode for PWM3. | |
| 4 | PWMSEL4 | 1 | Selects double edge controlled mode for the PWM4 output. | 0 |
| | | 0 | Selects single edge controlled mode for PWM4. | |
| 5 | PWMSEL5 | 1 | Selects double edge controlled mode for the PWM5 output. | 0 |
| | | 0 | Selects single edge controlled mode for PWM5. | |
| 6 | PWMSEL6 | 1 | Selects double edge controlled mode for the PWM6 output. | 0 |
| | | 0 | Selects single edge controlled mode for PWM6. | |
| 8:7 | - | | Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined. | NA |
| 9 | PWMENA1 | 1 | The PWM1 output enabled. | 0 |
| | | 0 | The PWM1 output disabled. | |
| 10 | PWMENA2 | 1 | The PWM2 output enabled. | 0 |
| | | 0 | The PWM2 output disabled. | |
| 11 | PWMENA3 | 1 | The PWM3 output enabled. | 0 |
| | | 0 | The PWM3 output disabled. | |
| 12 | PWMENA4 | 1 | The PWM4 output enabled. | 0 |
| | | 0 | The PWM4 output disabled. | |
| 13 | PWMENA5 | 1 | The PWM5 output enabled. | 0 |
| | | 0 | The PWM5 output disabled. | |
| 14 | PWMENA6 | 1 | The PWM6 output enabled. | 0 |
| | | 0 | The PWM6 output disabled. | |
| 31:15 | Unused | | Unused, always zero. | NA |

**Table 490: PWM Latch Enable Register (PWM1LER - address 0xE001 8050) bit description**

| Bit | Symbol | Description | Reset Value |
|---|---|---|---|
| 0 | Enable PWM Match 0 Latch | Writing a one to this bit allows the last value written to the PWM Match 0 register to be become effective when the timer is next reset by a PWM Match event. See Section 24–7.4 “PWM Match Control Register (PWM1MCR - 0xE001 8014)”. | 0 |
| 1 | Enable PWM Match 1 Latch | Writing a one to this bit allows the last value written to the PWM Match 1 register to be become effective when the timer is next reset by a PWM Match event. See Section 24–7.4 “PWM Match Control Register (PWM1MCR - 0xE001 8014)”. | 0 |
| 2 | Enable PWM Match 2 Latch | Writing a one to this bit allows the last value written to the PWM Match 2 register to be become effective when the timer is next reset by a PWM Match event. See Section 24–7.4 “PWM Match Control Register (PWM1MCR - 0xE001 8014)”. | 0 |
| 3 | Enable PWM Match 3 Latch | Writing a one to this bit allows the last value written to the PWM Match 3 register to be become effective when the timer is next reset by a PWM Match event. See Section 24–7.4 “PWM Match Control Register (PWM1MCR - 0xE001 8014)”. | 0 |
| 4 | Enable PWM Match 4 Latch | Writing a one to this bit allows the last value written to the PWM Match 4 register to be become effective when the timer is next reset by a PWM Match event. See Section 24–7.4 “PWM Match Control Register (PWM1MCR - 0xE001 8014)”. | 0 |
| 5 | Enable PWM Match 5 Latch | Writing a one to this bit allows the last value written to the PWM Match 5 register to be become effective when the timer is next reset by a PWM Match event. See Section 24–7.4 “PWM Match Control Register (PWM1MCR - 0xE001 8014)”. | 0 |
| 6 | Enable PWM Match 6 Latch | Writing a one to this bit allows the last value written to the PWM Match 6 register to be become effective when the timer is next reset by a PWM Match event. See Section 24–7.4 “PWM Match Control Register (PWM1MCR - 0xE001 8014)”. | 0 |
| 7 | - | Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined. | NA |

| | | | | |
|---|---|---|---|---|
| MR0 | Match Register 0. MR0 can be enabled in the MCR to reset the TC, stop both the TC and PC, and/or generate an interrupt when it matches the TC. In addition, a match between this value and the TC sets any PWM output that is in single-edge mode, and sets PWM1 if it's in double-edge mode. | R/W | 0 | PWM1MR0 - 0xE001 8018 |
| MR1 | Match Register 1. MR1 can be enabled in the MCR to reset the TC, stop both the TC and PC, and/or generate an interrupt when it matches the TC. In addition, a match between this value and the TC clears PWM1 in either edge mode, and sets PWM2 if it's in double-edge mode. | R/W | 0 | PWM1MR1 - 0xE001 801C |
| MR2 | Match Register 2. MR2 can be enabled in the MCR to reset the TC, stop both the TC and PC, and/or generate an interrupt when it matches the TC. In addition, a match between this value and the TC clears PWM2 in either edge mode, and sets PWM3 if it's in double-edge mode. | R/W | 0 | PWM1MR2 - 0xE001 8020 |
| MR3 | Match Register 3. MR3 can be enabled in the MCR to reset the TC, stop both the TC and PC, and/or generate an interrupt when it matches the TC. In addition, a match between this value and the TC clears PWM3 in either edge mode, and sets PWM4 if it's in double-edge mode. | R/W | 0 | PWM1MR3 - 0xE001 8024 |
| MR4 | Match Register 4. MR4 can be enabled in the MCR to reset the TC, stop both the TC and PC, and/or generate an interrupt when it matches the TC. In addition, a match between this value and the TC clears PWM4 in either edge mode, and sets PWM5 if it's in double-edge mode. | R/W | 0 | PWM1MR - 0xE001 8040 |
| MR5 | Match Register 5. MR5 can be enabled in the MCR to reset the TC, stop both the TC and PC, and/or generate an interrupt when it matches the TC. In addition, a match between this value and the TC clears PWM5 in either edge mode, and sets PWM6 if it's in double-edge mode. | R/W | 0 | PWM1MR - 0xE001 8044 |
| MR6 | Match Register 6. MR6 can be enabled in the MCR to reset the TC, stop both the TC and PC, and/or generate an interrupt when it matches the TC. In addition, a match between this value and the TC clears PWM6 in either edge mode. | R/W | 0 | PWM1MR - 0xE001 8048 |

## Table 480. Set and reset inputs for PWM Flip-Flops

| PWM Channel | Single Edge PWM (PWMSELn = 0) | | Double Edge PWM (PWMSELn = 1) | |
|---|---|---|---|---|
| | Set by | Reset by | Set by | Reset by |
| 1 | Match 0 | Match 1 | Match 0[1] | Match 1[1] |
| 2 | Match 0 | Match 2 | Match 1 | Match 2 |
| 3 | Match 0 | Match 3 | Match 2[2] | Match 3[2] |
| 4 | Match 0 | Match 4 | Match 3 | Match 4 |
| 5 | Match 0 | Match 5 | Match 4[2] | Match 5[2] |
| 6 | Match 0 | Match 6 | Match 5 | Match 6 |