Microcontrôleurs & Applications
Bus CAN

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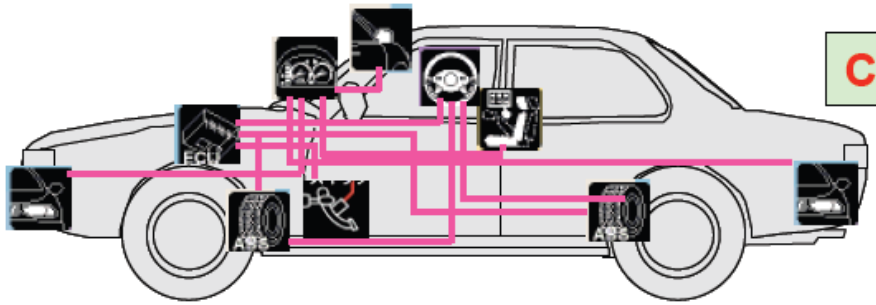
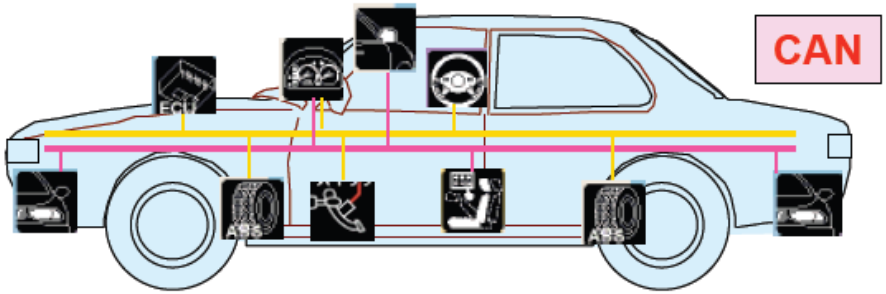
Bus de Terrain

- Rôle: Permettre un échange de données entre différents composants d'un système à un coût et une complexité réduits



Câblage traditionnel

Câbles : 2000 m, > 50 kg



CAN

2 câbles pour l'alimentation électrique 12 V DC

1 paire torsadée pour les transferts d'informations

Bus de Terrain

- Domaines d'application
  - **Automobile**
  - **Aéronautique**
  - **Electronique grand public**
  - **…**
- Protocoles de communication
  - **I²C**
  - **CAN**
  - **LIN**
  - **FlexRay**
  - **…**

Caractéristiques

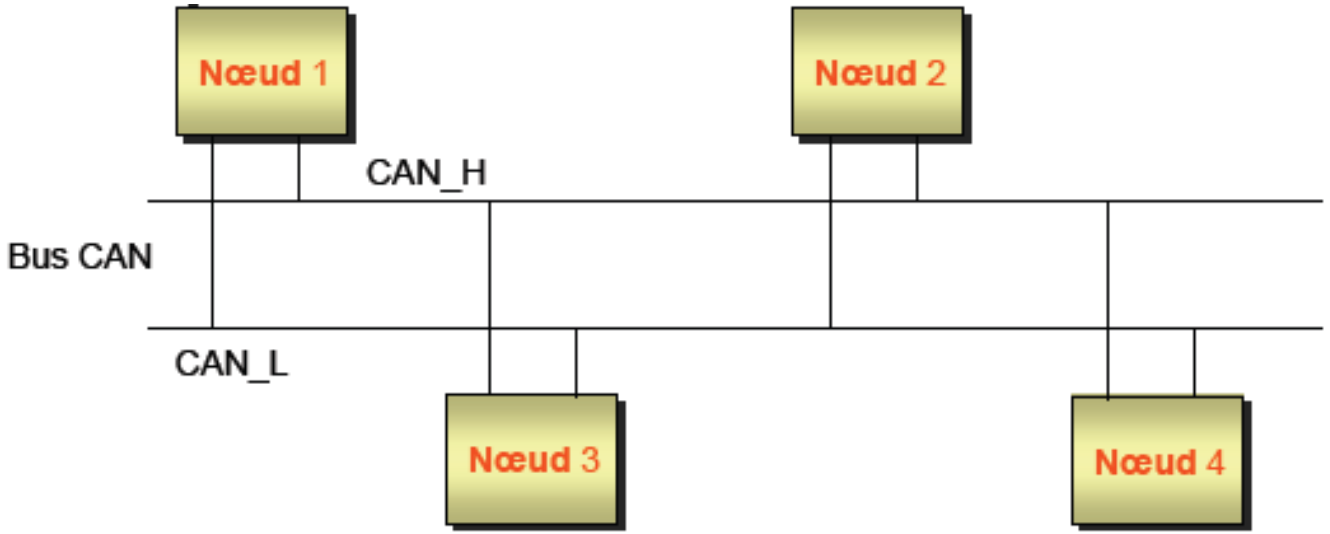
- Connectivité
  - **Combien de nœuds peut on connecter sur le bus**
- Débit
  - **Quel volume de données peut on transférer par seconde**
- Protocole
  - **Quelle est la forme du message transmis**
- Multimaître
  - **Plusieurs nœuds peuvent-ils émettre sur le bus**
- Taux d'erreur
  - **Quel est le nombre de bits erronés transmis**
- Sensibilité aux perturbations
  - **Le bus est-il sensible aux perturbations électromagnétiques de son environnement**

Bus CAN

- CAN: Controller Area Network
  - « Bus de terrain »
  - Crée par équipementier automobile BOSCH en 1980
  - Normalisé par ISO
    - CAN 2.0A ISO 11898
    - CAN 2.0B ISO 11519
- Introduit sur véhicules BMW 1989
  - Généralisé progressivement
  - Standard pour l'automobile et l'aéronautique
- Bibliographie CAN
  - http://uuu.enseirb.fr/~kadionik/formation/canbus/canbus.html
  - http://www.iufmrese.cict.fr/catalogue/2005/LimogesLT/diaporama/1-busCANtrame.ppt
  - Le Bus CAN, D. Paret, Dunod

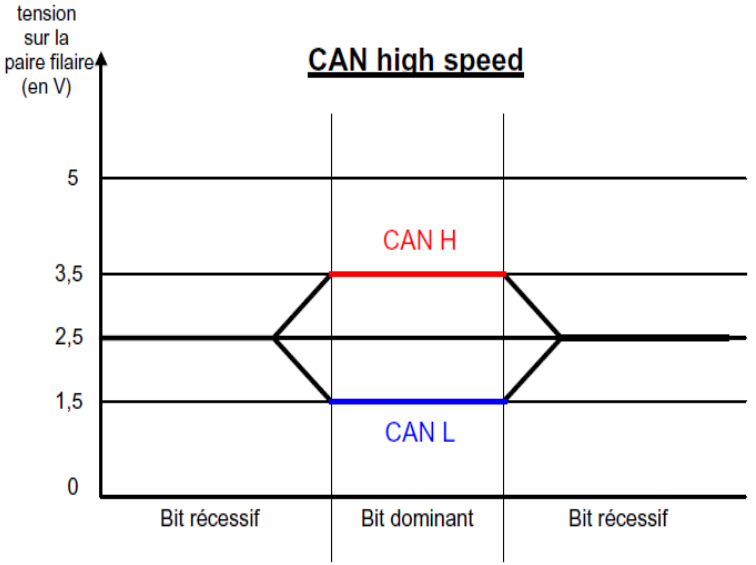
Bus CAN

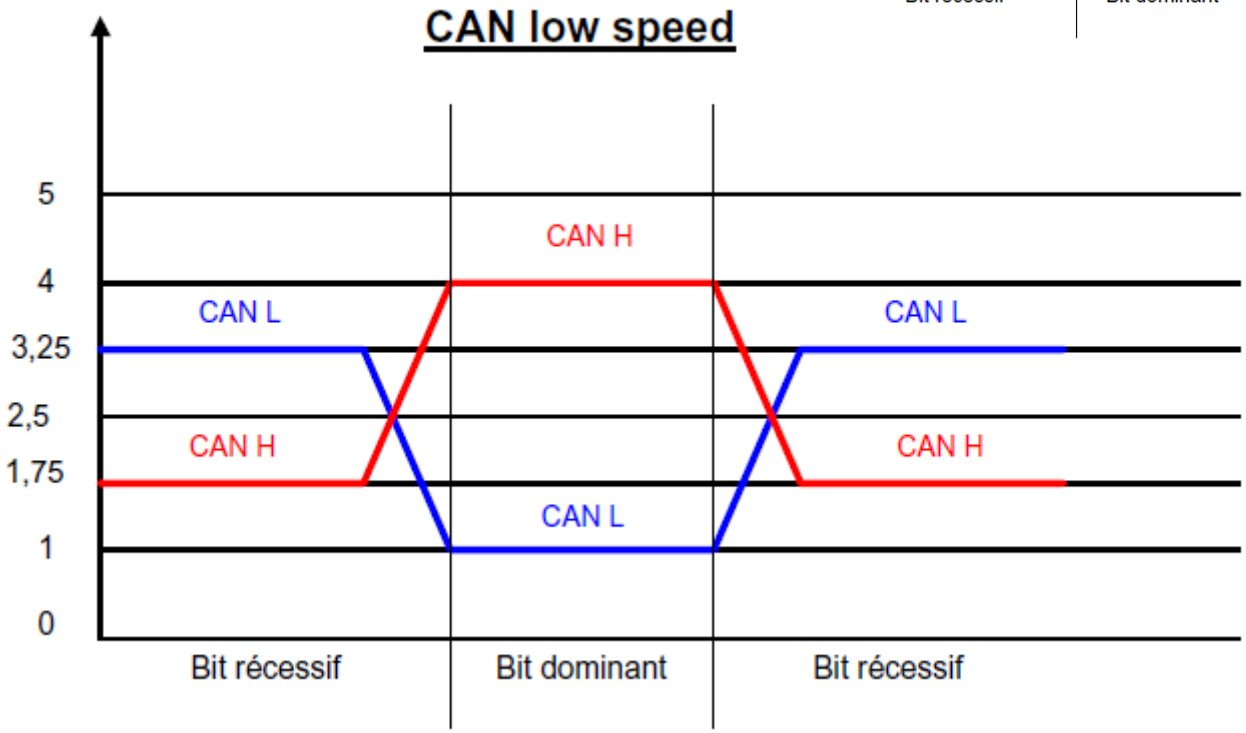
- Principe
  - **2 lignes de bus: CANL et CANH**
  - **Paire différentielle pour une meilleure résistance aux parasites**
  - **Niveau dominant: 0 / Niveau récessif: 1**



Bus CAN

- Deux normes
  - **Can High Speed**
  - **Can Low Speed**



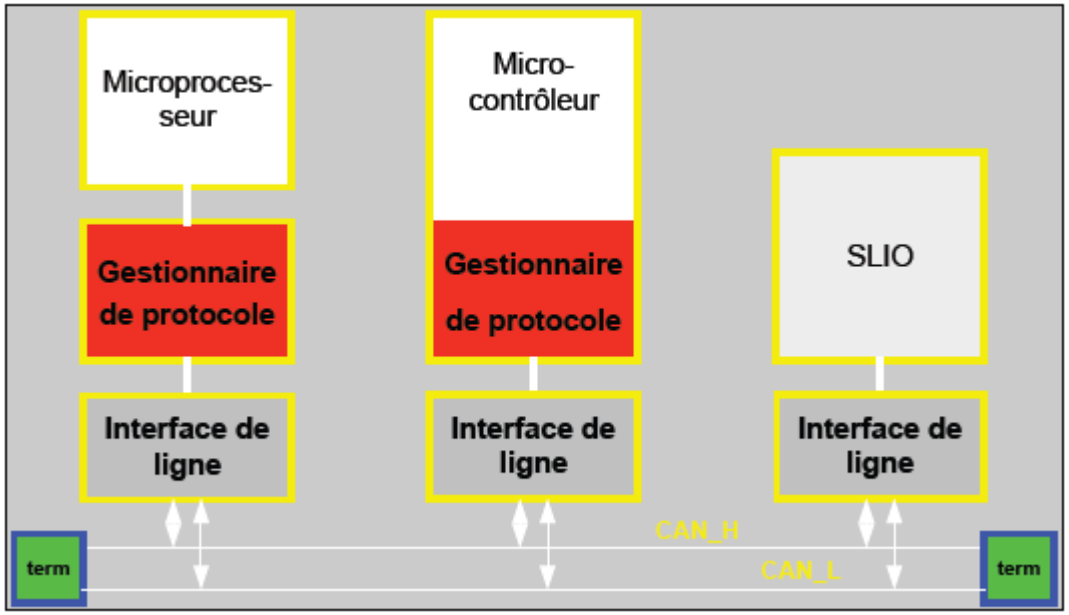


Bus CAN

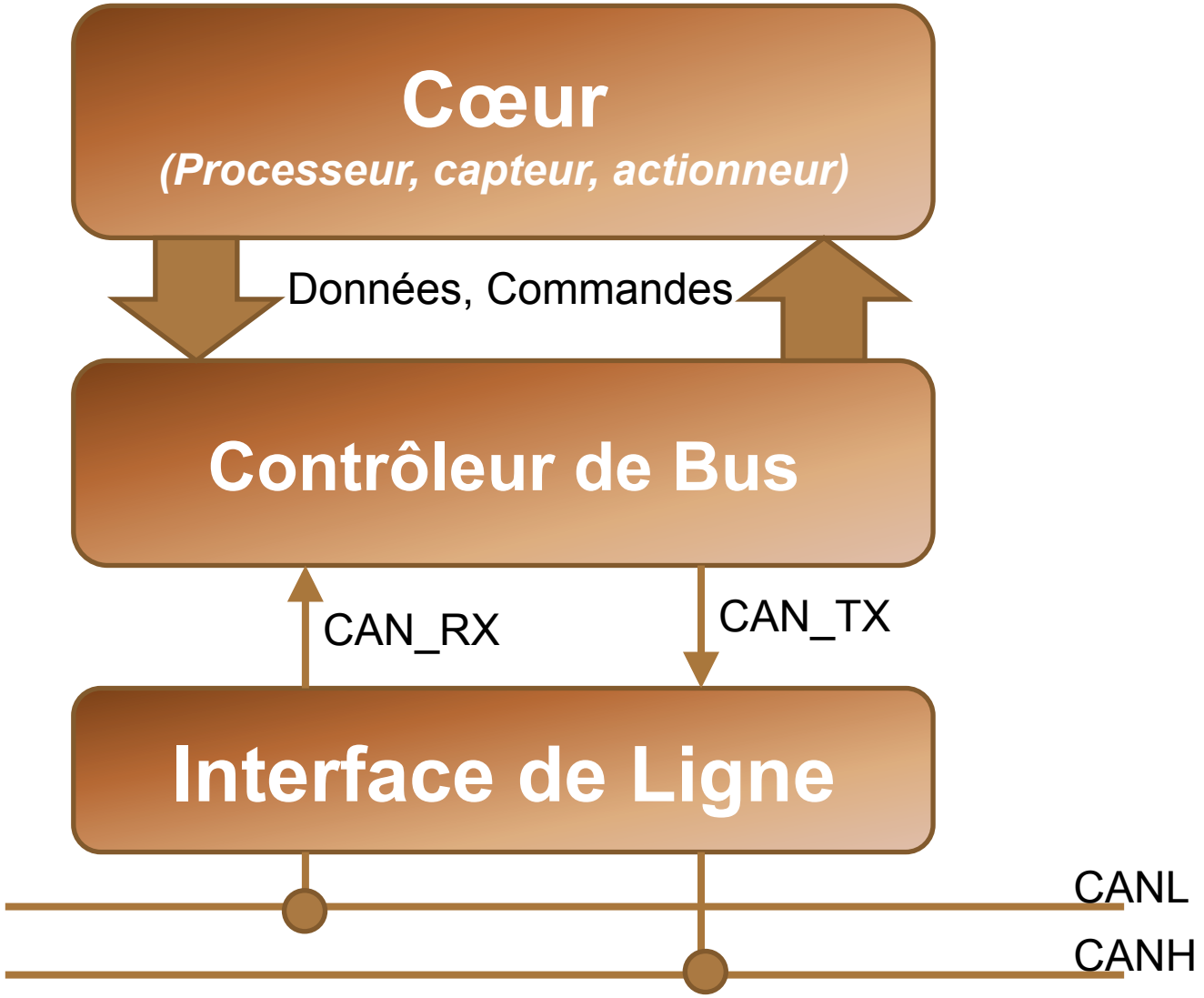
- Caractéristiques CAN High Speed / Low Speed

	CAN Low Speed	CAN High Speed
Débit	125 kbits/s	1Mbits/sec (60 m)
Nombre de Noeuds	Jusqu'à 20	Jusqu'à 30

- Architecture

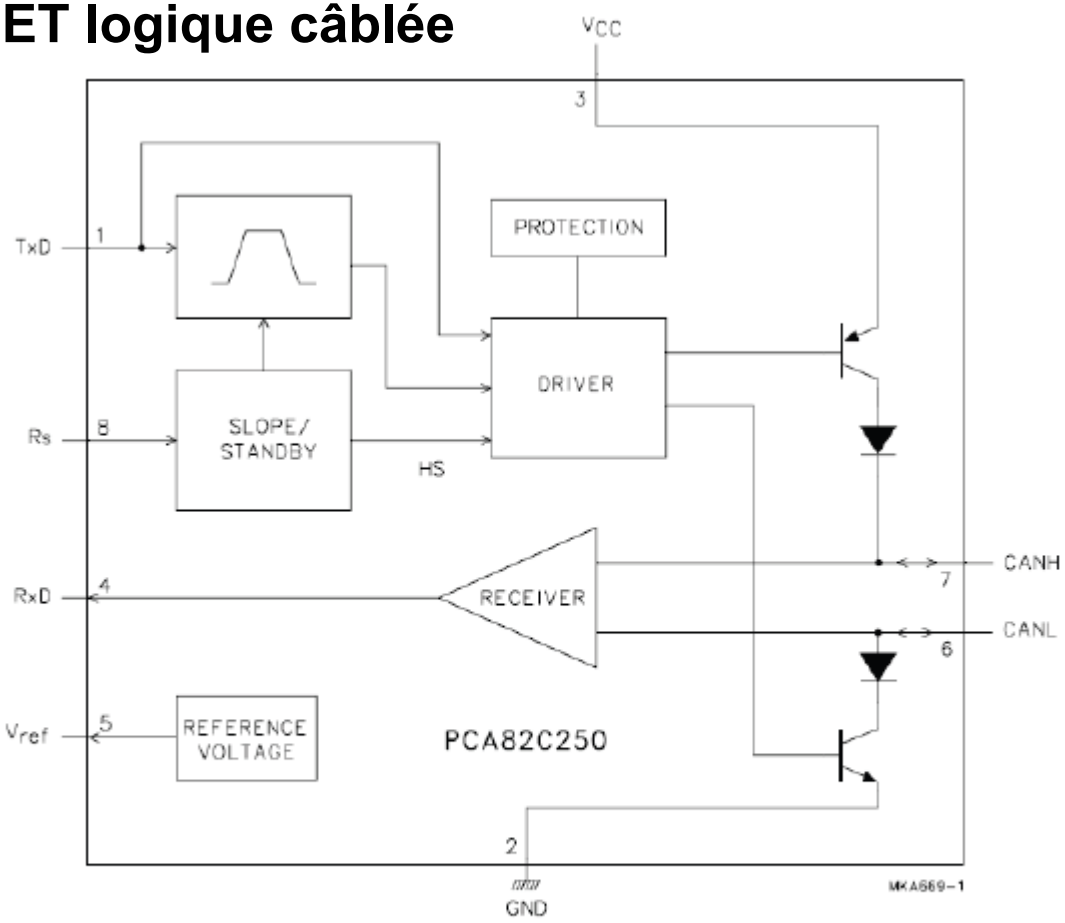


Architecture d'un Noeud



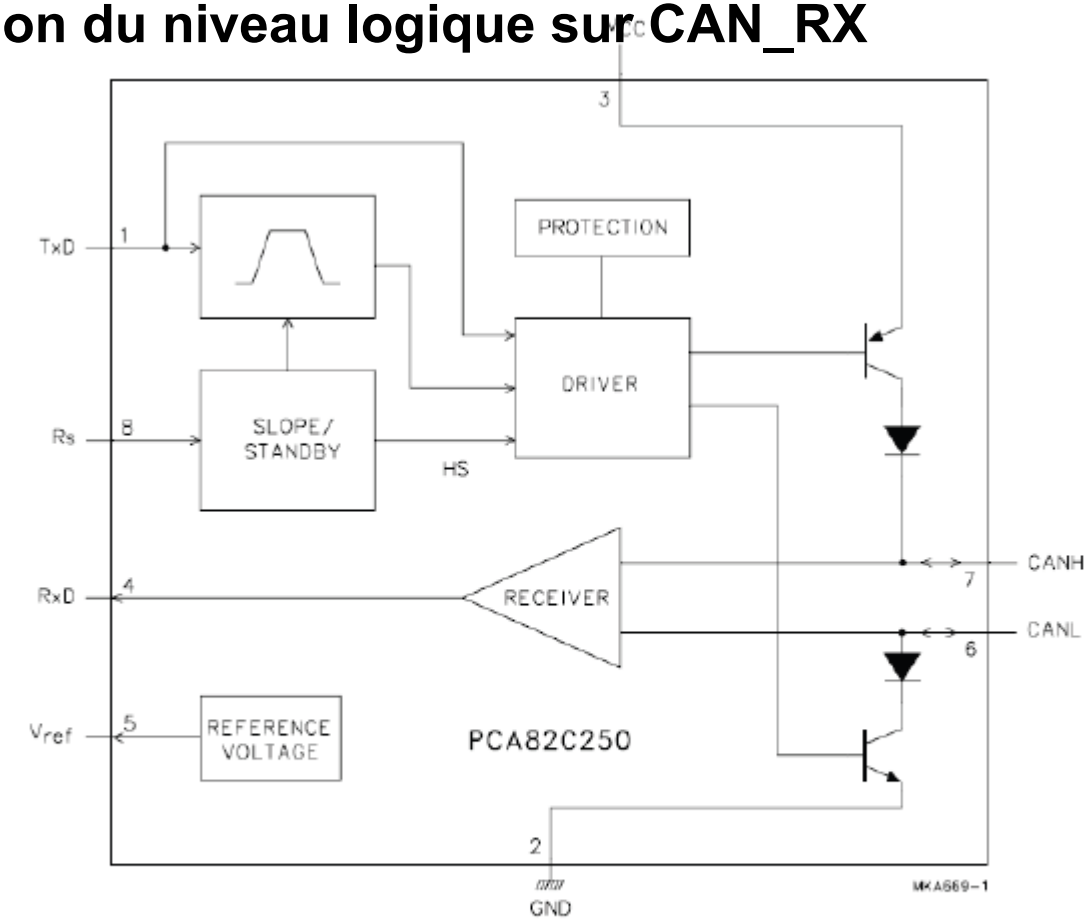
Interface de Ligne - Accès au Bus

- Circuit d'écriture
  - **Transistor collecteur/drain ouvert**
  - **Fonction ET logique câblée**



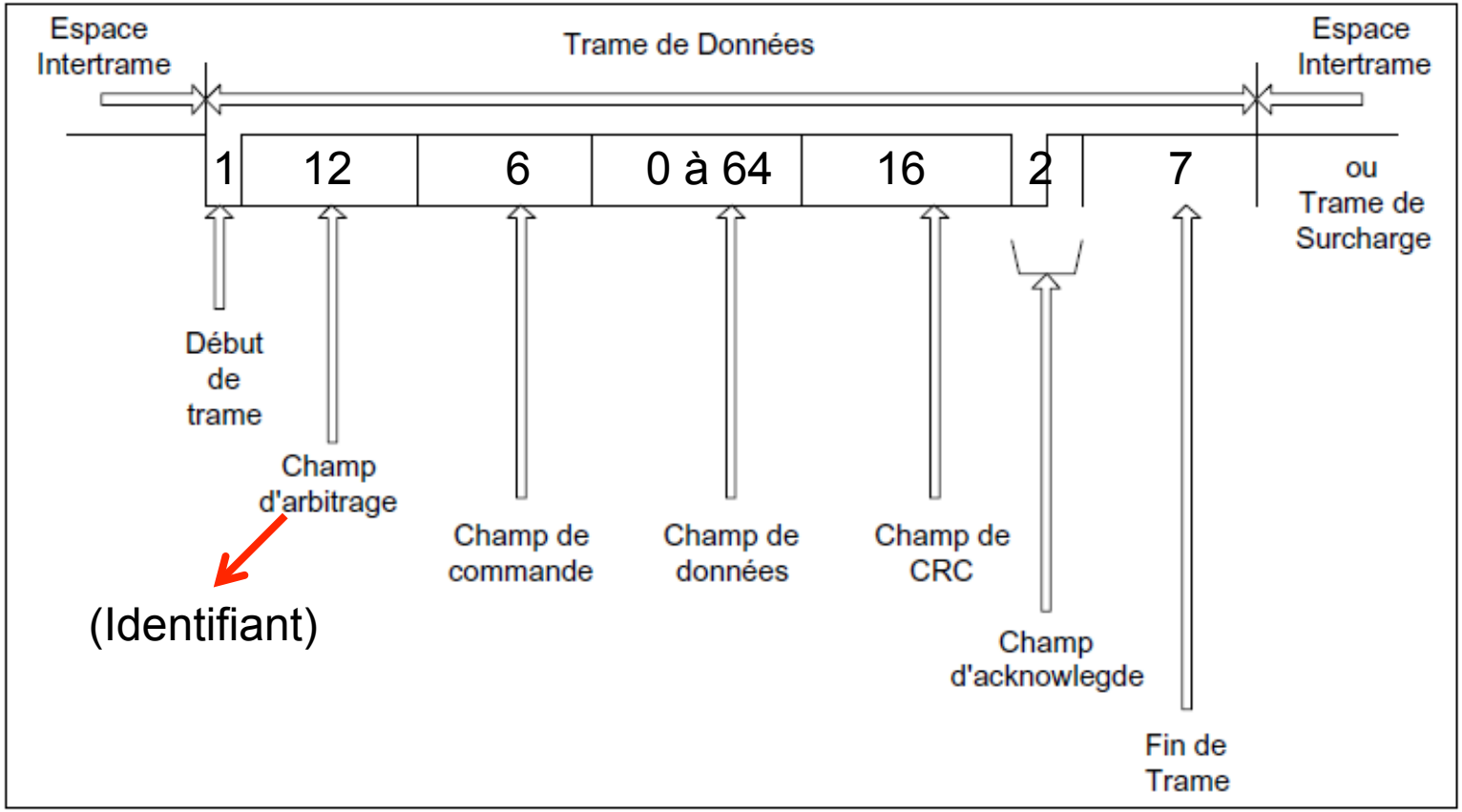
Interface de Ligne - Accès au Bus

- Circuit de lecture
  - **Comparateur entre CANH et CANL**
  - **Génération du niveau logique sur CAN_RX**



Protocole CAN

- Trame de Données

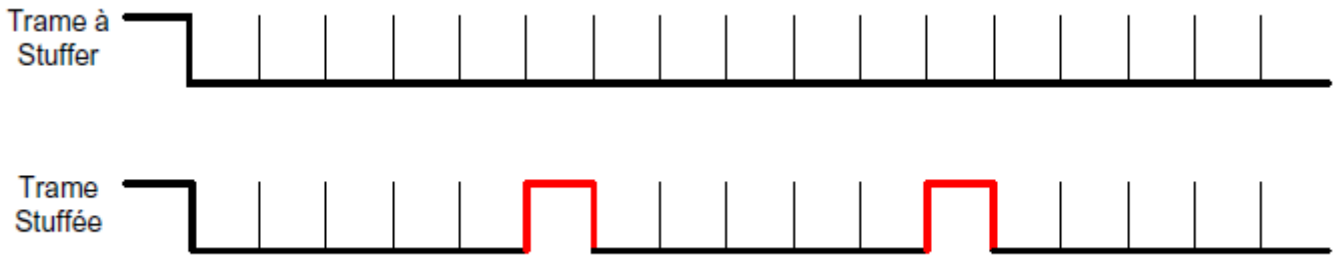


Protocole CAN

- Arbitrage
  - **Si deux nœuds émettent en même temps**
  - **Le nœud qui émet un 1 alors que l'autre émet 0 perd le contrôle du bus**
  - **Implémenté grâce au transistor en drain ouvert des circuits d'écriture des interface de ligne**

Protocole CAN

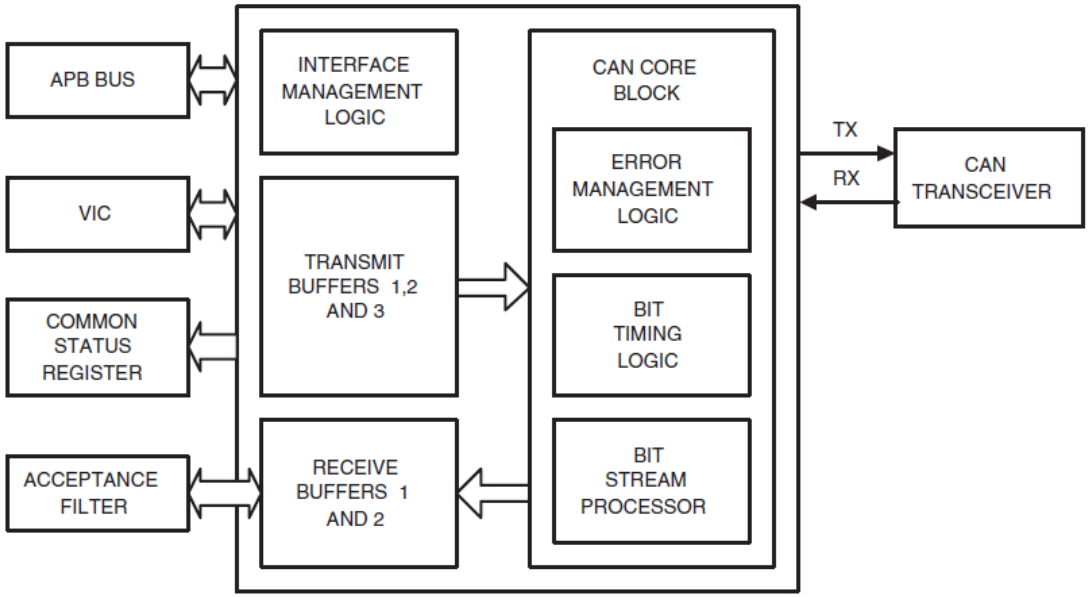
- Sûreté de la transmission
  - **Bit Stuffing:**
    - insertion de bits pour éviter de perdre la synchro.

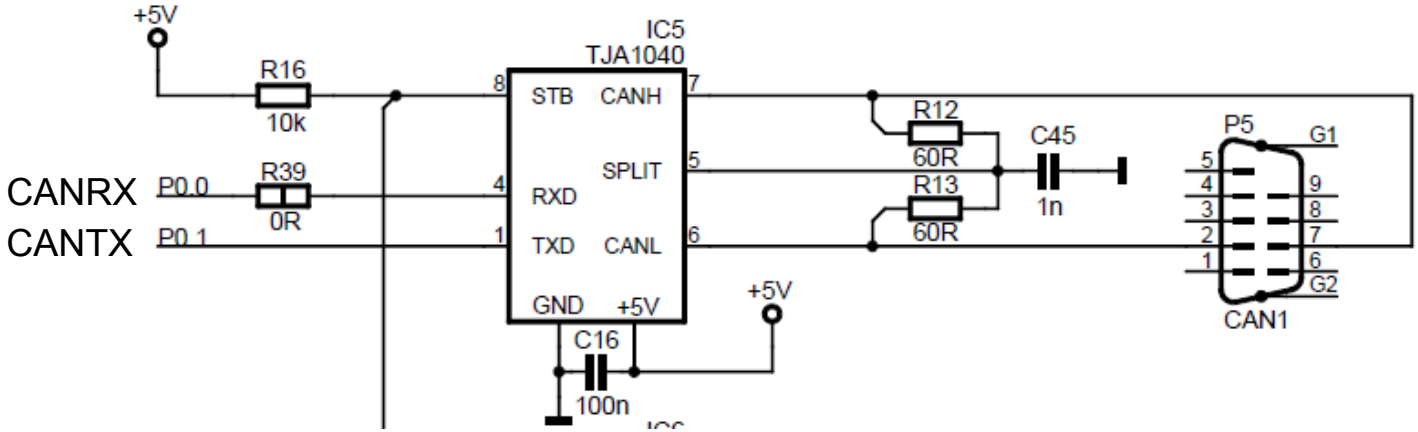


  - **CRC**
    - Calcul à la volée en réception d'un CRC
    - Comparaison avec le champ de CRC transmis
  - **Déconnexion automatique d'un nœud**
    - S'il provoque systématiquement des erreurs

Bus CAN et LPC2378 / Carte Keil

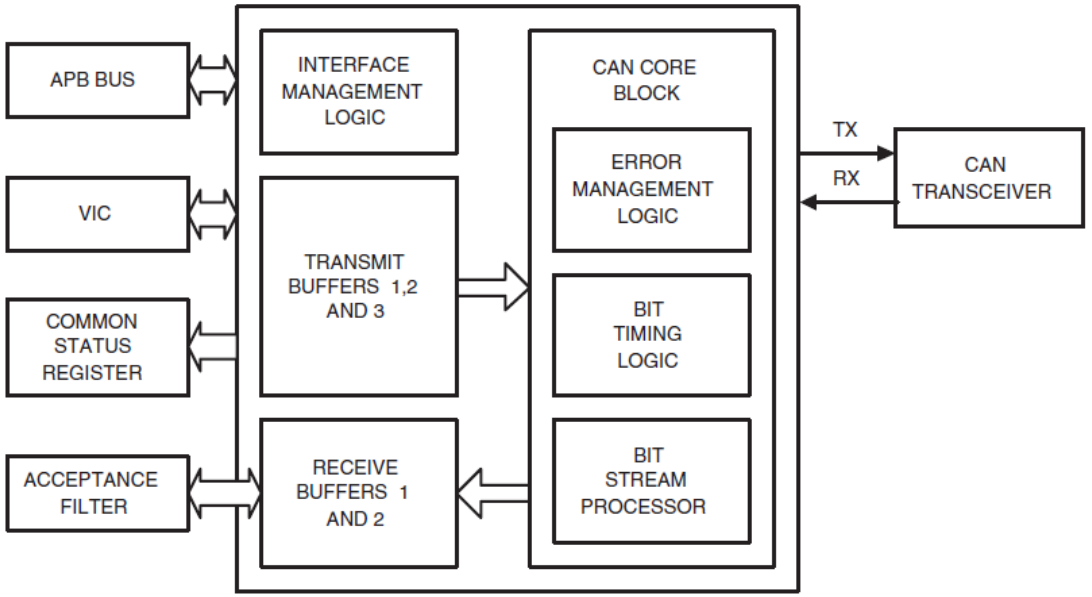
- Le LPC2378 possède 2 contrôleurs CAN





Bus CAN et LPC2378 / Carte Keil

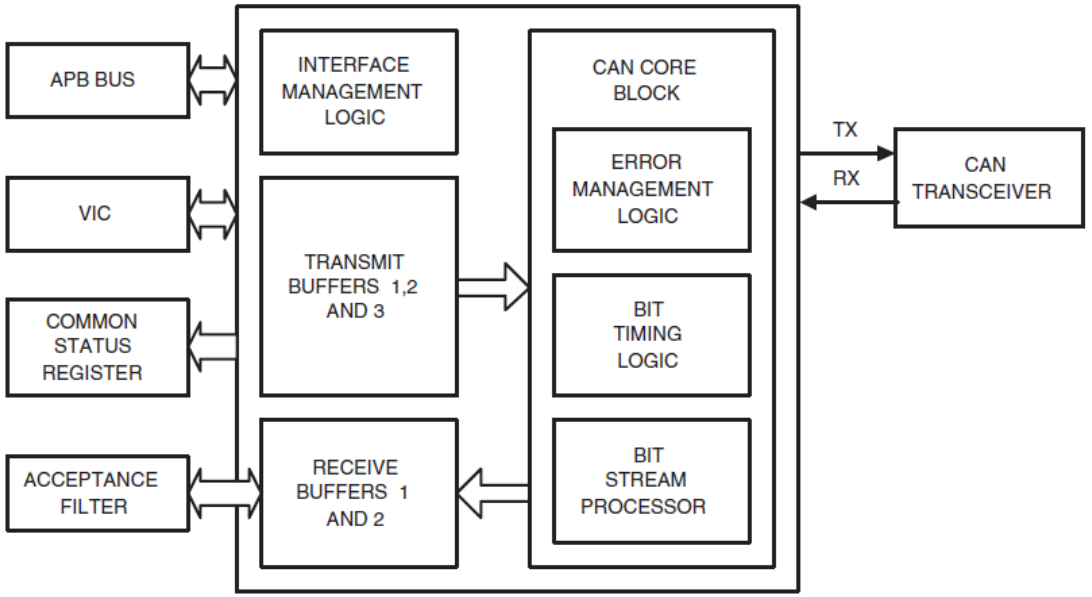
- Le LPC2378 possède 2 contrôleurs CAN



  - **Chaque contrôleur possède**
    - 3 buffers d'émission
    - 1 buffer de réception
    - 1 Filtre d'acceptation
      - Filtre les messages que le contrôleur va recevoir

Bus CAN et LPC2378 / Carte Keil

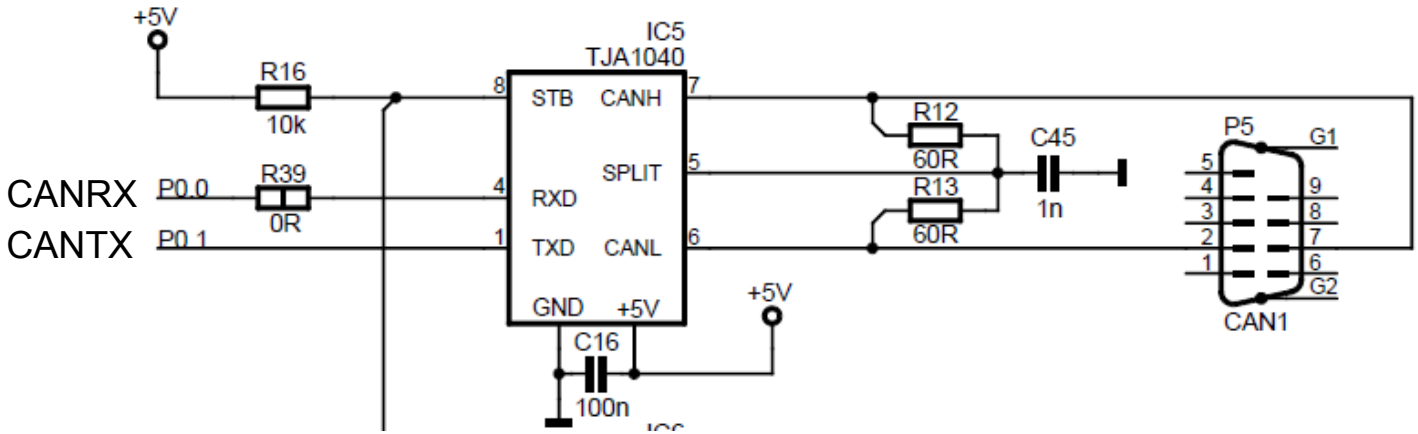
- Le LPC2378 possède 2 contrôleurs CAN



  - **CAN Core Block**
    - Génération de la trame de bit à envoyer
    - Gestion des timings du protocole CAN
    - Gestion des erreurs de transmission

Bus CAN et LPC2378 / Carte Keil

- Le LPC2378 possède 2 contrôleurs CAN
  - **Les lignes CAN_RX et CAN_TX sont connectées à l'interface ligne (CAN Transceiver)**
  - **L'interface génère les tensions correspondantes sur CANL et CANH**
  - **Connecteur de sortie de type DB9**



Filtre d'Acceptation

- Le filtre scrute les identifiants de tous les messages transitant sur le bus
- Il ne transmet au contrôleur que les messages correspondant à des identifiants « autorisés »
- Les autres messages sont ignorés
- Simplifie la gestion des messages par le contrôleur et évite des interruptions inutiles et systématiques

Configuration du LPC2378

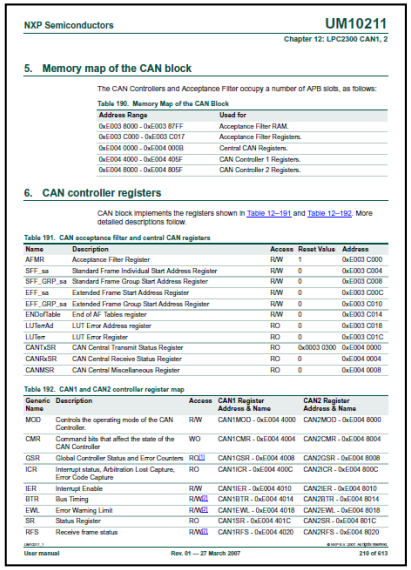
- Activation de l'horloge du contrôleur CAN
  - Les horloges des contrôleurs CAN ne sont pas activées par défaut
  - Modifier le registre PCONP en conséquence

- Sélection des fonction CAN sur les pattes d'E/S
  - En fonction du brochage sur la carte
    - CAN1 sur les broches P0.0 et P0.1
    - CAN2 sur les broches P0.4 et P0.5
  - Modifier les registres PINSEL correspondant pour choisir la fonction CAN

Registres des contrôleurs CAN

- La liste des registres relatifs aux contrôleurs CAN occupe 3 pages du datasheet NXP !

- Seule une partie de ces registres est utilisée pour effectuer des transmissions basiques



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5. Memory map of the CAN block

The CAN Controllers and Acceptance Filter occupy a number of APB slots, as follows:

Table 190. Memory Map of the CAN Block

Address Range	Used for
0xE003 8000 - 0xE003 87FF	Acceptance Filter RAM.
0xE003 C000 - 0xE003 C017	Acceptance Filter Registers.
0xE004 0000 - 0xE004 0093	Central CAN Registers.
0xE004 4000 - 0xE004 405F	CAN Controller 1 Registers.
0xE004 8000 - 0xE004 805F	CAN Controller 2 Registers.

6. CAN controller registers

CAN block implements the registers shown in Table 12–191 and Table 12–192. More detailed descriptions follow.

Table 191. CAN acceptance filter and central CAN registers

Name	Description	Access	Reset Value	Address
AFMR	Acceptance Filter Register	R/W	1	0xE003 C000
SFF_sa	Standard Frame Individual Start Address Register	R/W	0	0xE003 C004
SFF_GRP_sa	Standard Frame Group Start Address Register	R/W	0	0xE003 C008
EFF_sa	Extended Frame Start Address Register	R/W	0	0xE003 C00C
EFF_GRP_sa	Extended Frame Group Start Address Register	R/W	0	0xE003 C010
ENDofTable	End of AF Tables register	R/W	0	0xE003 C014
LUTerrAd	LUT Error Address register	RO	0	0xE003 C018
LUTerr	LUT Error Register	RO	0	0xE003 C01C
CANTxSR	CAN Central Transmit Status Register	RO	0x0003 0300	0xE004 0000
CANRxSR	CAN Central Receive Status Register	RO	0	0xE004 0004
CANMSR	CAN Central Miscellaneous Register	RO	0	0xE004 0008

Table 192. CAN1 and CAN2 controller register map

Generic Name	Description	Access	CAN1 Register Address & Name	CAN2 Register Address & Name
MOD	Controls the operating mode of the CAN Controller.	R/W	CAN1MOD - 0xE004 4000	CAN2MOD - 0xE004 8000
CMR	Command bits that affect the state of the CAN Controller	WO	CAN1CMR - 0xE004 4004	CAN2CMR - 0xE004 8004
GSR	Global Controller Status and Error Counters	RO[1]	CAN1GSR - 0xE004 4008	CAN2GSR - 0xE004 8008
ICR	Interrupt status, Arbitration Lost Capture, Error Code Capture	RO	CAN1ICR - 0xE004 400C	CAN2ICR - 0xE004 800C
IER	Interrupt Enable	R/W	CAN1IER - 0xE004 4010	CAN2IER - 0xE004 8010
BTR	Bus Timing	R/W[2]	CAN1BTR - 0xE004 4014	CAN2BTR - 0xE004 8014
EWL	Error Warning Limit	R/W[2]	CAN1EWL - 0xE004 4018	CAN2EWL - 0xE004 8018
SR	Status Register	RO	CAN1SR - 0xE004 401C	CAN2SR - 0xE004 801C
RFS	Receive frame status	R/W[2]	CAN1RFS - 0xE004 4020	CAN2RFS - 0xE004 8020

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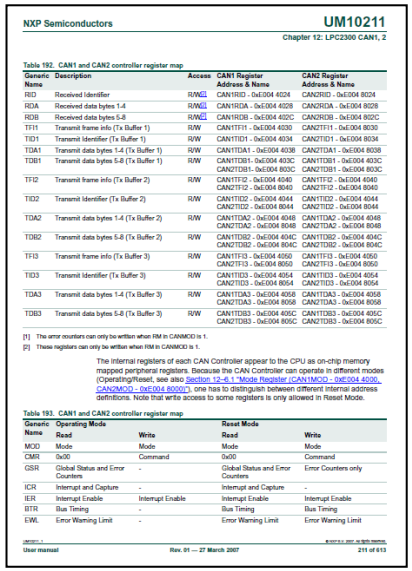

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Table 192. CAN1 and CAN2 controller register map

Generic Name	Description	Access	CAN1 Register Address & Name	CAN2 Register Address & Name
RID	Received Identifier	R/W[2]	CAN1RID - 0xE004 4024	CAN2RID - 0xE004 8024
RDA	Received data bytes 1-4	R/W[2]	CAN1RDA - 0xE004 4028	CAN2RDA - 0xE004 8028
RDB	Received data bytes 5-8	R/W[2]	CAN1RDB - 0xE004 402C	CAN2RDB - 0xE004 802C
TFI1	Transmit frame info (Tx Buffer 1)	R/W	CAN1TFI1 - 0xE004 4030	CAN2TFI1 - 0xE004 8030
TID1	Transmit Identifier (Tx Buffer 1)	R/W	CAN1TID1 - 0xE004 4034	CAN2TID1 - 0xE004 8034
TDA1	Transmit data bytes 1-4 (Tx Buffer 1)	R/W	CAN1TDA1 - 0xE004 4038	CAN2TDA1 - 0xE004 8038
TDB1	Transmit data bytes 5-8 (Tx Buffer 1)	R/W	CAN1TDB1 - 0xE004 403C CAN2TDB1 - 0xE004 803C	CAN1TDB1 - 0xE004 403C CAN2TDB1 - 0xE004 803C
TFI2	Transmit frame info (Tx Buffer 2)	R/W	CAN1TFI2 - 0xE004 4040 CAN2TFI2 - 0xE004 8040	CAN1TFI2 - 0xE004 4040 CAN2TFI2 - 0xE004 8040
TID2	Transmit Identifier (Tx Buffer 2)	R/W	CAN1TID2 - 0xE004 4044 CAN2TID2 - 0xE004 8044	CAN1TID2 - 0xE004 4044 CAN2TID2 - 0xE004 8044
TDA2	Transmit data bytes 1-4 (Tx Buffer 2)	R/W	CAN1TDA2 - 0xE004 4048 CAN2TDA2 - 0xE004 8048	CAN1TDA2 - 0xE004 4048 CAN2TDA2 - 0xE004 8048
TDB2	Transmit data bytes 5-8 (Tx Buffer 2)	R/W	CAN1TDB2 - 0xE004 404C CAN2TDB2 - 0xE004 804C	CAN1TDB2 - 0xE004 404C CAN2TDB2 - 0xE004 804C
TFI3	Transmit frame info (Tx Buffer 3)	R/W	CAN1TFI3 - 0xE004 4050 CAN2TFI3 - 0xE004 8050	CAN1TFI3 - 0xE004 4050 CAN2TFI3 - 0xE004 8050
TID3	Transmit Identifier (Tx Buffer 3)	R/W	CAN1TID3 - 0xE004 4054 CAN2TID3 - 0xE004 8054	CAN1TID3 - 0xE004 4054 CAN2TID3 - 0xE004 8054
TDA3	Transmit data bytes 1-4 (Tx Buffer 3)	R/W	CAN1TDA3 - 0xE004 4058 CAN2TDA3 - 0xE004 8058	CAN1TDA3 - 0xE004 4058 CAN2TDA3 - 0xE004 8058
TDB3	Transmit data bytes 5-8 (Tx Buffer 3)	R/W	CAN1TDB3 - 0xE004 405C CAN2TDB3 - 0xE004 805C	CAN1TDB3 - 0xE004 405C CAN2TDB3 - 0xE004 805C

[1] The error counters can only be written when RM in CANMOD is 1.
[2] These registers can only be written when RM in CANMOD is 1.

The internal registers of each CAN Controller appear to the CPU as on-chip memory mapped peripheral registers. Because the CAN Controller can operate in different modes (Operating/Reset, see also Section 12–6.1 "Mode Register (CAN1MOD - 0xE004 4000, CAN2MOD - 0xE004 8000)"), one has to distinguish between different internal address definitions. Note that write access to some registers is only allowed in Reset Mode.

Table 193. CAN1 and CAN2 controller register map

Generic Name	Operating Mode		Reset Mode	
	Read	Write	Read	Write
MOD	Mode	Mode	Mode	Mode
CMR	0x00	Command	0x00	Command
GSR	Global Status and Error Counters	-	Global Status and Error Counters	Error Counters only
ICR	Interrupt and Capture	-	Interrupt and Capture	-
IER	Interrupt Enable	Interrupt Enable	Interrupt Enable	Interrupt Enable
BTR	Bus Timing	-	Bus Timing	Bus Timing
EWL	Error Warning Limit	-	Error Warning Limit	Error Warning Limit

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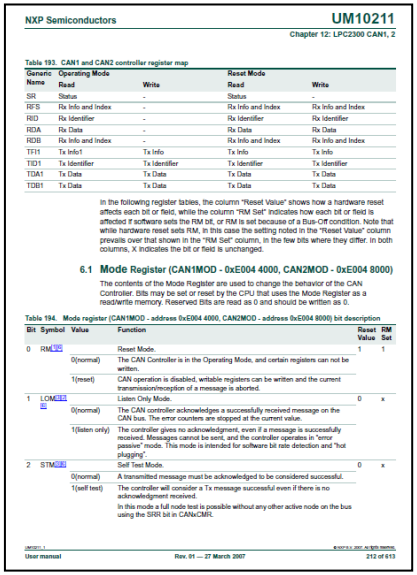

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Table 193. CAN1 and CAN2 controller register map

Generic Name	Operating Mode		Reset Mode	
	Read	Write	Read	Write
SR	Status	-	Status	-
RFS	Rx Info and Index	-	Rx Info and Index	Rx Info and Index
RID	Rx Identifier	-	Rx Identifier	Rx Identifier
RDA	Rx Data	-	Rx Data	Rx Data
RDB	Rx Info and Index	-	Rx Info and Index	Rx Info and Index
TFI1	Tx Info1	Tx Info	Tx Info	Tx Info
TID1	Tx Identifier	Tx Identifier	Tx Identifier	Tx Identifier
TDA1	Tx Data	Tx Data	Tx Data	Tx Data
TDB1	Tx Data	Tx Data	Tx Data	Tx Data

In the following register tables, the column "Reset Value" shows how a hardware reset affects each bit or field, while the column "RM Set" indicates how each bit or field is affected if software sets the RM bit, or RM is set because of a Bus-Off condition. Note that while hardware reset sets RM, in this case the setting noted in the "Reset Value" column prevails over that shown in the "RM Set" column, in the few bits where they differ. In both columns, X indicates the bit or field is unchanged.

6.1 Mode Register (CAN1MOD - 0xE004 4000, CAN2MOD - 0xE004 8000)

The contents of the Mode Register are used to change the behavior of the CAN Controller. Bits may be set or reset by the CPU that uses the Mode Register as a read/write memory. Reserved Bits are read as 0 and should be written as 0.

Table 194. Mode register (CAN1MOD - address 0xE004 4000, CAN2MOD - address 0xE004 8000) bit description

Bit	Symbol	Value	Function	Reset Value	RM Set
0	RM[1][2]		Reset Mode.	1	1
		0(normal)	The CAN Controller is in the Operating Mode, and certain registers can not be written.		
		1(reset)	CAN operation is disabled, writable registers can be written and the current transmission/reception of a message is aborted.		
1	LOM[1][2]		Listen Only Mode.	0	x
		0(normal)	The CAN controller acknowledges a successfully received message on the CAN bus. The error counters are stopped at the current value.		
		1(listen only)	The controller gives no acknowledgment, even if a message is successfully received. Messages cannot be sent, and the controller operates in "error passive" mode. This mode is intended for software bit rate detection and "hot plugging".		
2	STM[2]		Self Test Mode.	0	x
		0(normal)	A transmitted message must be acknowledged to be considered successful.		
		1(self test)	The controller will consider a Tx message successful even if there is no acknowledgment received. In this mode a full node test is possible without any other active node on the bus using the SRR bit in CANxCMR.		

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Registres des contrôleurs CAN

- Registres de Configuration
  - **Fixer le fonctionnement global du contrôleur**
- Registres du Filtre d'Acceptation
  - **Permet de Filtrer certains messages à l'entrée du contrôleur**
- Registres de Statut
  - **Etat du contrôleur et de ses buffers d'E/S**
- Registres de Transfert
  - **Fonctionnement et données dans les buffers d'émission et de réception**

Registres de Configuration

- CANxMOD
- CANxBTR
- CANxIER

Registre CANxMOD

- Fixe le mode de fonctionnement du contrôleur

- Registre 8 bits
  - Bit 0: Mode Reset
    - Permet d'écrire dans les autres registres de config.

Table 194. Mode register (CAN1MOD - address 0xE004 4000, CAN2MOD - address 0xE004 8000) bit description

Bit	Symbol	Value	Function	Reset Value
0	RM[1][6]		Reset Mode.	1
		0(normal)	The CAN Controller is in the Operating Mode, and certain registers can not be written.	
		1(reset)	CAN operation is disabled, writable registers can be written and the current transmission/reception of a message is aborted.	

  - Autres Bits: permettent de passer en mode
    - Veille (Sleep)
    - Ecoute Seule (Listen Only)
    - Test, etc…

Registre CANxBTR

- Précise les timings mis en œuvre sur le bus
  - **BRP: Fixe la période d'horloge du contrôleur**
  - **TESG1/TESG2: Précise le point d'échantillonnage**

Table 199. Bus Timing Register (CAN1BTR - address 0xE004 4014, CAN2BTR - address 0xE004 8014) bit description

Bit	Symbol	Value	Function	Reset Value
9:0	BRP		Baud Rate Prescaler. The APB clock is divided by (this value plus one) to produce the CAN clock.	0
13:10	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
15:14	SJW		The Synchronization Jump Width is (this value plus one) CAN clocks.	0
19:16	TESG1		The delay from the nominal Sync point to the sample point is (this value plus one) CAN clocks.	1100
22:20	TESG2		The delay from the sample point to the next nominal sync point is (this value plus one) CAN clocks. The nominal CAN bit time is (this value plus the value in TSEG1 plus 3) CAN clocks.	001
23	SAM		Sampling	
		0	The bus is sampled once (recommended for high speed buses)	0
		1	The bus is sampled 3 times (recommended for low to medium speed buses to filter spikes on the bus-line)	

Registre CANxIER

- Configuration des interruptions CAN
  - **Déclenchement d'une interruption sur**
    - Réception d'un message (Bit 0)
    - Transmission du message stocké dans les TxBuffers (Bits 1, 9 et 10)

Table 198. Interrupt Enable Register (CAN1IER - address 0xE004 4010, CAN2IER - address 0xE004 8010) bit description

Bit	Symbol	Function	Reset Value	RM Set
0	RIE	Receiver Interrupt Enable. When the Receive Buffer Status is 'full', the CAN Controller requests the respective interrupt.	0	X
1	TIE1	Transmit Interrupt Enable for Buffer1. When a message has been successfully transmitted out of TXB1 or Transmit Buffer 1 is accessible again (e.g. after an Abort Transmission command), the CAN Controller requests the respective interrupt.	0	X

Registre CANxIER

- Configuration des interruptions CAN
  - **Déclenchement d'une interruption sur**
    - En cas d'erreur de transmission (Bits 2, 5, 7.)
    - Etc…

Table 198. Interrupt Enable Register (CAN1IER - address 0xE004 4010, CAN2IER - address 0xE004 8010) bit description

Bit	Symbol	Function	Reset Value	RM Set
2	EIE	Error Warning Interrupt Enable. If the Error or Bus Status change (see Status Register), the CAN Controller requests the respective interrupt.	0	X
3	DOIE	Data Overrun Interrupt Enable. If the Data Overrun Status bit is set (see Status Register), the CAN Controller requests the respective interrupt.	0	X
4	WUIE	Wake-Up Interrupt Enable. If the sleeping CAN controller wakes up, the respective interrupt is requested.	0	X
5	EPIE	Error Passive Interrupt Enable. If the error status of the CAN Controller changes from error active to error passive or vice versa, the respective interrupt is requested.	0	X
6	ALIE	Arbitration Lost Interrupt Enable. If the CAN Controller has lost arbitration, the respective interrupt is requested.	0	X
7	BEIE	Bus Error Interrupt Enable. If a bus error has been detected, the CAN Controller requests the respective interrupt.	0	X

Registres du Filtre d'Acceptation

- CANxAFMR

- 7 autres registres permettant de sélectionner
  - **Les identifiants reconnus par le contrôleur**
  - **Les identifiants ignorés par le contrôleur**

Registre CANxAFMR

- Config. du Filtre d'Acceptation des Messages
  - **Bits 1 et 0**
    - **01: Config du Filtre avec les identifiants à filtrer**
    - **10: Pas de filtrage (mode bypass)**
    - **00: Filtre opérationnel**

Table 217. Acceptance Filter Mode Register (AFMR - address 0xE003 C000) bit description

Bit	Symbol	Value	Description	Reset Value
0	AccOff[2]	1	if AccBP is 0, the Acceptance Filter is not operational. All Rx messages on all CAN buses are ignored.	1
1	AccBP[1]	1	All Rx messages are accepted on enabled CAN controllers. Software must set this bit before modifying the contents of any of the registers described below, and before modifying the contents of Lookup Table RAM in any way other than setting or clearing Disable bits in Standard Identifier entries. When both this bit and AccOff are 0, the Acceptance filter operates to screen received CAN Identifiers.	0

Registres de Statut

- Plusieurs registres de statut par contrôleur
  - **CANxGSR : Global Status Register**
  - **CANxSR : Status Register**
  - **CANTxSR : Transmit Status Register**
  - **CANRxSR : Receive Status Register**
  - **CANMxSR : Miscellaneous Status Register**

- Leurs informations sont parfois redondantes

Registre CANxSR

- Statut des buffers d'émission/réception
  - **En particulier Bit 2: Etat du Buffer d'émission 1**
    - 0: Buffer verrouillé
      - Car il essaie déjà d'envoyer un autre message sur le bus
    - 1: Buffer disponible
      - On peut envoyer un nouveau message

Table 201. Status Register (CAN1SR - address 0xE004 401C, CAN2SR - address 0xE004 801C) bit description

Bit	Symbol	Value	Function	Reset Value
0	RBS		Receive Buffer Status. This bit is identical to the RBS bit in the CANxGSR.	0
1	DOS		Data Overrun Status. This bit is identical to the DOS bit in the CANxGSR.	0
2	TBS1[1]		Transmit Buffer Status 1.	1
		0(locked)	Software cannot access the Tx Buffer 1 nor write to the corresponding CANxTFI, CANxTID, CANxTDA, and CANxTDB registers because a message is either waiting for transmission or is in transmitting process.	
		1(released)	Software may write a message into the Transmit Buffer 1 and its CANxTFI, CANxTID, CANxTDA, and CANxTDB registers.	
3	TCS1[2]		Transmission Complete Status.	1
		0(incomplete)	The previously requested transmission for Tx Buffer 1 is not complete.	
		1(complete)	The previously requested transmission for Tx Buffer 1 has been successfully completed.	
4	RS		Receive Status. This bit is identical to the RS bit in the GSR.	1

Registres de Transfert

- Permettent de
  - **Configurer le type de message à envoyer sur le bus**
    - CANxTIDn
    - CANxTFIn
    - CANxTDAn
    - CANxTDBn
  - **Envoyer ce message sur les buffers d'émission**
    - CANxCMR

Registre CANxTIDn

- Donne l'identifiant pour les messages émis par le buffer d'émission n (n=1,2,3)
  - **Inclus au début de chaque message envoyé par le contrôleur**
  - **En mode CAN standard, l'identifiant est sur 11 bits**

Table 208. Transfer Identifier Register (CAN1TID[1/2/3] - address 0xE004 40[34/44/54], CAN2TID[1/2/3] - address 0xE004 80[34/44/54]) bit description

Bit	Symbol	Function	Reset Value	RM Set
10:0	ID	The 11 bit Identifier to be sent in the next transmit message.	0	X
31:11	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA	

Registre CANxTFIn

- Registre de configuration de la trame de données à envoyer sur le buffer n (n=1,2,3)
  - **Bits 19-16: Fixe la taille du message à transmettre (en nombre d'octets)**

Table 207. Transmit Frame Information Register (CAN1TFI[1/2/3] - address 0xE004 40[30/40/50], CAN2TFI[1/2/3] - 0xE004 80[30/40/50]) bit description

Bit	Symbol	Function	Reset Value
7:0	PRIO	If the TPM (Transmit Priority Mode) bit in the CANxMOD register is set to 1, enabled Tx Buffers contend for the right to send their messages based on this field. The buffer with the lowest TX Priority value wins the prioritization and is sent first.	
15:8	-	Reserved.	0
19:16	DLC	Data Length Code. This value is sent in the DLC field of the next transmit message. In addition, if RTR = 0, this value controls the number of Data bytes sent in the next transmit message, from the CANxTDA and CANxTDB registers: 0000-0111 = 0-7 bytes 1xxx = 8 bytes	0

Registre CANxTDAn

- Registre de donnés du buffer d'émission n (n=1,2,3)
  - **En accord avec la configuration de CANxTFIn**
  - **Le registre CANxTDBn permet de donner si besoin la valeur des octets 5 à 8 du message à envoyer**

Table 210. Transmit Data Register A (CAN1TDA[1/2/3] - address 0xE004 40[38/48/58], CAN2TDA[1/2/3] - address 0xE004 80[38/48/58]) bit description

Bit	Symbol	Function	Reset Value
7:0	Data 1	If RTR = 0 and DLC ≥ 0001 in the corresponding CANxTFI, this byte is sent as the first Data byte of the next transmit message.	0
15;8	Data 2	If RTR = 0 and DLC ≥ 0010 in the corresponding CANxTFI, this byte is sent as the 2nd Data byte of the next transmit message.	0
23:16	Data 3	If RTR = 0 and DLC ≥ 0011 in the corresponding CANxTFI, this byte is sent as the 3rd Data byte of the next transmit message.	0
31:24	Data 4	If RTR = 0 and DLC ≥ 0100 in the corresponding CANxTFI, this byte is sent as the 4th Data byte of the next transmit message.	0

Registres CANxCMR

- Permet d'initier une action sur les buffers d'émission et/ou de réception
  - **Bit 0: Demande de transmission**
    - **Se fait avec le buffer d'émission sélectionné**
  - **Bit 1: Annulation d'une demande de transmission**

Table 195. Command Register (CAN1CMR - address 0xE004 4004, CAN2CMR - address 0xE004 8004) bit description

Bit	Symbol	Value	Function	Reset Value	RM Set
0[1][2]	TR		Transmission Request.	0	0
		0 (absent)	No transmission request.		
		1 (present)	The message, previously written to the CANxTFI, CANxTID, and optionally the CANxTDA and CANxTDB registers, is queued for transmission from the selected Transmit Buffer. If at two or all three of STB1, STB2 and STB3 bits are selected when TR=1 is written, Transmit Buffer will be selected based on the chosen priority scheme (for details see Section 12–4.3 "Transmit Buffers (TXB)")		
1[1][3]	AT		Abort Transmission.	0	0
		0 (no action)	Do not abort the transmission.		
		1 (present)	if not already in progress, a pending Transmission Request for the selected Transmit Buffer is cancelled.		

Registres CANxCMR

- Permet d'initier une action sur les buffers d'émission et/ou de réception
  - **Bit 5-7: Sélection du buffer qui va transmettre le message**
  - **Possibilité de sélectionner plusieurs buffers**
    - **Un système de priorité est alors mis en oeuvre**

Table 195. Command Register (CAN1CMR - address 0xE004 4004, CAN2CMR - address 0xE004 8004) bit description

Bit	Symbol	Value	Function	Reset Value	RM Set
5	STB1		Select Tx Buffer 1.	0	0
		0 (not selected)	Tx Buffer 1 is not selected for transmission.		
		1 (selected)	Tx Buffer 1 is selected for transmission.		
6	STB2		Select Tx Buffer 2.	0	0
		0 (not selected)	Tx Buffer 2 is not selected for transmission.		
		1 (selected)	Tx Buffer 2 is selected for transmission.		
7	STB3		Select Tx Buffer 3.	0	0
		0 (not selected)	Tx Buffer 3 is not selected for transmission.		
		1 (selected)	Tx Buffer 3 is selected for transmission.		

Registres CANxCMR

- Permet d'initier une action sur les buffers d'émission et/ou de réception
  - **Bit 2: Relâche du buffer de réception**
    - **A effectuer lorsque l'on a récupéré le message stocké dans le buffer de réception**

Table 195. Command Register (CAN1CMR - address 0xE004 4004, CAN2CMR - address 0xE004 8004) bit description

Bit	Symbol	Value	Function	Reset Value	RM Set
2[4]	RRB		Release Receive Buffer.	0	0
		0 (no action)	Do not release the receive buffer.		
		1 (released)	The information in the Receive Buffer (consisting of CANxRFS, CANxRID, and if applicable the CANxRDA and CANxRDB registers) is released, and becomes eligible for replacement by the next received frame. If the next received frame is not available, writing this command clears the RBS bit in the Status Register(s).		

  - **Permet également d'acquitter l'interruption si elle a été configurée et activée pour le contrôleur CAN**

Registres CANxRID

- Contient l'identifiant du message reçu

Table 203. Receive Identifier Register (CAN1RID - address 0xE004 4024, CAN2RID - address 0xE004 8024) bit description

Bit	Symbol	Function	Reset Value	RM Set
10:0	ID	The 11 bit Identifier field of the current received message. In CAN 2.0A, these bits are called ID10-0, while in CAN 2.0B they're called ID29-18.	0	X
31:11	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA	

Registres CANxRSR

- Statut du buffer de réception
  - **Bits 19-16: Permet de connaître la taille du champ de données du message reçu**

Table 202. Receive Frame Status register (CAN1RFS - address 0xE004 4020, CAN2RFS - address 0xE004 8020) bit description

Bit	Symbol	Function	Reset Value	RM Set
19:16	DLC	The field contains the Data Length Code (DLC) field of the current received message. When RTR = 0, this is related to the number of data bytes available in the CANRDA and CANRDB registers as follows:	0	X

Registre CANxRDA

- Contient le champ de données du message reçu
  - **1 à 8 octets en fonction de l'information de CANxRSR**

Table 205. Receive Data register A (CAN1RDA - address 0xE004 4028, CAN2RDA - address 0xE004 8028) bit description

Bit	Symbol	Function	Reset Value	RM Set
7:0	Data 1	If the DLC field in CANRFS ≥ 0001, this contains the first Data byte of the current received message.	0	X
15:8	Data 2	If the DLC field in CANRFS ≥ 0010, this contains the first Data byte of the current received message.	0	X
23:16	Data 3	If the DLC field in CANRFS ≥ 0011, this contains the first Data byte of the current received message.	0	X
31:24	Data 4	If the DLC field in CANRFS ≥ 0100, this contains the first Data byte of the current received message.	0	X

CANxRDB