Microcontrôleurs & Applications

Convertisseurs A/N et N/A

J

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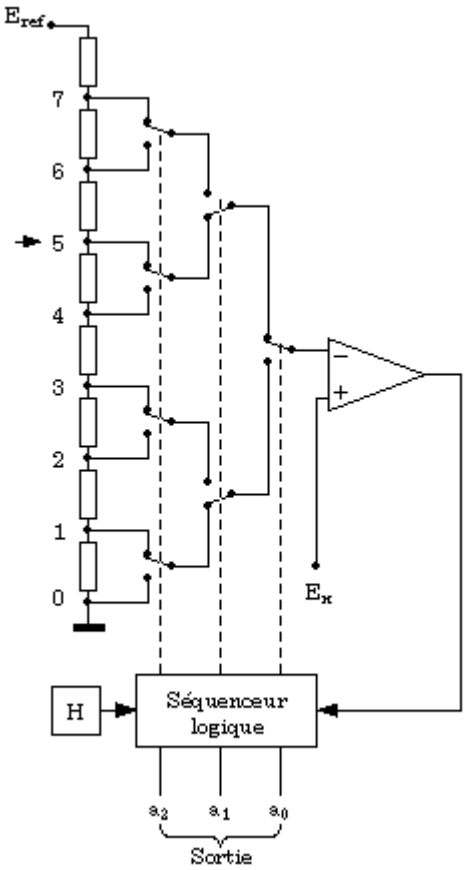
Convertisseurs et LPC2378

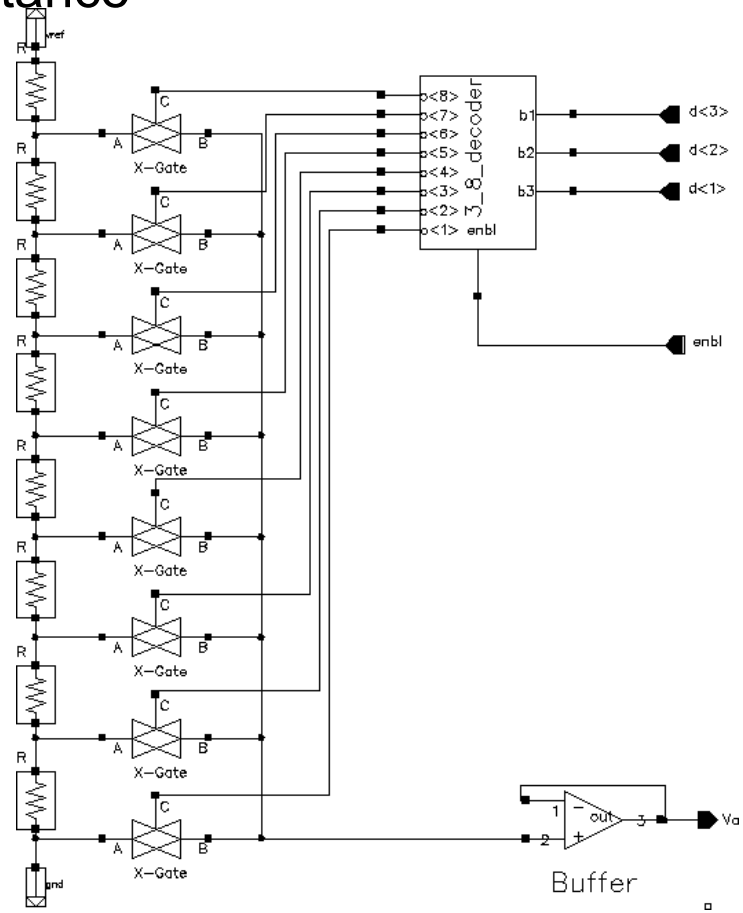
- Le microcontrôleur dispose
  - **D'un convertisseur analogique/numérique sur 10 bits**
    - CAN à approximations successives
    - 8 canaux d'entrée
    - Tension d'entrée de 0 à 3V



- Sur la carte KEIL
  - **Le CAN est relié à un potentiomètre (sur le canal 0)**

Convertisseurs et LPC2378

- Le microcontrôleur dispose
  - **D'un convertisseur numérique/analogique sur 10 bits**
    - CNA à réseau de résistance
- Sur la carte KEIL
  - **Le CNA est relié à un haut parleur (Port P0.26)**



Horloge

- Par défaut, le convertisseur analogique/ numérique n'est pas activé au démarrage du LPC2378
- Pour activer le périphérique, il faut modifier le registre PCONP (Power CONtrol for Peripherals) en positionnant le bit correspondant au CAN à 1
- Voir en annexe pour le détail de ce registre

Convertisseur A/N

- Registres de Contrôle
  - **AD0CR:** **Mode de fonctionnement du CAN**
  - **AD0STAT:** **Registre de statut**
  - **AD0INTEN:** **Autorisation des interruptions**

- Registres de Données
  - **AD0GDR:** **Registre de données global**
  - **ADDR0-7:** **Registre de données d'un canal**

Registre de Contrôle AD0CR

- Bits 7-0
  - **Sélection des canaux à convertir**
- Bits 15-8
  - **Fréquence de conversion**

Bit	Symbol	Value	Description	Reset Value
7:0	SEL		Selects which of the AD0.7:0 pins is (are) to be sampled and converted. For AD0, bit 0 selects Pin AD0.0, and bit 7 selects pin AD0.7. In software-controlled mode, only one of these bits should be 1. In hardware scan mode, any value containing 1 to 8 ones. All zeroes is equivalent to 0x01.	0x01
15:8	CLKDIV		The APB clock (PCLK) is divided by (this value plus one) to produce the clock for the A/D converter, which should be less than or equal to 4.5 MHz. Typically, software should program the smallest value in this field that yields a clock of 4.5 MHz or slightly less, but in certain cases (such as a high-impedance analog source) a slower clock may be desirable.	0

Registre de Contrôle AD0CR

- Bit 16: Sélection du mode burst (rafale)
- Bits 19-17: Durée et précision des conversions en mode burst

16	BURST	0	Conversions are software controlled and require 11 clocks.	0
		1	The AD converter does repeated conversions at the rate selected by the CLKS field, scanning (if necessary) through the pins selected by 1s in the SEL field. The first conversion after the start corresponds to the least-significant 1 in the SEL field, then higher numbered 1 bits (pins) if applicable. Repeated conversions can be terminated by clearing this bit, but the conversion that's in progress when this bit is cleared will be completed. **Important:** START bits must be 000 when BURST = 1 or conversions will not start.	
19:17	CLKS		This field selects the number of clocks used for each conversion in Burst mode, and the number of bits of accuracy of the result in the LS bits of ADDR, between 11 clocks (10 bits) and 4 clocks (3 bits).	000
		000	11 clocks / 10 bits	
		001	10 clocks / 9 bits	
		010	9 clocks / 8 bits	
		011	8 clocks / 7 bits	
		100	7 clocks / 6 bits	
		101	6 clocks / 5 bits	
		110	5 clocks / 4 bits	
		111	4 clocks / 3 bits	

Registre de Contrôle AD0CR

- Bit 21: Activation/Arrêt du CAN
- Bits 26-24: Démarrage des conversions
  - **Manuellement**
  - **Sur une transition (déterminée par le bit 27) d'une broche d'E/S**

21	PDN	1	The A/D converter is operational.	0
		0	The A/D converter is in power-down mode.	
23:22	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
26:24	START		When the BURST bit is 0, these bits control whether and when an A/D conversion is started:	0
		000	No start (this value should be used when clearing PDN to 0).	
		001	Start conversion now.	
		010	Start conversion when the edge selected by bit 27 occurs on P2.10/EINT0.	
		011	Start conversion when the edge selected by bit 27 occurs on P1.27/CAP0.1.	
		100	Start conversion when the edge selected by bit 27 occurs on MAT0.1[1].	
		101	Start conversion when the edge selected by bit 27 occurs on MAT0.3[1].	
		110	Start conversion when the edge selected by bit 27 occurs on MAT1.0[1].	
		111	Start conversion when the edge selected by bit 27 occurs on MAT1.1[1].	
27	EDGE		This bit is significant only when the START field contains 010-111. In these cases:	0
		1	Start conversion on a falling edge on the selected CAP/MAT signal.	
		0	Start conversion on a rising edge on the selected CAP/MAT signal.	

Registre de Statut AD0STAT

- Rassemble les statuts de tous les canaux de l'ADC
  - **Fin de conversion**
  - **Donnée écrasée par une nouvelle conversion**
  - **Drapeau d'interruption**
- Ces infos sont aussi consultables pour chaque canal dans les registres ADDRx

Table 458: A/D Status Register (ADSTAT - address 0xE003 4030) bit description

Bit	Symbol	Description	Reset Value
7:0	Done7:0	These bits mirror the DONE status flags that appear in the result register for each A/D channel.	0
15:8	Overrun7:0	These bits mirror the OVERRRUN status flags that appear in the result register for each A/D channel. Reading ADSTAT allows checking the status of all A/D channels simultaneously.	0
16	ADINT	This bit is the A/D interrupt flag. It is one when any of the individual A/D channel Done flags is asserted and enabled to contribute to the A/D interrupt via the ADINTEN register.	0
31:17	Unused	Unused, always 0.	0

Registre d'Interruptions: AD0INTEN

- Bits 7-0: Autorisation des interruptions pour chaque canal
- Bit 8: Autorisation globale

Table 459: A/D Interrupt Enable Register (ADINTEN - address 0xE003 400C) bit description

Bit	Symbol	Description	Reset Value
7:0	ADINTEN 7:0	These bits allow control over which A/D channels generate interrupts for conversion completion. When bit 0 is one, completion of a conversion on A/D channel 0 will generate an interrupt, when bit 1 is one, completion of a conversion on A/D channel 1 will generate an interrupt, etc.	0x00
8	ADGINTEN	When 1, enables the global DONE flag in ADDR to generate an interrupt. When 0, only the individual A/D channels enabled by ADINTEN 7:0 will generate interrupts.	1
31:9	Unused	Unused, always 0.	0

Registre de Données Global:

- AD0GDR
  - **Contient le résultat et le statut de la dernière conversion**
- Fonctionnement identique aux registres AD0DR0-AD0DR7
- Seule différence:
  - **Bits 26-24: Indique le numéro du canal ayant effectué la dernière conversion**

Registres de Données: AD0DRx

- Contient le résultat et le statut de la dernière conversion sur le canal x
  - **Bits15-6: Résultat de la conversion**
  - **La lecture de cette valeur remet à jour (si besoin) le drapeau d'interruption**

Table 460: A/D Data Registers (ADDR0 to ADDR7 - addresses 0xE003 4010 to 0xE003 402C) bit description

Bit	Symbol	Description	Reset Value
5:0	Unused	Unused, always 0. These bits always read as zeroes. They provide compatible expansion room for future, higher-resolution ADCs.	0
15:6	V/V_{REF}	When DONE is 1, this field contains a binary fraction representing the voltage on the Ain pin, divided by the voltage on the Vref pin. Zero in the field indicates that the voltage on the Ain pin was less than, equal to, or close to that on V_{REF}, while 0x3FF indicates that the voltage on Ain was close to, equal to, or greater than that on Vref.	NA

Registres de Données: AD0DRx

- Contient le résultat et le statut de la dernière conversion sur le canal x
  - **Bit 30: Indique qu'une valeur convertie non lue a été écrasée par une nouvelle conversion**
  - **Bit 31: Indique la fin d'une conversion**

29:16	Unused	These bits always read as zeroes. They allow accumulation of successive A/D values without AND-masking, for at least 256 values without overflow into the CHN field.	0
30	OVERRUN	This bit is 1 in burst mode if the results of one or more conversions was (were) lost and overwritten before the conversion that produced the result in the LS bits.This bit is cleared by reading this register.	0
31	DONE	This bit is set to 1 when an A/D conversion completes. It is cleared when this register is read.	0

Convertisseur N/A

- Piloté par un seul registre: DACR
- Le convertisseur est activé si la broche d'E/S du microcontrôleur est configurée en mode DAC
- Consulter la doc pour savoir quelle broche contient la fonction DAC

Registre DACR

- Bits 15-6: Valeur numérique à convertir

Table 462: D/A Converter Register (DACR - address 0xE006 C000) bit description

Bit	Symbol	Value	Description	Reset Value
5:0	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
15:6	VALUE		After the selected settling time after this field is written with a new VALUE, the voltage on the A_{OUT} pin (with respect to V_{SSA}) is VALUE/1024 × VREF.	0
16	BIAS	0	The settling time of the DAC is 1 μs max, and the maximum current is 700 υA.	0
		1	The settling time of the DAC is 2.5 μs and the maximum current is 350 μA.	
31:17	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA