Introduction to FPGAs and the Associated Workflow

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List of Acronyms

CPU	Central processing unit
HD	High-definition
2D	Two-dimensional
3D	Three-dimensional
GPU	Graphics processing unit
FPGA	Field programmable gate array
RTL	Register transfer level
HDL	Hardware descriptive language
CAD	Computer-aided design

Introduction

Central processing units (CPUs) can be viewed as the traditional method of computing due to their general-purpose functionality. Essentially, they receive a set of instructions from memory, referred to as machine code, and perform calculations [1]. Human-readable code written in a programming language, such as C++ or Python (may be an interpreted or compiled language), gets translated to machine code before being run on a CPU [2].

From the emergence of the CPU in the 1970s to the current day, CPUs went from executing thousands of instructions every second to efficiently executing billions, and this is only one metric of performance [1]. However, they only run as many concurrent processes as their number of cores [1]. Despite their impressive capabilities, there exist certain applications where this traditional method of computing does not make the cut.

To illustrate one such extreme performance application, the example of Avalon Holographics' latest display as of writing, NOVAC, will be used (see **Figure 1**) [3]. NOVAC can display high-definition (HD) holograms to the naked eye [3]. Due to the nature of the over-the-screen lens that creates the hologram, the underlying 2D (two-dimensional) resolution must be substantially higher than HD to achieve HD 3D (three-dimensional) resolution [4]. For NOVAC, the 2D resolution is in the range of 69120 by 77760 pixels, around 2 million times higher than most TVs and computer monitors today

(often 1920 by 1080 pixels) [4]. This 2D resolution is achieved by constructing NOVAC out of more than 2592 individual HD projectors packed into the size of a coffee table [4].

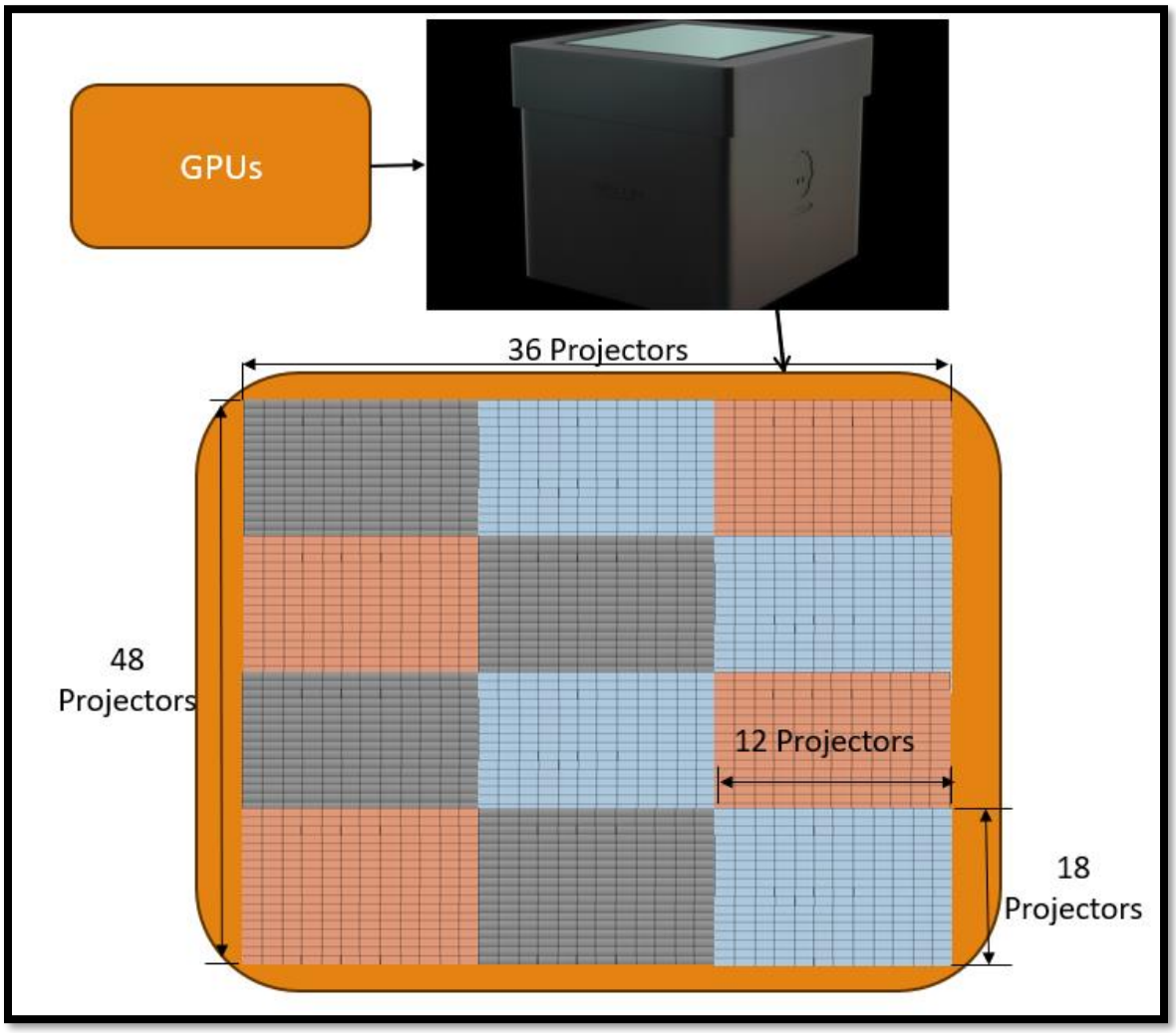

Figure 1: Diagram of the scale of NOVAC, Avalon Holographics' biggest 3D display. Reproduced from [4].

Data enters the NOVAC display from a high-power GPU (Graphics Processing Unit) server, but it does not go directly to the projectors [4]. Rather, the display hardware must interpret, buffer (store in memory), and manipulate the data for correction before displaying it [4]. The amount of data processed is equivalent to **several terabytes** per

second [4]. Even advanced CPUs cannot meet these throughput specifications [4]. A computing unit optimized for this specific application is needed, able to process large amounts of data in parallel. This overview illustrates one solution for this and similar problems: the field programmable gate array (FPGA).

Main Discussion

Introduction to the FPGA

An FPGA is a semiconductor device that can be programmed to produce a digital logic circuit [5]. A digital logic circuit, in turn, is an electronic circuit capable of taking inputs and producing outputs based on logical operations. By this definition, a digital logic circuit encompasses traffic light and vending machine controllers, coffee machine timers, and even GPUs and CPUs. In fact, all the logic circuit examples just mentioned can be and have been realized on an FPGA [6]. The idea behind an FPGA's advantage over a CPU in specialized applications is that the FPGA will produce a digital logic circuit optimized to perform *one* purpose. In contrast, a CPU aims to be general purpose.

The "field programmable" in FPGA refers to the fact that these chips are programmed after manufacture by the user, where the desired digital logic circuit is loaded on startup [5]. On the other hand, the "gate array" in FPGA indicates that these chips consist of, at the basic level, a 2D array of programmable logic blocks and interconnections, with in-out blocks at the periphery (see **Figure 2**) [5]. The FPGA's

programming specifies the functions that the logic blocks should implement and which logic/in-out blocks should be connected to which at the interconnections [5].

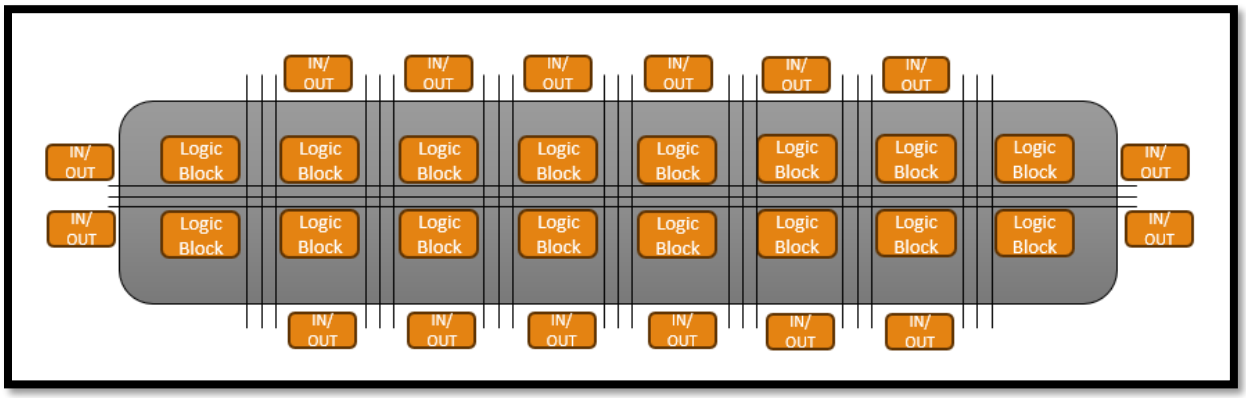

Figure 2: Conceptual Structure of FPGA Device. Redrawn from [7].

FPGA Programming Workflow

The FPGA programming workflow can be broken down into the following stages (see **Figure 3**) [7] [4]:

1. Design Architecture: Develop the abstract ideas and block diagrams of the design.
2. RTL Code: Realize the desired logic circuit using a hardware descriptive language (HDL).
3. Synthesis: Use computer-aided design (CAD) software sold by the FPGA vendor, compile/synthesize RTL code into its constituent logic functions.
4. Implementation: Use vendor software to:
    a. Translate: Merge all RTL files and module instantiations into one "netlist" or program, encompassing all instantiations of logic groups in the RTL.
    b. Map: Assign the synthesis and translation stage results to logic and in-out blocks.
    c. Place and route: Derive the physical layout of the design in the chip.

5. Generate Bitfile: Use vendor software to generate the binary file that the FPGA uses to program itself on startup.

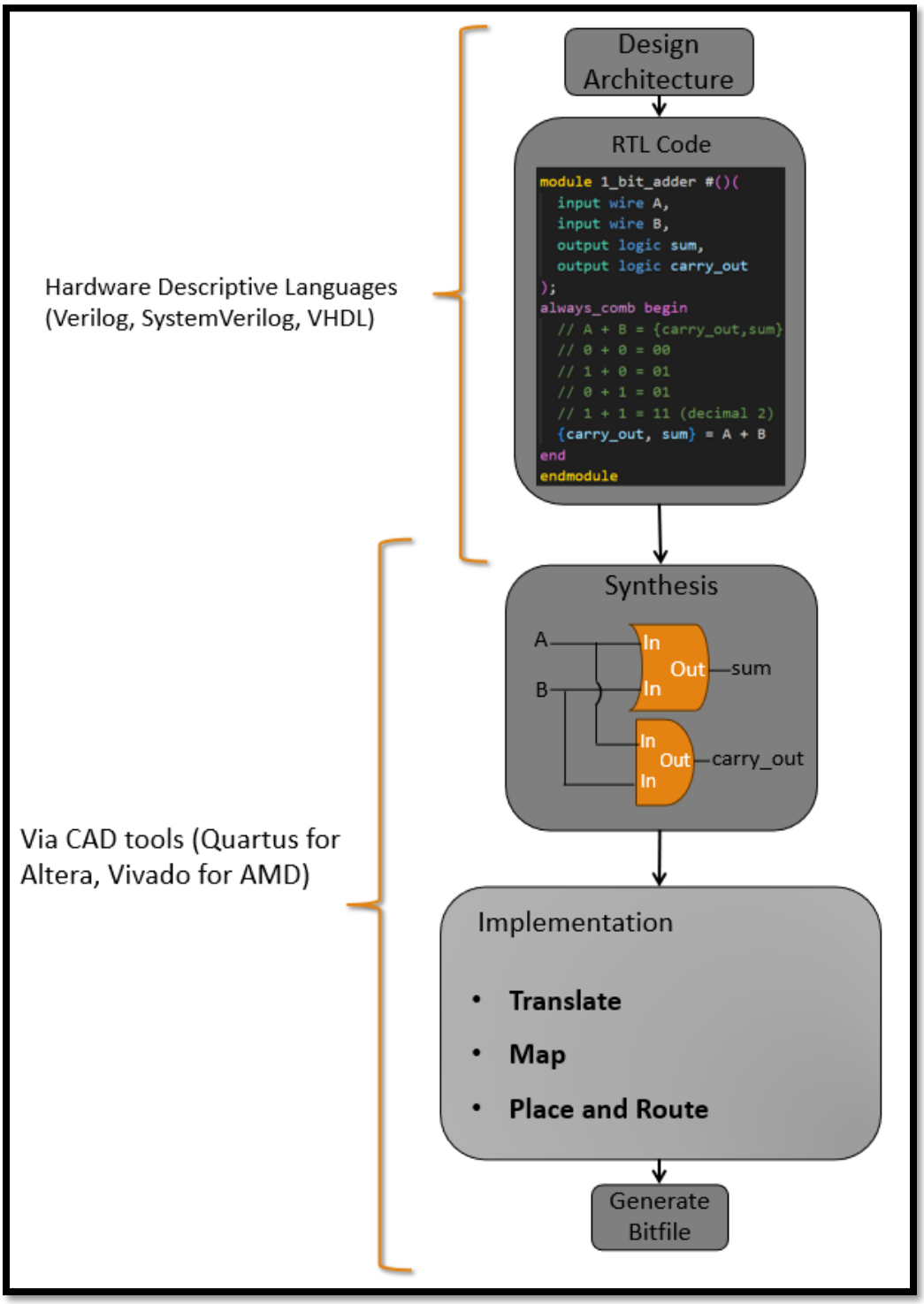

Figure 3: FPGA programming workflow flowchart. Adapted from [7].

Placement and Routing

Due to the number of combinations in which the desired logic circuit may be placed on the FPGA chip, the algorithms used in the implementation stage are quite complex and are improving over time [8]. In the placement and routing stage, algorithms usually start with a random seed and become more selective as FPGA resources are used up (see **Figure 4)** [8]. This may lead to the implementation stage failing due to size or timing constraints, prompting the engineer to return to the architecture design or RTL code stages or rerun the build with a different seed [4].

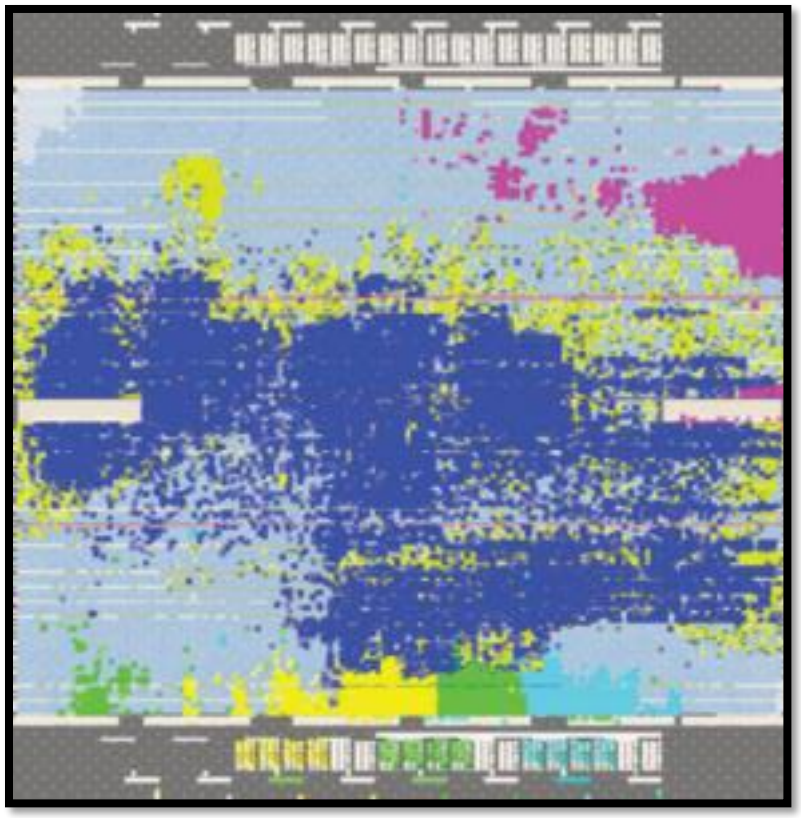

Figure 4: FPGA colour-coded floorplan in Altera's Quartus FPGA software, showing the physical locations of the instantiations of certain logic groups on an FPGA chip. Reproduced from [9].

Conclusion

In conclusion, certain high-performance applications that are not possible with traditional computing can be achieved using an FPGA chip. This was demonstrated by the example of the NOVAC display by Avalon Holographics. Although CPUs remain the best option for many computing needs, their architecture is unsuitable for handling the data throughput of NOVAC in the desired time. It was noted that, in this case, an FPGA succeeds as it is optimized for a specific purpose rather than aiming to be general purpose like with traditional computing.

The FPGA development workflow contrasts with conventional software or hardware design. For example, rather than writing a computer program to be compiled into machine code and executed in a sequential manner, code in an HDL is synthesized into logic blocks and processed concurrently. Also, FPGA CAD software heavily assists the engineer with the physical design of their circuit, more so than traditional hardware CAD tools. Overall, FPGAs are a strong option for engineers to realize high-performance and efficient digital logic design.

References

[1] S. Furber, "Microprocessors: the engines of the digital age," *Proceedings of the Royal Society A: Mathematical, Physical, and Engineering Sciences*, vol. 473, no. 2199, p. 20160893, 2017.

[2] A. Taylor, "Software: Running Programs," Standford University, [Online]. Available: https://web.stanford.edu/class/cs101/software-1.html. [Accessed 10 April 2024].

[3] Avalon Holographics Inc. , "NOVAC: The World's Most Advanced Holographic Display," 2024. [Online]. Available: https://novac3d.com/. [Accessed 14 April 2024].

[4] A. Cook, *Private Communications at Avalon Holographics*, April 2024.

[5] A. Moore, FPGA for Dummies, Altera Special Edition, New Jersey: John Wiley & Sons Inc., 2014, pp. 4-6.

[6] S. Vyazigin, A. Dyusembaev and M. Mansurova, "Emulation of x86 Computer on FPGA," in *2020 IEEE 8th Workshop on Advances in Information, Electronic and Electrical Engineering (AIEEE)*, Vilnius, Lithuania, 2021.

[7] P. P. Chu, FPGA Prototyping by Verilog Examples: Xilinx Spartan-3 Version, John Wiley & Sons Inc., 2008, pp. 16-21.

[8] U. Farooq, Z. Marrakchi and M. Habib, Tree-based Heterogeneous FPGA Architectures, New York: Springer New York, 2012, pp. 32-35.

[9] Intel Corporation, "Intel® Quartus® Prime Pro Edition User Guide: Design Optimization," 11 December 2018. [Online]. Available: https://www.intel.com/content/www/us/en/docs/programmable/683641/18-1/introduction.html. [Accessed 14 April 2024].

AVALON HOLOGRAPHICS

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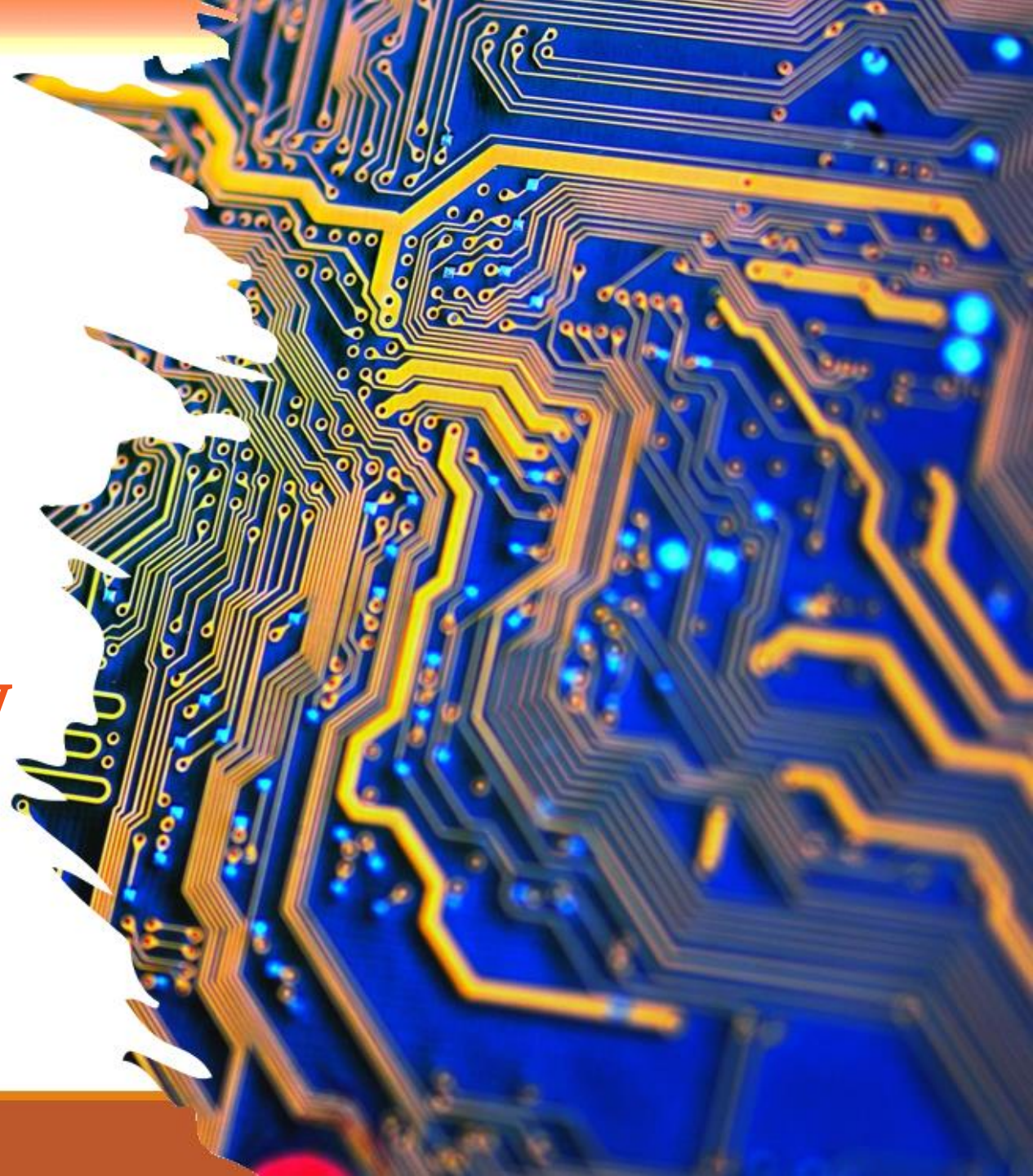


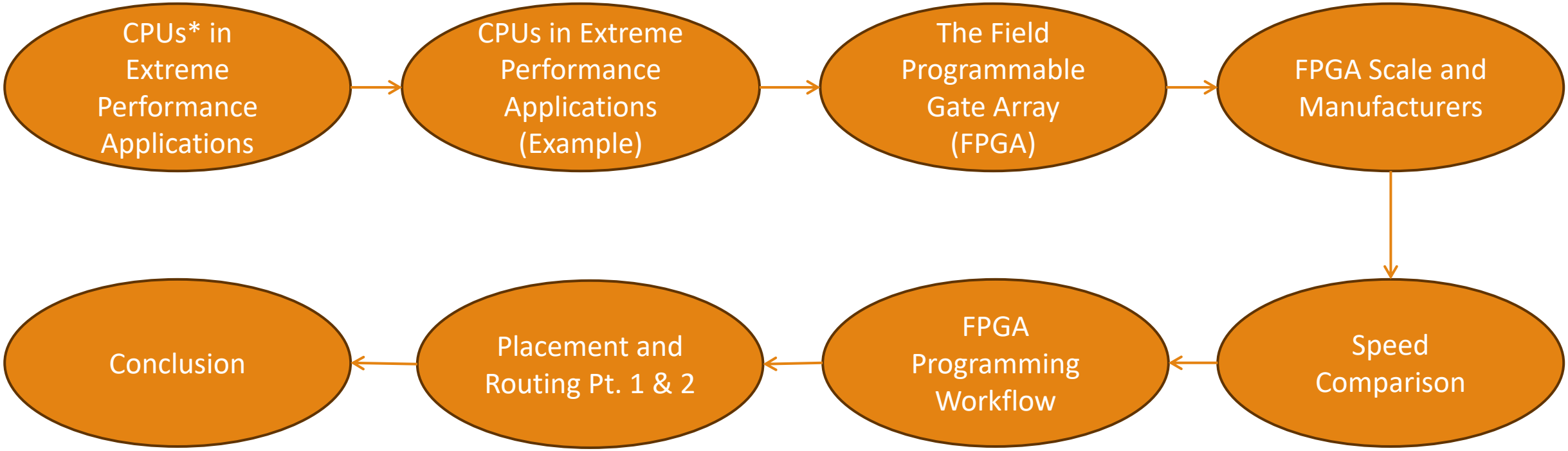
A Word About Avalon Holographics

Russ Baker (Left) and Wally Hass (Right).
Reproduced from [1].

- Founded in 2015 [1]
- 80+ permanent employees [2]
- Co-founded by Wally Hass and Russ Baker [1]
- Biggest asset is **invaluable talent base** and **pool of intellectual property**

Avalon Holographics 1st Gen Display Shoulder Example. Reproduced from [3].

Agenda

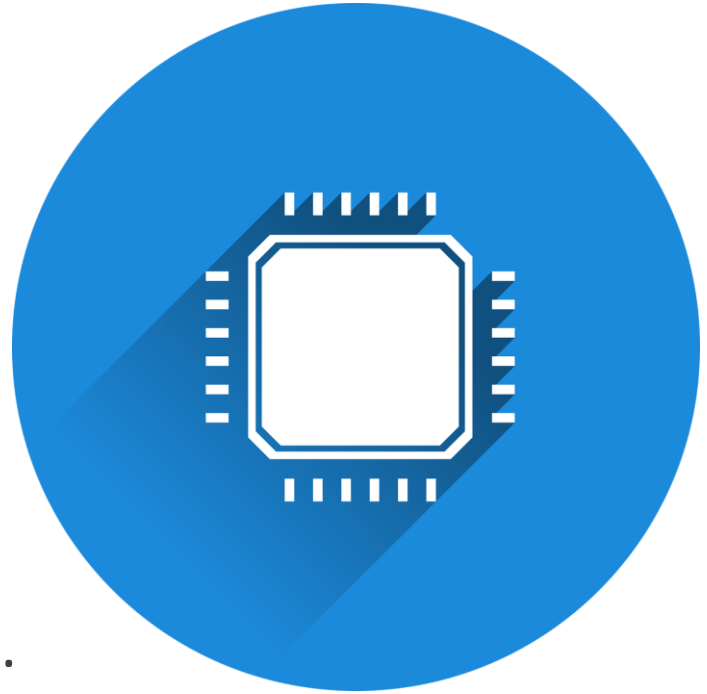


*CPU: Central Processing Unit

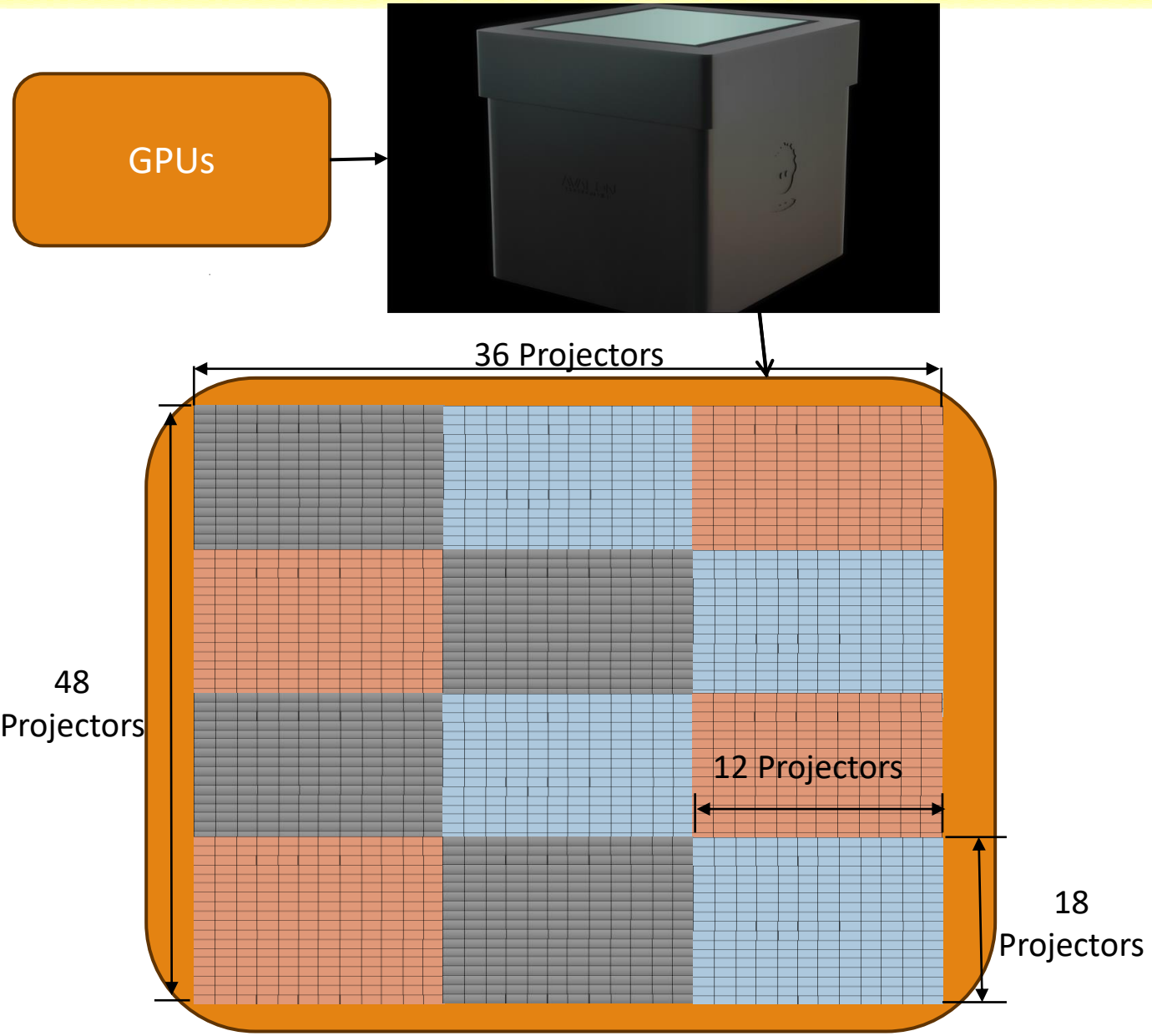
CPU Limitations in Extreme Performance Applications

Central Processing Units (CPUs) receive a set of instructions from memory and perform calculations [4].

- Most general-purpose processing unit, capable of running any program [4]



CPUs can **execute any set of instructions (i.e. run any program)** [4].

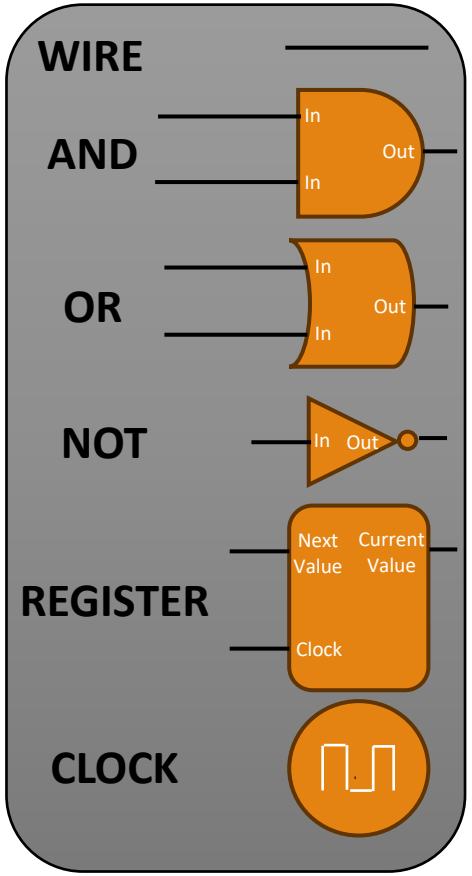


CPU Limitations in Extreme Performance Applications (Example)

- One display powered by 8+ Graphics Processing Units (GPUs) [2]
- 2592 individual HD 2D projectors, just to achieve HD 3D resolution! [2]
- Receiving, interpreting, storing, and manipulating **Terabytes** every second [2]

Diagram of the scale of NOVAC, Avalon Holographics' biggest 3D display. Reproduced from [2].

The Field Programmable Gate Array (FPGA)

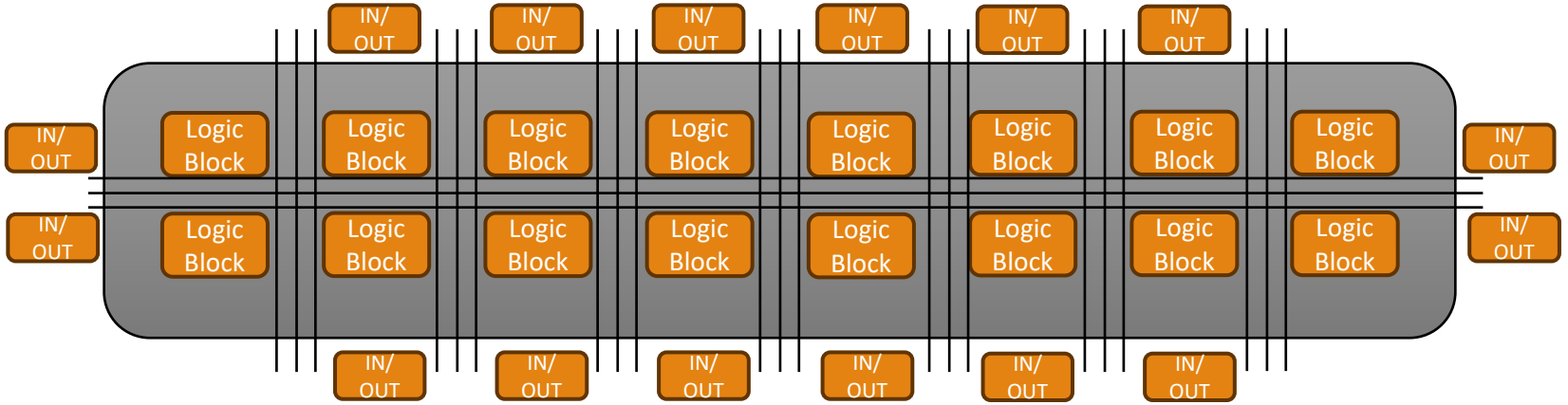


Basic components of a logic circuit. Redrawn from [5].

A Field Programmable Gate Array (FPGA) is a semiconductor device that can facilitate a digital logic circuit [5].

Field Programmable – Programmed after manufacture, desired logic circuit is loaded on startup [5]

Gate Array – Consists of programmable logic blocks and Interconnections [5]



Conceptual structure of FPGA device. Redrawn from [6].

FPGA Scale and Manufacturers

It’s possible to have between thousands to millions of logic elements in one FPGA chip [7].

- **Intel® Stratix® 10 GX 10M FPGA** has more than 10 *million* logic elements [7]

Major FPGA manufacturers. Reproduced from [8], [9], [10], and [11].

Speed Comparison

Speed comparison between simulation vs. FPGA implementation for Avalon Holographics' design. Adapted from [2].

Processing Unit	Time to Process Full Frame
CPU (FPGA Datapath Simulation)	50+ hours
FPGA Chip	> 2 seconds (0.5 to 1 Hz)

FPGA Programming Workflow

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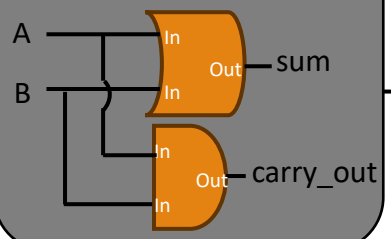
Design Architecture

Register Transfer Level (RTL) Code

```
module 1_bit_adder #()(
  input wire A,
  input wire B,
  output logic sum,
  output logic carry_out
);
always_comb begin
  // A + B = {carry_out,sum}
  // 0 + 0 = 00
  // 1 + 0 = 01
  // 0 + 1 = 01
  // 1 + 1 = 11 (decimal 2)
  {carry_out, sum} = A + B
end
endmodule
```

Simulation

Synthesis



Implementation

- **Translate –** Merge design files into one big program.
- **Map –** Assign generic gates in synthesis to logic and in/out blocks
- **Place and Route –** Derive physical layout inside chips.

Generate Bitfile

Hardware descriptive languages (Verilog, SystemVerilog, VHDL)

Via computer aided design (CAD) tools (Quartus for Altera, Vivado for AMD)

FPGA Programming Workflow Flowchart. Adapted from [6].

Placement and Routing Pt. 1

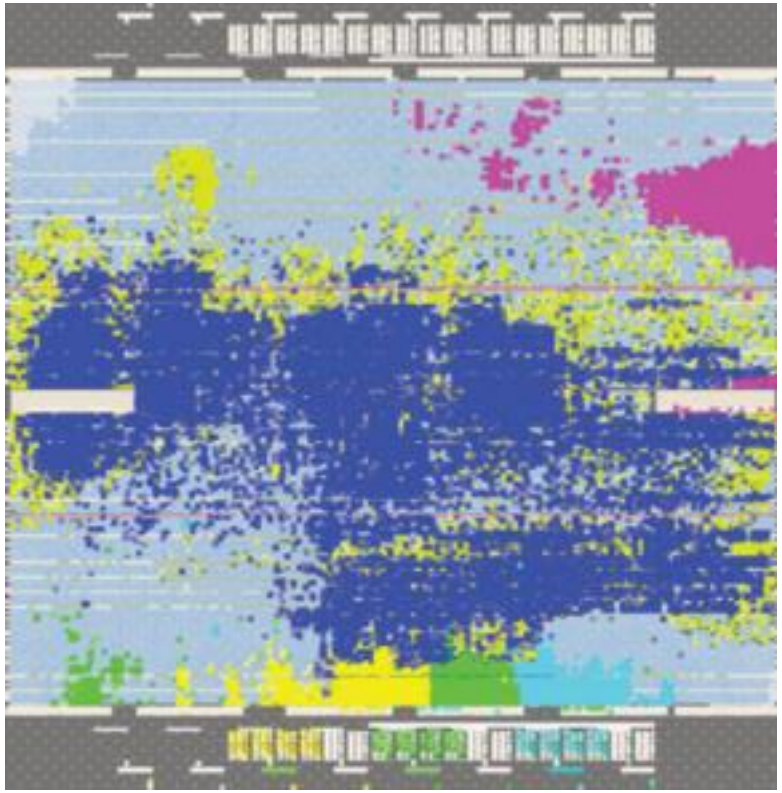
Placement and routing is preceded by clustering/packing [12].

- Clusters of logic blocks produced

Placement – Where to physically place logic blocks [12]

- Various placement strategies exist for certain needs

Routing – Optimize limited resources to achieve desired interconnections [12]



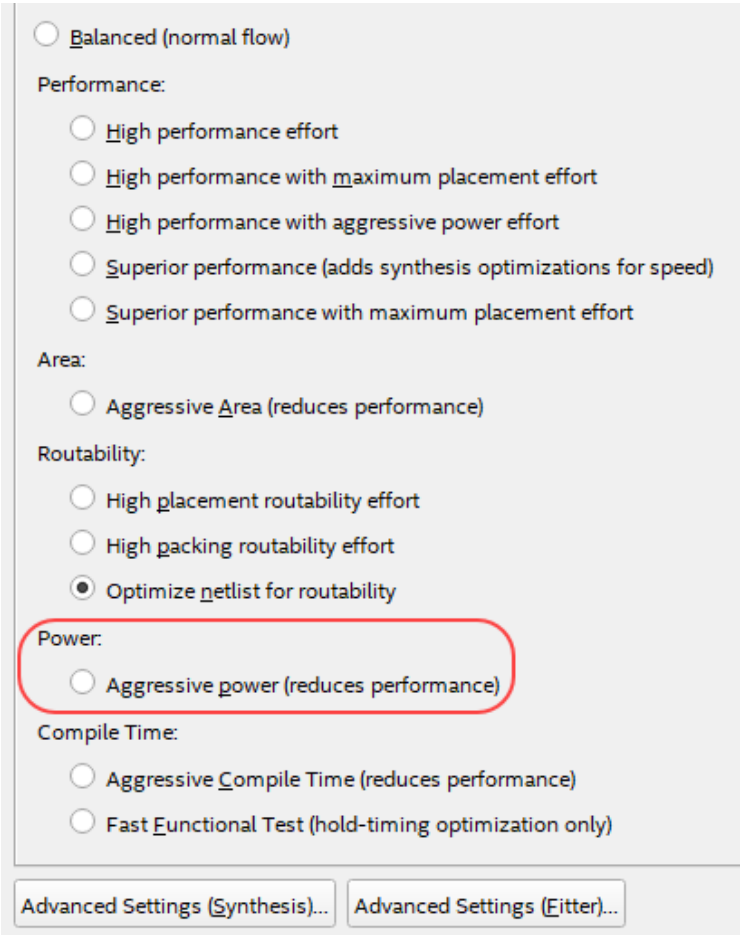
FPGA floorplan in Altera's Quartus FPGA software. Reproduced from [13].

Placement and Routing Pt. 2

Size & timing constraints can lead to build failures [2].

Resort to

- Optimization Settings [13]
- Deign Analysis [13]
  - Reducing logic
  - Changing timings
- Rerun build [12]



Altera's Quartus FPGA software compiler settings. Acquired from [13]

Conclusions

CPUs can execute **any** set of instructions.

- Not optimized for specific instruction sets

FPGAs are a solution.

Specialized workflow utilizes CAD tools in many stages, including:

- Placement
- Routing
- Build optimization & analysis

"Get the full picture, at a glance." Demo of Avalon Holographics' NOVAC display. Acquired from [14].

List of References

[1] Avalon Holographics Inc., "INTRODUCING OUR VISIONARY COFOUNDERS," 2024. [Online]. Available: https://www.avalonholographics.com/ourfounders. [Accessed 14 04 2024].

[2] A. Cook, *Private Communications at Avalon Holographics*, April 2024.

[3] Avalon Holographics Inc., "Main Page," 2024. [Online]. Available: https://www.avalonholographics.com/. [Accessed 14 04 2024].

[4] S. Furber, "Microprocessors: the engines of the digital age", Proceedings of the Royal Society A: Mathematical, Physical and Engineering Sciences, vol. 473, no. 2199, p. 20160893, 2017. https://doi.org/10.1098/rspa.2016.0893

[5] A. Moore, FPGA for Dummies, Altera Special Edition, New Jersey: John Wiley & Sons Inc., 2014, pp. 4-6.

[6] P. P. Chu, FPGA Prototyping by Verilog Examples: Xilinx Spartan-3 Version, John Wiley & Sons Inc., 2008, pp. 16-21.

[7] Intel Corporation, "Intel Satrix 10 GX FPGA," [Online]. Available: https://www.intel.com/content/www/us/en/products/details/fpga/stratix/10/gx/products.html. [Accessed 14 04 2024].

[8] Intel Corporation, "Intel Programmable Solutions Group is now Altera®, an Intel Company," [Online]. Available: https://www.intel.com/content/www/us/en/products/programmable.html#gs.7e3v24. [Accessed 14 04 2024].

[9] Advanced Micro Devices Inc. , "FPGAs & 3D ICs," 2024. [Online]. Available: https://www.xilinx.com/products/silicon-devices/fpga.html. [Accessed 14 04 2024].

[10] Lattice Semiconductor, "The Low Power Programmable Leader," [Online]. Available: https://www.latticesemi.com/. [Accessed 14 04 2024].

[11] Microchip Technology Inc., "Field-Programmable Gate Arrays (FPGAs) and Other Programmable Logic Devices (PLDs)," [Online]. Available: https://www.microchip.com/en-us/products/fpgas-and-plds. [Accessed 14 04 2024].

[12] U. Farooq, Z. Marrakchi and M. Habib, Tree-based Heterogeneous FPGA Architectures, New York: Springer New York, 2012, pp. 32-35.

[13] Intel Corporation, "Intel® Quartus® Prime Pro Edition User Guide: Design Optimization," 11 December 2018. [Online]. Available: https://www.intel.com/content/www/us/en/docs/programmable/683641/18-1/introduction.html. [Accessed 14 April 2024].

[14] Avalon Holographics Inc. , "NOVAC: The World's Most Advanced Holographic Display," 2024. [Online]. Available: https://novac3d.com/. [Accessed 14 April 2024].

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