

# Zaid Duraid

[zaidduraid.com](https://zaidduraid.com) | [linkedin.com/in/zaid-duraid](https://linkedin.com/in/zaid-duraid) | [github.com/Zaid-Duraid](https://github.com/Zaid-Duraid)

## EDUCATION

### Memorial University of Newfoundland

St. John's, NL

Bachelor of Engineering: **Computer Engineering** - CGPA: 4.00/4.00 (95.2%)

Sept. 2022 - April 2027

- **Dean's List (2022-2025)**
- **Scholarships:** Memorial University Alumni Entrance, Innovasea Computer Engineering, Verafin Inc. Computer Engineering, Charlie Sheppard Memorial - Hatch, PEGNL Past-President, Bob Thorburn Memorial, Gander Lions Club Community Leaders, NLESD Education Foundation, Town of Gander

## EXPERIENCE

### Advanced Research Electrical Engineer Intern

May. 2025 - Aug. 2025

Solace Power

St. John's, NL

- Improved the design of a multi-MHz synchronous rectifier by adding a **a PLL for closed-loop control** to maintain operation during ~100us loss of switch gate driver signal
- Designed and built single-layer PCBs to quickly verify **integration of subcircuits** (e.g., RC inverter delay line for phase shift on GaN FET driver signal) into multilayer PCBs
- Researched **EMC solutions for a tens of MHz wireless power system**, reducing noise on key harmonics
- Developed **C firmware for a TI F28003x microcontroller** to generate internal-clock or interrupt-driven PWM signals up to 9MHz, with adjustable frequency, duty cycle, and phase shift via CANBUS

### FPGA Hardware Engineer Intern

Jan. 2024 - Apr. 2024 and Sept. 2024 - Dec. 2024

Avalon Holographics Inc.

St. John's, NL

- Developed and documented **simulation testbenches for FPGA designs in SystemVerilog**, leading to the discovery and resolution of critical display datapath bugs
- Built new **internal verification tools using Python** that integrated with existing testbenches to verify hardware image correction for the holographic display
- Contributed to **FPGA RTL code in SystemVerilog**, including adding runtime-accessible register maps (regmaps) for debug and hardware image correction parameter loading
- Followed internal test processes by **assembling hardware, executing tests, and running TCL scripts** for the bring-up of new/refurbished PCBs and validation of FPGA build releases

### Software Team Co-Lead (Unpaid)

Aug. 2023 - Present

Eastern Edge Robotics

St. John's, NL

- Wrote **backend applications utilizing ROS2 and Docker with Python and C++** to run on a Raspberry Pi and interface between the piloting frontend and the ROV's thrusters, tools, sensors, and control profiles database
- Contributed to two independent **frontend applications, in ReactJS and C++**, providing both convenient (browser-based) and low-latency options for piloting the ROV
- Led and mentored software team by preparing **onboarding resources, documentation, and task assignments**, resulting in significant contributions and experience-gain by 5+ members
- Competed and presented alongside the team at the **International MATE ROV Competition Explorer Class** in 2023, 2024, and 2025, placing in 11th, 9th, and 3rd place in the world out of around 20-30 teams, respectively

## PROJECTS

### ROV Simulator - Gazebo, C++, ROS2, Python

Mar. 2024 - Present

- Implemented an **ROV simulation environment in Gazebo Harmonic with custom C++ plugins**, facilitating testing of the complete software stack, thruster configuration, and tooling for small ROV designs

### Photosphere Board - KiCad

Dec. 2024 - Jan. 2025

- Designed a **PCB in KiCad** that interfaces with the Raspberry Pi Compute Module 4 and includes **dual MIPI CSI camera ports and USB 2.0** for multi-view video streaming in a space-constrained environment

## SKILLS

**Programming Languages:** Python, SystemVerilog, C/C++, ReactJS, HTML/CSS, Bash

**Tools:** Git, KiCad, Questa, Quartus, Vivado, Docker, ROS, Gazebo, LTSpice, Altium, Solidworks, Bluebeam Revu

**Spoken Languages:** English and Arabic (Native), French (Fluent, DELF B1 Certified)