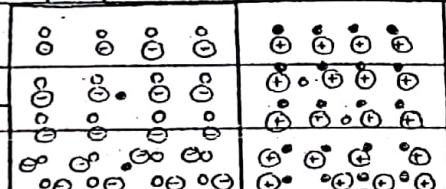


UNIT - 1

When p-type semiconductor and n-type semiconductor are joined metallurgically the resulting device is the p-n junction or diode.

p-type n-type majority charge carrier → electron



OPEN CIRCUITED P-n junction

DRIFT CURRENT

Due to minority

potential barrier

In n-type semiconductor there are high concentration of electron

In p-type semiconductor there are high concentration of holes

Because of difference in their concentration in two region diffusion of majority charge carrier takes place across the junction.

That means holes from p-side diffuse into n-region where these holes combine with the free electrons of the n-region.

Free electrons from n-region diffuse into p-region and combine with free holes of p-region as a result of this diffusion high rate of recombination takes place near the junction. Due to this process the negative immobile ions remains on p-side and positive immobile ions remains on n-side as shown in the figure. and these ions will

produce electric potential denoted by V_B across the junction and this electric potential is also called potential barrier. It stops the further diffusion of majority charge carrier across the junction. Because the additional holes trying to enter the n-side are repelled by positive immobile ion of n-region. Similarly the electrons from n-region are trying to diffuse are repelled by negative mobile ions of the p-region.

Therefore diffusion of majority charge carrier occurs for very short time.

→ If the process of diffusion and recombination will continue then all the holes and free electrons are eliminated and the device will be insulator. But practically this does not happen due to potential barrier which stops the further diffusion of majority charge carrier.

DEPLETION REGION :- The region contain uncompensated donor and acceptor ion is called depletion region.

ELECTRIC FIELD / POTENTIAL BARRIER :-

The electric field between donor and acceptor ions is called electric potential barrier.

$$V_B = 0.7 \text{ V} \quad \text{for silicon (Si)}$$

$$\text{OR } 0.6 \text{ V}$$

$$V_B = 0.2 \text{ OR } 0.3 \text{ V} \quad \text{for Ge}$$

DRIFT PROCESS :-

Due to the potential barrier there is flow of minority charge carrier across the junction that means electron from p-side being attracted towards n-side due to positive immobile ion and holes from n-side being attracted towards p-side due to negative immobile ions.

and majority charge carriers remains on each side of junction. i.e. holes stays on p-side and electrons on n-side.

But some of the majority charge carriers have very high energy therefore few of the majority charge carrier cross the junction. Hence the drift current constituted by minority charge carrier across the junction must be exactly counter balanced by diffusion current due to flow of same number of majority charge carrier across the junction.

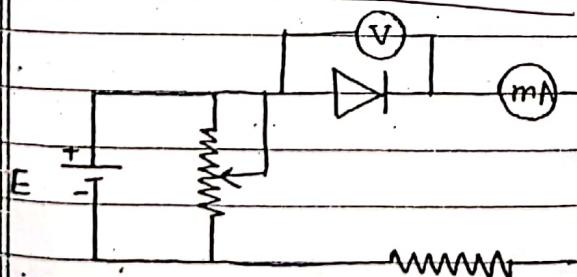
The barrier height adjust itself so that the resulting magnitude of V_B makes the number of majority charge carrier exactly equal to the minority charge carrier.

The net current resulting from the flow of minority charge carrier when no external field is applied across the junction is zero.

Therefore, semiconductor remains neutral although V_B appears across the junction.

TERMINAL CHARACTERISTICS OF DIODE :-

FORWARD CHARACTERISTICS :-



Variable supply is connected
Volmeter is connected across
the diode, in parallel to second
Voltage through the diode.
ammeter is connected across the
series to record the milli current in diode.

Series resistance is connected to the diode to limit the current through diode.

every diode has a limit of current if excess of current flows through the diode it will get damage.

The resistance r_m is connected in series to limit current through the diode if the V_a

BY 126

For this diode maximum current rating is 1A. If current flow more current diode will get damage.

If we increase the forward voltage the depletion width decreases and this has potential barrier of 0.7 V for Si and 0.3 V for Ge at 300K.

In the forward biased region for the voltage smaller than 0.5 V then current is negligible, as the applied V_f voltage reaches 0.5V current starts increasing. The voltage at which the current start increasing rapidly is called cutting voltage and denoted by V_t .

When the applied voltage is larger than cutting voltage than the small increase in the voltage produces sharp increase in the current. Thus the current increase exponentially by the according to diode equation.

$$I = I_o (e^{\frac{qV}{nKT}} - 1)$$

I = diode current

I_o = The reverse saturation current

q = electronic charge = 1.6×10^{-19} Coulomb

K = Boltzmann constant = 1.38×10^{-23} J/Kelvin

T = absolute temperature in Kelvin = $273 + \text{temp in } ^\circ\text{C}$

η = Empirical constant

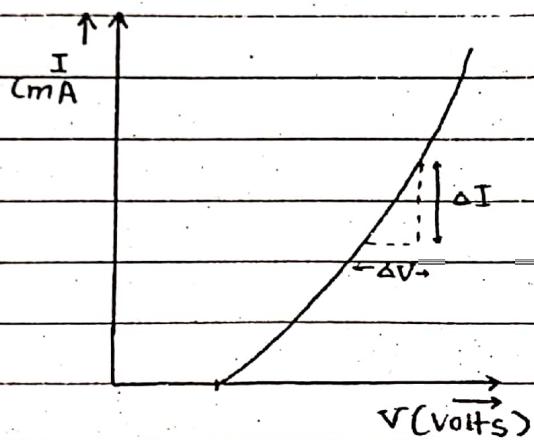
$\eta = 1$ when not specified

$\eta \approx 2$ for Si

$\eta \approx 1$ for Ge

$$V_T = \frac{kT}{q}$$

(iii) ... $I = I_0 (e^{V/\eta V_T} - 1)$. Simplified diode equation



diode resistance in the forward biased condition is of the order of few ohms.

from equation (iii) it can be seen that increase in the temperature causes decrease in the forward voltage and increase in the current I .

$I >> I_0$

I_0 (order of micro or nano)

for the higher current

$$I = I_0 e^{V/\eta V_T} \dots \text{(iv)}$$

$$V = \eta V_T \ln \frac{I}{I_0} \dots \text{(v)}$$

$$\text{for the diode } d_1 \rightarrow I_1 = I_0 e^{V_1/\eta V_T} \dots \text{(vi)}$$

$$\text{for the diode } d_2 \rightarrow I_2 = I_0 e^{V_2/\eta V_T} \dots \text{(vii)}$$

$$\frac{I_2}{I_1} = e^{(V_2 - V_1)/\eta V_T} \dots \text{(viii)}$$

$$(V_2 - V_1) = \eta V_T \ln \frac{I_2}{I_1} \dots \text{(ix)}$$

$$(V_2 - V_1) = 2.303 \eta V_T \log_{10} \frac{I_2}{I_1} \dots (x)$$

Consider a silicon diode with $\eta = 1.5$ find the change in voltage when the current changes from 0.1 mA to 10 mA

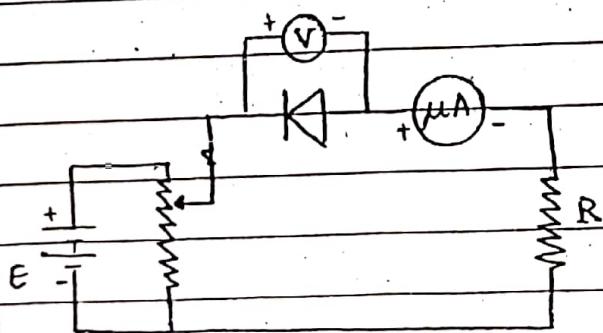
$$V_2 - V_1 = 2.303 \times 1.5 \times 26 \times 10^{-3} \log_{10} \frac{10}{0.1}$$

$$= 179.634 \times 10^{-3} \text{ V}$$

$$= 0.179 \text{ V}$$

at room temperature $V_T = 26 \text{ mV}$

2. REVERSE CHARACTERISTICS :-



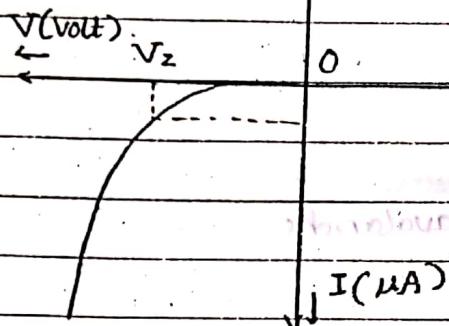
Diode equation

$$I = I_0 (e^{V/\eta V_T} - 1)$$

If Voltage is negative then exponential term approaches to zero and the current

$$I = -I_0$$

If we increase the reverse voltage across the diode the curve will reach the limiting value equal to I_0 which is called as reverse saturation current



If we continue to increase the reverse voltage than the reverse current suddenly shoots up as shown in the figure and this phenomena is called the breakdown of the voltage. And the voltage at which this phenomena take place is called breakdown voltage.

These breakdown is of two types

1. ZENER BREAKDOWN
2. AVALANCHE BREAKDOWN

ZENER BREAKDOWN :-

In the zener breakdown if we increase the reverse voltage the electric field at the junction increases and this high electric field causes the covalent bond break and the large number of charge carrier are generated due to this process resulting large reverse current (due to minority charge carriers).

AVALANCHE BREAKDOWN :-

If we increase the atom avalanche reverse voltage the velocity of the charge increases that means increase the reverse bias voltage faster the electrons moves.

It gains sufficient kinetic energy to break the covalent bond in the atom with which they collide thereby generating

large number of charge carriers and these charge carriers again moves with the high velocity due to increase reverse voltage and breaks other covalent bond.

In this way a large number of charge carriers are generated and give rise to high reverse current and this phenomenon is called ~~reverse breakdown~~ avalanche

1. DIODE MODEL :-

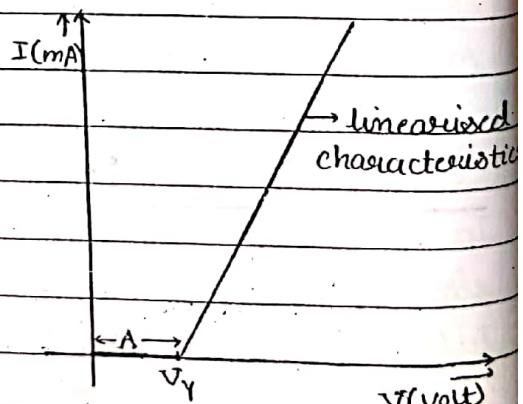
for large signal applications that means for large change in the diode current diode is replaced by its equivalent circuit (diode model).

→ So, that the standard analysis method can be applied to evaluate current and voltage in the circuit.

2. PIECE WISE LINEAR MODEL :-

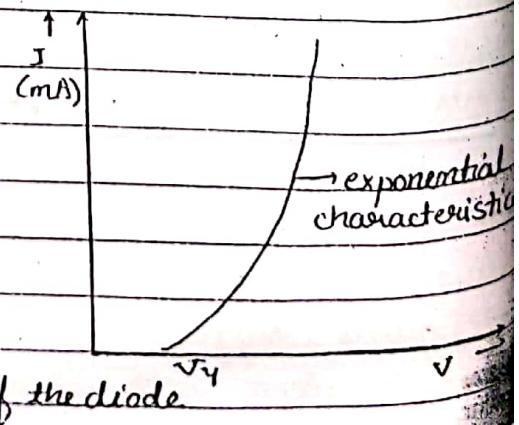
To simplify the analysis process the diode is approximated by two straight lines

→ for $V < V_A$, the diode current is very small it can be neglected and represented by straight line denoted by A.

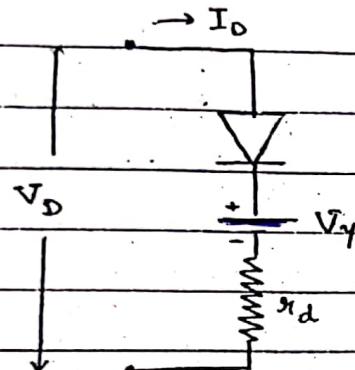


→ for $V > V_A$ current increases rapidly and this part of the characteristics is also assumed to be a straight line having the slope $\frac{1}{r_d}$

$$r_d = \text{resistance of the diode}$$



EQUIVALENT CIRCUIT OF PIECE WISE LINEAR MODEL :-



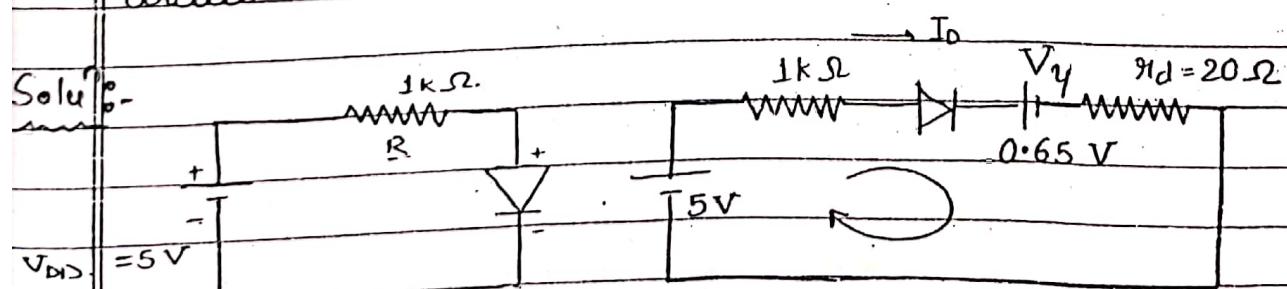
The diode is represented by ideal diode in series with the cutting voltage and in series with the resistance (R_d)

when we have to apply piece wise linear model the diode is replace by the equivalent circuit and analyse the circuit.

$$\rightarrow I_D = 0 \quad V < V_y$$

$$I_D = \frac{V_D - V_y}{R_d} \quad V \geq V_y$$

Ques Determine the current I_d and the diode voltage V_d for the circuit shown in figure by using piece wise linear model
 $V_y = 0.65 \text{ V}$ $R_d = 20 \Omega$ assume that diode have a current of 1mA at Voltage of 0.7V and its voltage drop changes by 0.1 V for every decade change in the current circuit.



From Kirchhoff Voltage Law

$$= -5 + 1000 \times I_D + 0.65 + 20 I_d = 0$$

$$1020 I_D = 4.35$$

$$I_D = 4.26 \times 10^{-3} \text{ A}$$

for diode voltage V_D

$$I_D = V_D - V_T$$

R_d

$$I_D R_d + V_T = V_D$$

$$V_T - 0.65 = 4.26 \times 10^{-3}$$

20

$$V_D = 0.085 + 0.65$$

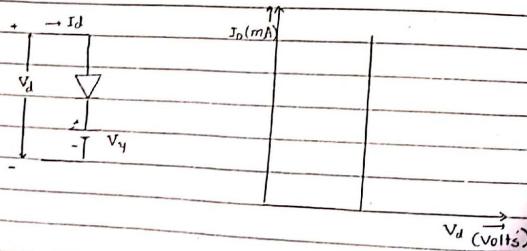
$$= 0.735V$$

2. CONSTANT

VOLTAGE DROP DIODE MODEL :-

For most of the application resistance of the diode is very small as compared to the network resistance so $R_d \ll R$.

Under this condition R_d is neglected from the circuit and the circuit consist of ideal diode in series with the voltage V_T :

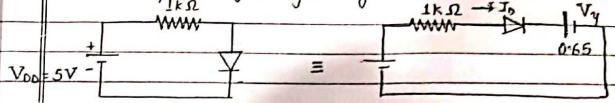


1. In this characteristic fast rising part of the exponential curve is approximated by vertical straight line as shown in the characteristic.

2. There is constant voltage independent of the diode current I_D .

$$V_T \text{ of Silicon} = 0.7V$$

Solve example 1 by using voltage drop diode model



$$= -5 + 1000 \times I_D + 0.65 = 0$$

$$1000 \times I_D = 5 - 0.65$$

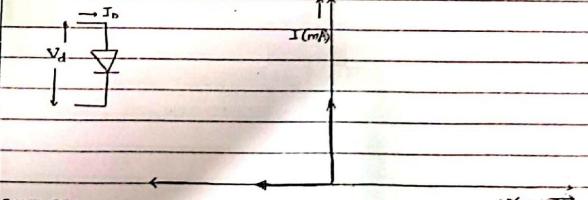
$$I_D = 4.35 = 4.35 \text{ mA}$$

$$1000 = 4.35 \times 10^{-3} \text{ A}$$

3. IDEAL DIODE MODEL :-

For most of the applications the R_d is very small as compared to the resistance of network, in addition to this applied voltage is very large as compared to the voltage of diode.

Under this condition the R_d , V_T are neglected and the circuit remain the same.



FEATURES

For ideal diode if applied voltage is less than the diode voltage then the diode is reverse biased ($V_D < 0$) when diode is reverse biased then no current flow through the diode and diode behave as open circuit as shown

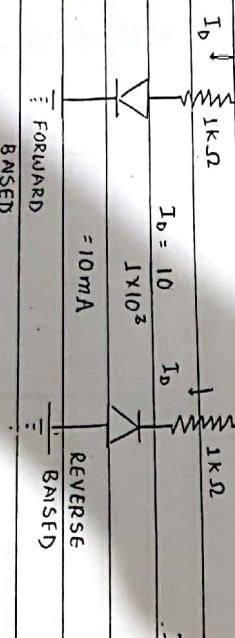


$$(V < 0, I_D = 0)$$

\rightarrow If positive current is applied to diode ($I_D > 0$) so $V_D = 0$ and diode is forward biased. When diode is forward biased voltage drop appears across the diode. zero voltage drop appears across the diode. \rightarrow Diode behaves as short circuited under forward biased condition as shown.

- \rightarrow Diode is a non-linear device because the characteristic is divided into two regions.
- \rightarrow Resistances are two-terminal device. It is a linear device.
- \rightarrow It can be noted that the external circuit must be designed to limit the forward current through the diode.

Calculate current through the diode.

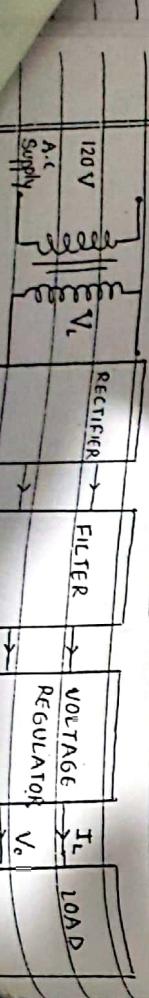


Diode rectifier converts input signal to the unipolar output and this output is not the pure DC but pulse rating DC. Hence filter the circuit is used to minimise the AC variation from the rectifier output voltage. The output of the rectifier filter is more constant than without filter but still consist of AC supply. The voltage regulator is used to reduce the ripples and stabilise the magnitude of DC output voltage against the variations caused by change in load current.

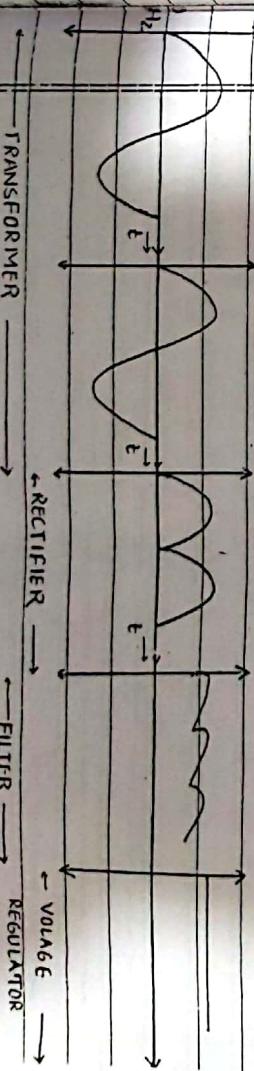
RECTIFIER :-

The circuit which convert AC voltage into DC voltage is called rectifier.

BLOCK DIAGRAM FOR RECTIFIER PROCESS :-



Block diagram for rectifier process :-

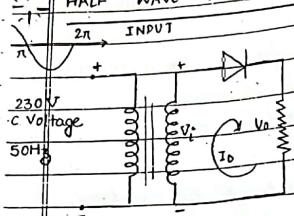


First block is the power transformer. It consists of primary winding having N_1 turns connected to 120V AC supply voltage and the secondary winding having N_2 number of turns is connected to the circuit of DC power supply. Thus an AC voltage V_1 of $(120 \frac{N_2}{N_1})$ Volts rms develops between

two terminals of the secondary winding. By selecting appropriate turns ratio from the transformer the voltage can be step-down depending on the requirement.

Also the transformer provide isolation between the electronic devices and the main power line and this isolation minimises the risk of electric shock.

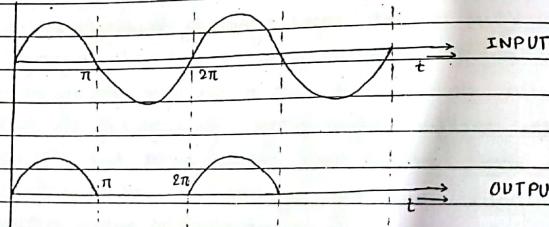
① HALF WAVE RECTIFIER (WITHOUT FILTER) :-



During positive half cycle diode is forward biased.

Input voltage (V_i) = $V_m \sin \omega t$
will behave as short circuit and
the current flows through the diode
and the load R_L as shown in figure

→ Since in forward biased diode has very small voltage drop (0.7V for Si, 0.3V for Ge) therefore voltage appearing across the load is same as the input voltage at every instant.



During the negative half cycle polarity of the input sin wave get reversed (from π to 2π) then diode is reverse biased as it is open circuited then no current flows in the circuit hence no voltage is developed across R_L ; therefore all the input voltage appears across the diode itself that means across the non conducting diode which is called peak inverse voltage.

PEAK INVERSE VOLTAGE :-

V_D is the maximum voltage that appears across the diode during the negative half cycle.

for $\pi \leq \omega t \leq 2\pi$

$$-V_D R_L + V_i - V_D = 0$$

$$V_i = V_D$$

$$V_D = V_m \sin \omega t$$

$$V_i = V_m \sin \omega t \quad 0 \leq t \leq \pi$$

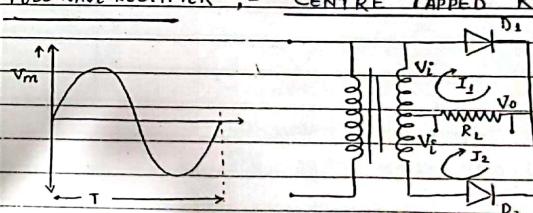
$$V_D = V_m \sin \omega t \quad 0 \leq t \leq \pi$$

$$V_o = 0 \quad \pi \leq t \leq 2\pi$$

Peak Inverse voltage = V_m

② FULL WAVE RECTIFIER :-

(a) CENTRE TAPPED RECTIFIER :-

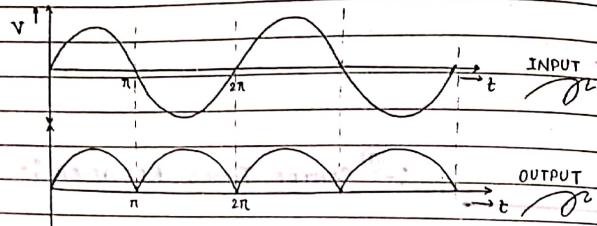


This is the circuit of full-wave rectifier with centre tapped transformer

→ During positive half cycle of the input voltage ($V_i = V_m \sin \omega t$) Diode D_1 is forward biased and D_2 is reverse biased during this cycle upper half of the transformer is connected to the load R_L through diode D_1 . The lower section of the transformer is disconnected from the load because diode D_2 is open circuited. The current I_1 flows through diode D_1 , load resistor R_L and upper half of the transformer winding and current I_2 is zero.

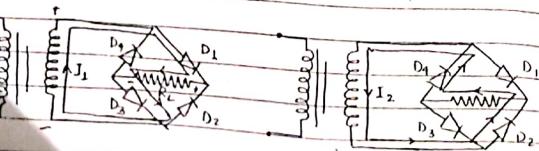
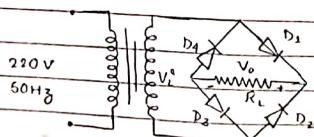
Date _____
Page _____

During negative half cycle of the input diode D_1 is reverse biased and D_2 is forward biased. the lower half of the transformer is connected to load R_L through diode D_2 because it behaves as short circuit. Then current I_2 flows through diode D_2 load R_L and lower half of the transformer and current I_1 is zero because diode D_3 is reverse biased. Hence, it behaves as open circuited disconnecting upper half of the transformer from load R_L .



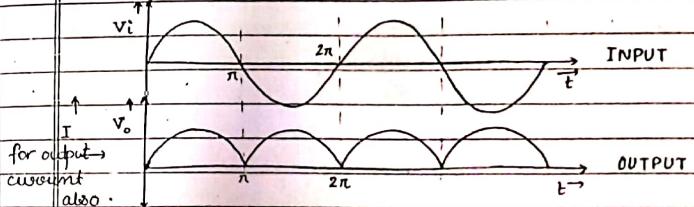
$$-V_i - V_{i\text{ peak}} + \text{peak inverse voltage} = 0 \\ (\text{PIV}) \quad \text{peak inverse voltage} = 2V_i$$

(b) BRIDGE RECTIFIER :-



→ During positive half cycle of input diode D_1 and D_2 are forward biased and diode D_3 and D_4 is reverse biased. on open circuit current I_1 flows through transformer (secondary winding) diode D_1 load R_L and diode D_3 as shown in figure.

→ During negative half cycle of the input diode D_3 and D_4 are forward biased and diode D_1 and D_2 are open circuited or reverse biased hence the current flow (I_2) flows through diode D_3 , D_4 , R_L and secondary winding of the transformer.

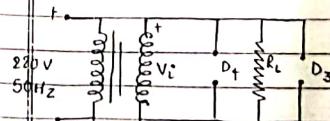


In both the cases that means during positive and negative half cycle current passes through R_L in the same direction output current

Therefore, unidirectional voltage is developed across the R_L .
Mathematical equation : $V_o = V_m \sin \omega t$

$$V_o = V_m \sin \omega t \quad 0 \leq t \leq \pi$$

$$V_o = V_m \sin \omega t \quad \pi \leq \omega t \leq 2\pi$$



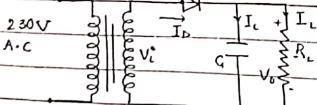
$$\text{Peak inverse voltage} = V_m$$

Page

1. DIFFERENCE BETWEEN FULL WAVE RECTIFIER WITH CENTRE TAPPED TRANSFORMER AND BRIDGE RECTIFIER

1. Peak inverse voltage for bridge rectifier is V_m and for full wave rectifier is $2V_m$.
- (Center tapped)
2. In bridge rectifier centre tapped transformer is not required.
3. The main disadvantage of the bridge rectifier is that it requires four diode which creates problem for low DC voltage application that is secondary voltage is low and two diode voltage drop (1.4 V for Si) becomes significant because out of four diodes two conducts on alternate half cycle. These voltage drops may be compensated by selecting a transformer with higher secondary winding voltage, but in this case voltage regulation will be poor therefore center tapped transformer based full wave rectifier is preferred for low voltage application that means which has only one diode voltage drop equal to (Example : 0.7 V for Si).

1. HALF WAVE RECTIFIER WITH FILTER :-

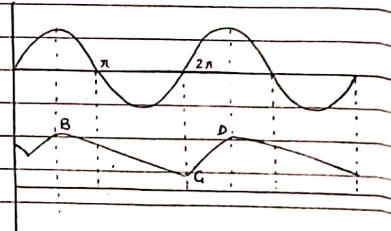


Output of half wave rectifier without filter is not pure DC but it is pulse rating DC. Filter is used to smooth out the AC variations from the rectified voltage. The shunt capacitor filter is the cheapest filter (the large value capacitor is connected in parallel with load R_L as shown).

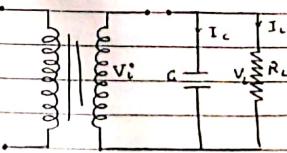
Date _____
Page _____

is called shunt

- The capacitor offers a low reactance path ($X_C = 1/\omega C$) to the AC component of current (that means if capacitor is large X_C is less) only small part of the AC component passes through the load producing small supply voltage.
- At δ frequency or DC it is an open circuit then all the DC current passes through the load R_L .
- During positive half cycle (first quarter cycle of the input voltage) diode is forward biased that means when the rectifier output voltage increases capacitor charge to peak voltage V_m when diode conducts the source voltage is directly connected across the capacitor. Hence voltage across the capacitor is V_m . Just pass the positive peak of the input voltage the rectifier output voltage starts to fall as shown by dotted line. But at this point 'B' the capacitor has $+V_m$ Voltage across it and the source voltage become less than V_m then diode is reverse biased on open circuit.



The source voltage disconnected from the load R_L then



During negative half cycle of the input voltage diode is reverse biased under this condition the capacitor starts to discharge to the load that

means the voltage across the capacitor starts decreasing.
Because there is some voltage drop across the load R_L . OR

because the same voltage loss $I^2 R_L$ across load R_L , the capacitor voltage starts decreasing.
The capacitor continues to discharge through the R_L until the source voltage becomes more than the capacitor voltage that means at point C in the figure.

The RC time constant is higher than that of the time period of the wave form. When the source voltage is greater than the capacitor voltage, the diode again starts conducting that means for the next cycle when the source voltage again reaches its maximum value (i.e. V_m) the capacitor is again charged to voltage V_m (point D).

During the time the capacitor is charging the rectifier supplies the charge current (I_C) through the capacitor as well as the load R_L . When capacitor discharges (from B to C). The rectifier does not supply any current. Then capacitor sends the current (I_C) through the load R_L . In this way current is maintained through the load all the time. The rate at which the capacitor discharges depends on the time constant RC . Larger the time constant more DC is the output wave form.

If the load current (I_L) is very small (that means if R_L is very large) then the capacitor does not discharge very much and V_{DC} output is less than V_m . Then any increase in the load current makes the time constant of the discharged path smaller and capacitor discharges more rapidly and the load voltage is not constant. Difficulties increases with increase in load current and also V_{DC} decreases this was the condition of selection of R_L .

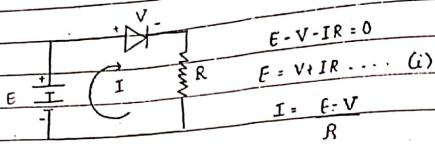
If the capacitor is too large, the more DC output can be obtained but if the capacitor is very large its size will be large and current required to charge the capacitor to a given voltage is also large.

The maximum current ratings of the current is given by the manufacturer so this put the limitation on the value of capacitor used in it.

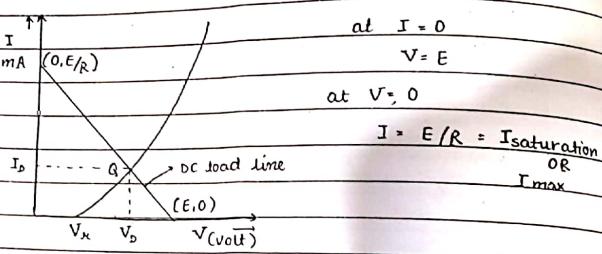
FULL WAVE RECTIFIER WITH FILTER :-

DC LOAD LINE :-

DC load line is useful to find the operating point (also called Q point) that means the current I_0 and Voltage V_D at which the diode is working.



GRAPHICAL METHOD



equation number (iii) is the equation of a straight line. It is called the saturation current because the current is maximum at this point. This is the graphical method of obtaining the point at which the diode is working that is voltage and current at which the diode is working.

DC STATIC RESISTANCE :-

Resistance of diode at a particular operating point is called DC static resistance of the diode

$$R_{dc} = \frac{V_D}{I_0} = V$$

$$I_0 (e^{\frac{V}{nV_T}} - 1)$$

V : diode voltage

I : diode current

Date _____
Page _____

from the graph it can be seen that DC resistance of the diode decreases as we approach in the region of high current and voltage. Since the diode is non-linear device its DC-resistance varies with the current.

FOR EXAMPLE : $I_0 = 10 \text{ mA}$ $V_D = 0.65 \text{ V}$

$$R_{dc} = \frac{0.65}{10 \text{ mA}} = 6.5 \Omega$$

This is also called as the forward resistance of the diode and it is the order of few ohms

$$I = 30 \text{ mA} \quad V_D = 0.75 \text{ V}$$

$$R_{dc} = \frac{0.75}{30} = 25 \Omega$$

$$I = 0.50 \text{ mA} \quad V = 0.85$$

$$R_{dc} = \frac{0.85}{0.50} = 17 \Omega$$

DC REVERSE RESISTANCE :-

It is the ratio of DC diode voltage and DC diode current at particular operating point under reverse biased condition

EXAMPLE $V = -20 \text{ V}$ $I = -25 \text{ mA}$

$$R = \frac{-20}{-25 \text{ mA}} = \frac{0.8 \times 10^3 \Omega}{25 \text{ mA}} = 800 \times 10^6 \Omega = 800 \text{ M}\Omega$$

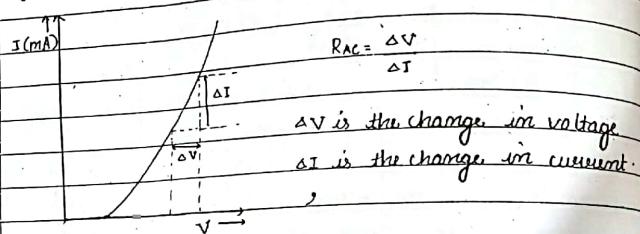
$$V = -75 \text{ V} \quad I = -5 \mu\text{A}$$

$$R = \frac{-75}{-5 \times 10^{-6}} = 15 \text{ M}\Omega$$

- Reverse resistance is very high of the order of mega ohm
- The DC resistance decreases as we approach the breakdown voltage but still very high of the order of mega ohms.
- Once the DC resistance of the diode is known for a particular operating point then diode can be replaced by

resistive element and it simplifies the analysis process

AC RESISTANCE OR DYNAMIC RESISTANCE OF THE DIODE
It is the resistance of the diode at Q-point determined by the slope of the characteristic curve.



→ Step to find the exact value straight line is drawn tangent to the characteristic curve through the Q -point and this will define particular change in current and voltage.

THEORETICAL METHOD

$$R_{AC} = \frac{\Delta V}{\Delta I} = \frac{dV}{dI} = \frac{1}{dI/dV}$$

$$I = I_0 (e^{\frac{V}{\eta V_T}} - 1)$$

$$\frac{dI}{dV} = I_0 \cdot \frac{1}{\eta V_T} e^{\frac{V}{\eta V_T}} = I + I_0 \quad \dots \text{(ii)}$$

$$R_{AC} = \frac{\eta V_T}{I_0 e^{\frac{V}{\eta V_T}}} \quad dI = I \quad \dots \text{(iii)}$$

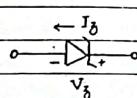
the vertical axis section of characteristic $\eta = 1$ for Germanium and Silicon (V_T at room temperature = 26 mV)

$R_{AC} = \frac{dV}{dI}$	$= 26 \text{ mV}$
I	

ZENER DIODE :-

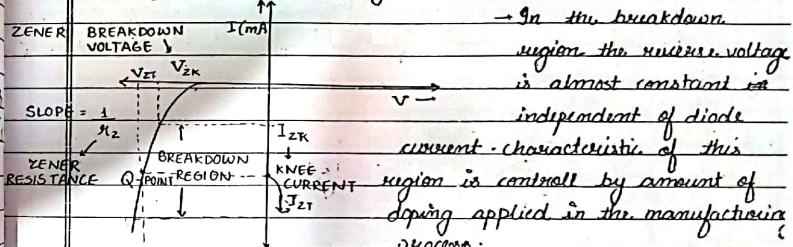
It is heavily doped diode designed to operate in the breakdown region without any damage.

It is possible to produce zener diode from breakdown voltage 2V to 200V



→ forward characteristic of zener diode is same to that of ideal silicon diode.

→ reverse characteristic exhibit the region called zener breakdown region.



→ From the IV characteristic shown in figure for the current greater than I_{ZT} (knee current) characteristic is almost a straight line. The voltage across zener diode (V_{ZT}) at specified test current I_{ZT} which is given by the manufacturer.

As the current through the zener diode deviates from I_{ZT} , the voltage across it will change slightly. The change in voltage ΔV corresponding to change in current ΔI is given by this equation.

$$\Delta V = g_z \Delta I \quad g_z = \frac{\Delta V}{\Delta I}$$

→ R_z is also called dynamic or incremental resistance of zener diode at operation point Q. This R_z is given by the manufacturer. The range of R_z is from few ohms to few 10 of ohms.

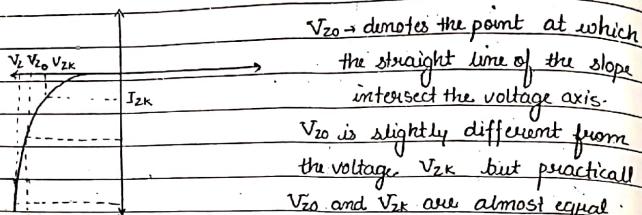
It can be seen from the characteristic I_z remains low and almost constant over wide range of current and increases considerably in the vicinity of the knee current.

$$P_z = V_z I_z \rightarrow \text{POWER OF ZENER DIODE}$$

The maximum power is also given by the manufacturer ($P_{z\max}$). When $P_z < P_{z\max}$, then zener diode operates in the breakdown region without any damage.

Similarly, the current

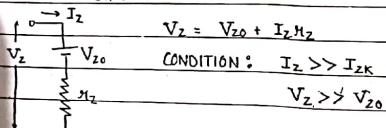
$$I_{z\max} = \frac{P_{z\max}}{V}$$



V_{z0} denotes the point at which the straight line of the slope intersects the voltage axis.

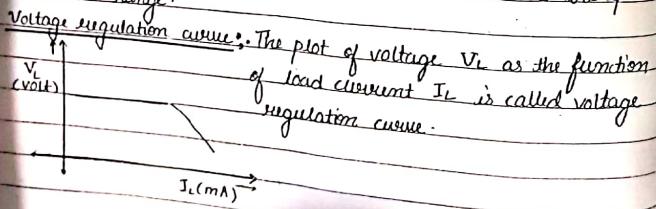
V_{z0} is slightly different from the voltage V_{zk} but practically V_{z0} and V_{zk} are almost equal.

EQUIVALENT CIRCUIT

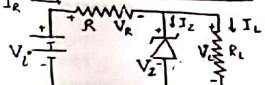


APPLICATION OF ZENER DIODE :-

AS VOLTAGE REGULATOR :- Voltage regulators are circuits that provide constant voltage (constant DC output voltage) even though the source voltage V_i and the load current I_L vary over wide range.



CIRCUIT FOR VOLTAGE REGULATOR :-



Date _____
Page _____

As long as the voltage across R_L is less than V_z diode is reverse biased or open circuited. Under this condition resistance R and R_L makes the potential divider across V_i . As V_i increases, the voltage across R_L becomes greater than V_z then zener diode is forward biased and operate in the breakdown region. So in the breakdown region the zener diode voltage V_z is almost constant even though current I_z is flowing through it may vary considerably.

$$I_R = I_z + I_L$$

If the load current I_L increases current I_z decreases by the same percentage in order to maintain the constant current I_R and hence the voltage drop across R is constant and the output voltage V_o remains constant ($V_o = V_i$)

If the load current I_L decreases current I_z increases to maintain the constant current I_R and hence the output voltage is stabilized.

If input voltage V_i increases zener diode current I_z is also large and thus there is extra voltage drop across R .

If V_i decreases then I_z also decreases and the voltage drop across R is reduced and because of the self adjusting voltage drop across R the output voltage V_o is almost constant with the variation of input V_i .

Determine the diode current at 20°C with reverse saturation current $I_0 = 50\text{ }\mu\text{A}$ and applied forward bias of 0.6 V

$$\eta = 1$$

$$V_T = 25\text{ mV}$$

$$\text{Diode Current} : I = I_0 (e^{V_T / (kT)} - 1)$$

$$= 50 \times 10^{-6} (e^{0.6 / (25 \times 10^{-3})} - 1)$$

$$= 50 \times 10^{-6} (e^{24} - 1)$$

$$= 2.66 \times 10^{-3} \times 10^{-6} \text{ A}$$

$$= 2.66 \times 10^{-9} \text{ A}$$

Ques. Current flowing in certain pn-junction at room temperature is $2 \times 10^{-7} \text{ A}$ when large reverse biased voltage is applied calculate the current flowing when 0.1 V is applied

Date _____
Page _____

$$I = I_0 (e^{\frac{V}{\eta V_T}} - 1)$$

$$= 2 \times 10^{-7} (e^{0.1/125 \times 10^{-3}} - 1)$$

when large reverse biased voltage is applied $I = I_0 = 2 \times 10^{-7} \text{ A}$

$$= 9.1 \mu\text{A}$$

Ques. Calculate the ratio of the current for forward biased of 0.06 V to the current for the same value of reverse biased applied to germanium pn junction diode at 27°C .

forward biased: $I = I_0 (e^{\frac{V}{\eta V_T}} - 1)$

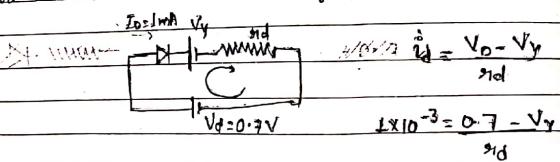
reverse biased: $I = I_0$

$$\text{Ratio} = \frac{e^{\frac{V}{\eta V_T}} - 1}{e^{\frac{0.06}{125 \times 10^{-3}}} - 1}$$

$$= e^{2.4} - 1$$

$$= 10.023$$

Ques. Find the parameters of piece wise linear model of diode for which $V_D = 0.7 \text{ V}$ and $I_0 = 1 \text{ mA}$ and $\eta = 2$.



Ans. (6)

Consider a silicon diode ($\eta = 1.5$) find the change in voltage if current is changes from 0.1 mA to 10 mA

$$\Delta V = V_2 - V_1$$

$$I_2 = p \frac{(V_2 - V_1)}{\eta V_T}$$

$$I_1$$

$$10 = e^{\frac{(V_2 - V_1)}{1.5 \times 25 \times 10^{-3}}}$$

$$0.1$$

$$V_2 - V_1 = 1.5 \times 10^{-3} \times 25 \log_{10} 100 = 172.5 \times 10^{-3} \text{ V}$$

Silicon diode with $\eta = 1$ has voltage $= 0.5 \text{ V}$ at this voltage $I = 0.1 \text{ mA}$ find the voltage drop at $i = 0.1 \text{ mA}$ and $i = 10 \text{ mA}$.

$$I = I_0 e^{\frac{V}{\eta V_T}}$$

$$I = I_0 e^{\frac{0.5}{125 \times 10^{-3}}}$$

$$I_0 = 6.9 \times 10^{-16} \text{ A}$$

Date _____
Page _____

$$10^{-3} \times 0.1 = 6.9 \times 10^{-16} \times e^{\frac{V}{125 \times 0.5}} \Rightarrow \text{FOR } 0.1 \text{ mA}$$

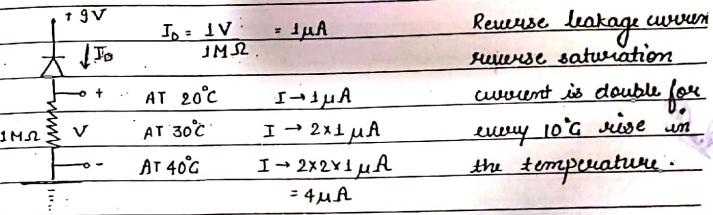
$$V = 0.64 \text{ V}$$

$$10 \times 10^{-3} = 6.9 \times 10^{-16} \times e^{\frac{V}{125 \times 0.5}} \Rightarrow \text{FOR } 10 \text{ mA}$$

$$V = 0.756 \text{ V}$$

Ques. The diode in the circuit is a large high current device whose reverse leakage is reasonably independent of the voltage. If $V = 1 \text{ V}$ at 20°C find the value of V at 40°C and 0°C

$$V = 1 \text{ V}$$



$$V = IR = 4 \times 10^{-6} \times 1 \times 10^6 = 4 \text{ V}$$

$$\text{AT } 0^\circ\text{C} \quad I = 0.25 \mu\text{A}$$

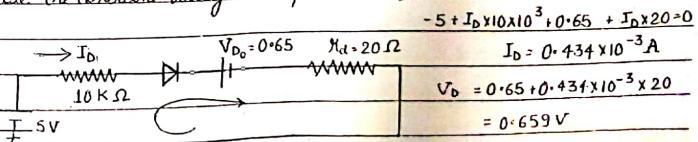
$$V = IR = 0.25 \times 10^{-6} \times 1 \times 10^6 = 0.25 \text{ V}$$

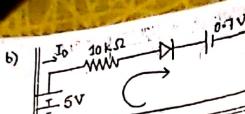
Ques. For the circuit shown in figure find current I_D and V_D for the case $V_{DD} = 5 \text{ V}$ and $R = 10 \text{ k}\Omega$

Assume that diode has voltage of 0.7 V at 1 mA and that the voltage changes by 0.1 V per decade of current change.

(a) use the piece wise linear model with $V_{D0} = 0.65 \text{ V}$ and $R_D = 20 \Omega$

(b) use the constant voltage drop model with $V_0 = 0.7 \text{ V}$





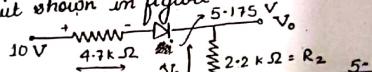
$$-5 + I_D \times 10^3 + 0.7 = 0$$

$$10000 I_D = 4.3$$

$$I_D = 4.3 \times 10^{-4}$$

$$= 0.43 \text{ mA}$$

Q12 Determine current I , voltage V_1 , V_2 and V_0 for the series circuit shown in figure.



$$I = 2.07 \text{ mA}$$

$$V_1 = 9.73 \text{ V}$$

$$V_2 = 4.55 \text{ V}$$

$$V_0 = 5.175 \text{ V}$$

$$-10 + 0.7 + 4.7 \times 10^3 \times I + V_0 = 0$$

$$-10 + 0.7 + 4.7 \times 10^3 \times 2.07 \times 10^{-3} + V_0 = 0$$

$$V_0 = 2.2 \times 10^3 \times 2.07 \times 10^{-3}$$

$$I = 2.07 \text{ mA}$$

$$V_1 = 4.7 \times 10^3 \times 2.07 \times 10^{-3} = 9.73 \text{ V}$$

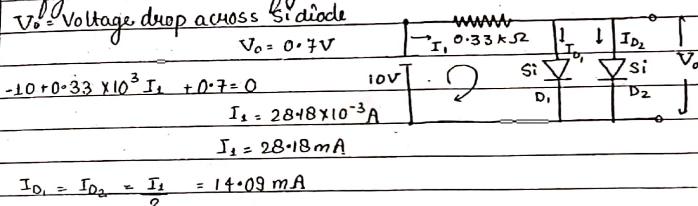
$$V_2 = -2.2 \times 10^3 \times 2.07 \times 10^{-3} = -0.46 \text{ V}$$

$$V_0 = 5.175 \text{ V}$$

$$V_2 = 2.2 \times 10^3 \times 2.07 \times 10^{-3}$$

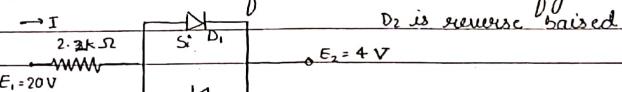
Q13 Determine the voltage V_0 , I , I_D , and I_R for parallel diode configuration shown in figure.

V_0 = Voltage drop across Si diode



$$I_D = I_{D2} = \frac{I}{2} = 14.09 \text{ mA}$$

Q14 Determine the current I for the network shown in figure.



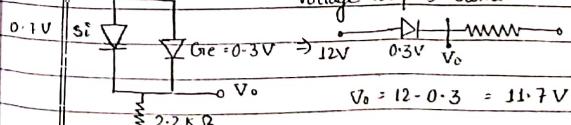
$$-16 + I \times 2.2 \times 10^3 + 0.7 = 0$$

$$15.3 = 2.2 \times 10^3 I$$

$$I = 6.96 \text{ mA}$$

Determine the voltage V_0 for the given circuit.

Ge and Si is in parallel and in parallel voltage drop is same



$$V_0 = 12 - 0.3 = 11.7 \text{ V}$$

Determine the currents I_1 , I_2 and I_{D2} for the circuit shown in figure.

(16)

$$(I_1 + I_2) \cdot 3.3k\Omega = 0.7 + 3 \cdot 3 \times 10^3 I_1 = 0$$

$$I_1 = 0.212 \text{ mA}$$

$$0.7 - 20 + 0.7 + (I_1 + I_2) \times 5.6 \times 10^3 = 0$$

$$I_1 + I_2 = 18.6 \text{ mA}$$

$$5.6 \times 10^3$$

$$3.32 \text{ mA} = 0.212 \text{ mA} + I_2$$

$$I_2 = 3.108 \text{ mA}$$

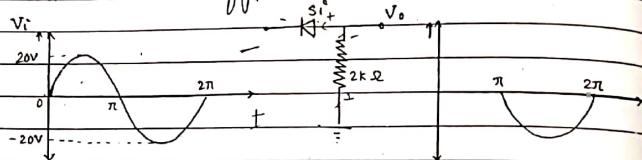
(17)

$$V_2 = (I_1 + I_2) R_2$$

$$= (3.32) \times 10^{-3} \times 5.6 \times 10^3$$

$$= 18.59 \text{ V} = 18.6 \text{ V}$$

Sketch the output voltage V_o and determine the D.C level of output for the network shown in figure.



During the positive half cycle the diode is reverse biased and during the negative half cycle the diode is forward biased.

$V_{DC} = 0.318$

$V_{DC} = -0.318 \times 20$

$= -6.36 \text{ V}$

(18) Repeat the above problem when ideal diode is replaced by silicon diode.

$V_{DC} = -0.318 (V_m - V_d)$

$= -0.318 \times 0.7$

$= -6.14 \text{ V}$

The resulting drop in the D.C level is 0.22V or 3.5%.

(19) Repeat the above two part if V_m is increased to 200V and compare the solution.

I_{DC}

WAVE SHAPING CIRCUITS

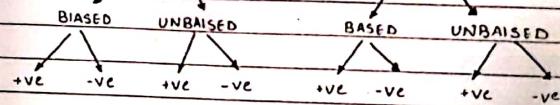
1. Clipper

2. Clamp

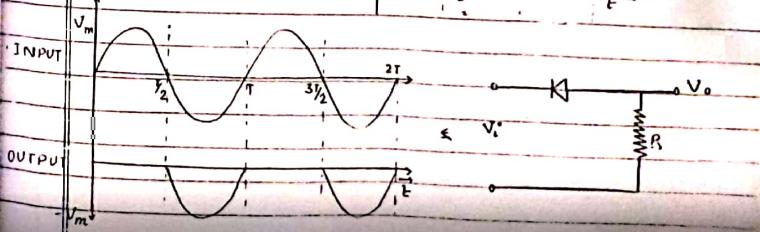
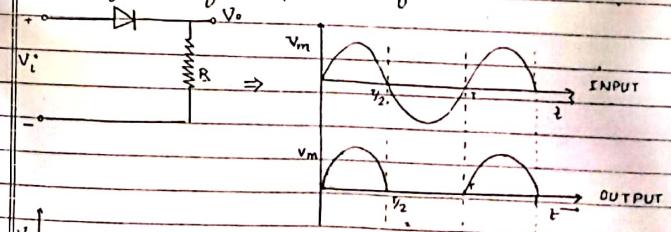
CLIPPER

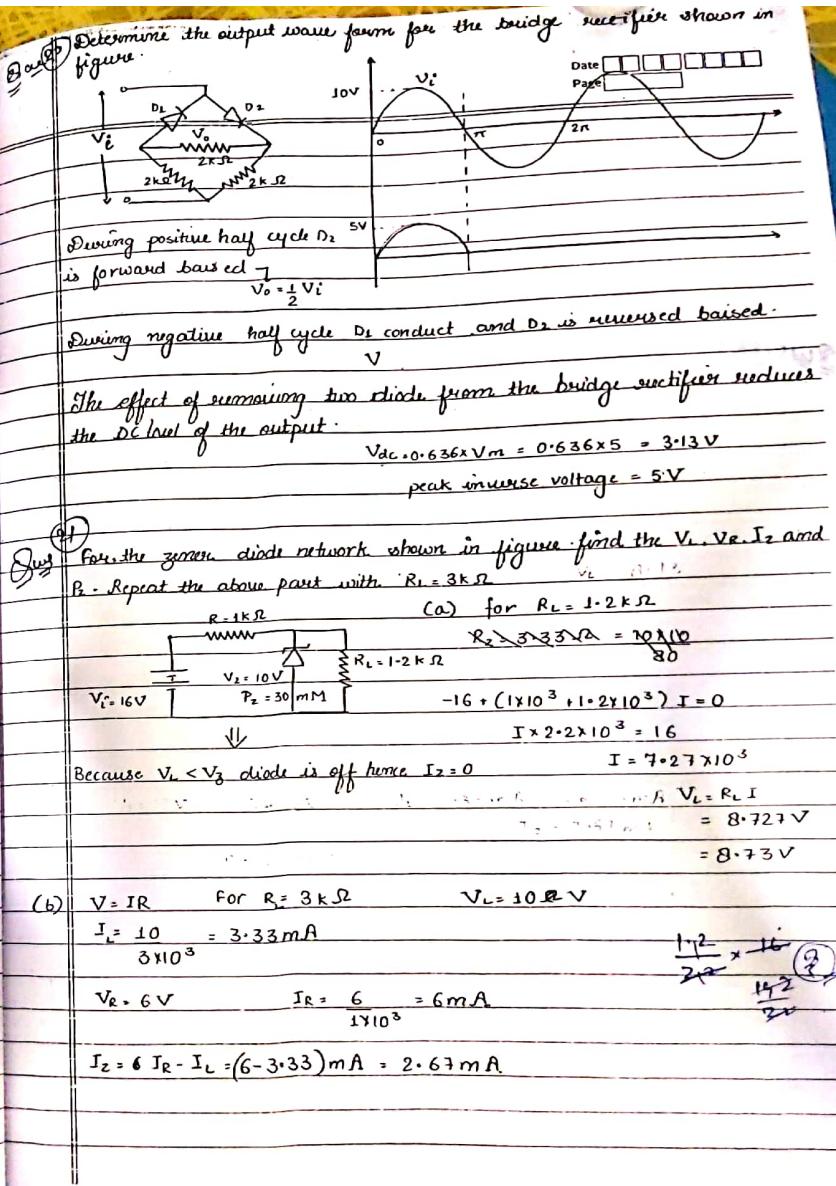
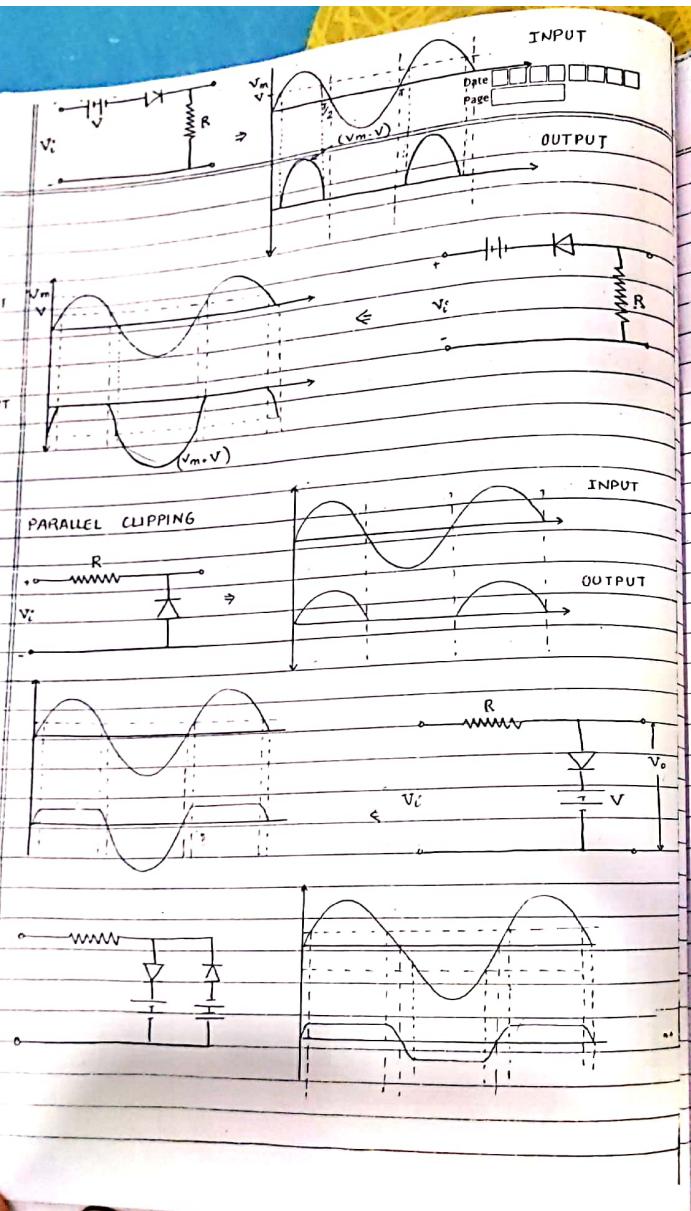
SERIES CLIPPER

PARALLEL CLIPPER



Clippers are those circuits/network which employ a diode to clip away a portion of an input signal without distorting the remaining part of the applied waveform.





Ques 21) A 9.1 V zener diode exhibit nominal voltage at test current of 20 mA at this current the incremental resistance is specified at 50Ω . Find V_{Z0} of the zener model. Find the zener voltage at the current of 10 mA and at 100 mA.

Date / /
Page

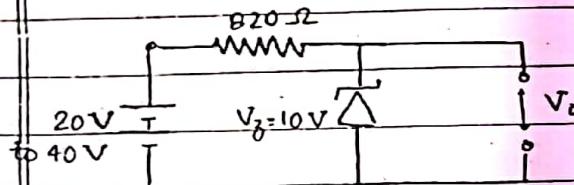
At 10 mA

$V_{Z0} = 9.55 V$

$V_Z = 9.1 V$

Ques 22)

The zener diode of the given figure has $V_Z = 10V$ use ideal zener approximation to find maximum and minimum zener current.



for minimum current $-20 + 820 i_3 + 10 = 0$

$$i_3 = 10/820 = 0.01219 A = 12.2 \text{ mA}$$

for maximum current $-40 + 820 i_3 + 10 = 0$

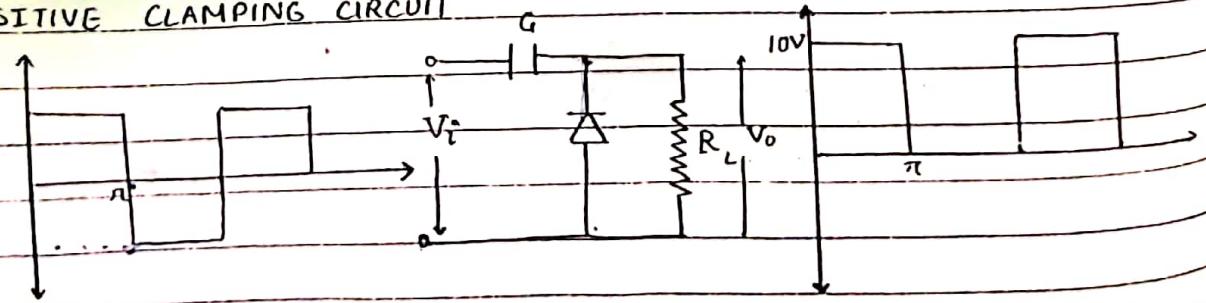
$$i_3 = 30/820 = 0.03658 A = 36.6 \text{ mA}$$

CLAMPING CIRCUIT

This is the circuit that places the either positive or negative peak of the signal at desired D.C level.

TYPES OF CLAMPING CIRCUIT

1. POSITIVE CLAMPING CIRCUIT

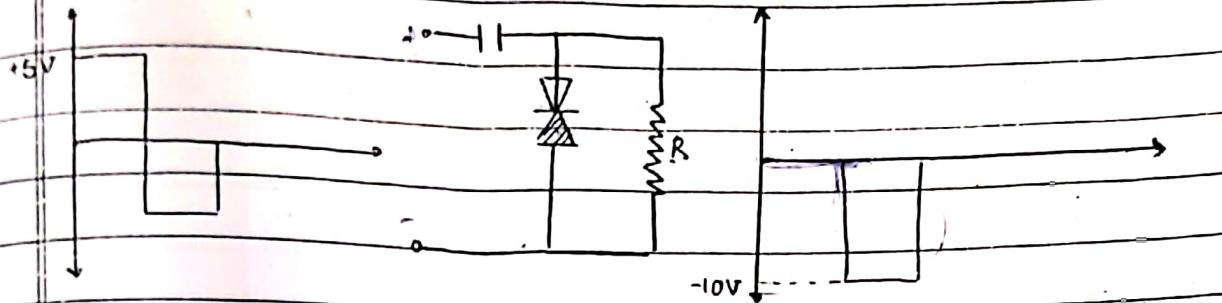


During the negative half cycle diode is forward biased and behaves as short circuited. The time constant $RC = 0$ because the resistance of forward biased diode is zero. Consequently the capacitor charges

-5V and stays at that level during the negative half cycle. During the positive half cycle of the input (for +5V) then diode is reverse biased so that the capacitor fails to discharge through the load R_L . Apply KVL to the circuit output voltage is 10V. 5V across capacitor.

Date _____
Page _____

NEGATIVE CLAMPING CIRCUIT.



During positive half cycle diode is forward biased. The time constant $RC = 0$ (Resistance of forward biased diode is zero). Capacitor charges to +5V and stays at that level for entire positive half cycle.

During negative half cycle diode is reverse biased and capacitor fails to discharge through the load R_L .

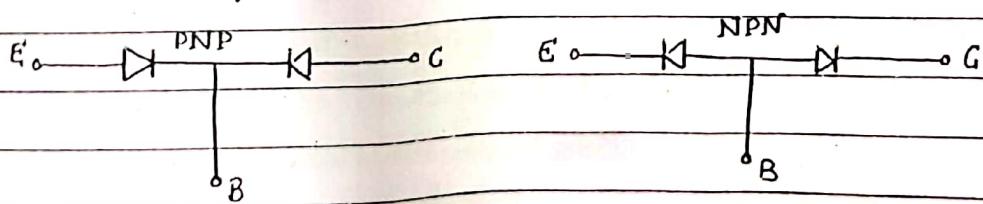
\Rightarrow That means the signal has been pushed downward by 5V.

UNIT 2 TRANSISTER

Transistor is a 3-layer device consists of 3 terminals - collector, base and emitter.

OR

It is two p-n junctions connected in back to back mode.



CONSTRUCTION PART:

The size of collector is largest because it has to collect all the injected carriers. Base region is thin and lightly doped so that most of the injected carriers do not recombine in the base region but diffuse to the collector region.

The size of emitter is in between that of collector and base. Emitter is heavily doped because the function of emitter is to emit the majority charge carriers and minority charge carriers into the base region.

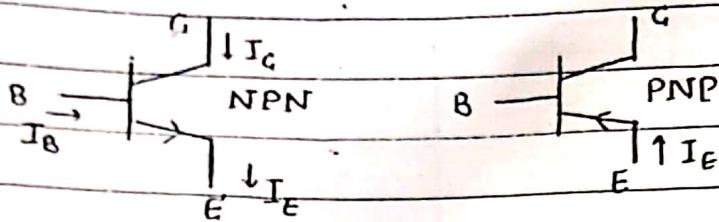
Base is lightly doped and collector doping is in between the emitter and base.

JUNCTIONS OF TRANSISTOR

Date _____
Page _____

1. Emitter Base Junction

2. Collector Base Junction.



BIASING OF A TRANSISTOR

1. BIASING FOR ACTIVE REGION

Emitter base junction is forward biased and collector base junction is reverse biased.

2. BIASING FOR CUT-OFF REGION

Emitter base junction and collector base junction both are reverse biased.

3. SATURATION REGION

Emitter base junction and conduction base junction are forward biased.

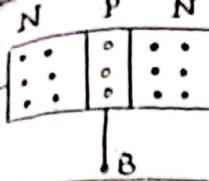
4. INVERSE ACTIVE REGION

Emitter base junction is reverse biased, and conduction base junction is a forward biased.

OPEN CIRCUITED TRANSISTOR

When no external supply is connected across the transistor then all the transistor currents must be 0 and majority charge carrier moves across the junction and creates potential barrier at thermal equilibrium.

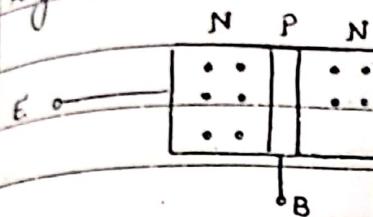
Depletion layer at the two junction prevents further movement of free carriers across the junction.



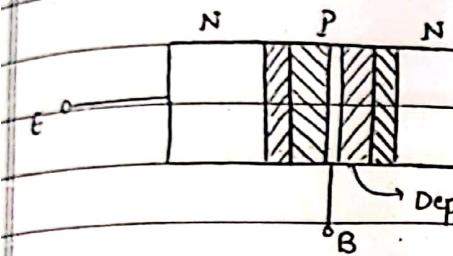
The three regions have different doping levels. depletion layers do not have same width. The region which is heavily doped consists of greater concentration of ions near the junction. So the depletion layer is thin in the emitter region and wide in the base region.

Date _____
Page _____

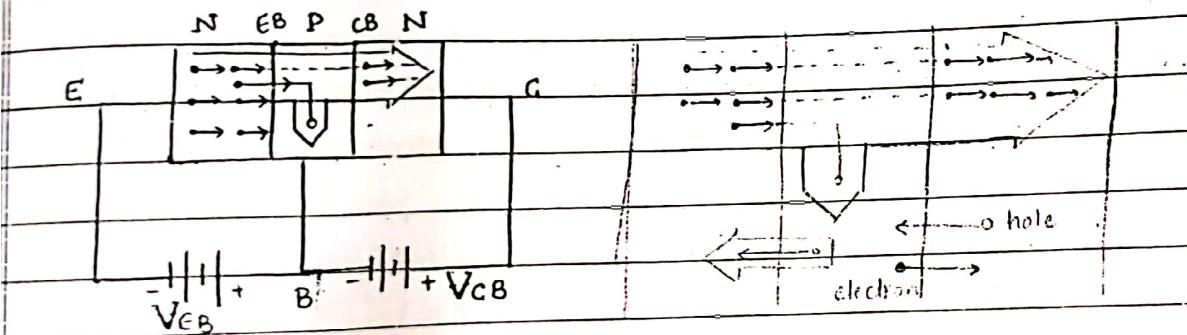
doped consists of greater concentration of ions near the junction. So the depletion layer is thin in the emitter region and wide in the base region.



Similarly in the collector side it is thin in the collector region and wide in the base region.



PRINCIPLE OF OPERATION OF BIPOLAR JUNCTION TRANSISTOR



Emitter-base junction is forward biased and collector-base junction is reverse biased for active region. With the forward biased, emitter junction depletion width or depletion layer decreased and majority charge carrier diffuse across the junction that means emitter emits the electron into p-type base region that means these electrons become minority carrier in the base region. Since the base region is thin and lightly doped therefore few electrons recombine with the holes of base region and constitute the portion of base current. Therefore majority electrons moves towards the collector region.

Since the collector-base junction is reverse biased hence there is large depletion layer at collector junction this causes movement of minority charge carrier in collector region.

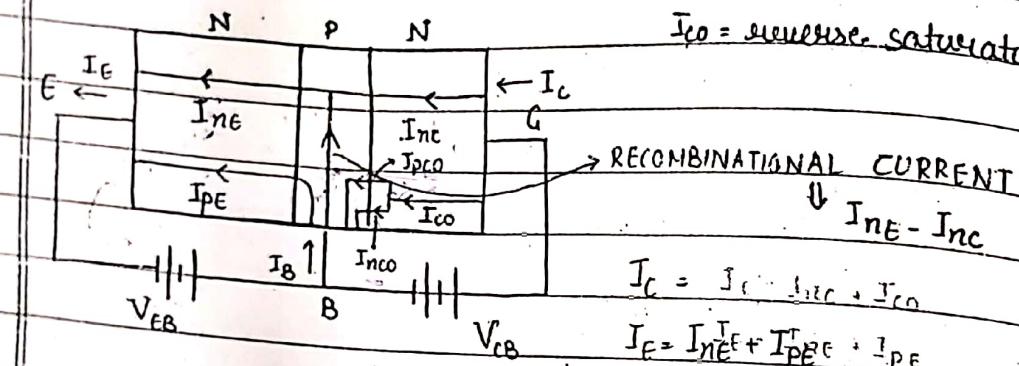
The minority holes from collector side move towards the base region similarly minority electrons of the base region moves towards the collector region and this movement of minority charge carrier shows the minority current. Therefore the large number (90%) of electron entering the base region reaches the collector region.

Page

current. Therefore the large number (90%) of electron entering the base region reaches the collector region.

WORKING PRINCIPLE OF PNP TRANSISTOR

CURRENT COMPOSITION OF BIPOLAR JUNCTION BIASED IN ACTIVE REGION



I_{CO} = reverse saturation current

RECOMBINATIONAL CURRENT

$$I_{RE} = I_{NE} - I_{NC}$$

$$I_C = I_{RE} + I_{RC}$$

$$I_F = I_{NE} + I_{PE} + I_{PC}$$

$$I_B = I_B = I_{NE} - I_{NC} + I_{PE} - I_{PC} - I_{CO}$$

The emitter current consist of hole current and electron current

I_{PE} = Current due to movement of holes from base to emitter

I_{NE} = Current due to movement of electron from emitter to base

$$I_E = I_{NE} + I_{PE}$$

EMITTER EFFICIENCY: Ratio of current injected from emitter to base to the total emitter current I_E (γ_0)

$$\gamma_0 = \frac{I_{NE}}{I_E} = \frac{I_{NE}}{I_{NE} + I_{PE}}$$

under this condition $I_{PE} \ll I_{NE}$ this is because emitter region is highly doped as compare to base region under this condition $\gamma_0 \approx 0.995$

$$I_B = I_{NE} - I_{NC} + I_{PE} - I_{PC} - I_{CO}$$

$$= I_{NE} + I_{PE} - I_{NC} - I_{PC} - I_{CO}$$

$$= I_E - I_{NC} - I_{CO} = I_E - (I_{NC} + I_{CO})$$

$$I_B = I_E - I_C$$

BASE TRANSPORTATION FACTOR

$$\beta_0 = \frac{I_{nc}}{I_{ne}}$$

INC

It is the ratio of injected carrier current reaching the collector junction to the injected carrier at emitter junction

Date _____
Page _____

at collector current consists of

I_{nc} = It is the component of collector current due to fraction of emitter current which reaches the collector. This current can also be written as αI_E

I_{co} = Reverse saturation current

$$I_{nc} \quad I_{pc0}$$

The current due to movement of minority electron from base to collector

This is due to the current due to movement of minority holes from collector to base

$$I_{co} = I_{nc} + I_{pc0} \dots (ii)$$

$$I_C = I_{nc} + I_{co} \dots (iii)$$

$$I_C = \alpha I_E + I_{nc} + I_{pc0} \dots (iv)$$

$$I_C = \alpha I_E + I_{co} \dots (v)$$

Relation between α and β

$$I_C = \alpha I_E + I_{co} \dots (iv)$$

$$I_C = \alpha (I_E + I_B) + I_{co}$$

$$I_C (1-\alpha) = \alpha I_B + I_{co}$$

$$I_C = \frac{\alpha}{(1-\alpha)} I_B + \frac{I_{co}}{(1-\alpha)}$$

$$\left[\frac{\alpha}{(1-\alpha)} = \beta \right]$$

$$I_C = \beta I_B + (1+\beta) I_{co} \dots (v)$$

$$I_{co} \ll I_C \text{ and } I_B$$

$$I_C = \beta I_B$$

β = D.C gain of the transistor

$$\beta = \frac{I_C}{I_B}$$

FORWARD CURRENT TRANSFER RATIO

$$\alpha_{dc} = \beta_0 \gamma_0 = \frac{I_{ne} \cdot I_{nc}}{I_E \cdot I_{ne}} = \frac{I_{nc}}{I_E} = \frac{I_C - I_{co}}{I_E}$$

$$I_{co} \ll I_C \text{ & } I_E$$

$$\alpha_{dc} = \frac{I_C}{I_E}$$

COLLECTOR EFFICIENCY

It is the ratio of current crossing the collector junction to the electron current arriving at base side of the junction.

denoted by β

Date _____
Page _____

$S = 1 - \text{mostly}$

→ Collector current is less than emitter current because

(i) part of the emitter current consist of holes (NPN) does not contribute to the collector current.

(ii) not all the electrons injected into the base successfully reaches the collector.

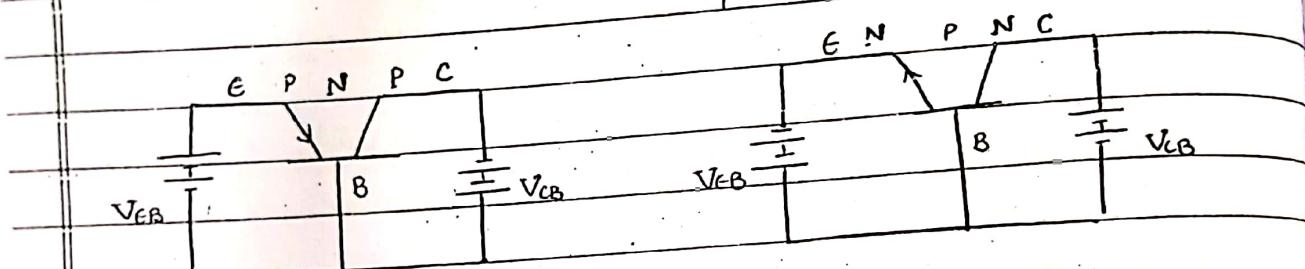
CONFIGURATION OF THE TRANSISTOR

1. Common base configuration

3. Common collector configuration

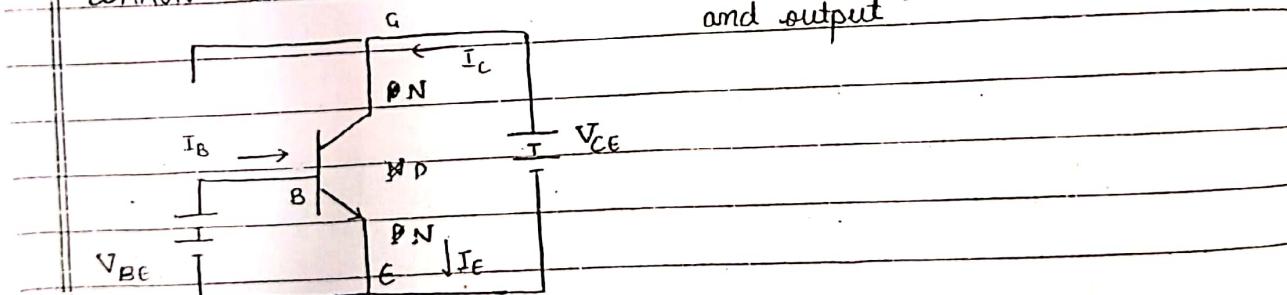
2. Common emitter configuration

COMMON BASE CONFIGURATION: Base is common in both input and output.



COMMON Emitter Configuration

Emitter is common in both input and output



INPUT CHARACTERISTIC FOR COMMON Emitter CONFIGURATION

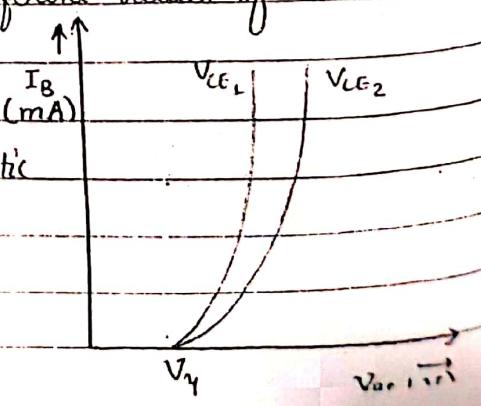
Curve plotted between I_B and V_{BE} for different values of V_{CE} is called input characteristic.

FEATURES

Input characteristic is forward characteristic of diode formed between emitter base junction with small effect of voltage V_{CE} .

However the base current is very small

If $V_{BE} = 0$ then $I_B = 0$



I_B start increasing when $V_{BE} > V_T$ (potential barrier)

OUTPUT CHARACTERISTIC FOR COMMON Emitter

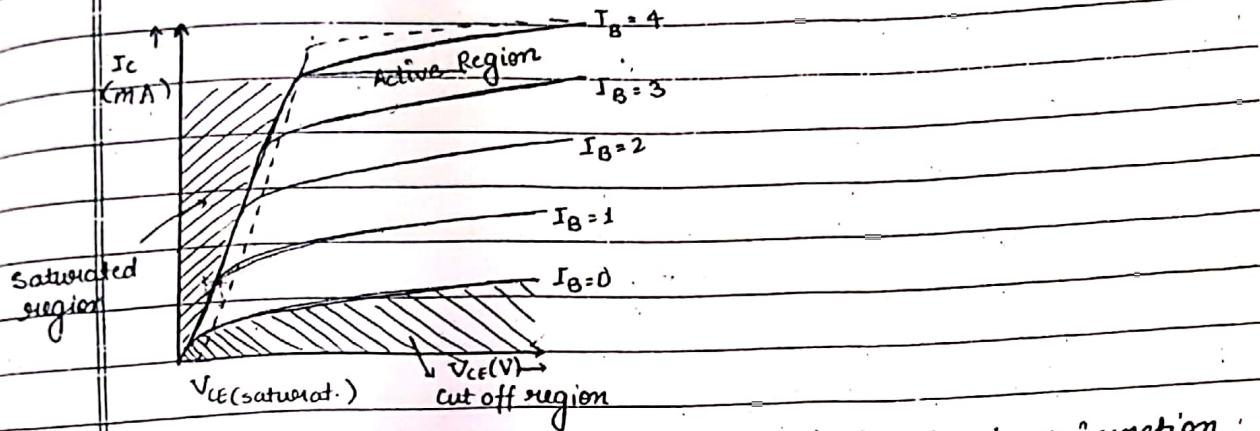
Curve plotted between I_C and V_{CE} for different values of I_B called the output characteristics

Date _____
Page _____

output characteristic is divided into three region depending on biasing.

1. Active region
2. Saturation region
3. cut-off region

OUTPUT CHARACTERISTIC FOR COMMON Emitter Configuration



→ Emitter base junction is reverse biased and collector base junction is forward biased for active region

The region above $I_B = 0$ and to the right of V_{CE} saturation is active region. In this region I_C increases slowly as V_{CE} increases

Reason: The slope of these characteristic curve greater than common base output characteristic curve.

REASON: In the common base configuration I_E is the input current and I_C is the output current.

$$V = I_C \quad I_C = \alpha I_E$$

$$I_E \quad I_C = 0.995 I_E$$

for common emitter configuration

I_B is the input current, I_C is the output current

$$\beta = \frac{I_C}{I_B} \quad I_C = \beta I_B$$

FEATURES OF ACTIVE REGION

For I_B constant I_C increases with V_{CE} it indicated that β increases with V_{CE} .

$$\beta = \frac{I_C}{I_E} \quad \text{small effect of } V_{CE}$$

In active region collector current I_C is β times greater than I_B that means small input current produces large change in the output current.

Date / /
Page

FEATURES OF CUT-OFF REGION

The region below $I_B = 0$ is cut-off region.

$$I_C = \beta I_B + (1+\beta) I_{CO} \dots (i)$$

when $I_B = 0$

$$I_C = (1+\beta) I_{CO} \dots (ii)$$

$$\alpha = 0.996$$

$$\beta = \frac{0.996}{1-0.996} = 249$$

$$I_C = (1+249) I_{CO}$$

$$I_C = 250 I_{CO}$$

I_{CO} = reverse saturation current

In cut-off region emitter base junction and collector base junction both are reverse biased.

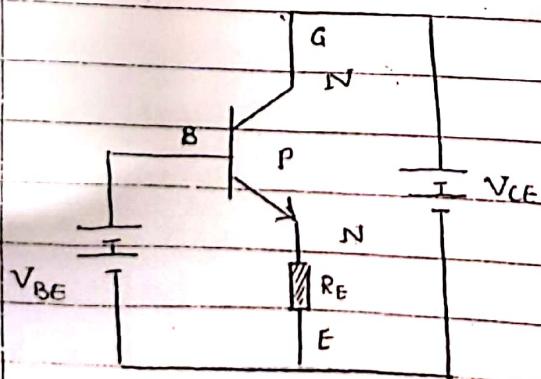
FEATURES OF SATURATED REGION

In this region collector base junction and emitter base junction both are forward biased.

For saturation region small change in V_{CE} produces large collector current as I_B increases the value of I_C increases until it equals I_C (saturation) and further increase in I_B will not produce any change in I_C .

COMMON COLLECTOR CONFIGURATION

Collector is common to both input and output



The common collector configuration has high input impedance and low output impedance. In the common collector configuration output is taken at emitter rather than collector.

Common emitter and common collector configuration is same but difference is explain above.

Also the load resistance R_L connected between collector and ground and emitter. Hence this

Date _____
Page _____

circuit is also called emitter follower.

Input current is I_B , output current is I_E .

The voltage across resistance R_E is considered as output voltage V_E therefore the output current $I_E = I_B(1+\beta) \dots (i)$ because I_{CO} is neglected.

$$I_C = \alpha I_E + I_{CO} \dots (i)$$

$$I_E = I_C + I_B$$

$$I_C = \alpha I_C + \alpha I_B + I_{CO}$$

$$(1-\alpha) I_C = \alpha I_B + I_{CO}$$

$$\cancel{I_C} =$$

$$I_E / I_B = \alpha I_E + I_{CO}$$

$$(1-\alpha) I_E = I_B + I_{CO}$$

$$I_E = \alpha I_E + I_{CO} + I_B \dots (ii)$$

$$(1-\alpha) I_E = I_{CO} + I_B$$

$$I_E = \frac{I_{CO}}{1-\alpha} + \frac{I_B}{1-\alpha}$$

$$I_E = (1+\beta) I_{CO} + (1+\beta) I_B$$

I_{CO} is neglected

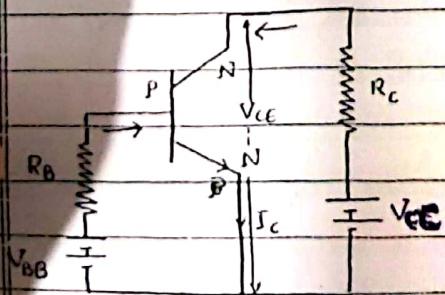
$$I_E = I_B (1+\beta)$$

$$\frac{I_E}{I_B} = 1+\beta$$

The reverse saturation current is as high as in common emitter configuration. Common collector configuration are useful in application where high input resistances are required.

DC LOAD LINE

SIGNIFICANCE: To find out the operating point that means current and voltage at which the transistor is working.



for output circuit

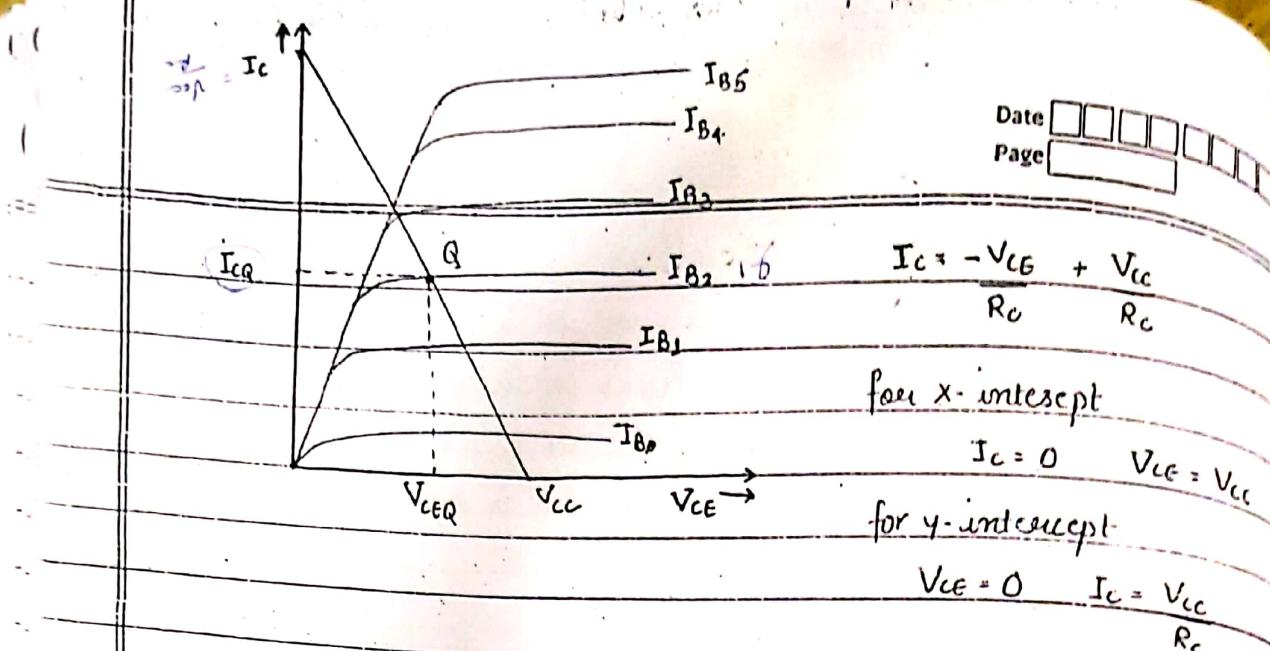
KVL equation

$$V_{CE} = I_C R_L + V_{BE} \dots (i)$$

$$V_{CE} - V_{BE} = I_C$$

R_C

$$I_C = -\frac{V_{CE}}{R_C} + \frac{V_{BE}}{R_C} \dots (ii)$$



for input circuit

$$V_{BB} = I_B R_B + V_{BE}$$

$$I_B = V_{BB} - V_{BE}$$

R_B

Qpoint = (V_{CEQ} , I_{CQ})

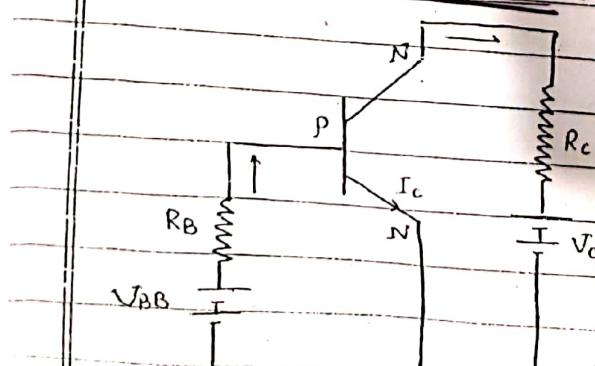
slope of the DC load line is $-1/R_C$ and it is decided by value of R_C .

→ R_C is the DC load of the amplifier therefore it is called DC load line.

Operating conditions of transistors are described by the value of V_{CE} and I_C . In addition to this the other factors are V_{CC} , R_C , R_B , V_{BB} and V_{BE} .

The operating point must lie on the DC load line. The exact operating point will lie at the intersection of DC load line and characteristic curve corresponding to I_B .

TRANSISTOR AS AN AMPLIFIER :-



The main function of the transistor is to amplify the electrical signal.

Common base configuration is also a amplifier but in this case gain is very less so it cannot amplify properly. So, the common emitter configuration is a better amplifier as current gain is more.

Que 24 Signal V_i is connected in input circuit for example load $R_L = 5k\Omega$ is connected in the output circuit then output voltage V_o is developed across R_L .

Date _____

Page _____

Input signal is 20mV. $R_L = 5k\Omega$, $R_i = 40V$, find output voltage

$$V_{cc} = 9V \quad \beta = 50$$

$$V_{cc} = 9V$$

for silicon $\times 10^{-3} = 0.7$ $V_{BB} = 20mV$
 $R_B = 40V$

$$I_B = \frac{20 \times 10^{-3} - 0.7}{40} = \frac{0.02 \times 0.7}{40} = \frac{2 \times 10^{-3}}{4} = 0.5 \times 10^{-3}$$

$$\beta = I_C$$

$$I_B$$

$$V_o = I_C R_L$$

$$= \beta I_B R_L$$

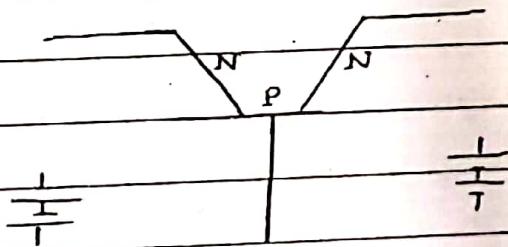
$$= 50 \times 5 \times 10^3 I_B$$

$$= 250 \times 10^3 \times 0.5 \times 10^{-3}$$

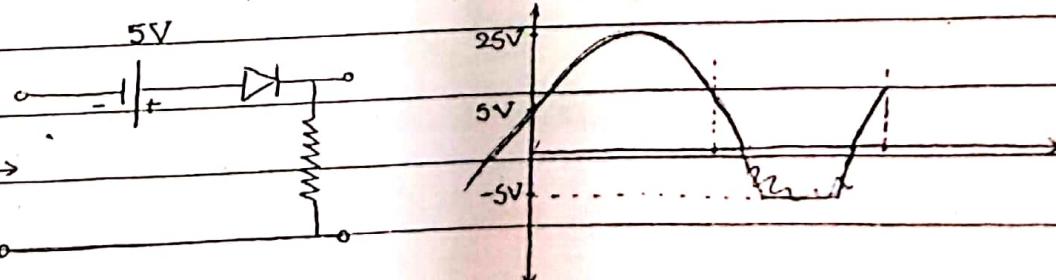
$$= 125 \text{ Volts}$$

In the common emitter circuit the R_B is used to limit the current

COMMON BASE as an amplifier.

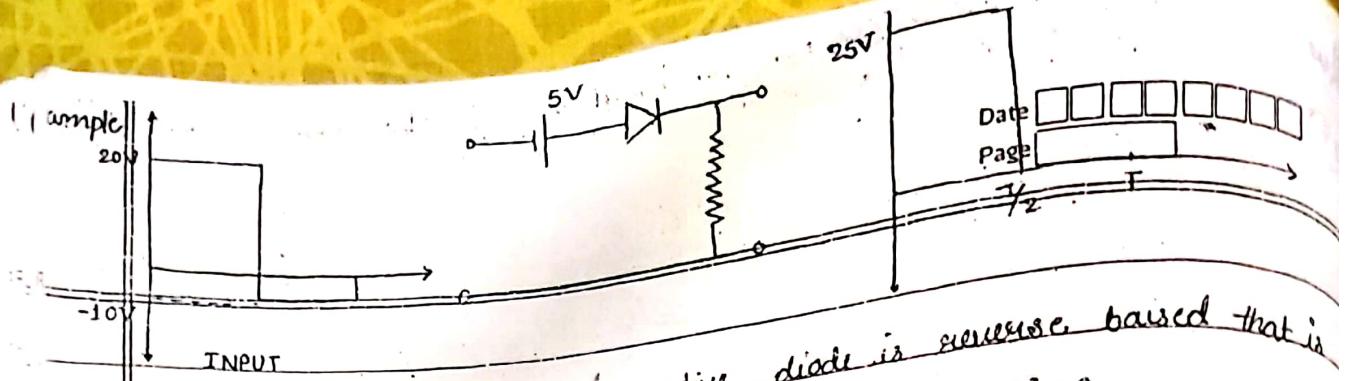


Que 25 Determine the output wave form for the network shown in figure.



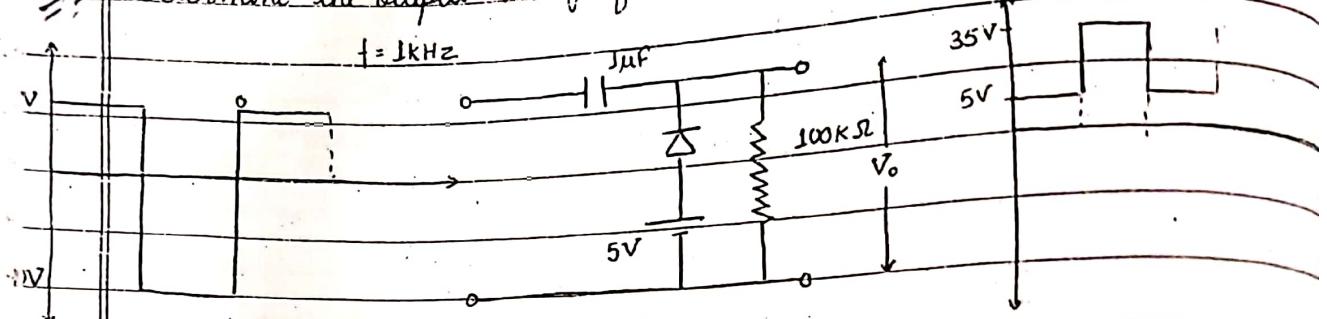
During positive half cycle diode is forward biased.

for input voltage (V_i) more negative than -5V the diode is open circuited while for the voltage more positive than -5V diode is short circuited or forward biased.



When input voltage is more negative, diode is reverse biased that is when $V_i = -10V$ diode is off where $V_o = 0$

Q26 Determine the output voltage for the network shown in figure.



During the negative half cycle, diode is forward biased that is short circuited.

$$-20 + 10 \neq 0 \quad -20 + V_c - 5V = 0$$

$$V_c = 25V$$

$$V_R = V_o = 5V$$

During positive half cycle

$$10 \sqrt{1/(2\pi f R C)} \quad V_o = V_i + V_c$$

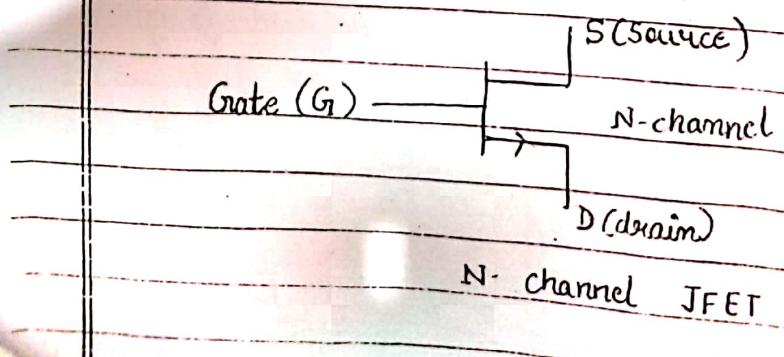
$$= 10 + 25 = 35V$$

$$\text{Time constant} = RC = 100 \times 10^3 \times 1 \times 10^{-6}$$

It is started from negative half cycle because diode conducts then only capacitor charges to 25V for positive half cycle diode is open circuited hence capacitor is not charging.

MOSFET:

Metal oxide semiconductor field effect transistor



It is unipolar design device in which conduction of current is by one type of charge carriers electron-hole.

1) N-channel 2) P-channel

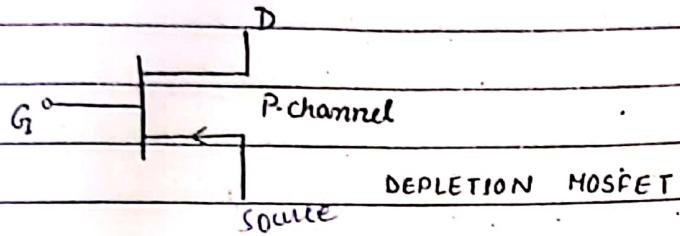
MOSFET is classified as

1) Depletion MOSFET

2) Enhancement MOSFET

N-channel P-channel

N-channel P-channel

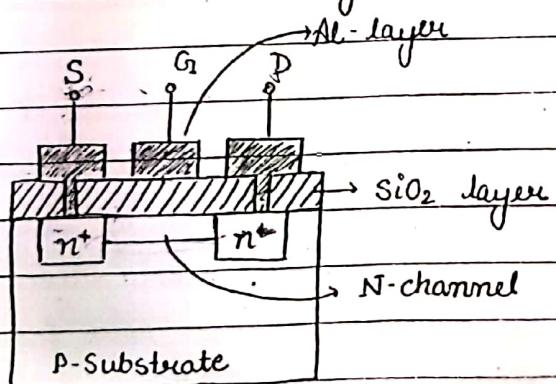


Construction of Depletion (N-channel) MOSFET

P-type semiconductor has been used as a base material on the P-substrate the two end

In between two regions there is a P-channel and between two heavily doped N-channel

a layer of silicon dioxide is placed over the surface. After this holes are cut into oxide layer to form the metal contact for the drainage and a source and layer of Al is place over the SiO_2 layer



P-type material has been used as base

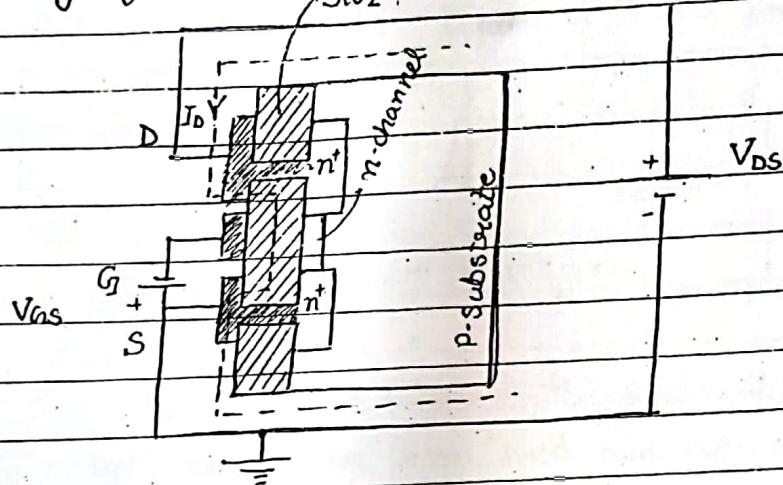
on lightly doped P-substrate two heavily doped n-regions are diffused separated by $25\mu\text{m}$ thickness and these 2 heavily doped region are drain and source. Then layer of insulating SiO_2 is then deposited over this surface. Holes

are cut into oxide layer through which the metal contacts drain and source are made. Conducting layer of Al is placed over the oxide layer which behaves as gate. There is N-channel between the two heavily doped n-region.

Date / /
Page

Gate and the N-channel forms parallel plate capacitor with SiO_2 as dielectric. The insulating layer of SiO_2 has very high input resistance of the order of (10^{10} to $10^{15} \Omega$)

Biasing of N-channel depletion (MOSFET)



For N-channel depletion MOSFET, drain is biased positive with respect to source and gate is biased negative with respect to source.

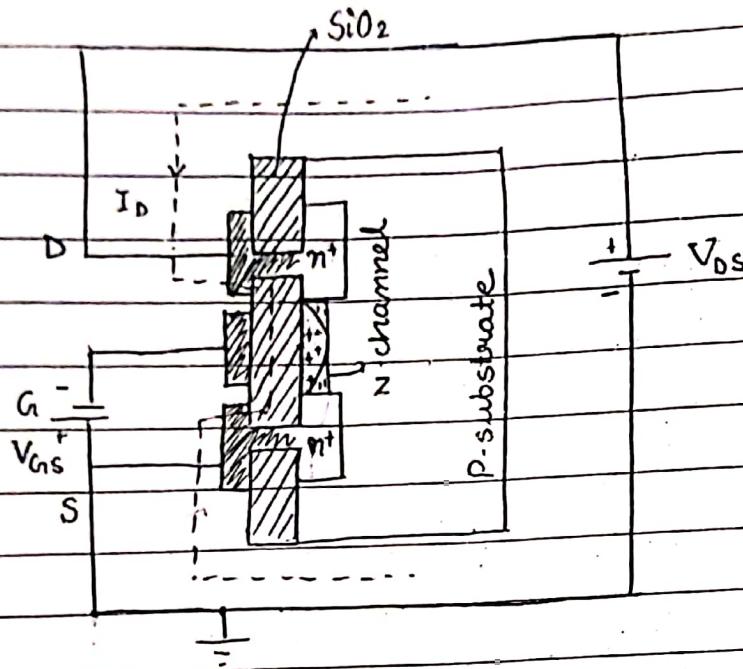
When $V_{GS} = 0$, application of the positive V_{DS} produces large drain current denoted by I_{DS} . Because of positive potential at the drain the electrons of the N-channel are attracted towards the drain. Current flow from drain to source through N-regions.

Because of the negative V_{GS} (when V_{GS} is -1V applied at the gate) positive charges are accumulated in the region in the N-channel because N-channel consists of large number of electrons and negative gate voltage repel these electron towards P-substrate. In addition to this holes from p-substrate are attracted towards N-channel. Hence the recombination of electron and holes takes place depending on magnitude of V_{GS} . Hence number of free electrons are reduced in the N-channel and due to this the current is small.

V_{GS} is more negative (-3V) than state of recombination is high and the drain current is smaller. The least negative value of V_{GS} for which the channel is depleted of majority charge carriers the current

Date _____
Page _____

$I_D \approx 0$ because channel is approximately eliminated.

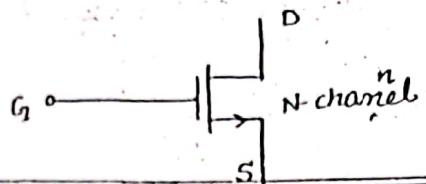


At constant V_{GS} increasing value of V_{DS} causes I_D to saturate as the channel is pinched off. Because of the voltage drop due to drain current. The channel region near the drain end is more as compared to source. This is because the potential drop is not same throughout the length of channel.

Depletion MOSFET can also be used in enhancement mode when positive gate voltage is applied negative charges are induced in the N-channel because minority electrons from P-substrate are attracted towards positive gate. Additional electrons are induced in the N-channel hence the current I_D increases and is greater than I_{oss} .

Enhancement MOSFET

For $V_{GS} = 0$ the current is zero and this current from drain to source is zero between the drain and source



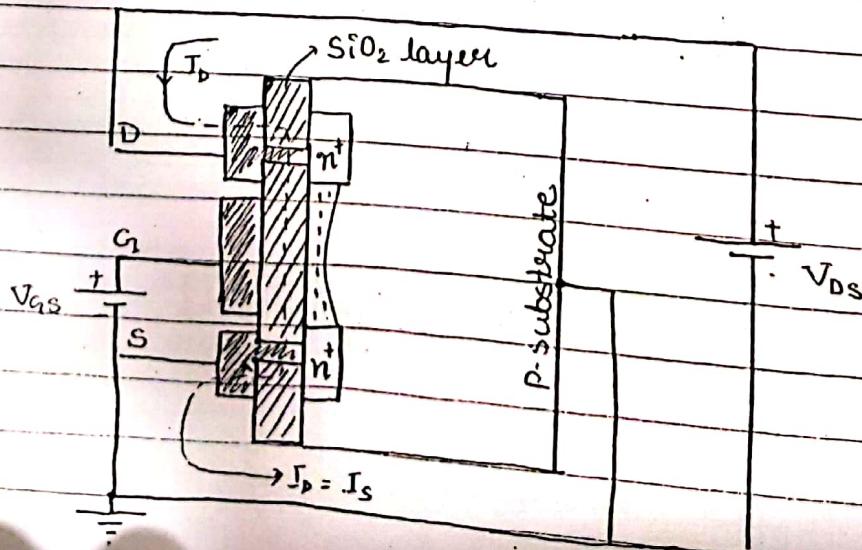
Date _____
Page _____

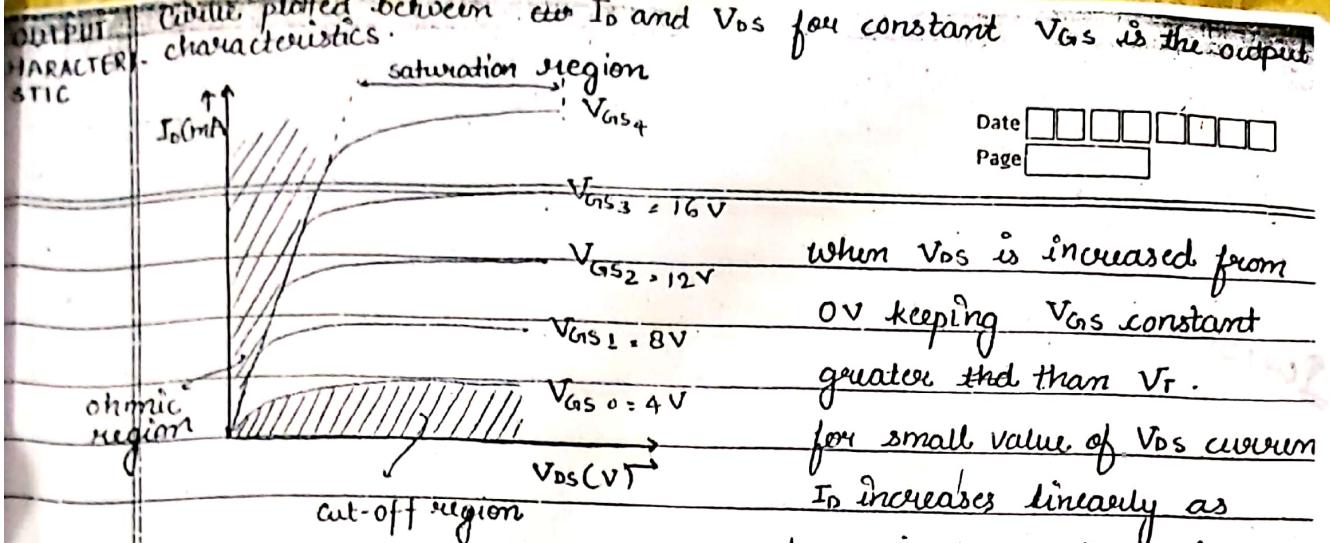
Construction for enhancement MOSFET is same as depletion MOSFET.

Principle operation for enhancement MOSFET
when both V_{GS} and V_{DS} are positive greater than zero volt that means drain and gate are biased positive with respect to source. Because of the positive potential at gate the holes are expelled into the p-substrate (base material). In addition to this electrons from p-substrate are attracted towards the positive gate. (that is minority electron) and accumulated in the region between drain and source. In this way the negative charge accumulated between drain and source and this layer of electron is called inversion layer. Because of inversion from p-type semiconductor to n-type semiconductor takes place this inversion layer is called n-channel.

The level of V_{GS} that gives significant increase in drain current is called threshold energy and denoted by V_T .

As the gate voltage increases beyond V_T number of induced negative charges increases in the n-channel and hence current I_D increases. Because positive V_{DS} is applied between drain and source it and hence current I_D flows from drain to source. The current I_D increases by increasing the gate voltage. Hence the device is called enhancement constant.



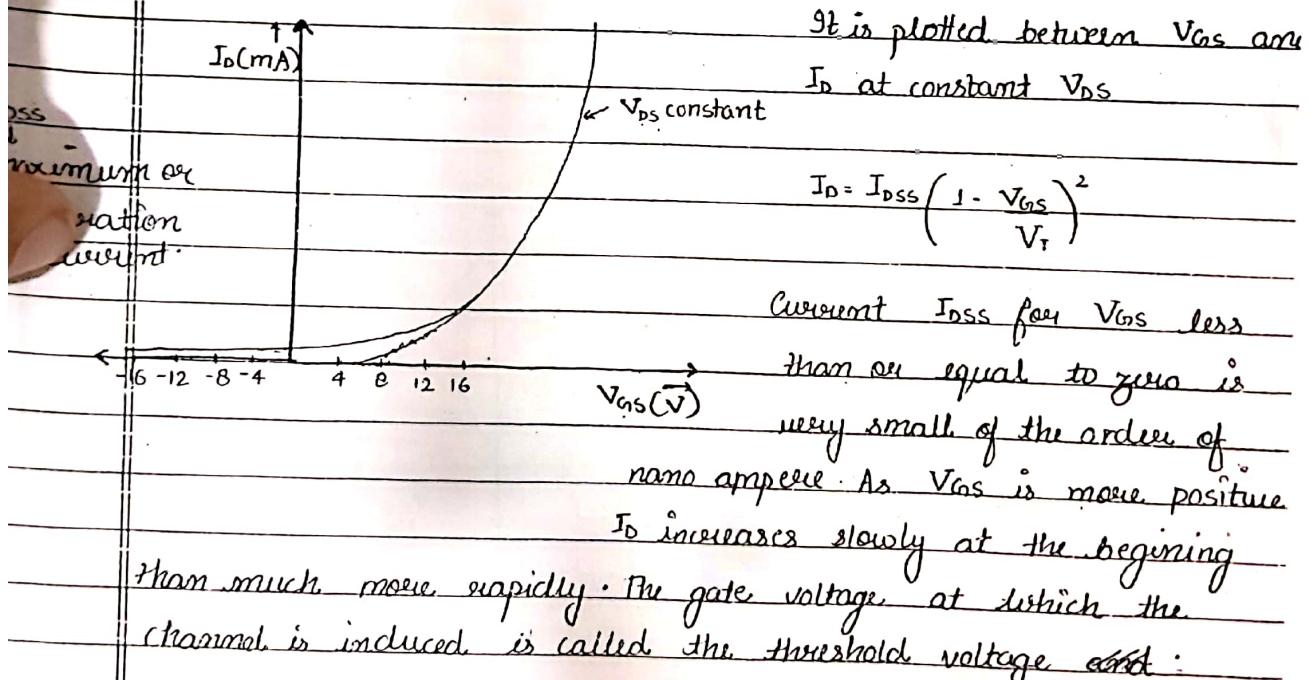


when V_{DS} is increased from 0V keeping V_{GS} constant greater than V_T . for small value of V_{DS} current I_D increases linearly as shown in figure (so this part is called ohmic region). for further increase in V_{DS} I_D will not change. I_D is almost constant and saturation current exist due to pinch off process depicted by narrow channel at the drain end of the induced channel.

$$V_{DG} = V_{DS} - V_{GS}$$

Below $V_{GS} = 4V$ this characteristic part is called cut-off region

TRANSFER CHARACTERISTIC OR INPUT CHARACTERISTIC



ADVANTAGES OF MOSFET

Since the gate is metallic and insulated from the channel hence the negligible current flows even when the gate voltage is positive and the input resistance of the MOSFET is very high of the order of $10000\text{ M}\Omega$ to $10000000\text{ M}\Omega$.

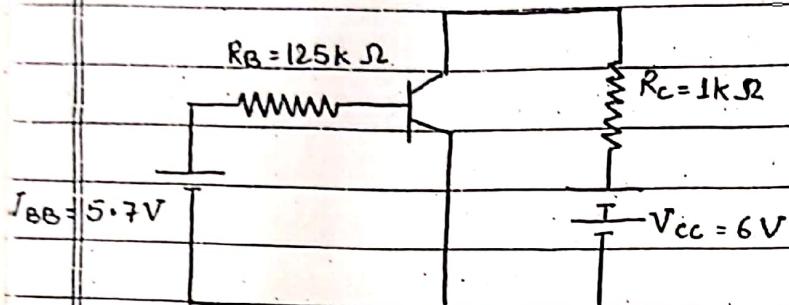
- because SiO_2 layer is dielectric
2. lower power consumption
 3. Small chip area to fabricate in the ~~big~~ ^{integrated circuit} form.

Date
Page

BIPOLAR JUNCTION TRANSISTOR

Ques 27

Find the Q-point and draw D.C load line for the following circuit shown in figure. $\beta = 60$ transistor is silicon



according to Kirchoff Voltage law

$$V_{cc} = V_{CE} + I_c R_c \dots (i)$$

for input circuit

$$V_{BR} = I_B R_B + V_{BE} \dots (ii)$$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5.7 - 0.7}{125 \times 10^{-3}}$$

$$= \frac{5}{125} \times 10^3 = 40\text{ }\mu\text{A}$$

$$= \frac{5 \times 1000}{125} = 40\text{ }\mu\text{A}$$

$$\beta = \frac{I_c}{I_B}$$

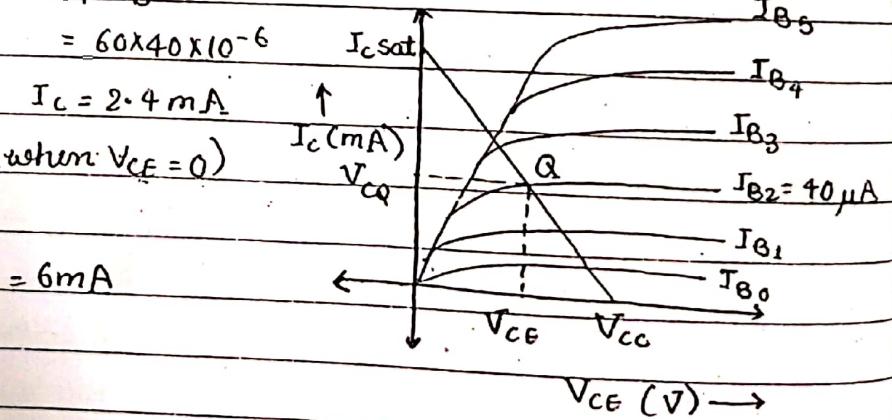
$$I_c = \beta \cdot I_B$$

$$= 60 \times 40 \times 10^{-6}$$

$$I_c = 2.4\text{ mA}$$

$$I_{c\max} = V_{cc} \quad (\text{when } V_{CE} = 0) \quad R_C$$

$$I_{c\text{ sat}} = \frac{6}{1} = 6\text{ mA}$$

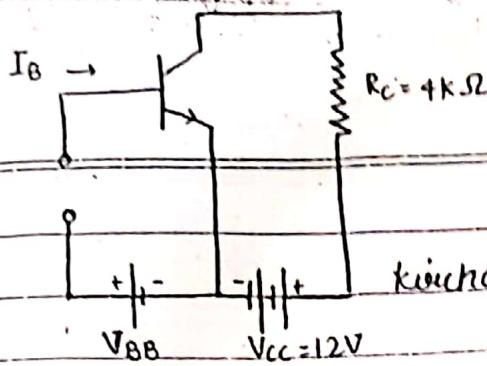


From equation (i)

$$\beta \cdot I_{cRc} = V_{CE} = 3.6\text{ V}$$

Ques 28

For the circuit shown in figure determine the D.C load line and determine the Q-point if the zero signal base current is $40\text{ }\mu\text{A}$ and $\beta = 50$ for Si transistor.



$$I_B = 40 \mu A$$

$$\beta = 50$$

$$I_C = \beta I_B$$

$$= 50 \times 40 = 2000 \mu A$$

$$= 2mA$$

Date _____
Page _____

Kirchhoff voltage law of output circuit

$$V_{CE} = V_{CB} + I_C R_C$$

$$I_{C\max} = \frac{V_{CC}}{R_C} \quad (V_{CE} = 0)$$

$$I_{C\text{sat}} = \frac{12}{4} = 8mA$$

$$I_C = 0$$

$$V_{CC} = V_{CE}$$

$$V_{CEQ} = 4V$$

Ques 29

The common emitter transistor circuit $V_{CC} = 12V$ and the zero signal collector current also called quiescent current = $1mA$. Determine the operating point when collector load is $6k\Omega$. What will be new Q-point if the load resistor is replaced by $4k\Omega$.

$4k\Omega$

$$V_{CE} = V_{CE} + I_C R_C$$

$$\text{when } R_C = 6k\Omega$$

$$V_{CEQ} = 6V$$

$$I_{CQ} = 1mA$$

$$\text{when } R_C = 4k\Omega$$

$$V_{CEQ} = 8V$$

$$I_{CQ} = 1mA$$

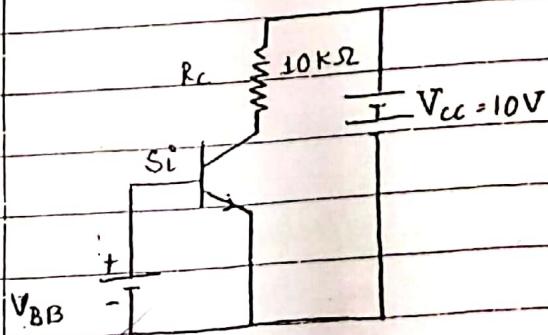
Ques 30

Find the Q-point of the circuit in given figure. Also draw the D.C. load line. find I_{CQ} and V_{CE} $\beta = 50$

$$I_C = 0.99mA$$

$$V_{CEQ} = 0.1V$$

$$I_{CQ} = 0.99mA$$



Q1) In a common emitter circuit collector supply is 12V ($V_{CC} = 12V$). The resistor $R_C = 2k\Omega$. The voltage drop across it is 2V and $\alpha = 0.98$. Determine V_{CE} , I_C and I_B

Date _____
Page _____

$$V_{CE} = 10V$$

$$I_C = 1mA$$

$$I_B = 41.67 \mu A$$

Q2)

In the common base configuration the emitter current $I_E = 1mA$. If the collector current is $30 \mu A$ then emitter circuit is. The total current when $\alpha = 0.98$ and also calculate the base current.

$$I = 9.8mA$$

$$I_B = 0.02mA$$

Q3)

The emitter current I_E in a transistor is $3mA$. If the leakage current $I_{CBO} = 5 \mu A$. If $\alpha = 0.98$. calculate collector and base current

$$I_B = 55 \mu A$$

$$I_C = 2.94mA$$

Q4)

In the common-emitter configuration the collector supply voltage $V_{CC} = 10V$ and $R_C = 1k\Omega$ is connected in the collector circuit. This voltage drop across it is $0.5V$, $\alpha = 0.98$. Determine V_{CE} and I_B .

$$V_{CE} = 9.5V$$

$$I_B = 10.2 \mu A$$

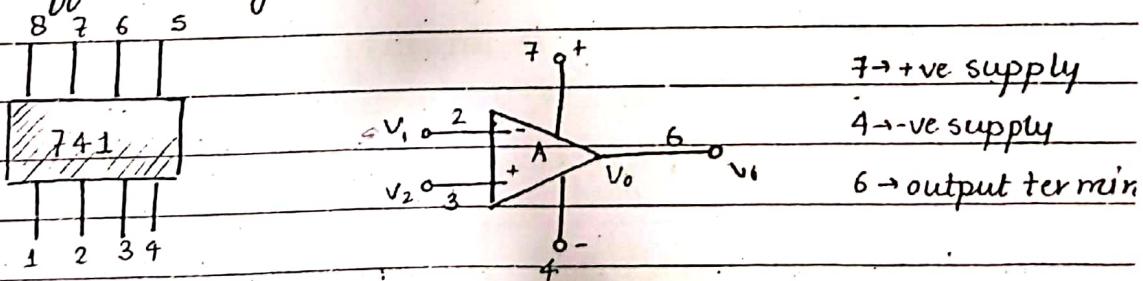
OPERATIONAL AMPLIFIER

It is high gain direct coupled differential voltage control voltage source device, to which feedback is added to control its overall frequency response.

It is used to perform wide varieties of operation linear and non-linear both. Example: multiplication, addition subtraction, division, integration, differentiation both.

ADVANTAGE

- 1. Small size
- 2. ~~low~~ cost
- 3. high reliability
- 4. Temperature tracking \rightarrow performance is not effected by temperature
- 5. low offset voltage and current.



If V_1 and V_2 are applied at inverting and non-inverting terminal

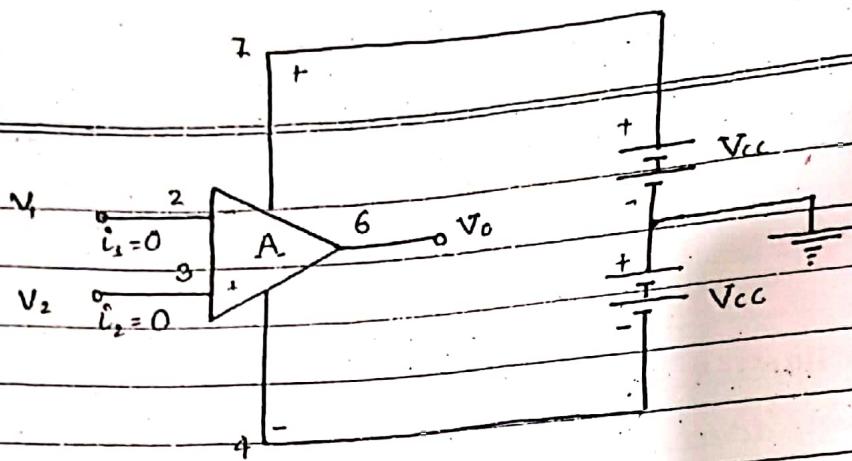
where $A = \text{open loop}$

where when there is no feedback ^{is} connected in the operational amplifier then it is called open loop opamp.

when there is feedback pass from input to output terminal it is called closed loop opamp.

output voltage of operational amplifier

$$\rightarrow V_o = A(V_2 - V_1) \dots (i)$$



It can be seen that there are two power supplies with the common ground. It should be noted that reference in ground point in open circuit is just the common terminal of the two power supply that is state there is no ground terminal in the operation amplifier chip.

CHARACTERISTIC OF DEVICE

IDEAL

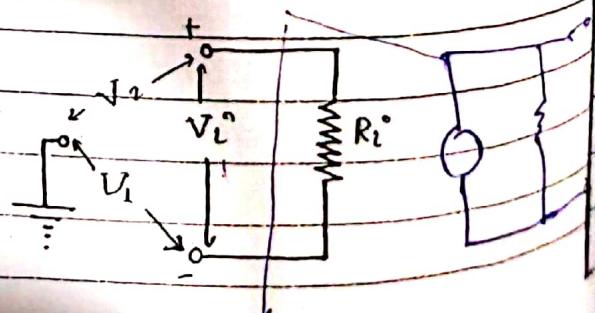
1. Input resistance of device is infinite $R_i \rightarrow \infty$
2. Output resistance of device is zero $R_o \rightarrow 0$
3. Open loop gain is infinite $A \rightarrow \infty$
4. Band width of a device is infinity $Bw \rightarrow \infty$
5. perfect balance that is $V_0 = 0$ when $V_1 = V_2$
6. Characteristic is not affected by the temperature

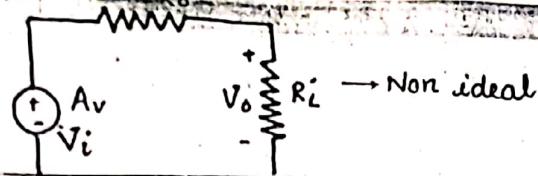
NON IDEAL OR PRACTICAL CHARACTERISTIC

1. $R_i \rightarrow \infty$ = ~~8MΩ~~ 2MΩ
2. $R_o \rightarrow$ = 75 Ω
3. $A \rightarrow 10^6$
4. $Bw \rightarrow 1\text{MHz}$

5. Perfect balance when $V_1 = V_2$ then there is some small voltage V_0 between is offset voltage.

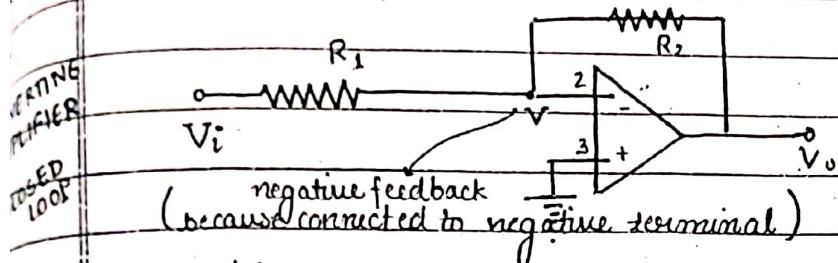
EQUIVALENT CIRCUIT





Date _____
Page _____

APPLICATION OF OPERATIONAL AMPLIFIER



node equation

$$V(G_1 + G_2) = G_1 V_o + G_2 V_i \dots (i)$$

↓ admittances

$$V(G_1 + G_2) = 0 \text{ because of virtual ground}$$

$$\frac{V_o}{V_i} = -\frac{G_2}{G_1} = -\frac{R_2}{R_1}$$

VIRTUAL SHORT

If $A \rightarrow \infty$ in equation (i)

$$\frac{V_o}{V_i} = (V_2 - V_1) \dots (ii)$$

now using (ii)

$$V_2 - V_1 = 0$$

$$V_1 = V_2$$

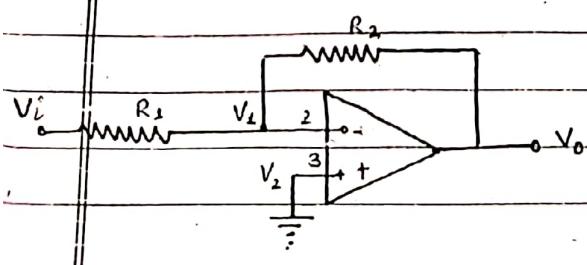
If one point is grounded

If one of the input terminal of the opamp is grounded then other terminal's voltage is also zero it is called virtual ground.

$A \rightarrow \infty$

If $V_3 = 0$ then $V_2 = 0$

INVERTING AMPLIFIER with (A is finite)



$$V_o = A(V_2 - V_1)$$

$$V_o = A(V_1) \dots (i)$$

$$V_1 (G_{r1} + G_{r2}) = G_{r1} V_i + G_{r2} V_o \dots (ii)$$

$$V_1 = \frac{G_{r1} V_i + G_{r2} V_o}{(G_{r1} + G_{r2})}$$

$$V_1 = -V_o (G_{r1} + G_{r2}) = G_{r1} V_i + G_{r2} V_o \dots (iii)$$

A

$$A G_{r2} V_o + V_o (G_{r1} + G_{r2}) = -G_{r1} V_i A$$

$$V_2 = \frac{R_2 V_i + R_1 V_o}{R_2 + R_1} = -V_o$$

$$A R_2 V_i + A R_1 V_o = -V_o (R_2 + R_1)$$

$$V_o (A R_1 + (R_2 + R_1)) = -A R_2 V_i$$

$$V_o = -A R_2$$

$$V_i = \frac{-A R_2}{A R_2 + R_2 + R_1}$$

V_o	$= -R_2 / R_1$
V_i	$\frac{1 + (1 + R_2 / R_1)}{A}$

$$\Rightarrow \boxed{V_o = -R_2 / R_1}$$

nodal equation

$$V_i (G_{r1} + R(G_{r2})) = G_{r1} V_2 + G_{r2} V_o$$

$$V_i (G_{r1} + G_{r2}) = G_{r2} V_o \dots (i)$$

$$V_i = G_{r2}$$

$$V_o = G_{r1} + G_{r2}$$

$$= \frac{1}{R_2}$$

$$(R_1 + R_2) / R_1 R_2$$

V_i	$= R_1$
V_o	$R_1 + R_2$

$$V_o = A(V_i - V_1)$$

$$V_o = V_i - V_1$$

$A \rightarrow \infty$

$$\frac{V_o}{A} \rightarrow 0$$

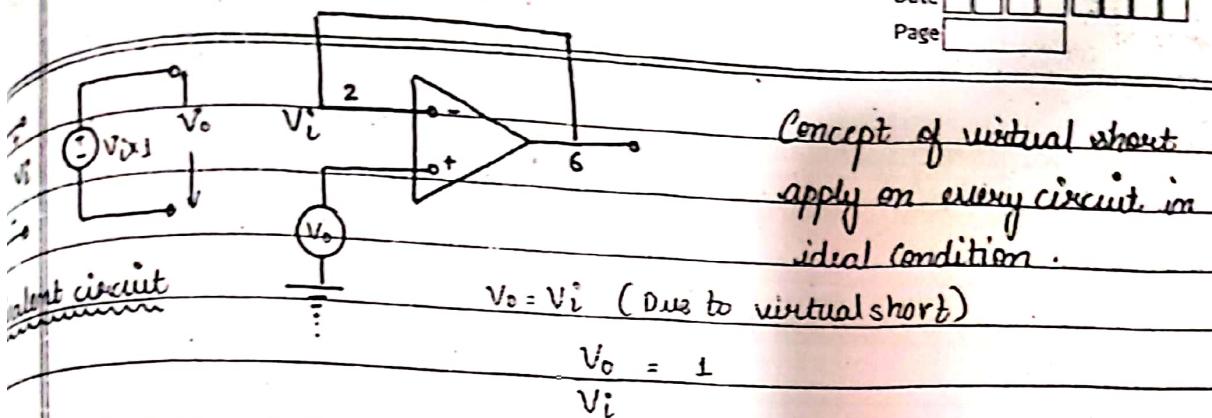
$$V_i = V_1 \dots (ii)$$

V_i	$= R_1$
V_o	$R_1 + R_2$

$$\frac{V_o}{V_i} = \frac{R_1 + R_2}{R_1} = 1 + \frac{R_2}{R_1}$$

UNITY GAIN AMPLIFIER (BUFFER)

Date _____
Page _____

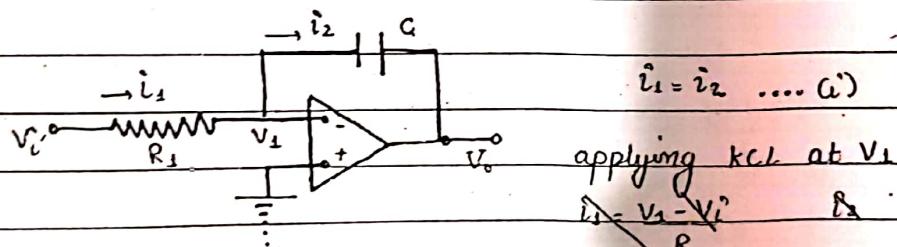


Concept of virtual short
apply on every circuit in
ideal condition.

If analyse non-inverting amplifier under non ideal condition (opamp)

The property of unity gain amplifier that it can be used as buffer to connect a source with high impedance to low impedance load.

INTEGRATOR



because of virtual ground

$$V_1 = 0 \quad \frac{V_i - V_1}{R} = -\frac{dV_o}{dt} \dots (ii)$$

$$-\frac{V_i}{RC} = \frac{dV_o}{dt}$$

$$V_o = - \int_0^t \frac{V_i}{RC} dt \quad V_o = - \frac{V_i t}{RC}$$

$$V_1(G_1 + X_C) = V_i G_1 + V_o X_C$$

$$V_1(G_1 + SC) = V_i G_1 + V_o SC$$

$$V_i G_1 = -V_o SC$$

$$\frac{V_o}{V_i} = \frac{1}{R, SC} \dots (iii)$$

The function of integration is to provide the output voltage which is proportional to integral of input voltage.

$$\left| \frac{V_o}{V_i} \right| = \frac{1}{\omega RC} \dots (iv)$$

phase of the integrator $\phi = 90^\circ$
for this $\omega = \frac{1}{RC}$ the gain magnitude is unity

this frequency is called the frequency of integrator where
 RC is the time constant of integrator.

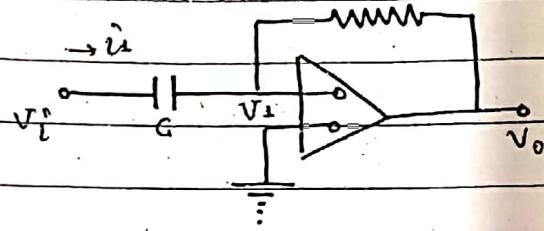
$$V_i = V_{\text{constant}}$$

$$V_o = - \frac{1}{RC} \int_0^t V_i dt$$

$$V_o = - \frac{Vt}{RC} \dots (v)$$

If input is constant then output voltage will be ramp function.

DIFFERENTIATOR



$$V_i (B_{11} + SC) = V_i SC + V_o G_{11} \dots (i)$$

$$V_i SC = - V_o G_{11}$$

$$\frac{V_o}{V_i} = - \frac{SC}{G_{11}} = - \frac{1}{\omega RC} = - SCR$$

$$i_1 = i_2 \dots$$

$$- C \frac{dV_i}{dt} = V_o - V_i \dots (ii)$$

$$V_o = - RC \frac{dV_i}{dt}$$

$$V_i = - \frac{V_o}{RC} \int dt \quad \text{# H/H}$$

EXAMPLE If $V_i = \sin \omega t$

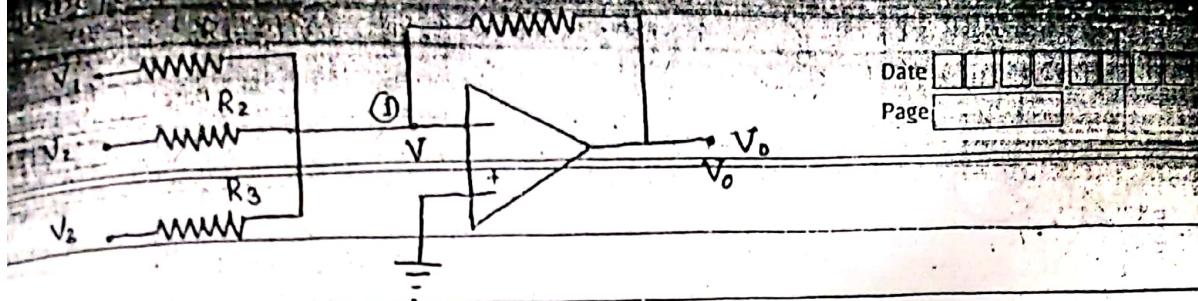
$$- CR \cos \omega t \cdot \omega = V_o \dots (iv)$$

equation (iv) shows that output voltage increases linearly with frequency and differentiator has high gain at high frequency. This result in the amplification of high frequency component of amplifier noise.

$$\left| \frac{V_o}{V_i} \right| = \omega RC$$

$$\omega_{\text{diff}} = \frac{1}{RC}$$

$$\Phi = -90^\circ$$



$$V(G_1 + G_2 + G_3 + G_4) = G_1 V_1 + G_2 V_2 + G_3 V_3 + G_4 V_0 \dots (i)$$

$$A \rightarrow \infty \quad V \rightarrow 0 \dots (ii)$$

$$V_0 = - \left(\frac{R_1 V_1}{R_1} + \frac{R_2 V_2}{R_2} + \frac{R_3 V_3}{R_3} \right) \dots (iii)$$

$$V_0 = - \frac{R}{R'} [V_1 + V_2 + V_3] \dots$$

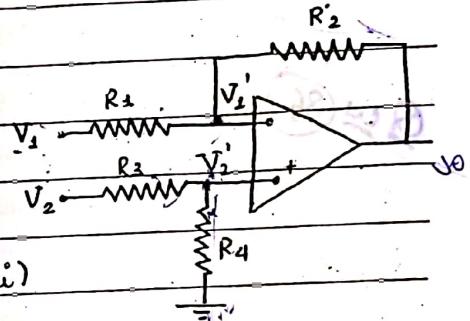
$$R_1 = R_2 = R_3 = R' \dots (iv)$$

Output voltage of adder circuit is equal to the algebraic sum of input voltage each multiplied by constant gain factor.

Difference amplifier/Subtractor

one of the application of amplifier:

$$V_1' (G_1 + G_2) = G_1 V_1 + G_2 V_0 \dots (i)$$



$$V_2' (G_3 + G_4) = G_3 V_2 + G_4 \times 0 \dots (ii)$$

under ideal condition

$$\text{due to mutual short} \quad V_1' = V_2' \quad \frac{V_1 - V_0}{R_1} = \frac{V_1 - V_0}{R_2}$$

$$V_1' = \frac{G_1 V_1 + G_2 V_0}{G_1 + G_2}$$

$$V_2' = \frac{G_3 V_2}{G_3 + G_4}$$

$$\frac{V_1 - V_1'}{R_1} = I = \frac{V_1 - V_0}{R_2}$$

$$\frac{V_1 G_1 + G_2 V_0}{(G_1 + G_2)} = \frac{G_3 V_2}{(G_3 + G_4)}$$

$$\frac{V_2 - V_2'}{R_3} = \frac{V_2' - 0}{R_4}$$

$$\frac{R_1 V_1 + R_2 V_0}{R_1 + R_2} = \frac{R_4 V_2}{R_3 + R_4}$$

$$\frac{V_2}{R_3} = \frac{V_2' + V_2}{R_3}$$

$$V_0 = \frac{(R_1 V_1 + R_2 V_0)(R_3 + R_4) - R_2 V_1}{(R_3 + R_4)}$$

$$\frac{V_2}{R_3} = \left(\frac{1}{R_3} + \frac{1}{R_4} \right) V_2'$$

$$V_0 = \frac{R_2}{R_1} \left[-V_1 + \frac{\left(\frac{1}{R_1} + \frac{1}{R_2} \right) V_2}{\left(\frac{1}{R_3} + \frac{1}{R_4} \right)} \right]$$

$$\frac{V_2}{R_3} \times \frac{1}{\frac{1}{R_3} + \frac{1}{R_4}} = V_2'$$

$$\frac{R_1}{R_2} = \frac{R_3}{R_4}$$

$$V_0 = \frac{R_2}{R_1} (V_2 - V_1)$$

$$\frac{R_2}{R_1} = A_d$$

$$V_0 = A_d (V_2 - V_1)$$

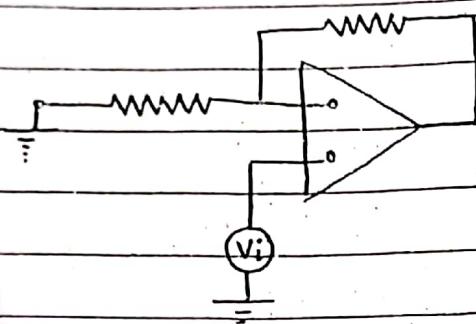
It can be seen from the output voltage, output, is difference of input V_1 and V_2 , multiplied by the factor A_d . (This is called differential gain)

Date _____
Page _____

-80

2.13

Design a non inverting amplifier with gain of 2 at the maximum output voltage of 10V. The current in the voltage divider is to be $10\mu A$



$$V_o = \frac{R_1 + R_2}{R_1} \cdot V_i$$

$$\frac{R_2}{R_1} = 1 \quad R_2 = R_1$$

$$R_1 = R_2 = 10k\Omega \quad (\text{selection})$$

$$i = \frac{V_o}{R_1 + R_2} = \frac{10}{10k\Omega} = 10\mu A$$

$$R_1 + R_2 = 1M\Omega \quad \frac{10 \times 10^6}{10} = 2R \quad R = 5 \times 10^5 \Omega \\ = 0.5M\Omega$$

180 (35)

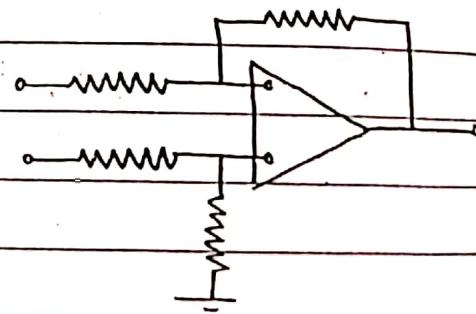
2.15 Consider the difference amplifier of the given circuit for the case

$$R_1 = R_3 = 2k\Omega \text{ and } R_2 = R_4 = 200k\Omega$$

(a) find the value of differential gain (A_d)

(b) output resistance (R_o)

$$A_d = \frac{R_2}{R_1} = \frac{200 \times 10^3}{2 \times 10^3} = 100$$



ideally $R_o = 0$

31

find the values for the resistances in the circuit of difference amplifier with input resistance of $20k\Omega$ and gain = 10

$$R_1 = R_3 = 10k\Omega$$

$$R_2 = R_4 = 100k\Omega$$

using ideal operational amplifier design inverting integrator
 with an input resistance of $10k\Omega$ and Date
 integrating time constant of 10^{-3} sec Page

(a) what is the gain magnitude and phase angle of the circuit at 10 rad/sec and at 1 rad/sec

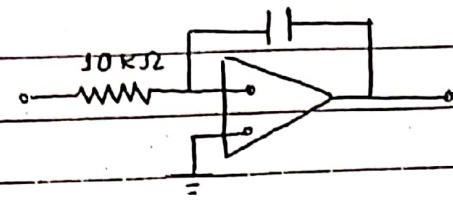
(b) what is the frequency at which the gain magnitude is unity.

$$R_i = R = 10k\Omega$$

$$RC = 10^{-3} \text{ sec}$$

$$C = \frac{1}{10 \times 10^3} = 0.1 \times 10^{-6} \text{ F}$$

$$= 0.1 \mu\text{F}$$



$$\left| \frac{V_o}{V_i} \right| = \frac{1}{\omega RC} = \frac{1}{10 \times 10^{-3}} = 100 \quad \phi = -90^\circ$$

$$\left| \frac{V_o}{V_i} \right| = \frac{1}{\omega RC} = \frac{1}{1 \times 10^{-3}} = 1000$$

$$\left| \frac{V_o}{V_i} \right| = \frac{1}{\omega RC} = \frac{1}{RC} \quad \omega = \frac{1}{RC} = 1000 \text{ rad/sec}$$

30
114

BASED ON DIFFERENTIATOR

Ex 2.2

Pg 123

Ex 2.8

Pg 124

Ex 2.11

Pg 125

Ex 2.12

Pg 125

Ex 2.13

Pg 125

Ex 2.14

Pg 125

Ex 2.20

Pg 125

Ex 2.23

Pg 126

Ex 2.29

Pg 126

2.36

Pg 128

2.38

Pg 128

2.44

Pg 129

Ex 2.14

Pg 129

Ex 2.20

Pg 131

Ex 2.23

Pg 131

2.60

Pg 131

2.61

Pg 131

2.(80, 81, 82, 85)

Pg 134

2.113

Pg 136

2.114

Pg 136

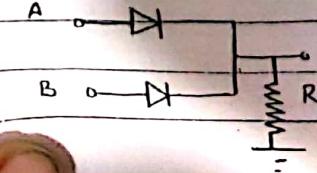
LOGIC GATES

OR GATE

$$Y = A + B$$



A	B	Y
1	0	1
0	1	1
0	0	0
1	1	1



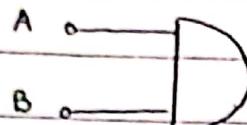
if all the inputs are zero diodes are off condition or open circuited then output is low if any of the input is high then corresponding diode

conducts and output is high
 Positive logic system is considered in which voltage values close to 0V correspond to the logic 0 and the voltage values close to +5V corresponds to logic 1 or high

Date _____
 Page _____

OR GATE

$$Y = A \cdot B$$



			+5V	A	B	Y
				0	0	0
				0	1	0
				1	0	0
				1	1	0

NOT GATE

$$Y = \bar{A} = \text{not } A$$



A	Y	V _O	R	+5V
0	1			
1	0			

Not gate is also called inverter it has one input and one output signal.

when switch S is closed (LOGIC 1) then output voltage is zero (LOGIC 0)

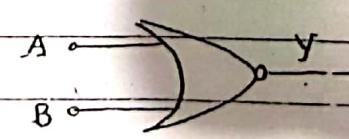
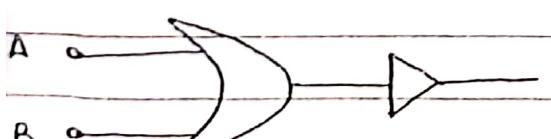
when switch S is open (LOGIC 0) then output voltage is equal to supply voltage +5V (LOGIC 1)

NOR GATE

NOR Gate is the combination of OR gate and NOT gate.

In this case the output is high (LOGIC 1) when all inputs must be low (LOGIC 0)

$$Y = \bar{A} + \bar{B}$$

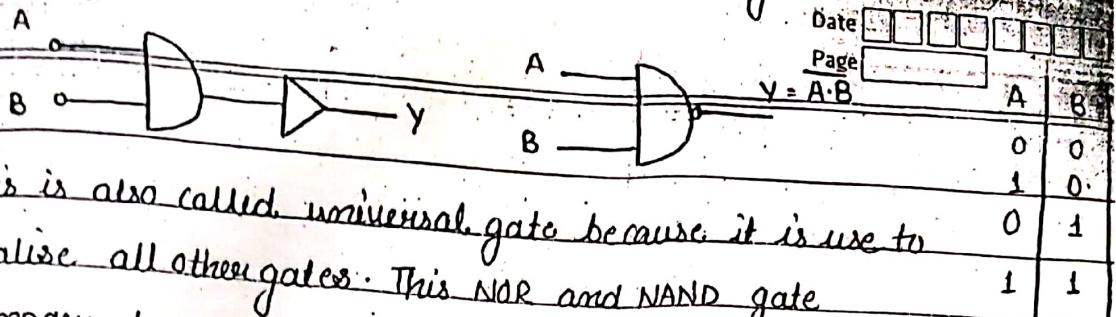


A	B	Y = $\bar{A} + \bar{B}$
0	0	1
0	1	0
1	0	0
1	1	0

NOR Gate is also called universal gate because it is use to realize the other gate.

It is the combination of AND gate and NOT gate.

$$Y = \overline{A \cdot B}$$



This is also called universal gate because it is used to realise all other gates. This NOR and NAND gate consume less power as compared to other gates.

ASSIGNMENT

Study of octal and hexadecimal numbers.

X → Addition and subtraction X

Problem based on difference amplifier

2.61, 2.80

Pg 131 Pg 134

Boolean Algebra Relations That means input can be changed in OR and AND gate

1. Commutative law

$$A+B = B+A \dots (i)$$

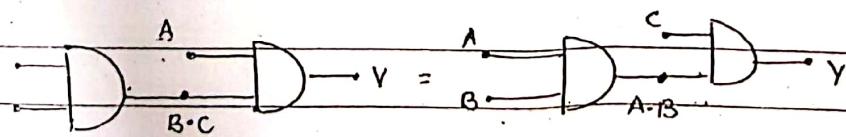
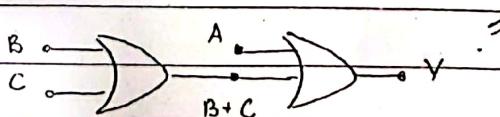
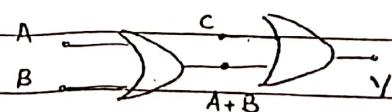


$$A \cdot B = B \cdot A \dots (ii)$$



2. Associative law

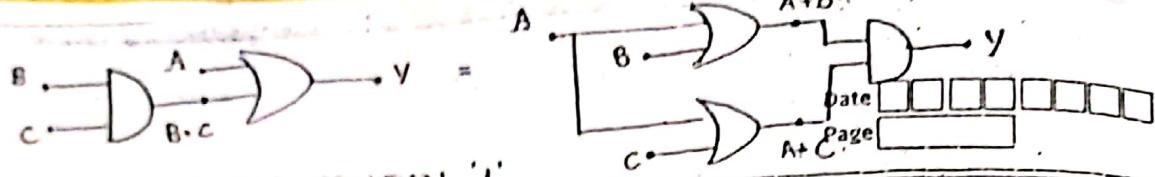
$$A + (B+C) = (A+B)+C$$



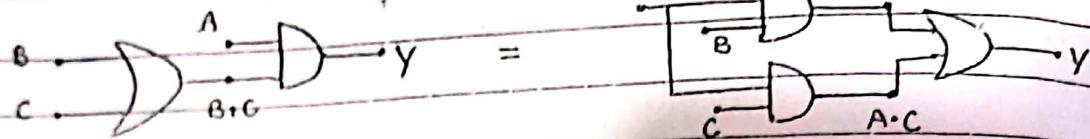
Distribution law

$$A + (B \cdot C) = (A+B) \cdot (A+C) \dots (i)$$

$$A \cdot (B+C) = A \cdot B + A \cdot C \dots (ii)$$



CIRCUIT FOR EQUATION '1'



CIRCUIT FOR EQUATION '2'

OR LAWS

In the study of OR Gate the following laws becomes self evident.

$$A + A = A \quad \dots \text{(i)}$$

$$A + 1 = 1 \quad \dots \text{(ii)}$$

$$A + 0 = A \quad \dots \text{(iii)}$$

$$A + \bar{A} = 1 \quad \dots \text{(iv)}$$

AND LAWS

$$A \cdot A = A$$

$$A = 0$$

$$A \cdot 1 = A$$

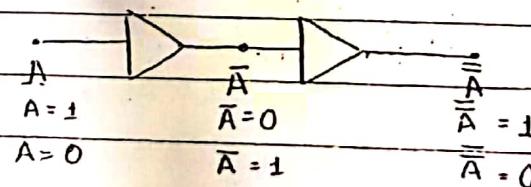
$$A = 1$$

$$A \cdot 0 = 0$$

$$A \cdot \bar{A} = 0$$

DOUBLE INVERSION

$$\bar{\bar{A}} = A$$



REDUNDANCY LAW

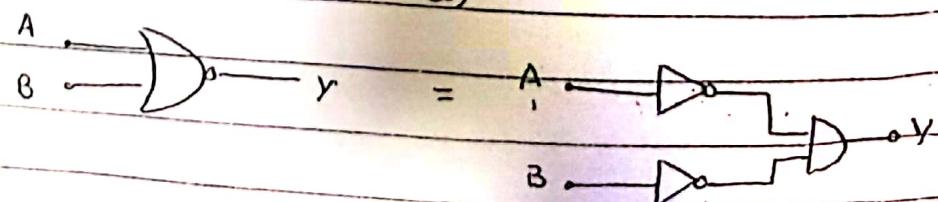
$$A + A \cdot B = A$$

$$A \cdot (A + B) = A$$

DE MORGAN'S THEOREM

FIRST THEOREM

$$\overline{A+B} = \bar{A} \cdot \bar{B} \quad \dots \text{(i)}$$

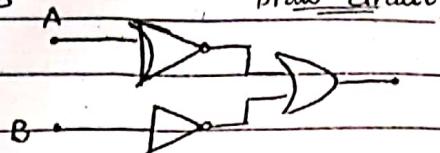
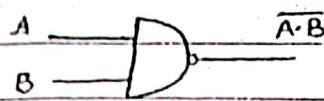


SECOND THEOREM

$$\overline{AB} = \overline{A} + \overline{B}$$

Date

Page



BINARY FRACTIONS

8568 2568 → decimal number

Two is the most significant digit and 8 is the least significant digit.

$$2568 = 2000 + 500 + 60 + 8$$

$$= 2 \times 10^3 + 5 \times 10^2 + 6 \times 10^1 + 8 \times 10^0$$

CONVERSION OF BINARY NUMBER TO DECIMAL NUMBER

1100101 → decimal

1. Start from least significant digit.

2. Apply the formula to calculate the weight of every bit

$$\text{FORMULA} = n^{\text{th}} \text{ bit} \times 2^{n-1}$$

3. Then calculate the weight of each bit and add.

Example: $1100101 = 1 \times 2^6 + 1 \times 2^5 + 0 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0$

$$\begin{aligned}
 &= 2^6 + 2^5 + 2^2 + 1 \\
 &= 64 + 32 + 4 + 1 \\
 &= (101)_{10}
 \end{aligned}$$

Example: $10110101 = 1 \times 2^7 + 0 \times 2^6 + 1 \times 2^5 + 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0$

$$\begin{aligned}
 &= 2^7 + 2^5 + 2^4 + 2^2 + 1 \\
 &= 128 + 32 + 16 + 4 + 1 \\
 &= (181)_{10}
 \end{aligned}$$

CONVERSION TO DECIMAL NUMBER TO BINARY NUMBER

27

2 | 27 → least significant digit

2 | 13 → 1

2 | 6 → 1

11011

2 | 3 → 0

2 | 1 → 1

0 | 1 → 1

Convert

METHODS :

1. To convert decimal number into binary number based on successive division of decimal number by 2.
2. The quotient and the remainders are noted regularly till the complete division process.
3. The remainders gives the binary number by a given procedure of positioning.

The first remainder is always least significant bit.

The last remainder is most significant bit.

Example:

2 | 25

2	12	→ 1	11001
2	6	→ 0	
2	3	→ 0	
2	1	→ 1	
0		→ 1	

2 | 45

2	22	→ 1	
2	11	→ 0	
2	5	→ 1	101101
2	2	→ 1	
2	1	→ 0	
0		→ 1	

Give the logic implementation of the expression

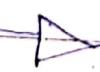
(i) $y = \bar{A} \cdot BC + A \cdot B \cdot C + \bar{A} \cdot \bar{B} \bar{C}$

(ii) $y = A(A+B)(C+D)(E+F)$

(iii) $y = AB + A\bar{B}$

Draw the logic circuit to implement Boolean expression

$$y = AB + AC + BD + CD$$



A ⊕

$$\begin{array}{l} \text{---} \\ \text{---} \end{array} \quad (A+B) \quad (A+B) \\ \text{---} \quad \text{---} \\ (A+\bar{A}B) \quad (A+B)$$