Unit-2 (Part-2)

Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

TOPICS COVERED

- INTRODUCTION TO MOSFET
- ENHANCEMENT MOSFET,
  - CONSTRUCTION
  - OPERATION AND CHARACTERISTICS
  - CURRENT EQUATION

Introduction

The metal-oxide semiconductor field-effect transistor (MOSFET) is another three-terminal semiconductor device that is used in a variety of applications similar to the BJT. Due to its unique features and areas of application, the MOSFET has become by far the most widely used electronic device, especially in the design of integrated circuits (ICs), which are entire circuits fabricated on a single silicon chip. Compared to BJTs, MOSFETs require very small area on the silicon IC chip, simpler manufacturing process and also requires comparatively little power. Furthermore, it has also been possible to implement digital and analog functions utilizing MOSFETs with essentially no (or very low) diodes or resistors required. These unique properties have led to the revolution of the semiconductor industry.

Classification of MOSFETs

Depending upon the type of materials used in the construction, and the type of operation, the MOSFETs are classified as in the following figure.

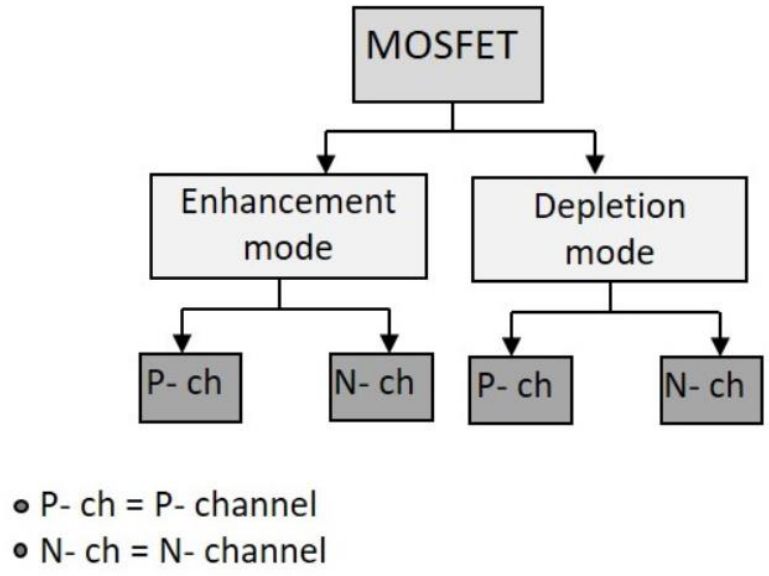


Fig.1 Classification of MOSFET

Enhancement-type MOSFET

The enhancement-type MOSFET is the most widely used field-effect transistor. In this section we learn about its structure and physical operation by considering n-channel enhancement MOSFET, also known as NMOS.

Construction

Figure 2, shows the physical construction of the *n*-channel enhancement-type MOSFET. The transistor is fabricated on a *p*-type substrate, known as **body.** Two heavily doped *n*-type regions, indicated in the figure as the *n*+ **source** and the *n*+ **drain** regions, are diffused in the substrate. A thin SiO_2 layer (that works as insulator) is grown on the surface of the substrate, covering the area between the source and drain regions. Metal is deposited on top of the oxide layer to form the **gate electrode** of the device. Similar metal contacts are also made to the source region, the drain region, and the substrate. The four terminals of the MOSFET are: the gate **(G)**, the source **(S)**, the drain **(D),** and the substrate or body **(SS/B).**

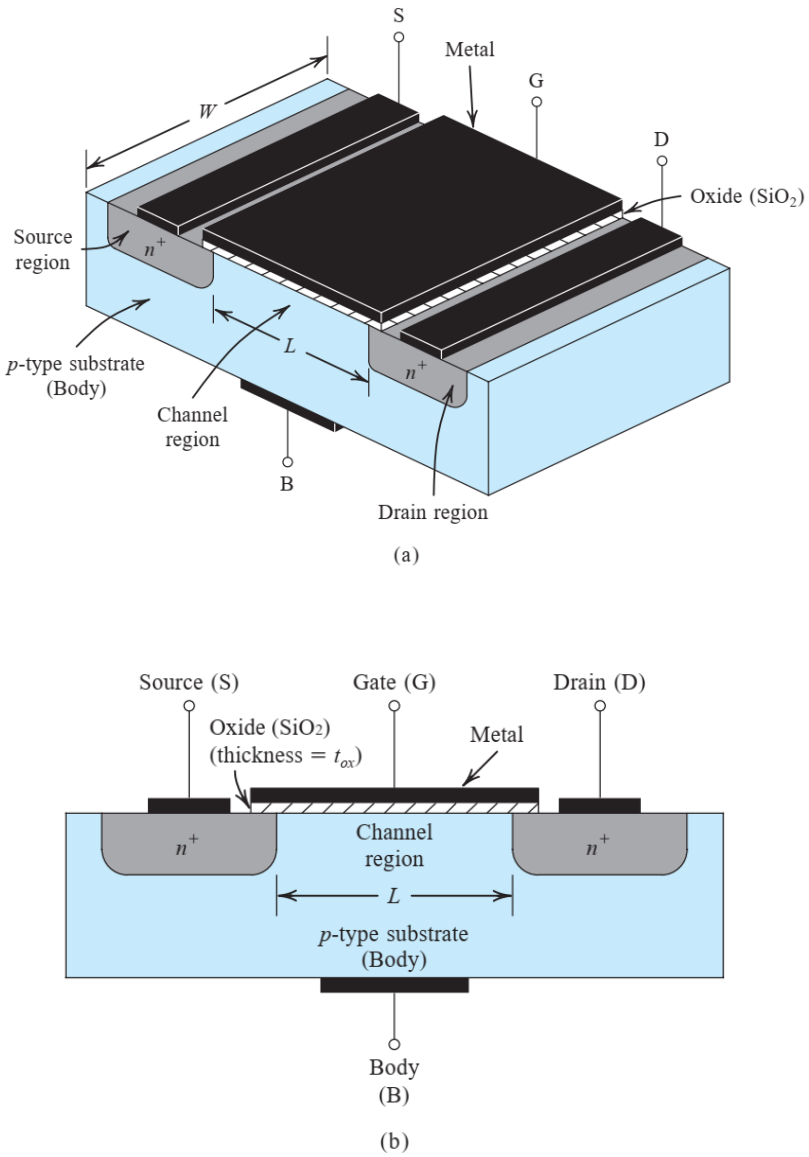


Fig.2 (a) Structure of n-Channel Enhancement MOSFET, (b) side view

The region between source and drain is known as **channel** region. However, in enhancement type MOSFET there is no physically constructed channel. There are some phenomena due to which the channel is created during the device's operation, as discussed shortly. Since the gate electrode is electrically insulated from the body (by the oxide layer), MOSFET is also known as **insulated-gate FET** or **IGFET**.

Device Operation

The basic operation of the *n*-channel enhancement-type MOSFET can be explained by the help of Fig. 3, in which the device is rotated vertically to keep drain on upper side. The source and body are connected to ground. The V_{GS} and V_{DS} denotes the voltage applied at gate and drain terminal with reference to source (or body).

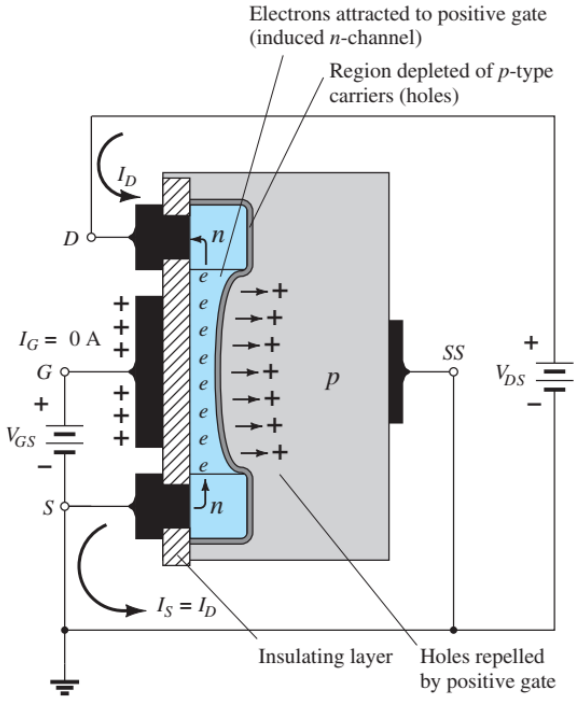


Fig. 3 Creating a channel for current flow. A positive voltage is applied to the gate with drain, source and body at ground

The MOSFET operation can also be understood by the help of a Water-tap analogy. The water tank can be understood as the drain terminal, the vessel which collects water is analogous to the source terminal. The flow of water is analogous to the flow of current from drain to source. The "gate," through an applied signal (potential), controls the flow of water (current) from "drain" to the "source."

- With V_{GS} =0 V and positive V_{DS} there is absence of a channel (with its generous number of free carriers) which result in a no drain current.
  This is analogous to the situation, when tap is closed (V_{GS}=0). No matter how much is the water in the drain, no water will come into the source.

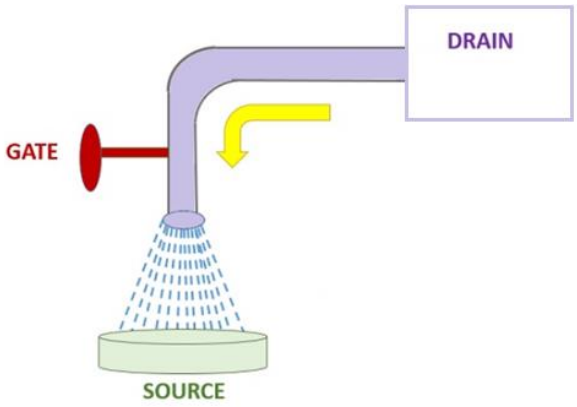


Fig.4 Understanding MOSFET through water analogy

- **Both V_{DS} and V_{GS} have been set at some positive voltage greater than 0 V**
  The positive voltage on the gate (i) repels the free holes from the region of the substrate near the gate (the channel region), these holes are pushed to deeper into the substrate, leaving behind a carrier-depletion region, and (ii) attracts electrons from the *n*+ source and drain regions (where they are in abundance) into the channel region. When a sufficient number of electrons accumulate in the channel region, an *n* region is in effect created, connecting the source and drain regions.
  - The channel is created by *inverting* the substrate surface from *p*-type to *n*-type. Hence the induced channel is also called an **inversion layer.**
  - The value of V_{GS} at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the **threshold voltage** and is denoted by V_{th}.
  - As V_{GS} is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. (Since, increasing above the threshold voltage enhances the channel, hence the names **enhancement-mode operation** and **enhancement-type MOSFET**.)

    This is analogous to the situation, when there is water in tank (positive V_{DS}) and we start opening the tap ($V_{GS} \geq V_{th}$) then water will come out and flow of water will increase if we open the tap by larger extent.

- **V_{GS} is fixed at a voltage above V_{th} and V_{DS} is further increased**

  If we fix V_{GS} constant at a voltage above V_{th} and increase the level of V_{DS}, V_{GS} will become less and less positive with respect to the V_{DS}. This leads to reduction in gate-to-drain voltage (V_{GD}) and will in turn reduce the attractive forces responsible for attracting the electrons from drain to the channel region. This will cause a reduction in the effective channel width. As V_{DS} is increased, the channel becomes more tapered and eventually, the channel will be reduced to the point of pinch-off. The MOSFET is then said to have entered the **saturation region.** The drain current ideally saturates and becomes independent of V_{DS}.

  - The voltage V_{DS} at which saturation occurs is denoted by V_{DSsat}

$$V_{DSsat} = V_{GS} - V_{th}$$

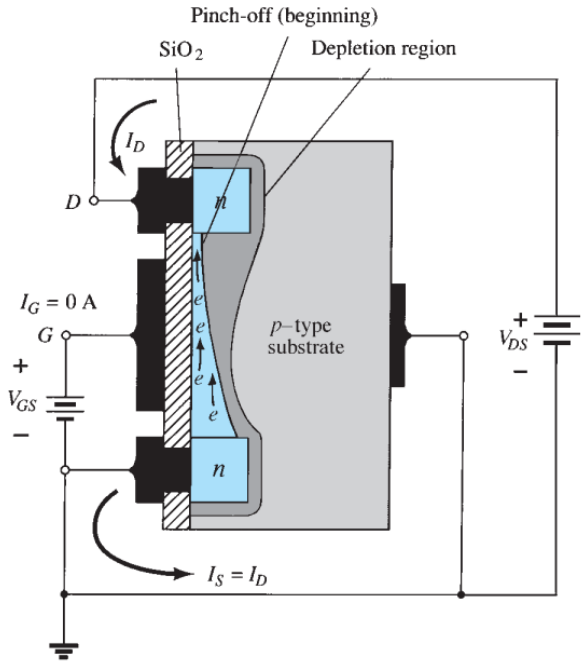


Fig. 4 Operation of the enhancement NMOS transistor as V_{DS} is increased. The induced channel acquires a tapered shape.

The term '$V_{GS} - V_{th}$' is also known as overdrive voltage V_{OV}.

P-channel enhancement MOSFET:

The structure is similar to that of the NMOS device except that here the substrate is *n* type and the source and the drain regions are p^+ type.

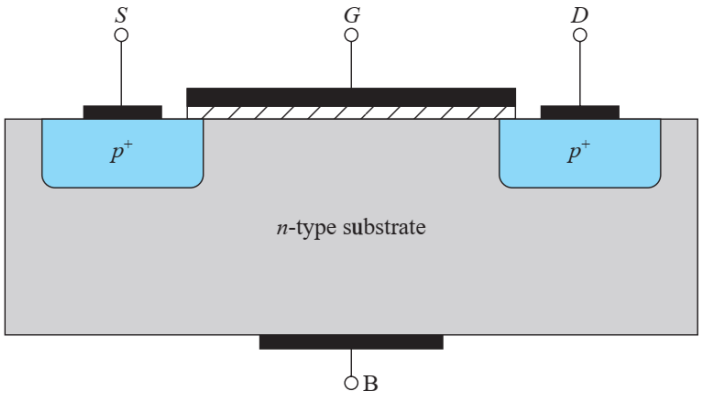
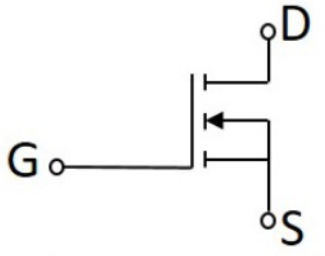
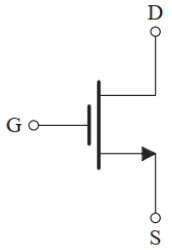


Fig. 5 Device structure of p-channel enhancement MOSFET

Device Symbol

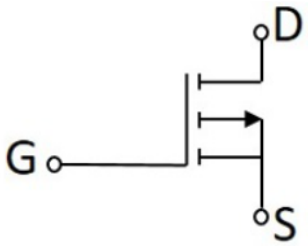
- N-channel enhancement MOSFET (NMOS)

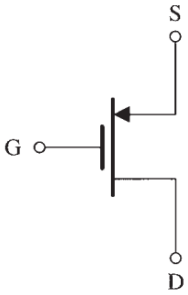




(Simplified, B and S are connected)

- P-channel enhancement MOSFET (PMOS)





(Simplified, B and S are connected)

Region of Operation and Characteristics

There are three regions of operation:

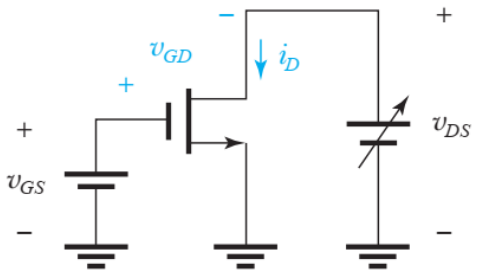
i. Cut-off: $\mathbf{V_{GS} < V_{th}}$, no channel is created, the drain current (i_D) is zero
ii. Triode region: $\mathbf{V_{GS} \geq V_{th}}$, Channel is induced**,** i_D starts flowing, varies almost linearly with V_{DS} till $V_{DSsat.}$
iii. Saturation region: $\mathbf{V_{GS} \geq V_{th}}$ and $\mathbf{V_{DS} \geq V_{DSsat}}$, i_D saturates.

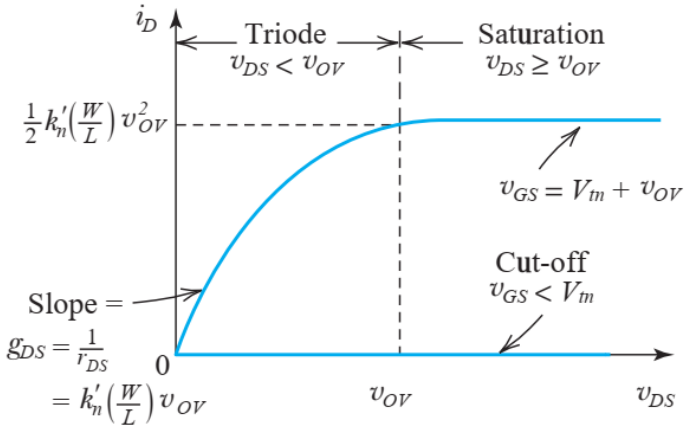
The conditions and current equations in various regions of operation for the Enhancement NMOS Transistor is summarised below. V_{tn} denotes the threshold voltage (V_{th}) of NMOS transistor. K_n' is the process transconductance parameter of NMOS.

$$k'_n = \mu_n C_{ox} \qquad \text{(In amperes per volt squared (A/V2))}$$

Summary Chart for n-channel enhancement MOSFET:

$(V_{OV} = V_{GS} - V_{th})$





- $v_{GS} < V_{tn}$: no channel; transistor in cut-off; $i_D = 0$
- $v_{GS} = V_{tn} + v_{OV}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched-off at the drain end;

Triode Region

Continuous channel, obtained by:

$$v_{GD} > V_{tn}$$

or equivalently:

$$v_{DS} < v_{OV}$$

Then,

$$\boxed{i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right]}$$

or equivalently,

$$i_D = k_n'\left(\frac{W}{L}\right)\left(v_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{GD} \leq V_{tn}$$

or equivalently:

$$v_{DS} \geq v_{OV}$$

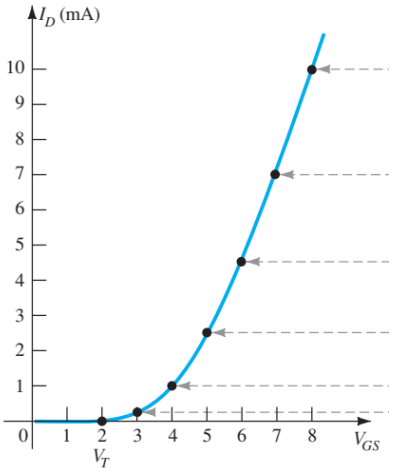
Then

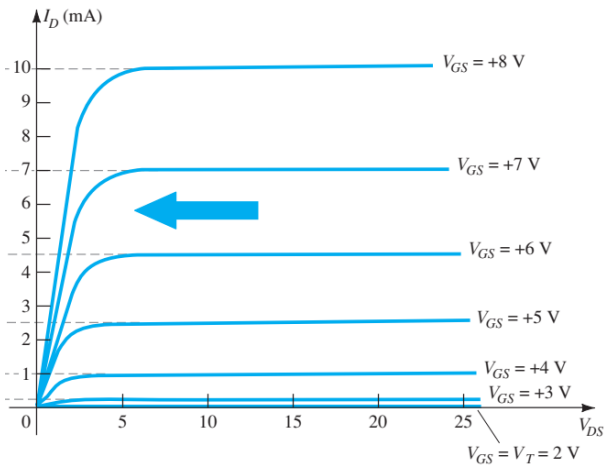
$$\boxed{i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2}$$

or equivalently,

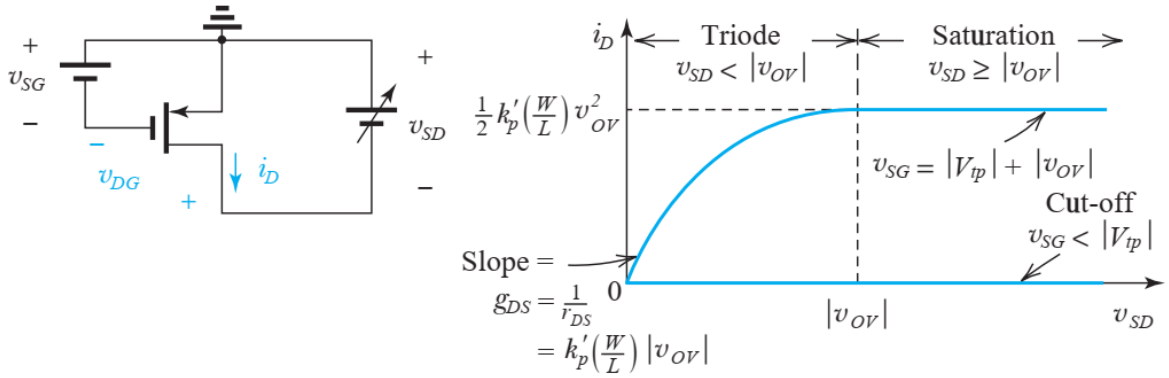
$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$$

i_D-V_{GS} and i_D-V_{DS} curve for NMOS





Summary Chart for P-channel enhancement MOSFET:



- $v_{SG} < |V_{tp}|$: no channel; transistor in cut-off; $i_D = 0$
- $v_{SG} = |V_{tp}| + |v_{OV}|$: a channel is induced; transistor operates in the triode region or in the saturation region depending on whether the channel is continuous or pinched-off at the drain end;

Triode Region

Continuous channel, obtained by:

$$v_{DG} > |V_{tp}|$$

or equivalently:

$$v_{SD} < |v_{OV}|$$

Then,

$$i_D = k_p'\left(\frac{W}{L}\right)\left[(v_{SG} - |V_{tp}|)v_{SD} - \frac{1}{2}v_{SD}^2\right]$$

or equivalently

$$i_D = k_p'\left(\frac{W}{L}\right)\left(|v_{OV}| - \frac{1}{2}v_{SD}\right)v_{SD}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{DG} \leq |V_{tp}|$$

or equivalently

$$v_{SD} \geq |v_{OV}|$$

Then

$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)(v_{SG} - |V_{tp}|)^2$$

or equivalently

$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)v_{OV}^2$$

Reference Material for further study

Sr. No.	Item	Source	Description/link
1	Theory	YouTube (Recommended)	https://www.youtube.com/watch?v=l9LBIy9Ioxo
2		NPTEL	https://www.youtube.com/watch?v=MuBiC9yz2fc
3		Boylestead Book (11th Ed.)	Section **6.8**
4	Problems for practice	Sedra Smith Book (6th Ed.)	Solved problem: **5.1, 5.5, 5.6** Exercise: **5.11, 5.12** Problems: **5.18, 5.19, 5.45, 5.46, 5.48** **Problem Sheet Provided**