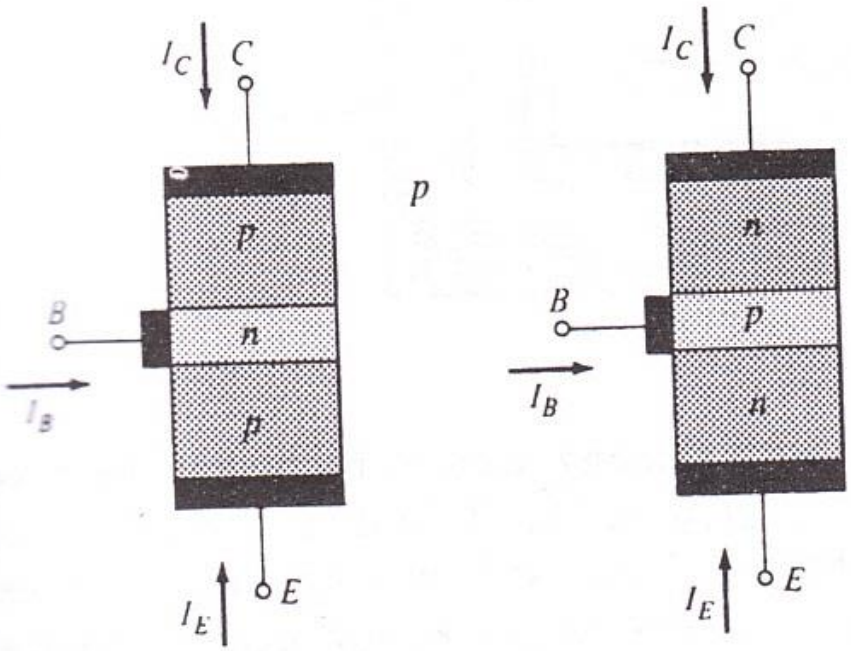
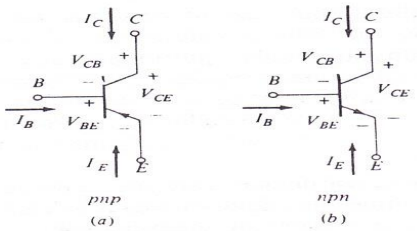
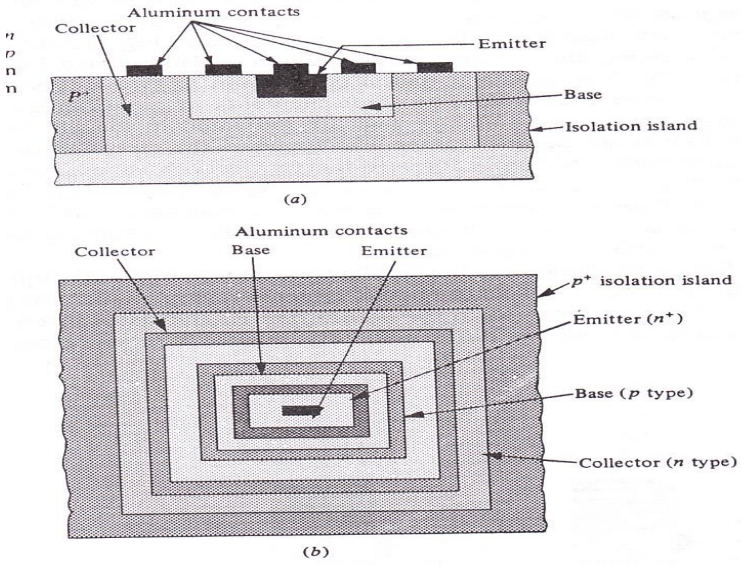
Bipolar Junction Transistor

The bipolar junction transistor (BJT) is a three-element device formed from two junctions which share the common semiconductor layer. There are two types of BJTs: pnp and npn. The three elements of the BJT are referred to as the **emitter**, **base**, and the **collector**. This is depicted in the figure below. The arrow on the emitter lead specifies the direction of the current when the emitter-base junction is forward-biased.


I_C
C
p
n
p
B
I_B
I_E
E
(a)
I_C
C
n
p
n
B
I_B
I_E
E
(b)


I_C
C
V_{CB}
+
B
–
+
V_{CE}
–
I_B
+
V_{BE}
–
I_E
E
pnp
(a)
I_C
C
V_{CB}
+
B
–
+
V_{CE}
–
I_B
+
V_{BE}
–
I_E
E
npn
(b)


n
p
n
n
Aluminum contacts
Collector
Emitter
P^+
Base
Isolation island
(a)
Aluminum contacts
Collector
Base
Emitter
p^+ isolation island
Emitter (n^+)
Base (p type)
Collector (n type)
(b)

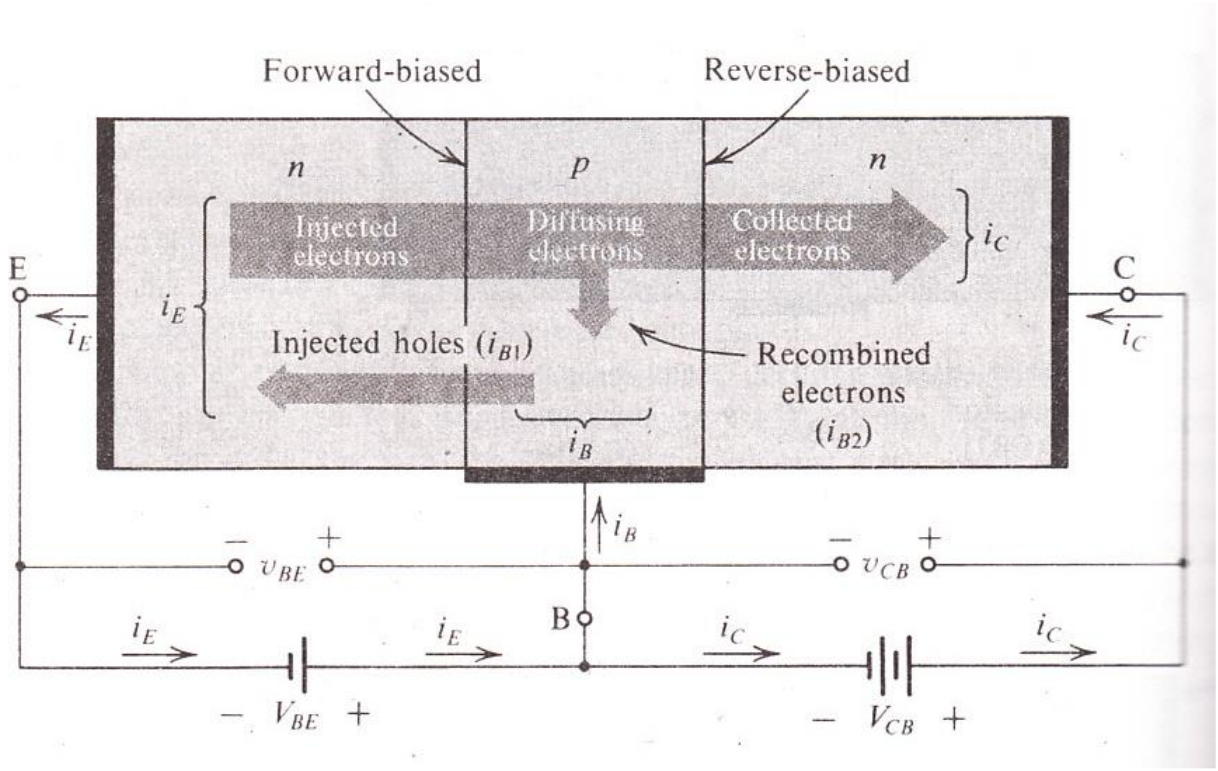
Bipolar Junction Transistor

As illustrated in the figure above, the emitter area is considerably smaller than the collector area. The difference is mainly due to the fact that in the most prevalent uses of BJTs, the collector region must handle most power than the emitter. Hence, more surface area is required for heat dissipation. A second difference is the doping densities of the emitter and collector regions. The emitter generally serves as the source of mobile charges. Therefore a high density is used in emitter to make many carriers available. When the emitter-base junction is forward biased, the emitter injects electrons into the base region where they move towards the collector. If the collector-base junction is reverse-biased, the minority carrier electron in the base are swept into the collector region, where they become the major component of the collector current. The base region is doped at a level between the emitter and collector concentration.

BJT modes of operation

Cutoff	EBJ is Reverse Biased	CBJ is Reverse Biased
Active	EBJ is Forward Biased	CBJ is Reverse Biased
Reverse Active	EBJ is Reverse Biased	CBJ is Forward Biased
Saturation	EBJ is Forward Biased	CBJ is Forward Biased

Operation of The npn Transistor in the Active Mode



Operation of npn BJT in Active Mode

The forward bias on the emitter-base junction will cause the current to flow across this junction. Current consists of two components: electrons injected from the emitter into the base, and holes injected from the base into the emitter. It is highly desirable to have the first component (electrons from emitter to base) at a much higher level than the second component (holes from the base to emitter). This can be accomplished by fabricating the device with a heavily doped emitter and a lightly doped base. The current that flows across the emitter-base junction will constitute the emitter current i_E.

The Electrons injected from emitter into the base will be minority carriers in the p-type base region. Because the Base is usually very thin, in the steady state the electron concentration will be highest at the emitter side and lowest at the collector side.

Some of the electrons that are diffusing through the base region will combine with holes which are the majority carriers in the base. However, since the base is actually very thin, the proportion of electrons lost due to recombination will be quite small.

The Collector Current

Most of the diffusing electrons from emitter will reach the boundary of the collector-base depletion region. Since the collector is more positive than the base, these electrons will be swept across the CBJ depletion region into the collector. They will get collected to constitute the collector current i_C.

$$i_C = I_S e^{\frac{V_{BE}}{V_T}}$$

$$i_E = i_C + i_B$$

$$i_C = \beta i_B$$

$$i_C = \frac{\beta}{\beta + 1} i_E$$

$$\alpha = \frac{\beta}{\beta + 1} \qquad \beta = \frac{\alpha}{1 - \alpha}$$

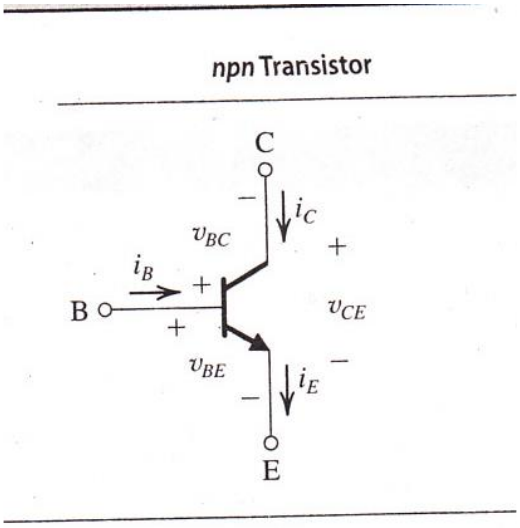
Where

β = common-emitter current gain

α = common-base current gain

The BJT as an Amplifier

The basis for the amplifier application is the fact that when the BJT is operated in the active mode, it acts as a voltage controlled current source. Changes in the base-emitter voltage gives rise to changes in the collector current i_C. Thus in the active mode BJT can be used to implement a transconductance amplifier. The amplifier circuit is illustrated below.



Operation in the Active Mode (for Amplifier Application)

Conditions:

1. EBJ Forward Biased

$v_{BE} > V_{BE\text{on}}$; $V_{BE\text{on}} \cong 0.5$ V

Typically, $v_{BE} = 0.7$ V

2. CBJ Reversed Biased

$v_{BC} \leq V_{BC\text{on}}$; $V_{BC\text{on}} \cong 0.4$ V

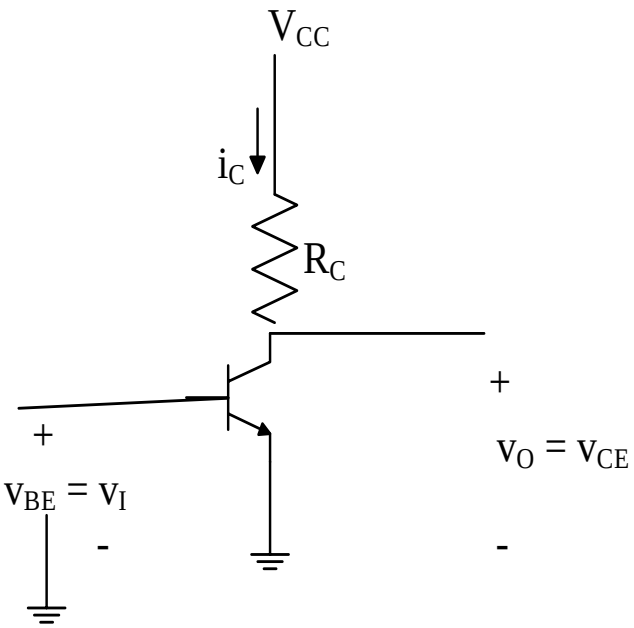
$\Rightarrow v_{CE} \geq 0.3$ V

Current-Voltage Relationships

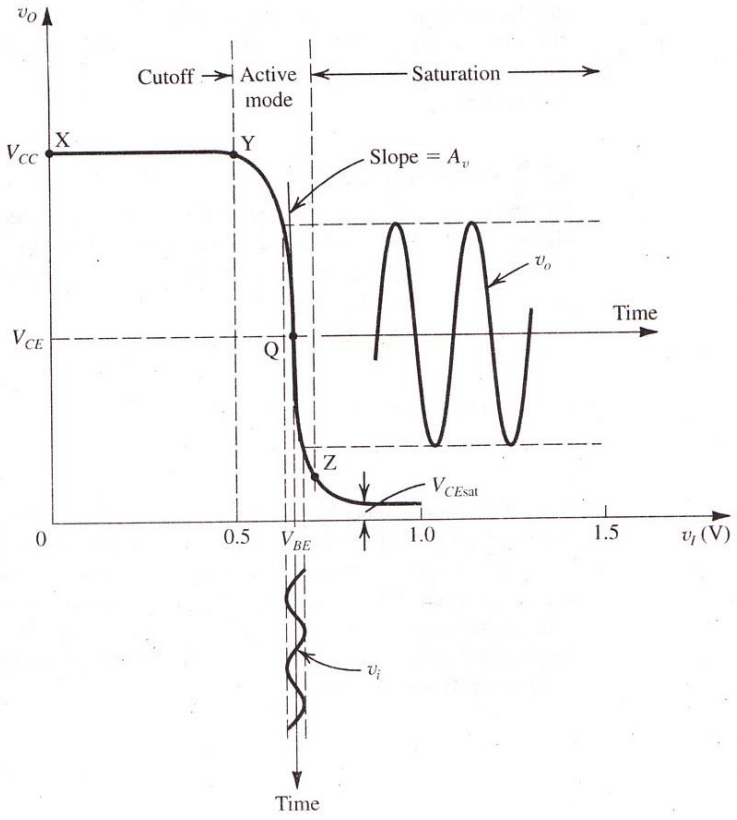
- $i_C = I_S e^{v_{BE}/V_T}$
- $i_B = i_C/\beta \quad \Leftrightarrow \quad i_C = \beta i_B$
- $i_E = i_C/\alpha \quad \Leftrightarrow \quad i_C = \alpha i_E$
- $\beta = \dfrac{\alpha}{1-\alpha} \quad \Leftrightarrow \quad \alpha = \dfrac{\beta}{\beta+1}$

Large-Signal Operation of npn Transistor

The figure given below show the basic structure of the most commonly used BJT amplifier, the grounded-emitter or common-emitter (CE) circuit. The total input voltage v_I (bias+signal) is applied between the base and emitter ($v_{BE} = v_I$). The total output voltage v_O (bias+signal) is taken between collector and ground ($v_O = v_{CE}$). The resistor R_C has two functions, first to establish a desired dc bias voltage at the collector, and to convert the collector signal current i_C to an output voltage v_{CE} or v_O.


V_{CC}
i_C
R_C
+
$v_{BE} = v_I$
-
+
$v_O = v_{CE}$
-

(a)


v_O
Cutoff
Active mode
Saturation
V_{CC}
X
Y
Slope = A_v
v_o
Time
V_{CE}
Q
Z
V_{CEsat}
0
0.5
V_{BE}
1.0
1.5
v_I (V)
v_i
Time

(b)

The transfer characteristics of the circuit in (a) is given in (b) above. The amplifier is biased at the point Q, and a small signal v_I is superimposed on the bias voltage v_{BE}. The resulting output signal v_O, appears superimposed on the dc collector voiltage V_{CE}. The amplitude of v_O is larger than that of v_I by voltage gain A_v.

$$v_O = v_{CE} = V_{CC} - R_C i_C$$

$$i_C = I_S e^{\frac{v_{BE}}{V_T}}$$

$$= I_S e^{\frac{v_I}{V_T}}$$

Thus we obtain

$$v_O = V_{CC} - R_C I_S e^{\frac{v_I}{V_T}}$$

We observe that the exponential term in this equation gives rise to the steep slope of the YZ segment of the transfer curve. Active mode operation ends when the collector voltage (v_O or v_{CE}) falls by 0.4 V or so below that of the base (v_I or v_{BE}). At this point, the CBJ turns on, and the transistor enters the saturation region. This is indicated by the point Z on the transfer curve. A further increase in v_{BE} causes v_{CE} to decrease only slightly. In saturation region $v_{CE} = V_{CEsat}$, which falls in the narrow range of 0.1 V to 0.2 V. The collector current will also remain nearly constant at the value I_{Csat}.

Amplifier Gain

To operated the BJT as a linear amplifier, it must be biased at the point in the active region. The figure given above shows such point, labeled Q (for quiesent point) and characterized by a dc base-emitter voltage V_{BE} and a dc collector-emitter voiltage V_{CE}. Then,

$$V_{CE} = V_{CC} - R_C I_C$$

Small signal Amplifier gain A_V can be found out by differentiating the expression in v_O given above and evaluating the derivative at point Q for $v_I = V_{BE}$.

$$A_v \equiv \frac{dv_O}{d_{v_I}}\Big|_{v_I = V_{BE}}$$

$$= -\frac{1}{V_T} I_S e^{V_{BE}/V_T} R_C \qquad = -\frac{I_C R_C}{V_T} \qquad = -\frac{V_{RC}}{V_T}$$

Where V_{RC} is the dc voltage drop across R_C

$$V_{RC} = V_{CC} - V_{CE}$$

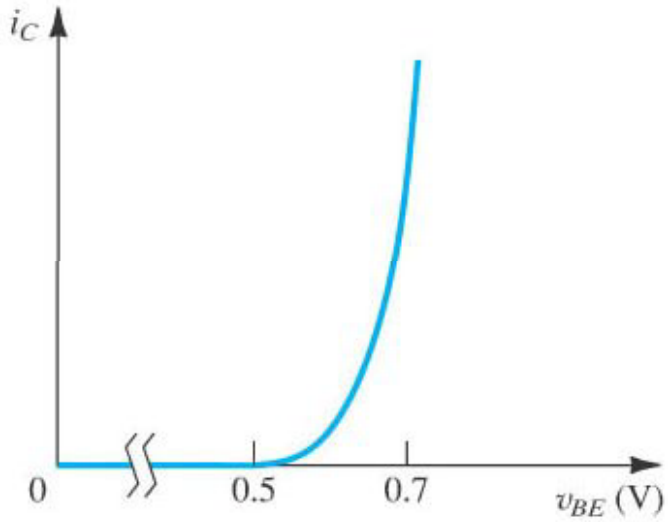
Observe that the CE amplifier is inverting, that is, the output is 180^0 out of phase relative to the input signal. It follows that to maximize the voltage gain we should use as large a voltage drop across R_C as possible. Thus for a given value of V_{CC}, to increase V_{RC} we have to operate at lower V_{CE}. The lowest V_{CE} is V_{CEsat}. Hence,

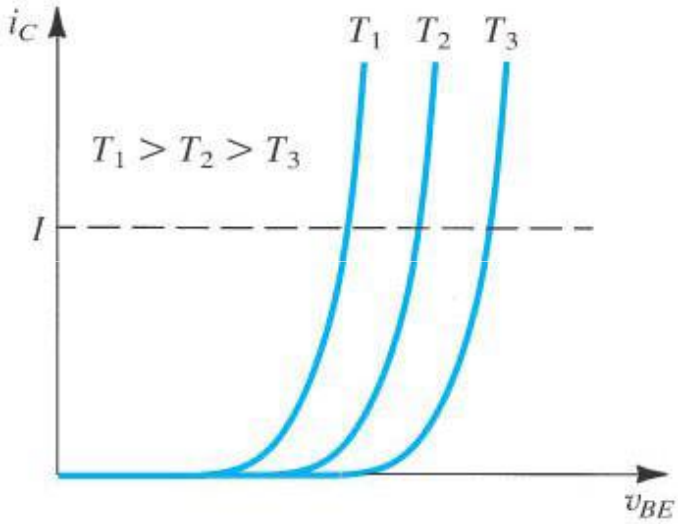
$$A_v = -\frac{V_{CC} - V_{CEsat}}{V_T}$$

$$A_{v\max} \cong -\frac{V_{CC}}{V_T}$$

Graphical Representation of Transistor Characteristics

The figure given below shows the i_C-v_{BE} characteristics of a BJT



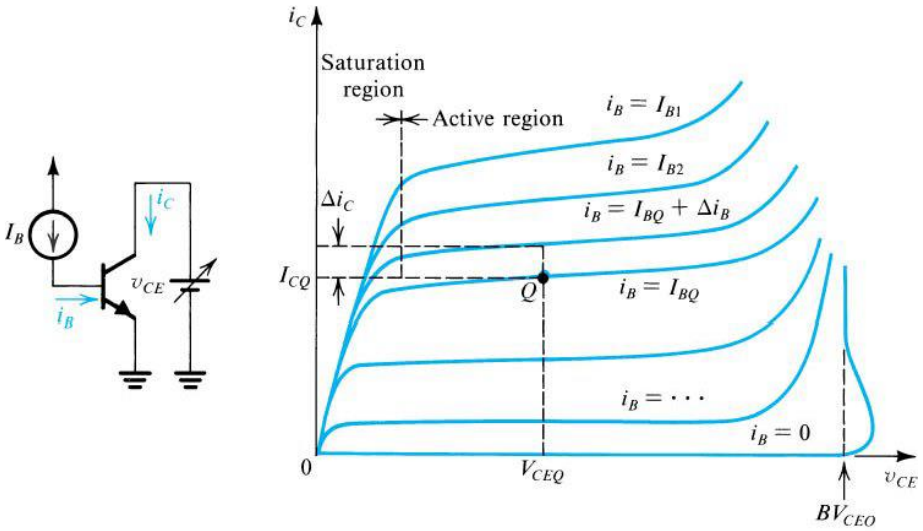


As in silicon diodes the voltage across the emitter-base junction decreases by about 2 mV for each rise of 1^0 C in temperature, provided that the junction is operating at the constant current I as shown in the figure above.

$$i_C = I_S e^{\frac{v_{BE}}{V_T}}$$

The Common-Emitter Characteristics

An alternative way of expressing the transistor common-emitter characteristics is illustrated in figure below. Here the base current i_B rather than the base-emitter voltage v_{BE} is used as a parameter.



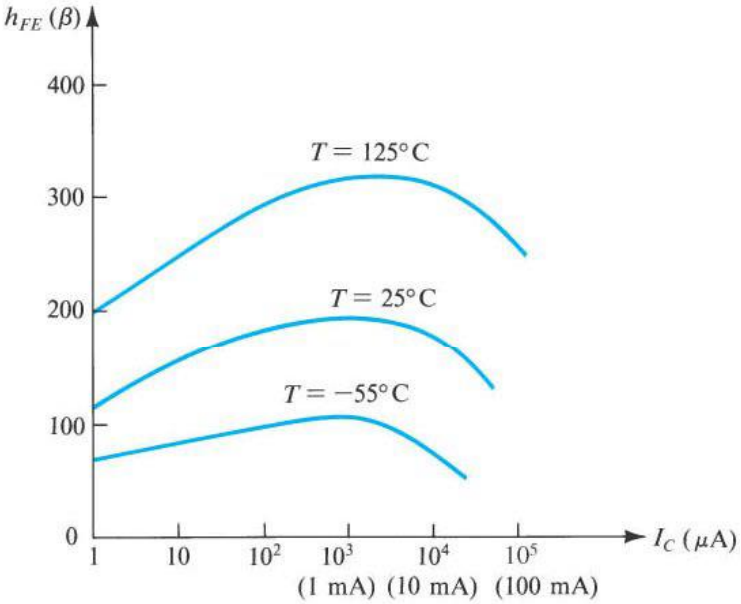
(a) (b)

An important parameter is the common-emitter current gain β. Consider the transistor operating in the active region at the point labelled Q as shown in Fig (b) above. The collector current at this point is I_{CQ} and base current as I_{BQ} and the collector voltage V_{CEQ}. The ratio of the collector current to base current is the large-signal or dc β.

$$\beta_{dc} \equiv \frac{I_{CQ}}{I_{BQ}} \qquad \beta_{ac} = \frac{\Delta i_C}{\Delta i_B}\bigg|_{v_{CE}=constant}$$

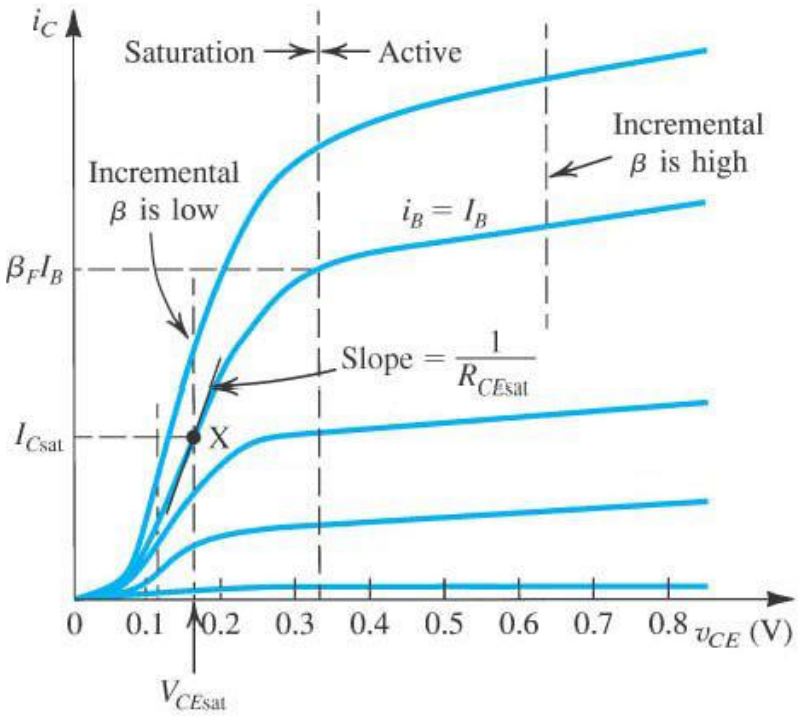
Which is the β we have been using in our description of the transistor operation. It is commonly referred to on the manufacturer's data sheets as h_{fe} . One can define another β based on incremental or small-signal quantities. So, keeping v_{CE} constant at point V_{CEQ}, changing i_B from I_{BQ} to $(I_{BQ} + \Delta i_B)$ results in i_C increasing from I_{CQ} to $(I_{CQ} + \Delta i_C)$. Thus we can write the incremental or ac β as β_{ac} .

The magnitude of β_{ac} and β_{dc} differ, typically by approximately 10% to 20%. Finally, it should be mentioned here that the small-signal β or β_{ac} is known by an alternate symbol h_{fe}. Because the small-signal β or h_{fe} is defined and measured at a constant v_{CE}, that is with a zero signal component between collector and emitter, it is known as the **short-circuit common-emitter current gain**.



The figure shows the typical dependence of β on I_C and on temperature in a modern integrated-circuit npn silicon transistor intended for operation around 1 mA. The value of β depends on the current at which the transistor is operating as shown by the above relationship. It also shows the temperature dependence of β.

An expanded view of the common-emitter characteristics in the saturation region



As can be seen from the figure the incremental β is lower in the saturation region than in the active region. A possible operating point in the saturation region is that labelled X. It is characterised by a base current I_B, a collector current Icsat and a collector -emitter voltage V_{CEsat}. Note that $I_{Csat} < \beta_F I_B$. Since the value of I_{Csat} is established by the circuit designer, a saturation transistor is said to be operating at a **forced β** given by

$$\beta_{forced} \equiv \frac{I_{Csat}}{I_B} \qquad \text{Thus,} \qquad \beta_{forced} < \beta_F$$

The ratio of β_F to β_{forced} is known as the **overdrive factor**. The greater the overdrive factor, the deeper the transistor is driven into saturation and the lower the V_{CEsat} becomes.The collector to emitter resistance R_{CEsat} is given below. Typically R_{CEsat} ranges between a few ohms to a few tens of ohms.

$$R_{CEsat} \equiv \left. \frac{\partial v_{CE}}{\partial i_C} \right|_{i_B = I_B, i_C = I_{Csat}}$$

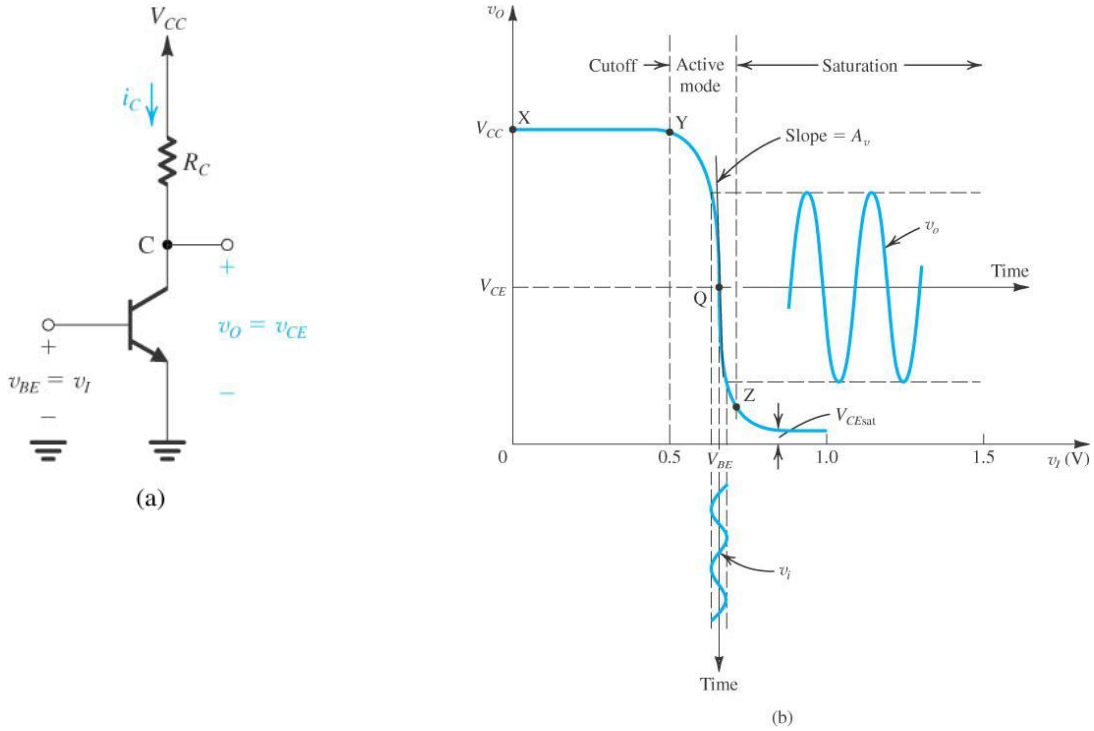


Figure (a) Basic common-emitter amplifier circuit. **(b)** Transfer characteristic of the circuit in (a). The amplifier is biased at a point Q, and a small voltage signal vi is superimposed on the dc bias voltage VBE. The resulting output signal vo appears superimposed on the dc collector voltage VCE. The amplitude of vo is larger than that of vi by the voltage gain Av.

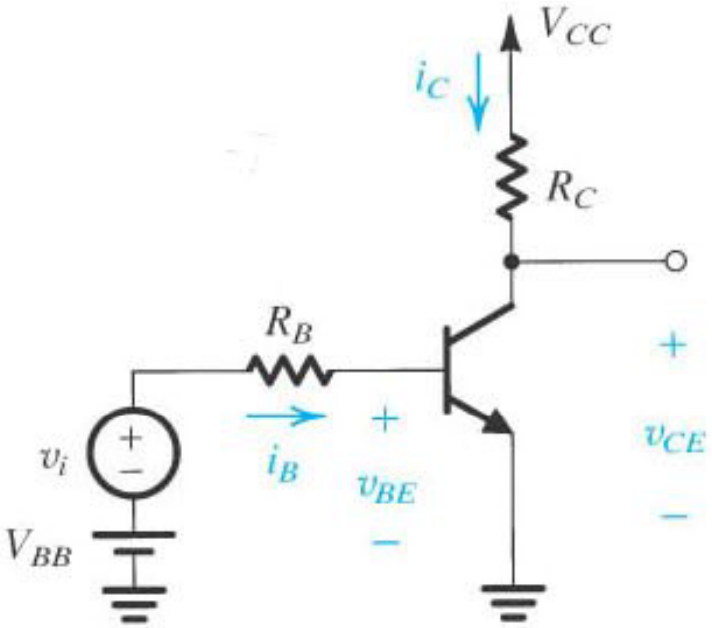


Figure Circuit whose operation is to be analyzed graphically

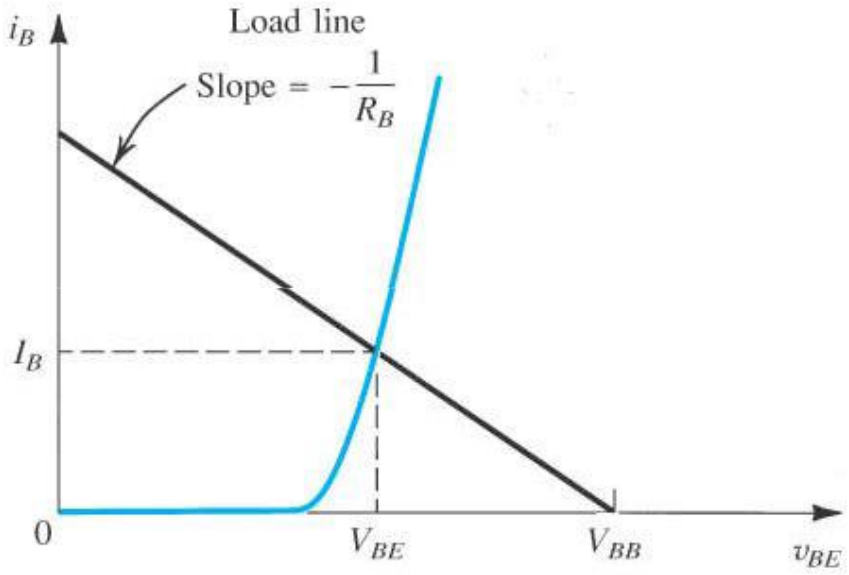


Figure Graphical construction for the determination of the dc base current in the circuit of Fig. given before.

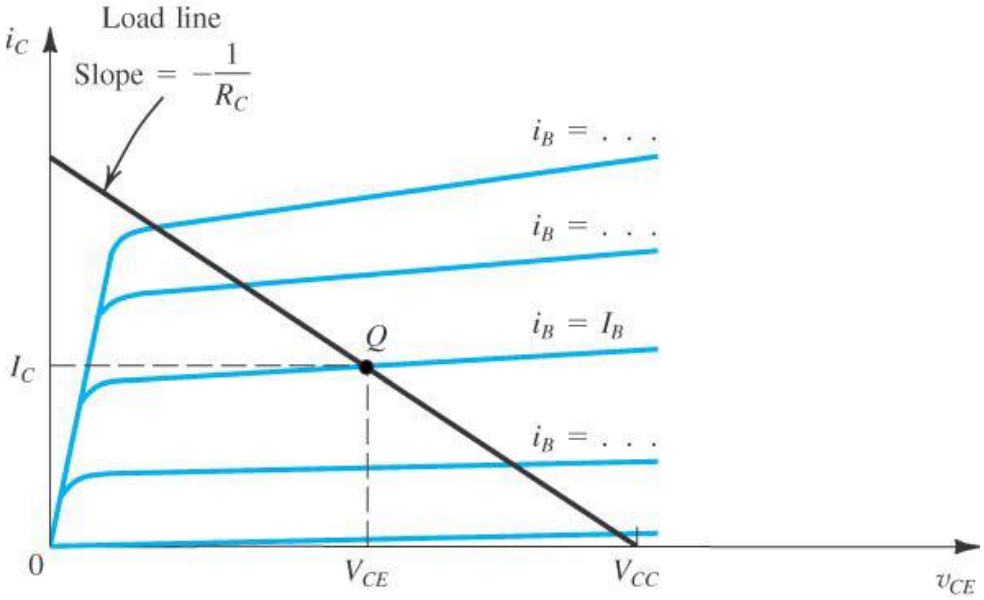
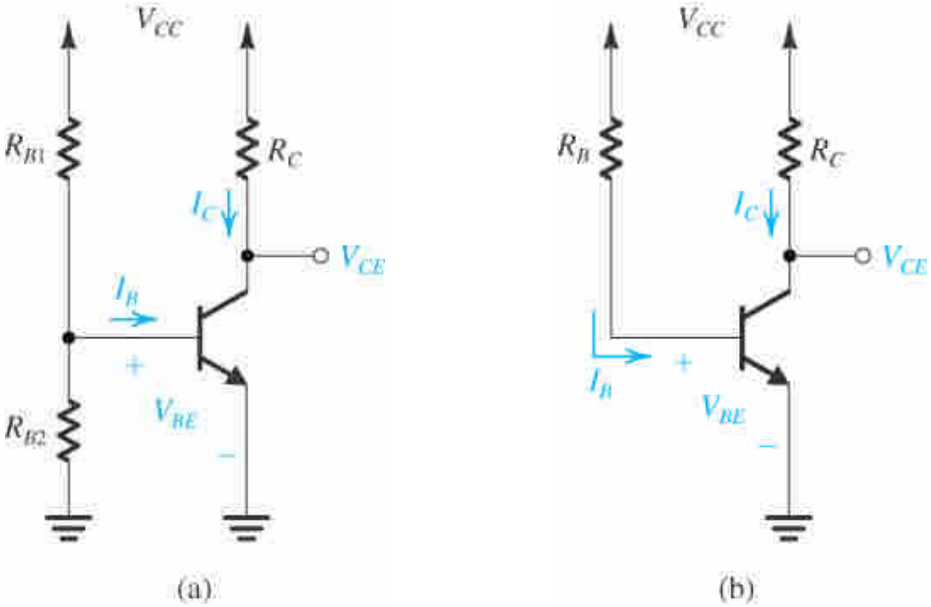


Figure Graphical construction for determining the dc collector current IC and the collector-to-emitter voltage VCE in the circuit of Fig. given before.

Biasing in BJT Amplifier Circuits

The biasing problem is that of establishing a constant dc current in the collector of the BJT. This current has to be calculated, predictable, and insensitive to the variations in temperature and to a large variations in the value of β encountered among the transistors of the same type.

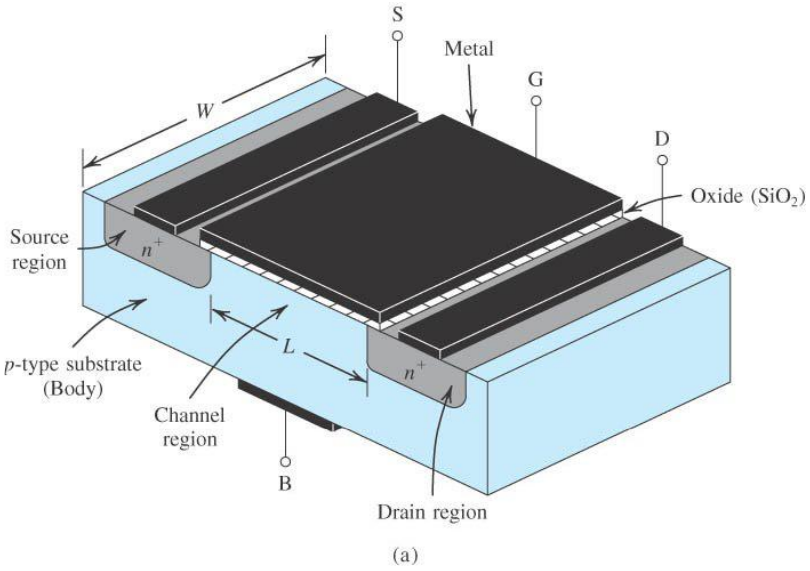
Attempting to bias the BJT by fixing the voltage V_{BE} by using a voltage divider across the power supply V_{CC}, as shown in figure below (a) is not viable approach. The very sharp exponential relationship $i_C - v_{BE}$ means that any small and inevitable differences in V_{BE} from the desired value will result in large differences in I_C and V_{CE}. Secondly, biasing the BJT by establishing a constant current in the base, as shown in (b) below, where $I_B \equiv (V_{CC} - 0.7)/R_B$, is also not recommended approach. Here the typical large variations in the value of β among units of the same device type will result in corresponding large variations in I_C and hence V_{CE}.

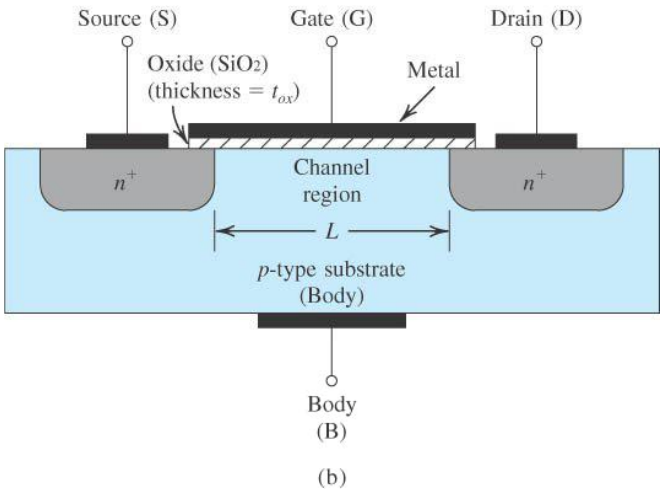


Two obvious schemes for biasing the BJT: **(a)** by fixing V_{BE}; **(b)** by fixing I_B. Both result in wide variations in I_C and hence in V_{CE} and therefore are considered to be "bad." Neither scheme is recommended.

Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

The transistor is fabricated on a p-type substrate, which is single-crystal silicon wafer that provides physical support for the device. Two heavily doped n-type regions, indicated in the figure below as n+ **source** and the n+ **drain** regions, are created in the substrate. A thin layer of silicon dioxide (SiO_2) of the thickness typically between 2-50 nm serves as an excellent electrical insulator, is grown on the surface of the substrate covering the area between the **source** and the **drain** regions. Metal is deposited on top of the oxide layer to form the **gate electrode** of the device.

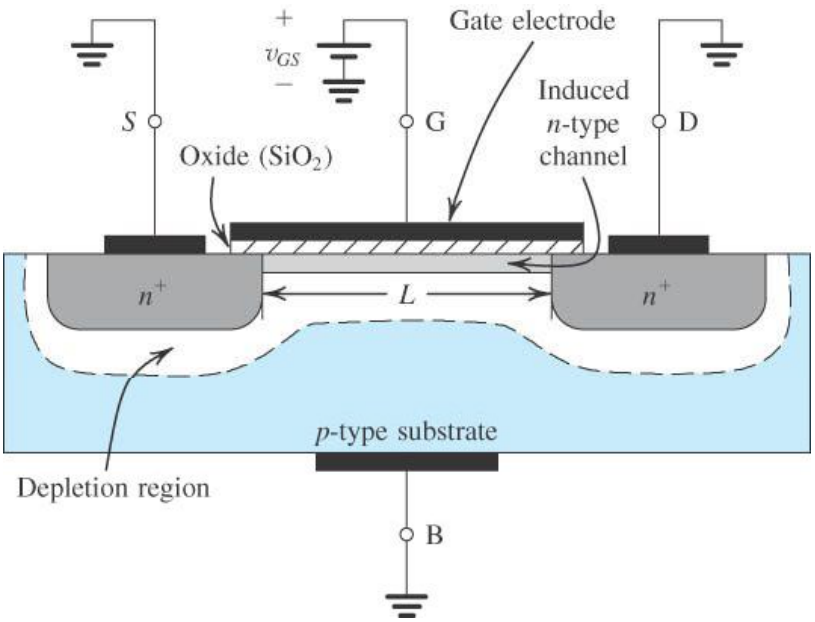




Physical structure of the enhancement-type NMOS transistor

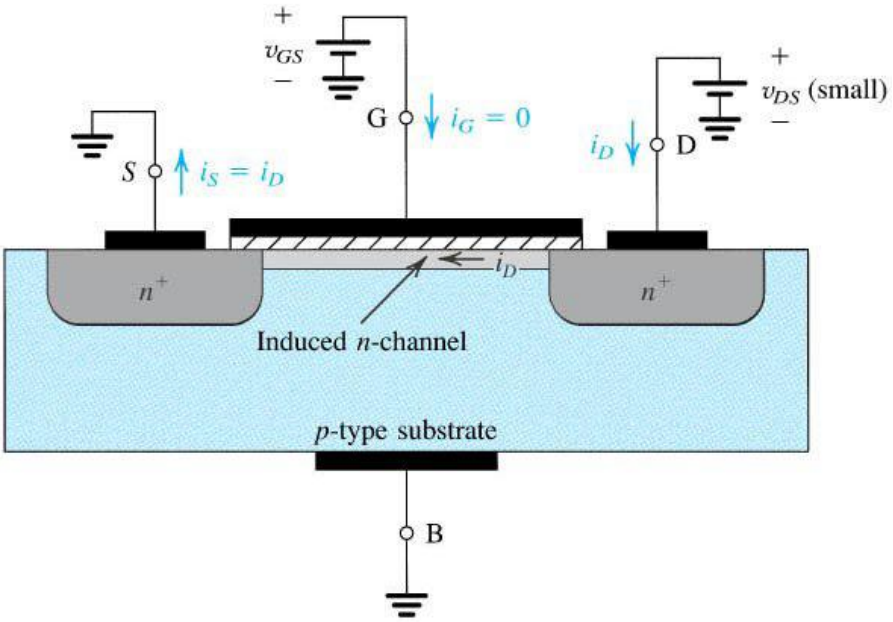
(a) Perspective View (b) Cross-section

Another name for the MOSFET is the insulated-gate FET or IGFET. This name also arise from the physical structure of the device, emphasizing the fact that the gate electrode is electrically insulated from the device body (by the oxide layer). It is this insulation that causes the current in the gate terminal to be extremely small (of the order of 10^{-15} A).



The enhancement-type NMOS transistor with a positive voltage applied to the gate is shown in the figure. An n-channel is induced at the top of the substrate beneath the gate. The value of the v_{GS} at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the **threshold voltage** and is denoted by V_t which is positive for n-channel FET. The value of V_t is controlled during device fabrication and typically lies in the range 0.5 V to 1.0 V.

The gate and the channel region of the MOSFET form a parallel plate capacitor, with the oxide layer acting as the capacitor dielectric. The positive gate voltage causes positive charge to accumulate on the top plate of the capacitor. The corresponding negative charge on the bottom plate is formed by electrons in the induced channel. An Electrical field thus develops in the vertical direction. It is this field that controls the amount of charge in the channel, and thus determines the channel conductivity and, in turn, the current that will flow through the channel when the voltage v_{DS} is applied.

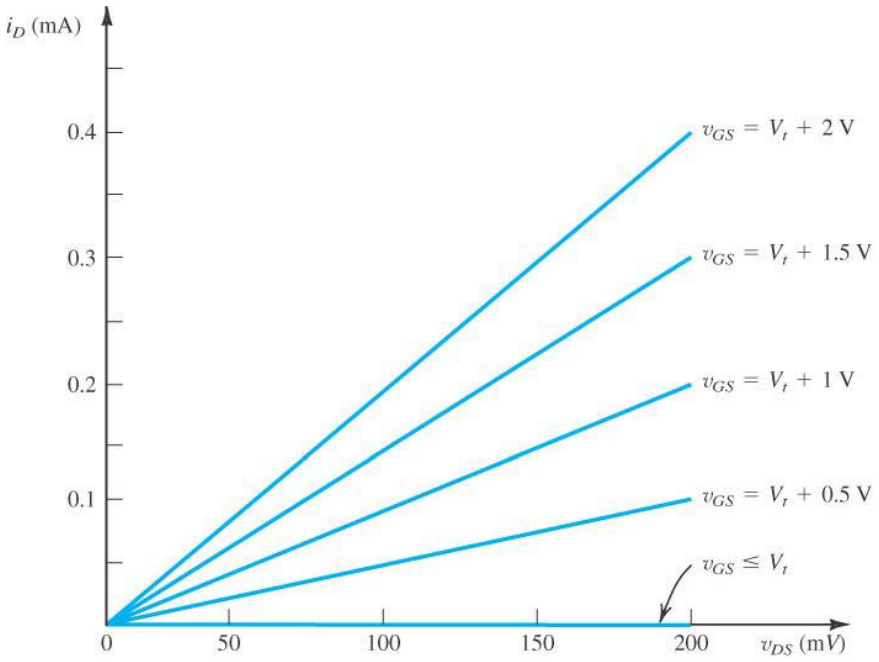


Applying a small v_{DS}

An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a resistance whose value is determined by v_{GS}. Specifically, the channel conductance is proportional to $v_{GS} - V_t$ and thus i_D is proportional to $(v_{GS} - V_t)$ and v_{DS}. Current is carried by free electrons travelling from the source to drain. By convention, the direction of the current flow is opposite to that of the flow of negative charge. Thus the current flows from the drain to source in the channel. The magnitude of i_D depends upon the density of the electrons in the channel, which in turn depends upon the magnitude of v_{GS}. Specifically, for $v_{GS} = V_t$, the channel is just induced and the current conducted is still negligibly small.

As v_{GS} exceeds V_t, more electrons are attracted into the channel. We may visualize the increase in charge carriers in the channel as the increase in the channel depth. The result is a channel of increased conductance or, equivalently, reduced resistance.

Figure given below shows a sketch of i_D versus v_{DS} for various values of v_{GS}. We observe that the MOSFET is operating as a linear resistance whose value is controlled by v_{GS}. The resistance is infinite for $v_{GS} \leq V_t$ and its value decreases v_{GS} exceeds V_t.



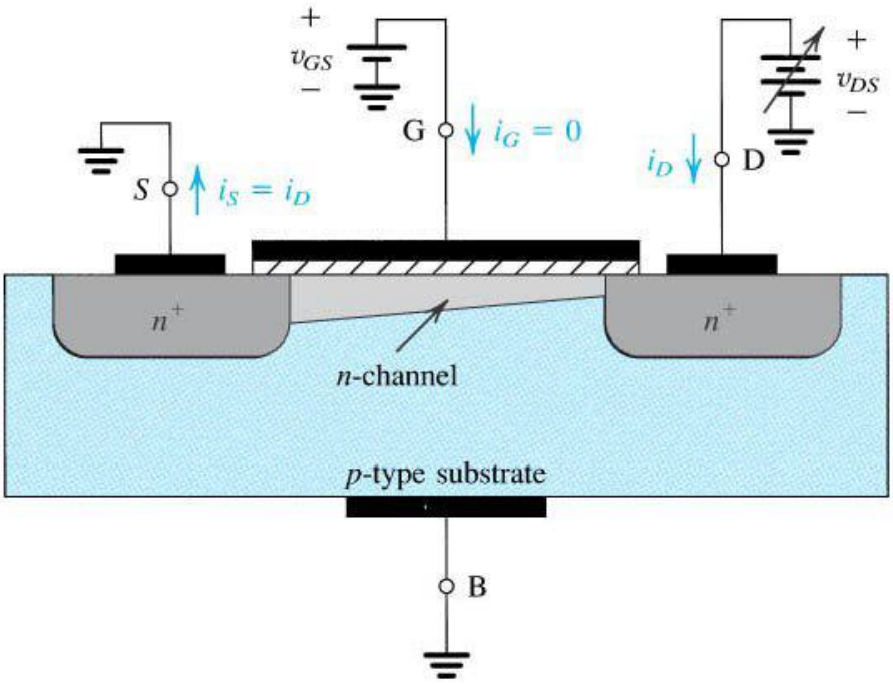
The i_D–v_{DS} characteristics of the MOSFET in this figure when the voltage applied between drain and source, v_{DS}, is kept small. The device operates as a linear resistor whose value is controlled by v_{GS}.

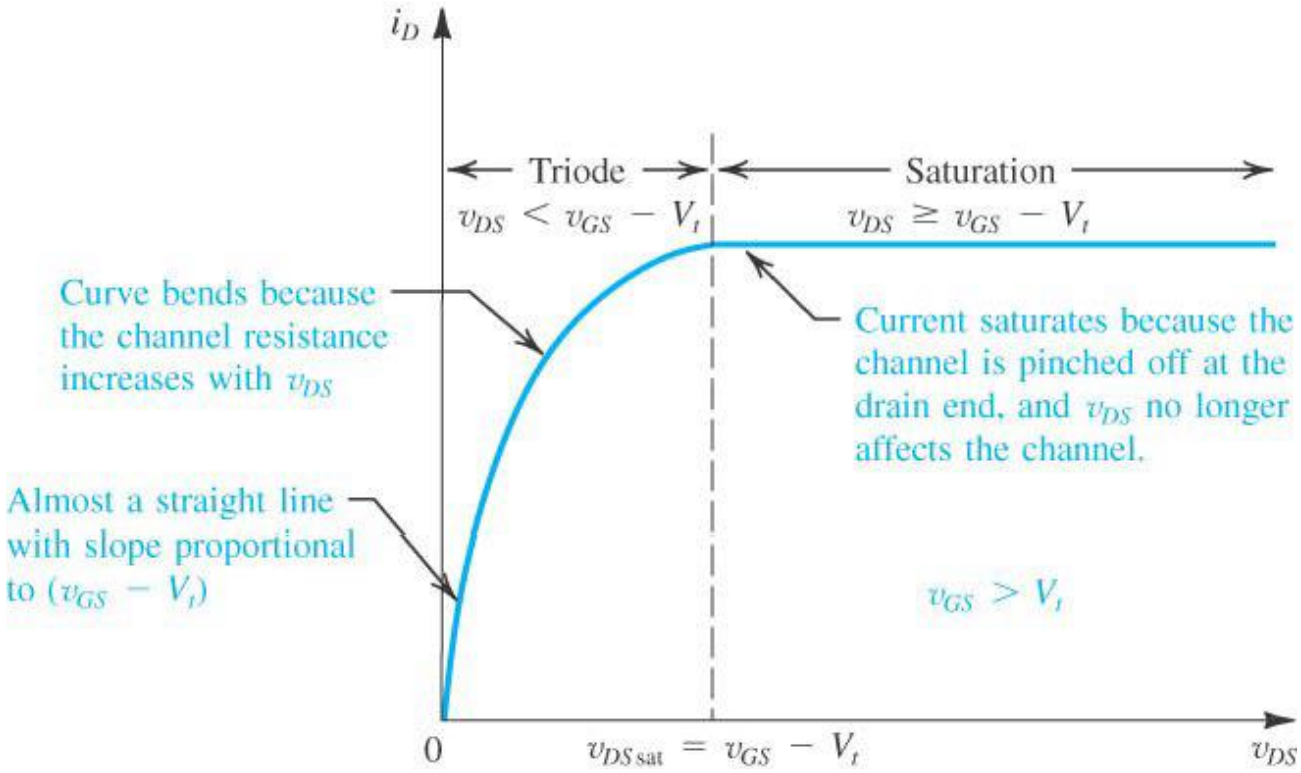
For the MOSFET to conduct a channel has to be induced. Then, increasing the v_{GS} above the threshold voltage V_t enhances the channel, hence the name of this type of MOSFET is **enhancement-type** MOSFET. Finally, we note that the current that leaves the source terminal (i_S) is equal to the current that enters the drain terminal (i_D) and the gate current $i_G = 0$.

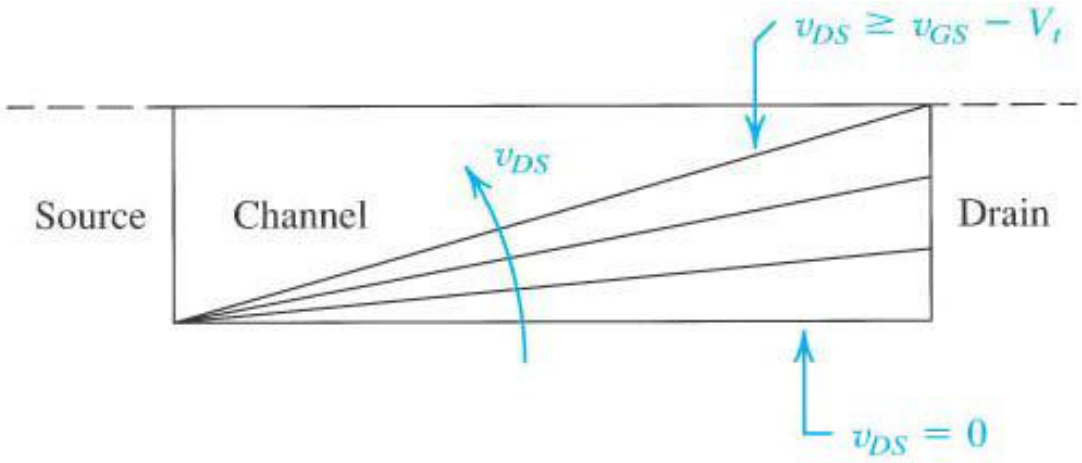
Operation as v_{DS} is Increased

For this purpose let v_{GS} be held constant at a value greater than V_t. The voltage between the gate and the points along the channel decreases from v_{GS} at the source end to $v_{GS} - v_{DS}$ at the drain end. Since the channel depth depends upon this voltage, we find that the channel is no longer uniform in depth; rather the channel is tapering as shown in figure below, being deepest at the source and shallowest at the drain end. As v_{DS} is increased, the channel becomes more tapered and its resistance increases correspondingly. Eventually, when v_{DS} is increased to the value that reduces the voltage between gate and channel at the drain end to V_t that is, $v_{GD} = V_t$ or $v_{GS} - v_{DS} = V_t$ or $v_{DS} = V_{GS} - V_t$ the channel depth at the drain end decreases to almost zero, and the channel is said to be **pinched-off**. The drain current thus **saturates** at this value and the MOSFET is said to have entered the **saturation region** of operation. The voltage v_{DS} at which the saturation occurs is denoted by v_{DSsat} where

$$v_{DSsat} = v_{GS} - V_t$$




i_D
Triode
$v_{DS} < v_{GS} - V_t$
Saturation
$v_{DS} \geq v_{GS} - V_t$
Curve bends because the channel resistance increases with v_{DS}
Current saturates because the channel is pinched off at the drain end, and v_{DS} no longer affects the channel.
Almost a straight line with slope proportional to $(v_{GS} - V_t)$
$v_{GS} > V_t$
0
$v_{DS\,sat} = v_{GS} - V_t$
v_{DS}



Obviously for every value of $v_{GS} \geq V_t$, there is a corresponding value of v_{DSsat}. The device operates in the saturation region if $v_{DS} \geq v_{DSsat}$. The region of i_D-v_{DS} characteristics obtained for $v_{DS} < v_{DSsat}$ is called the **triode region**.

The i_D-v_{DS} Characteristics

The characteristics given in the following figure indicate that there are three distinct regions of operation: the **cutoff region**, the **triode region**, and the **saturation region**. The saturation region is used if the FET is to operate as an amplifier. For operation as a switch, the cutoff and triode regions are utilized. The device is cut off when $v_{GS} < V_t$. To operate the MOSFET in the triode region we must first induce a channel,

$$v_{GS} \geq V_t \text{ (induced channel)}$$

And then keep v_{DS} small enough so that the channel remains continuous. This is achieved by ensuring that the gate-to-drain voltage is

$$v_{GD} > V_t \text{ (continuous channel)}$$

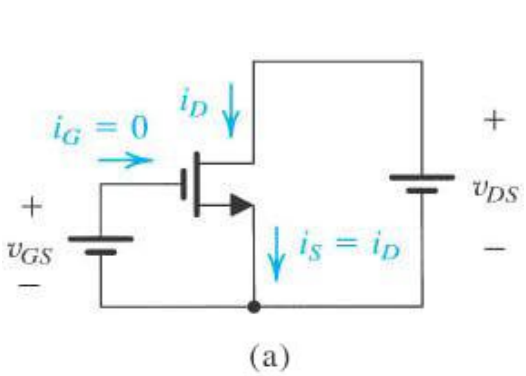
This condition can be stated explicitly in terms of v_{DS} by writing $v_{GD} = v_{GS} + v_{SD} = v_{GS} - v_{DS}$
Thus,

$$v_{GS} - v_{DS} > V_t$$

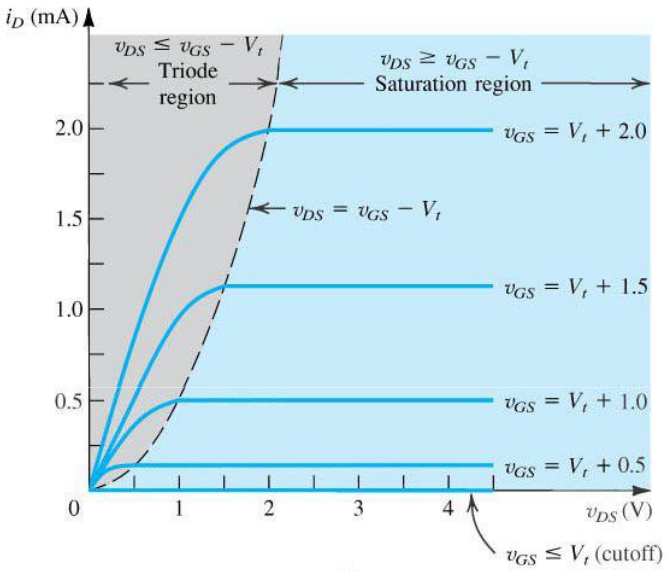
Which can be rearranged to yield

$$v_{GD} < v_{GS} - V_t \text{ (continuous channel)}$$

In words, the n-channel enhancement-type MOSFET operates in the triode region when v_{GS} is greater than V_t, and the drain voltage is lower than the gate voltage by at least V_t volts.



(a)



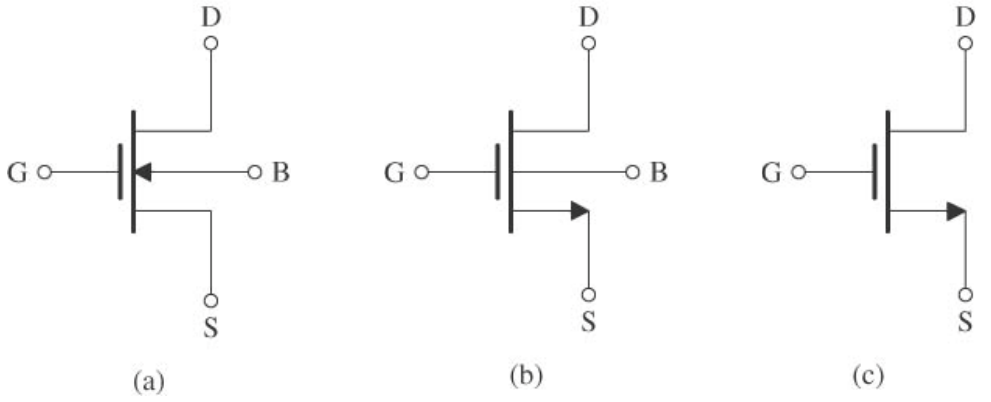
(b)

(a) An n-channel enhancement-type MOSFET with v_{GS} and v_{DS} applied and with the normal directions of current flow indicated.

(b) The i_D–v_{DS} characteristics for a device with k'n (W/L) = 1.0 mA/V^2.

Circuit Symbol

The figure below shows the circuit symbol for the n-channel enhancement-type MOSFET. Although the MOSFET is a symmetrical device, it is often useful in circuit design to designate one terminal as the source and the other as the drain (without having to write S and D beside the terminals). The arrowhead points in the normal direction of current flow and thus indicates the polarity of the device. The figure clearly distinguishes the source from the drain, the drain is always positive relative to the source in an n-channel FET.



(a) Circuit symbol for the n-channel enhancement-type MOSFET.

(b) Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain and to indicate device polarity (i.e., n channel).

(c) Simplified circuit symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

In the triode region the i_D-v_{DS} characteristics can be described by the relationship

$$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

Where k_n' is the process transconductance parameter (is equal to $\mu_n C_{ox}$), its value is determined by the fabrication technology. If v_{DS} is sufficiently small so that we can neglect the V_{DS}^2 term in equation above, we obtain for i_D-v_{DS} characteristics near the origin the relationship

$$i_D \cong k_n' \frac{W}{L}(v_{GS} - V_t)v_{DS}$$

This linear relationship represents the operation of the MOS transistor as a linear resistance whose value is controlled by v_{GS}. Specifically, for v_{GS} set to a value V_{GS}, r_{DS} is given by

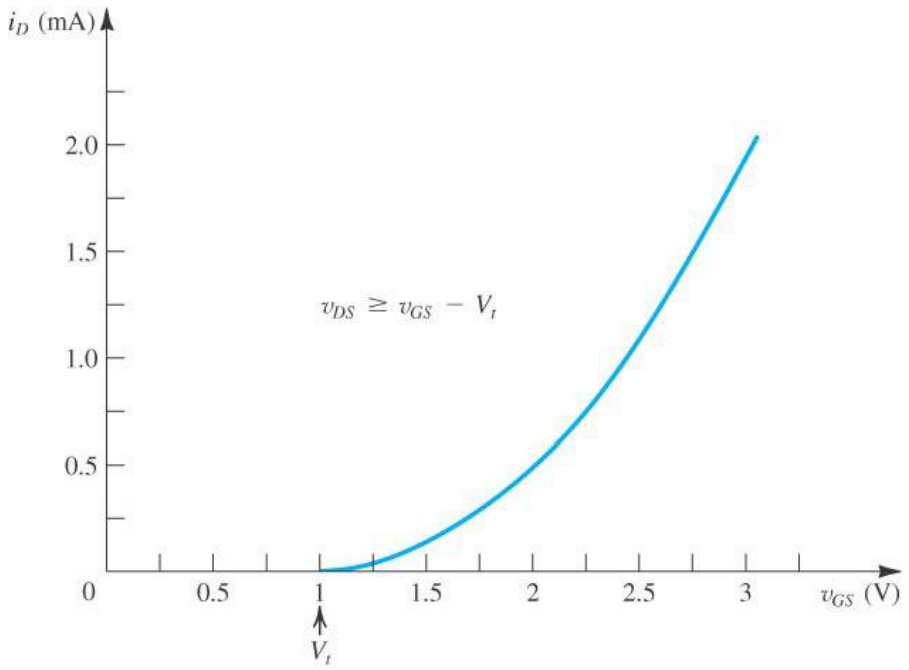
$$r_{DS} \equiv \frac{v_{DS}}{i_D}\bigg|_{\substack{v_{DS}\,small \\ v_{GS}=V_{GS}}} = \left[k_n^{'}\frac{W}{L}(V_{GS}-V_t)\right]^{-1}$$

The boundary between the triode and saturation regions is characterised by

$$v_{DS} = v_{GS} - V_t$$

Substituting in the first equation above we get

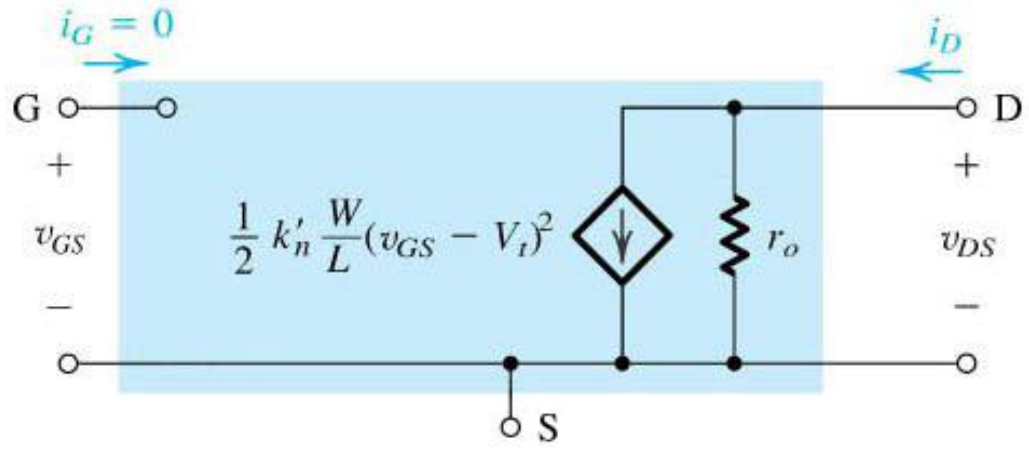
$$i_D = \frac{1}{2}k_n^{'}\frac{W}{L}(v_{GS}-V_t)^2$$



The i_D–v_{GS} characteristic for an enhancement-type NMOS transistor in saturation ($V_t = 1$ V, $k_n'W/L = 1.0$ mA/V^2)

Temperature Effects

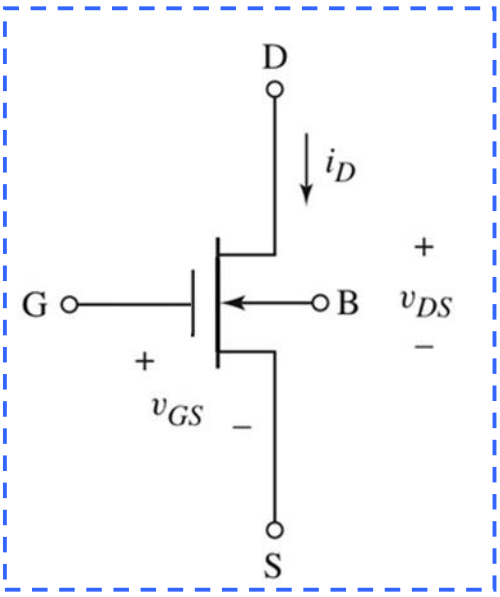
Both V_t and k' are temperature sensitive. The magnitude of V_t decreases by about 2 mV for every 1°C rise in temperature. This decrease in $|V_t|$ gives rise to a corresponding increase in drain current as the temperature is increased. However, k' decreases with the temperature and its effect is dominant one, the overall observed effect of a temperature increase is a decrease in drain current.

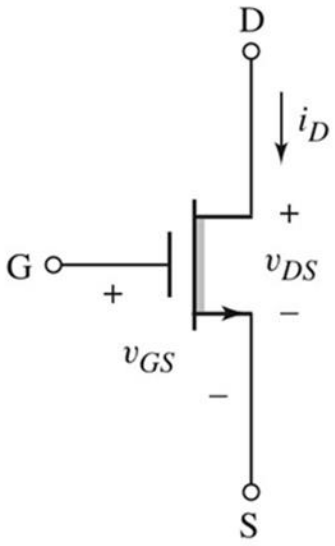


Where I_D is the drain current without the channel-length modulation taken into account. That is

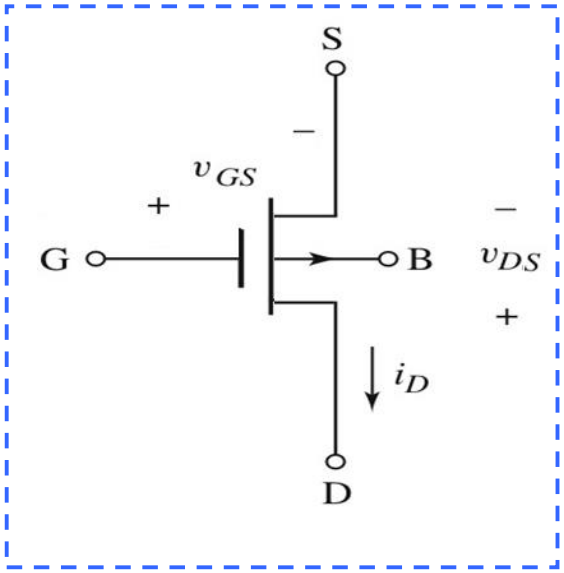
$$I_D = \frac{1}{2} k_n' \frac{W}{L} \left(V_{GS} - V_t\right)^2 = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left(V_{GS} - V_t\right)^2$$

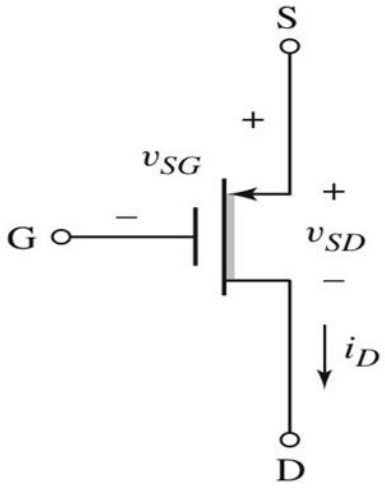
Symbols for n channel Depletion Mode MOSFET

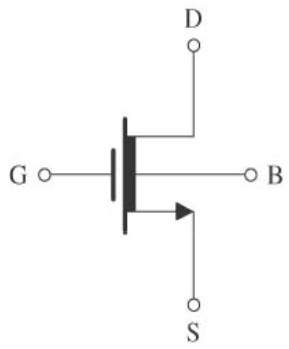




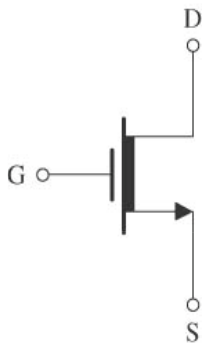
Symbols for p channel Depletion Mode MOSFET





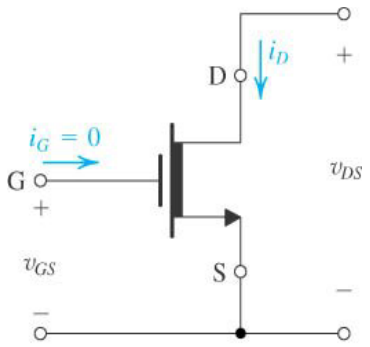


(a)

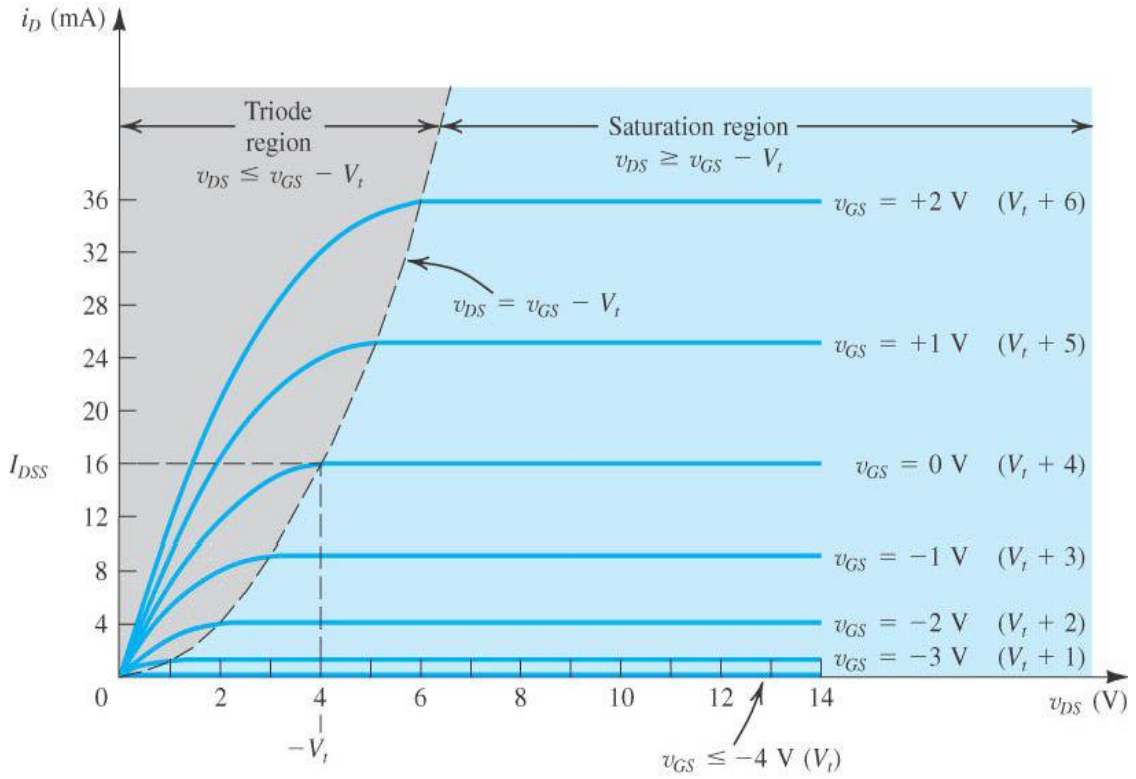


(b)

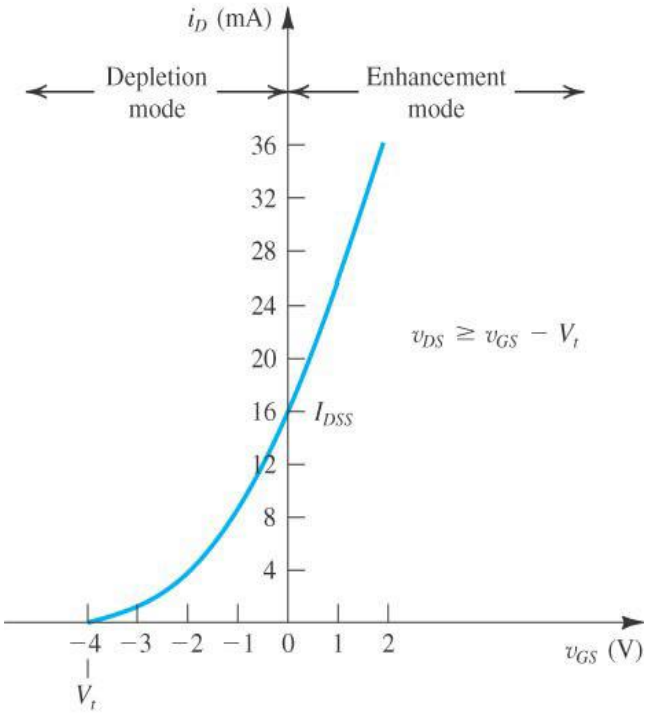
Figure 4.59 (a) Circuit symbol for the n-channel depletion-type MOSFET. **(b)** Simplified circuit symbol applicable for the case the substrate (B) is connected to the source (S).


D
i_D
+
$i_G = 0$
G
+
v_{DS}
v_{GS}
S
−
−

(a)


i_D (mA)
Triode region
$v_{DS} \leq v_{GS} - V_t$
Saturation region
$v_{DS} \geq v_{GS} - V_t$
36
32
28
24
20
I_{DSS}
16
12
8
4
0
2
4
6
8
10
12
14
v_{DS} (V)
$v_{DS} = v_{GS} - V_t$
$v_{GS} = +2$ V $(V_t + 6)$
$v_{GS} = +1$ V $(V_t + 5)$
$v_{GS} = 0$ V $(V_t + 4)$
$v_{GS} = -1$ V $(V_t + 3)$
$v_{GS} = -2$ V $(V_t + 2)$
$v_{GS} = -3$ V $(V_t + 1)$
$-V_t$
$v_{GS} \leq -4$ V (V_t)

(b)



(c)

Figure 4.60 The current-voltage characteristics of a depletion-type n-channel MOSFET for which $V_t = -4$ V and $k_n(W/L) = 2$ mA/V^2
(a) transistor with current and voltage polarities indicated;
(b) the i_D–v_{DS} characteristics;
(c) the i_D–v_{GS} characteristic in saturation.