UNIT :4

COMBINATIONAL CIRCUITS
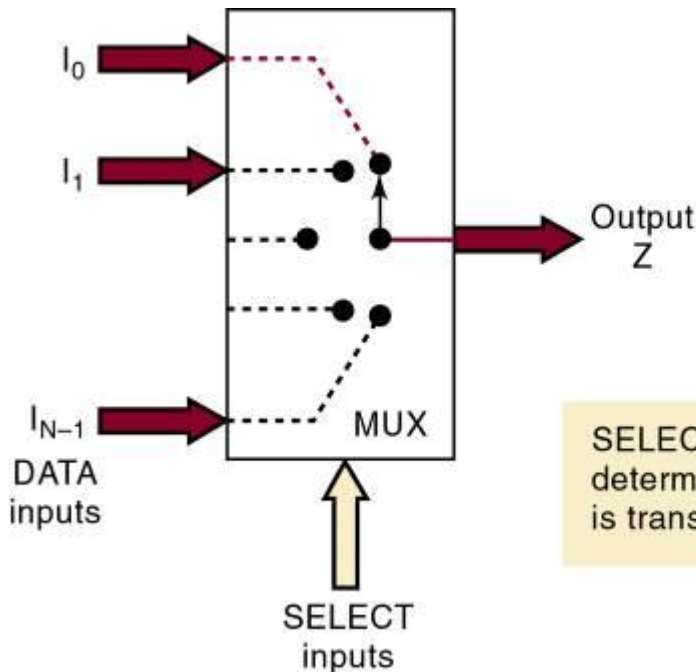
LOGIC CIRCUITS

- 2.1 Multiplexers (MUX)

- 2.2 Decoders

- 2.3 Encoders

2.1) Multiplexers (Data Selectors)

- A **multiplexer (MUX)** selects 1 of *N* input data sources and transmits the selected data to a single output—called **multiplexing.**
  - Basic function: select one of its 2^N data input lines and place the corresponding information onto a single output line.
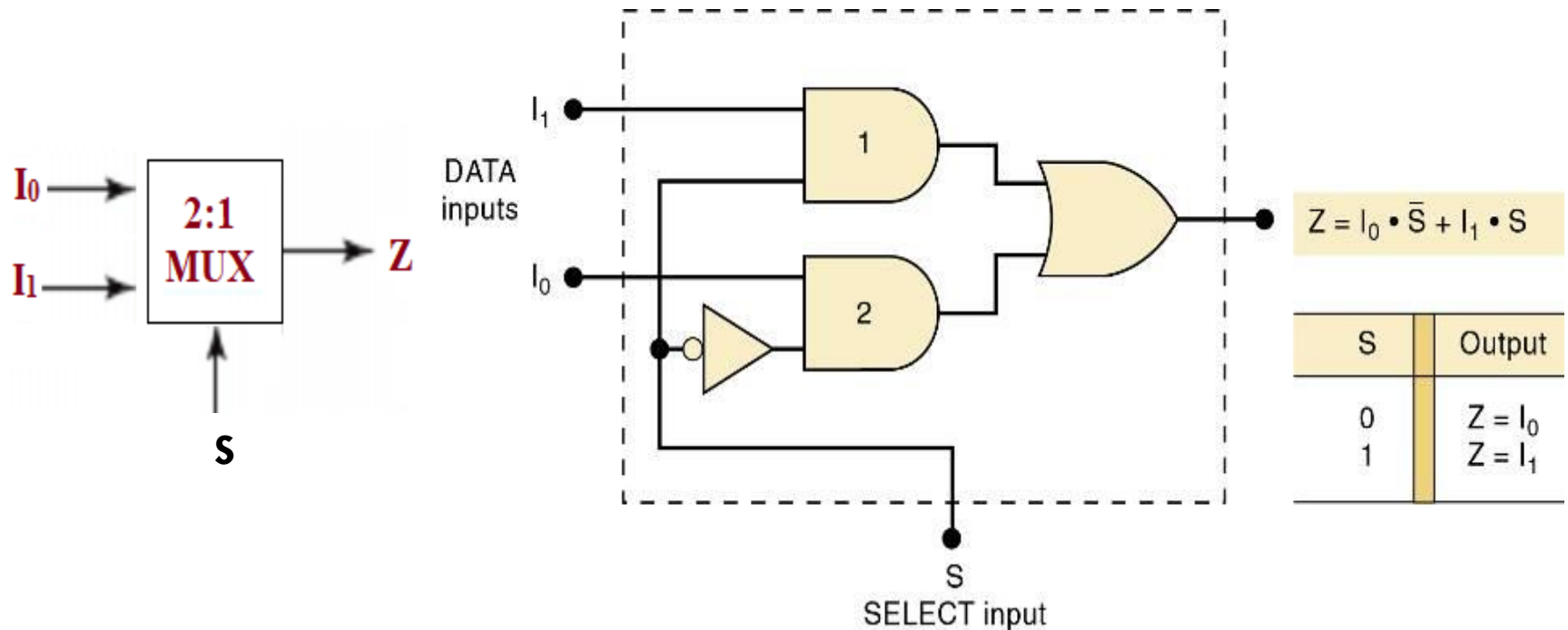

Routing control of desired data input to output by SELECT inputs—referred to as ADDRESS inputs.

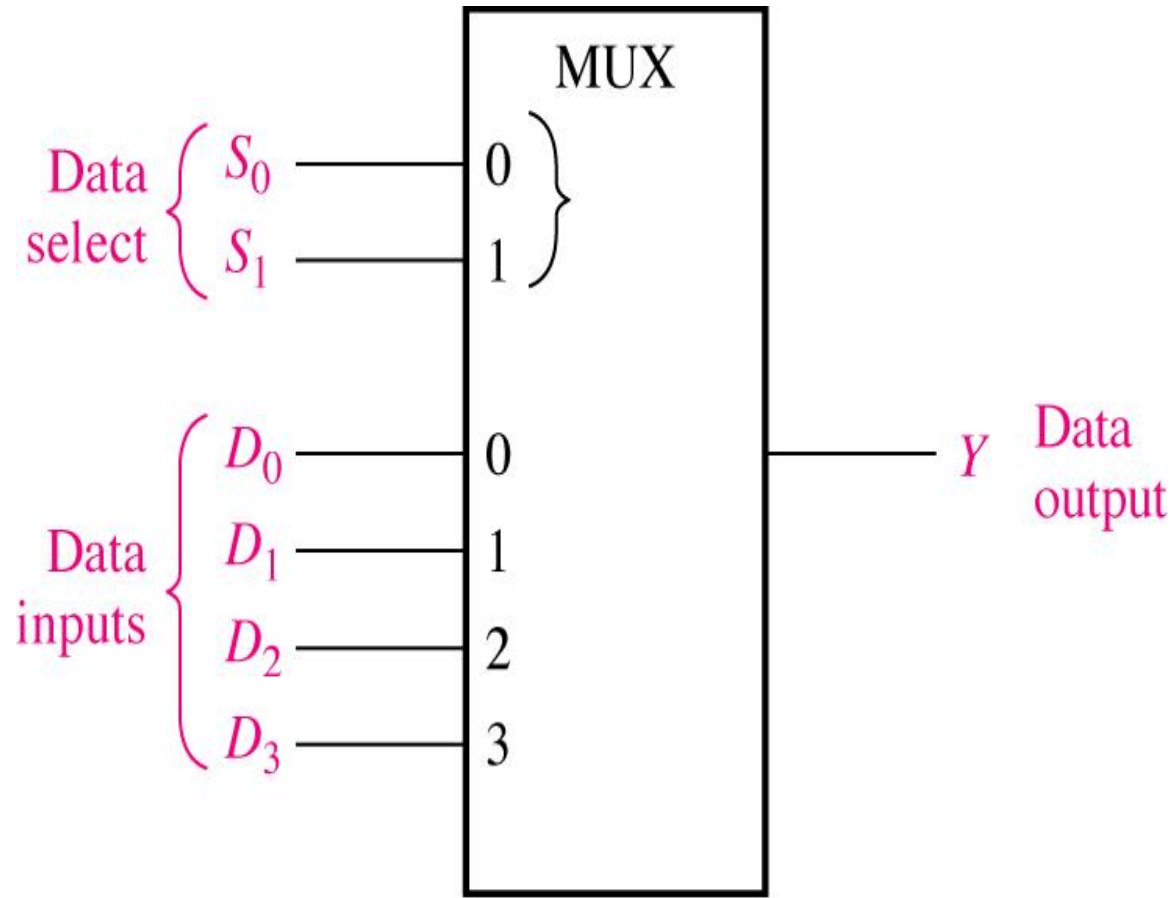SELECT input code determines which input is transmitted to output Z.

2-1 Multiplexer

- A two-input MUX comprises of 2 Data Input's I_0 & I_1
- It comprises of a single Select Input S
- Based on the value of S (either 0/1), either the value of I_0 or I_1 is transferred at the output

$$Z = I_0 \cdot \bar{S} + I_1 \cdot S$$

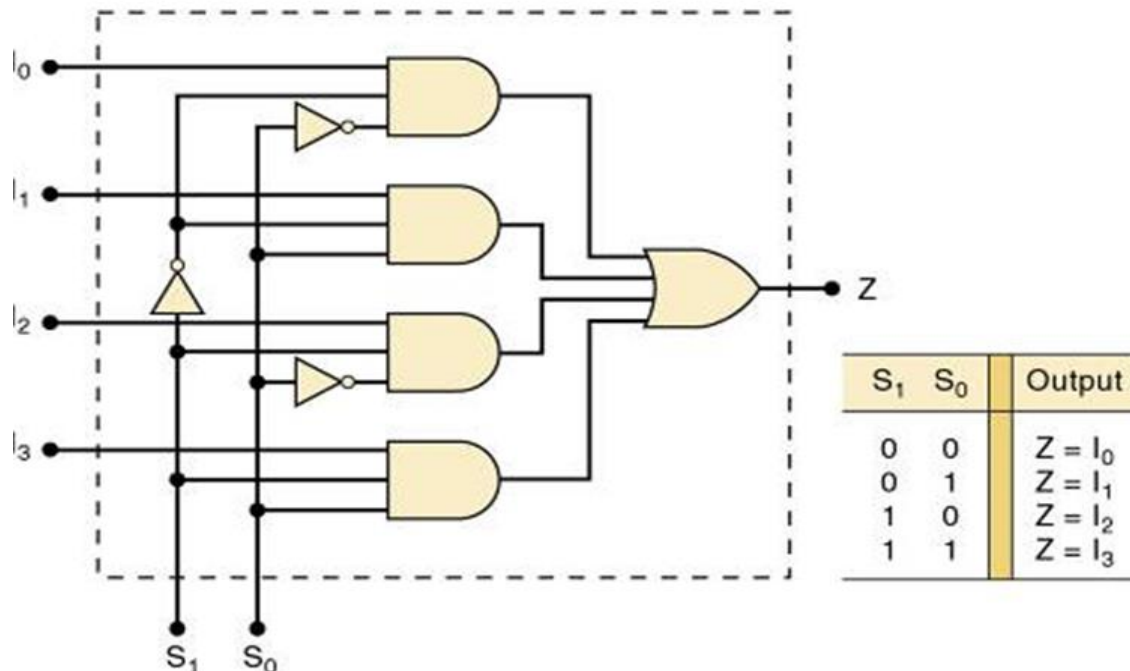| S	Output
0	$Z = I_0$
1	$Z = I_1$

Logic Symbol of 4-1 Multiplexer

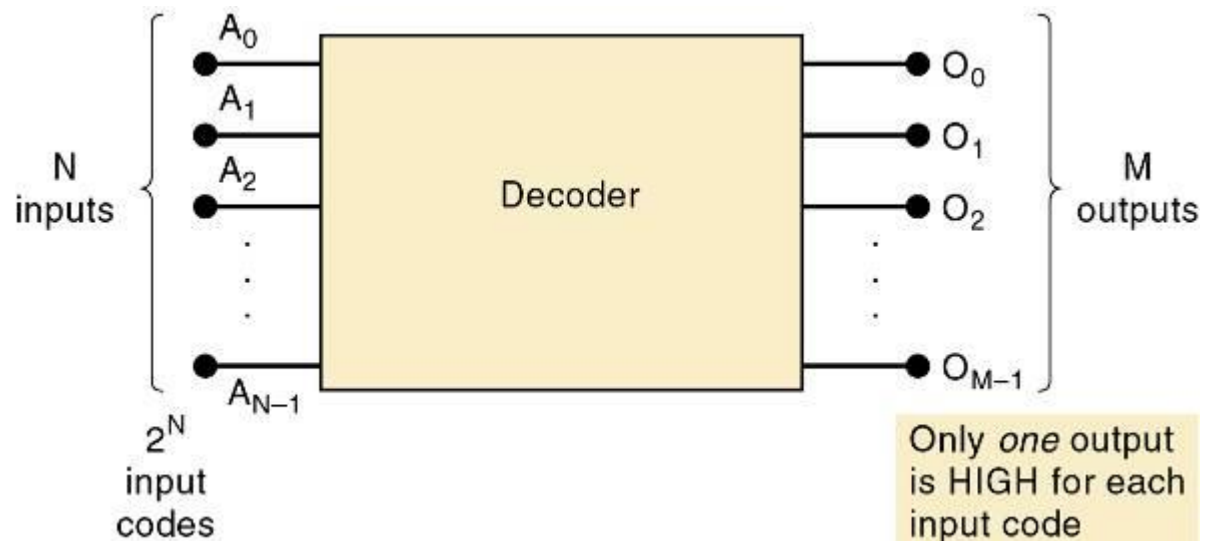# 4-1 Multiplexers (Data Selectors)

- Four Input Multiplexer comprises of 4 Data Inputs & 2 Select Input lines
  - Based on the combination of select inputs, either of the data input is transferred to the output.

S_1	S_0	Output
0	0	$Z = I_0$
0	1	$Z = I_1$
1	0	$Z = I_2$
1	1	$Z = I_3$

2.2) Decoders

- A **decoder** accepts a set of inputs that represents a binary number—activating only the output that corresponds to the input number.

For each of these input combinations, only one of the M outputs will be active (HIGH); all the other outputs are LOW.

N inputs

2^N input codes

A_0
A_1
A_2
A_{N-1}

Decoder

O_0
O_1
O_2
O_{M-1}

M outputs
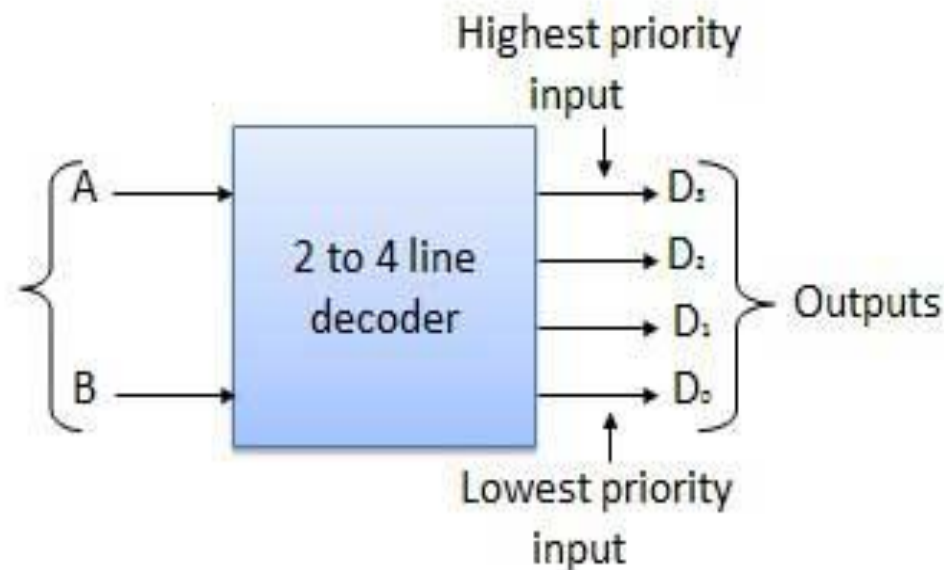
Only *one* output is HIGH for each input code

Many decoders are designed to produce active-LOW outputs, where only the selected output is LOW while all others are HIGH.

2 line to 4 line Decoder

- Block diagram of 2-line to 4-line Decoder comprising of 2 Inputs & 4 Outputs is shown in the figure.

2 line to 4 line Decoder

- When A= 0 & B =0 ,Output D_0 is activated (Logic 1) , remaining all outputs are deactivated (Logic 0)
- When A= 0 & B =1 ,Output D_1 is activated (Logic 1) , remaining all outputs are deactivated (Logic 0)
- When A= 1 & B =0 ,Output D_2 is activated (Logic 1) , remaining all outputs are deactivated (Logic 0)
- When A= 1 & B =1 ,Output D_3 is activated (Logic 1) , remaining all outputs are deactivated (Logic 0)

INPUTS		OUTPUTS			
A (MSB)	B (LSB)	D_3 (MSB)	D_2	D_1	D_0 (LSB)
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

3 line to 8 line Decoder

- A 3 line to 8 line Decoder has 3 Inputs and 8 Outputs.

- Also called Binary to Octal Decoder-taking 3 bit binary input code and activating one of eight (octal) outputs

- Also referred to as a 1-of-a-8-Decoder-only 1 of the 8 outputs is activated at a time.

3 line to 8 line Decoder

- Truth Table of 3 line to 8 line Decoder is given below
- Assignment Question : Draw the block level diagram of 3 line to 8 line Decoder & explain the operation

A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

2.3) Encoders

- Most decoders accept an input code & produce a HIGH (or LOW) at *one* and *only one* output line.
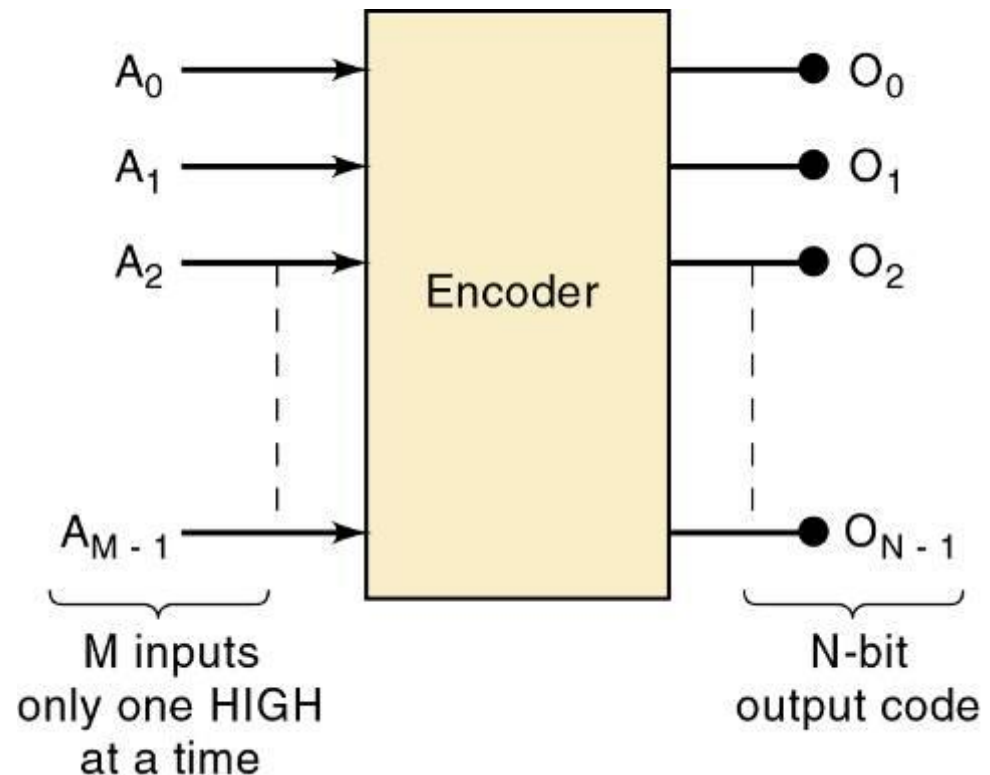 - A decoder identifies, recognizes, or detects a particular code.

2.3) Encoders

- The opposite of decoding process is **encoding.**
  - Performed by a logic circuit called an **encode**r.

An encoder has a number of input lines, only **one** of which is activated at a given time.

Shown is an encoder with M inputs and N outputs.

Inputs are active-HIGH, which means that they are normally LOW.

It produces an N-bit output code, depending on which input is activated.

A_0 → | Encoder | → O_0
A_1 → | | → O_1
A_2 → | | → O_2
A_{M-1} → | | → O_{N-1}

M inputs only one HIGH at a time

N-bit output code

4 line to 2 line Encoder

- A 4 line to 2 line Encoder comprises of 4 Inputs and 2 Outputs.

- Based on the Input that's being activated a 2 bit code is generated at the output.

- The block diagram and truth table of the aforementioned is shown

4 line to 2 line Encoder
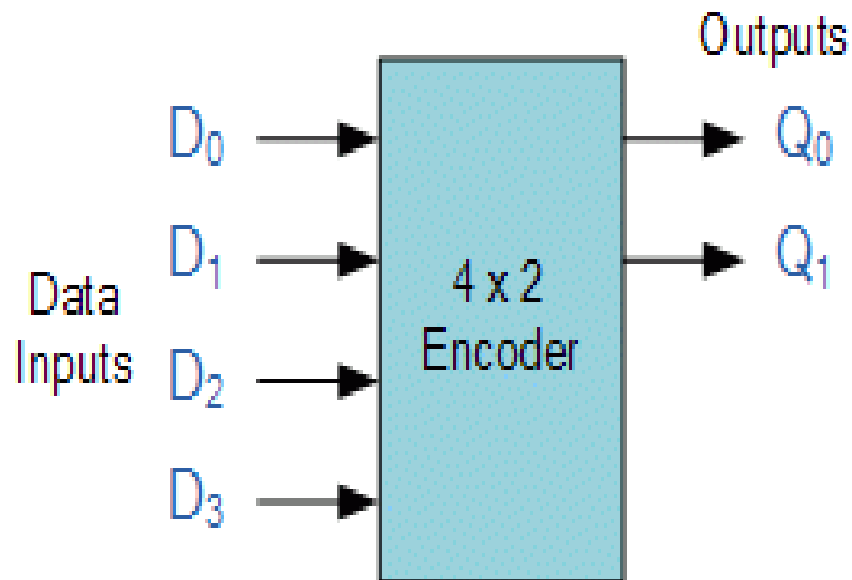
Inputs				Outputs	
D_3	D_2	D_1	D_0	Q_1	Q_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1
0	0	0	0	x	x