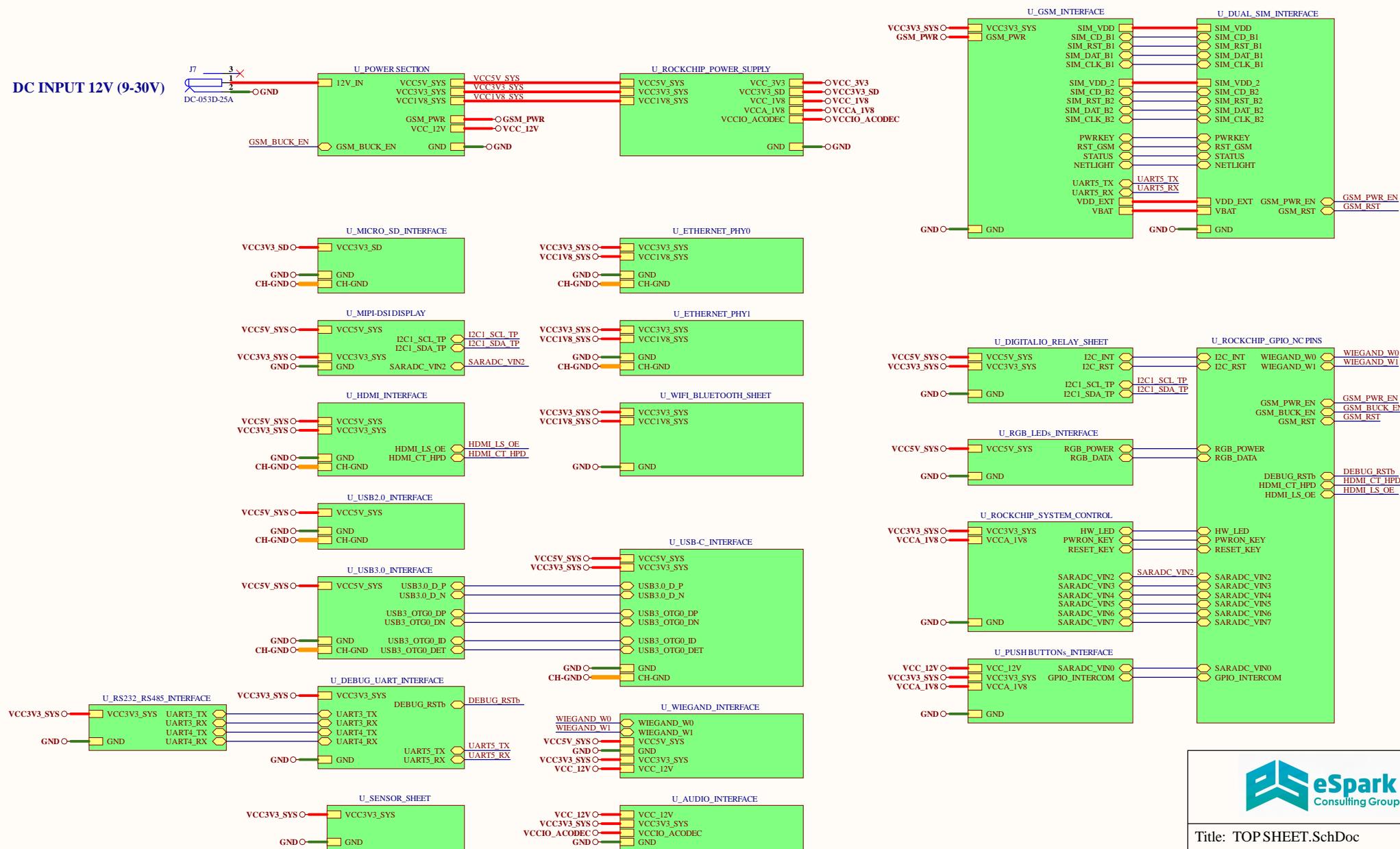


TOP SHEET

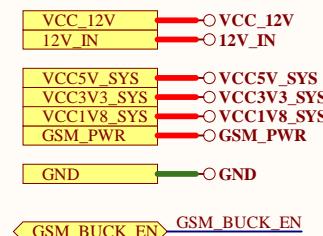
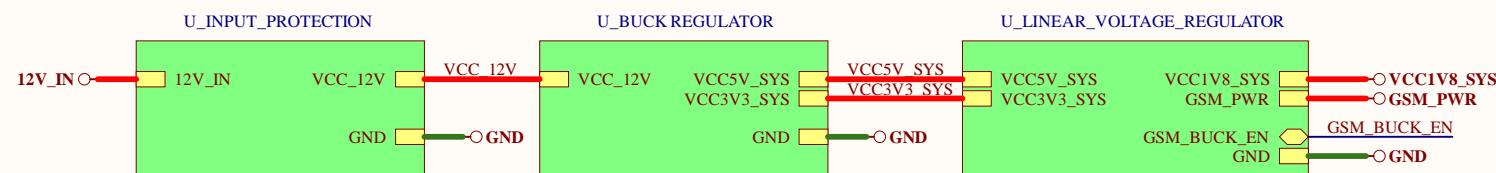


Title: TOP SHEET.SchDoc

File: Carrier-Board-v1.0.PjrPcb

Date: 10/05/2024	Page Num: 1
Drawn By: Huzaifa Ali	Page Total: 27

POWER SECTION



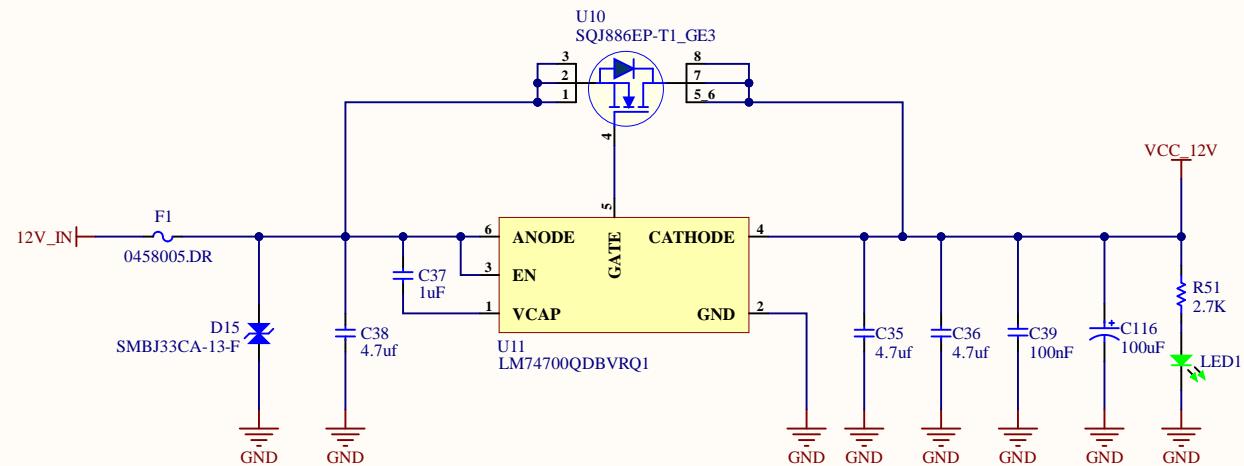
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File: Carrier-Board-v1.0.PrjPcb

Date: 10/05/2024 Page Num: 2

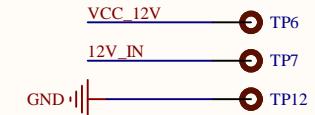
Drawn By: Huzaifa Ali Page Total: 27

INPUT PROTECTION CIRCUIT



REVERSE POLARITY PROTECTION

TEST POINTs

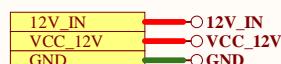


Title: INPUT_PROTECTION.SchDoc

File: Carrier-Board-v1.0.PrjPcb

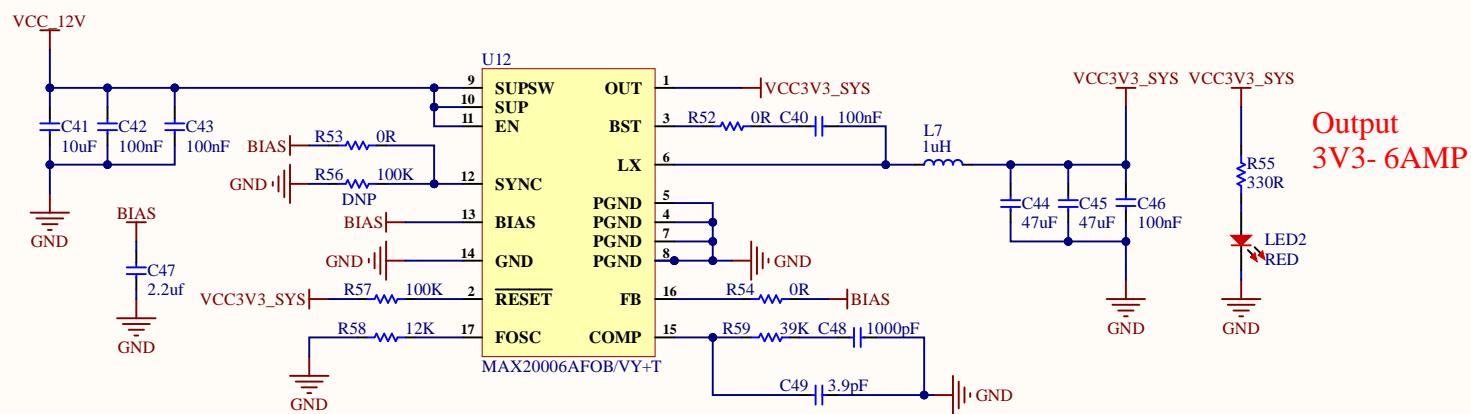
Date: 10/05/2024 Page Num: 3

Drawn By: Huzaifa Ali Page Total: 27



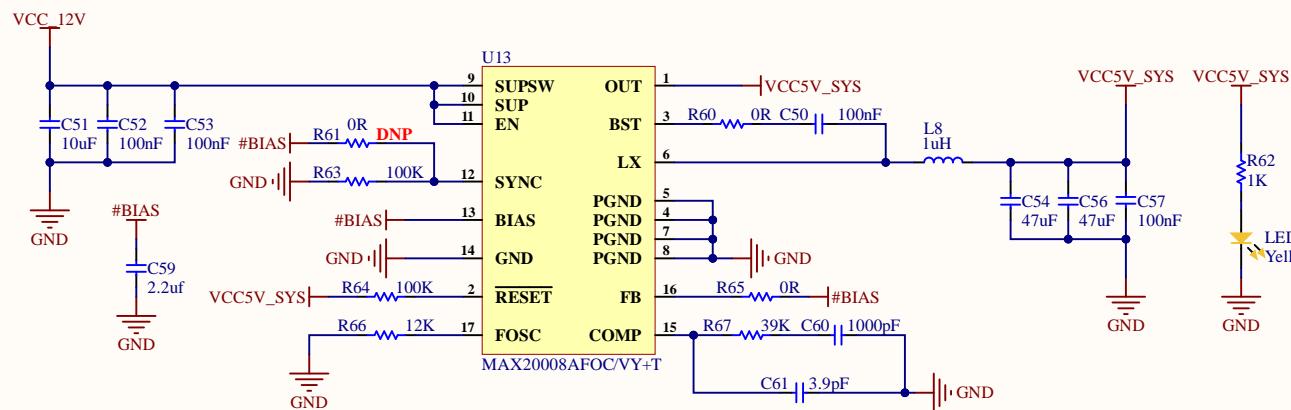
BUCK REGULATOR

A



Output
3V3- 6AMP

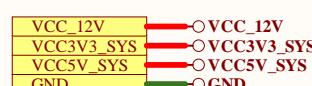
B



Output
5V- 8AMP

TEST POINTS

- VCC5V_SYS** → TP8
- VCC3V3_SYS** → TP9



Title: BUCK REGULATOR.SchDoc

File: Carrier-Board-v1.0.PrjPcb

Date: 10/05/2024 Page Num: 4

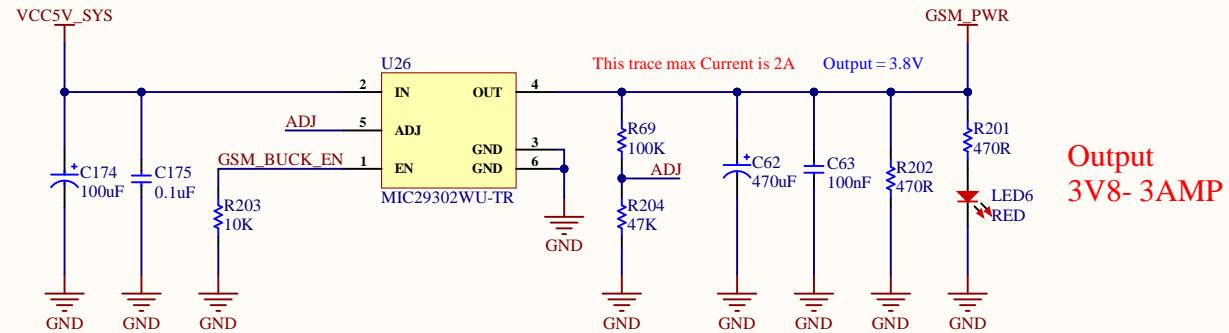
Drawn By: Huzaifa Ali Page Total: 27

LINEAR_VOLTAGE_REGULATOR

A

A

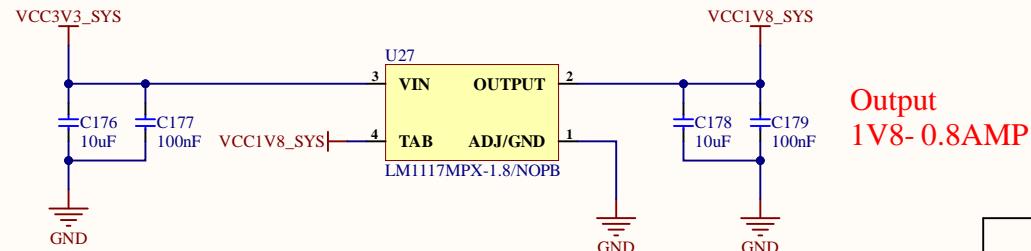
LDO FOR GSM POWER



B

B

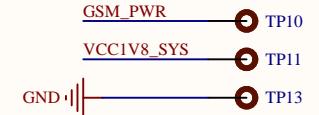
1V8 LDO



C

C

TEST POINTs



D

D



Title: LINEAR VOLTAGE REG.SchDoc

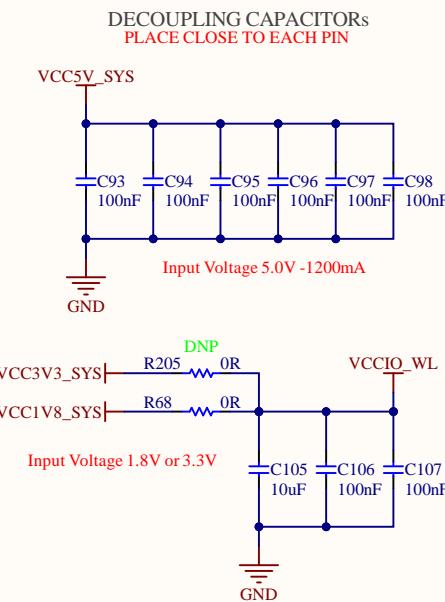
File: Carrier-Board-v1.0.PrjPcb

Date: 24/05/2024 Page Num: 5

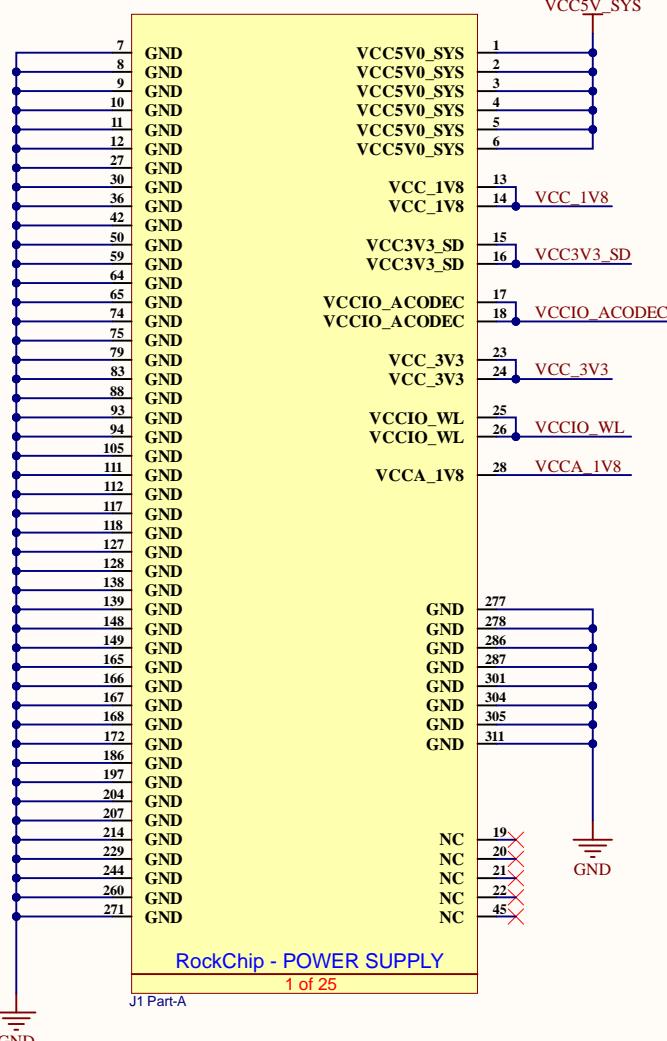
Drawn By: Huzaifa Ali Page Total: 27

ROCKCHIP POWER SUPPLY

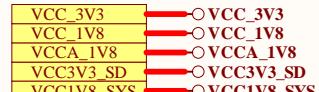
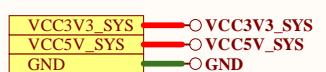
A



B



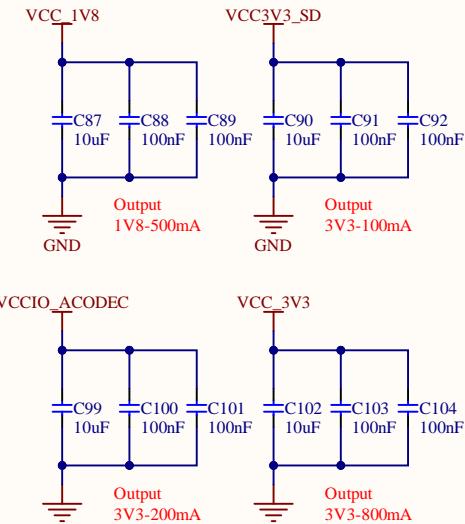
C



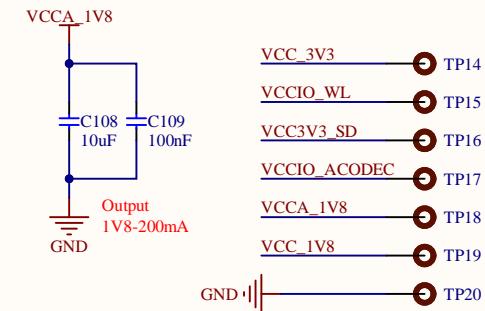
VCCIO_ACODEC —○— VCCIO_ACODEC

D

DECOUPLING CAPACITORS
PLACE CLOSE TO EACH PIN



TEST POINTs



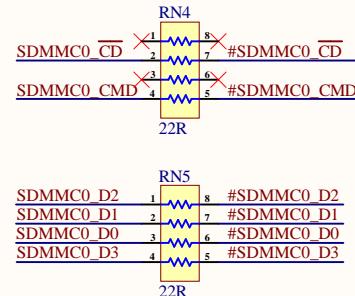
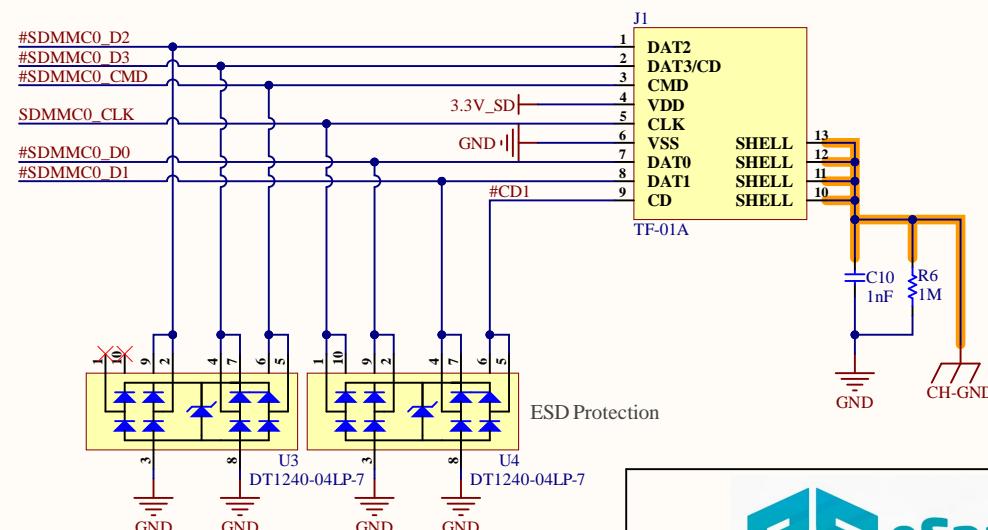
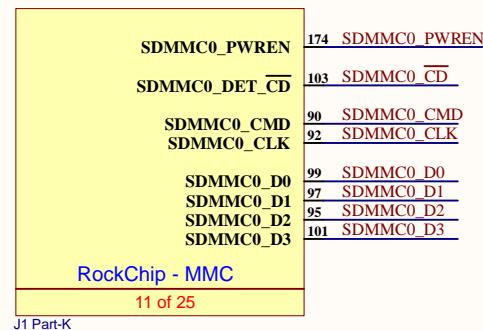
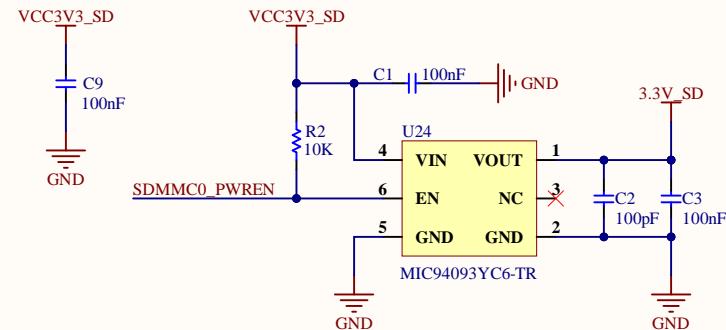
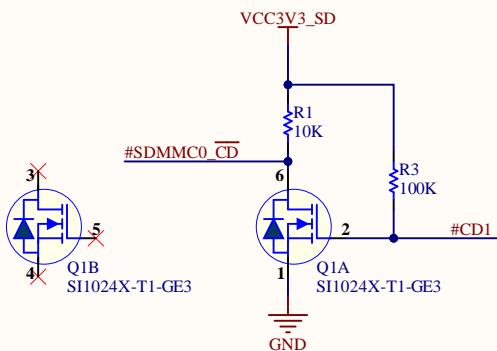
Title: ROCKCHIP_PWR_SUPPLY.SchDoc

File: Carrier-Board-v1.0.PrjPcb

Date: 10/05/2024 Page Num: 6

Drawn By: Huzaifa Ali Page Total: 27

MICRO SD CARD INTERFACE



VCC3V3_SD GND CH-GND



Title: MICRO_SD_INTERFACE.SchDoc

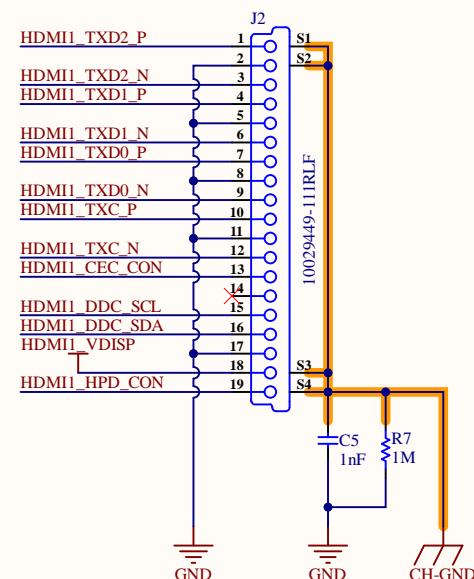
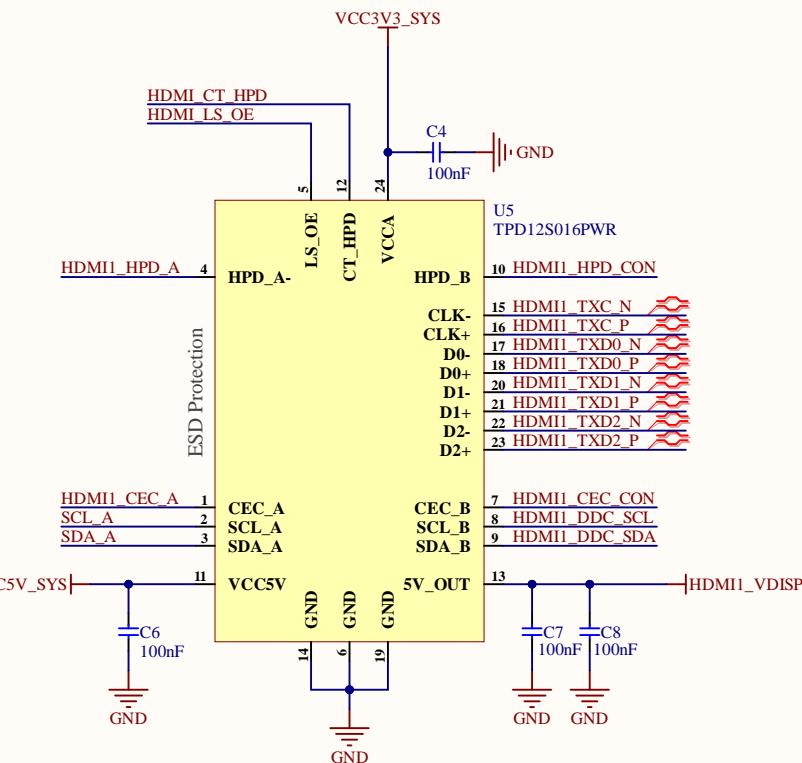
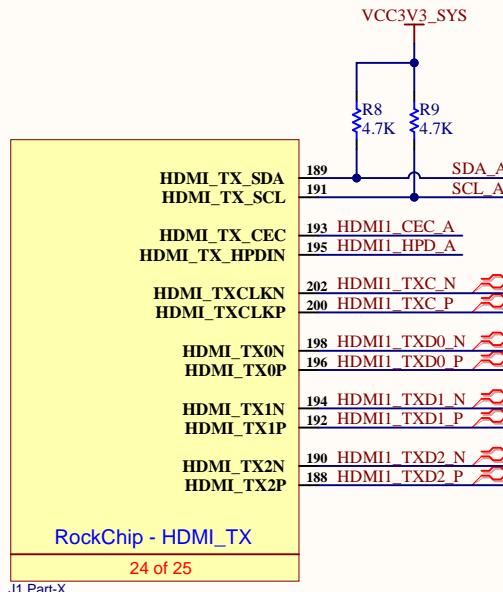
File: Carrier-Board-v1.0.PrjPcb

Date: 10/05/2024 Page Num: 7

Drawn By: Huzaifa Ali Page Total: 27

HDMI INTERFACE

A



TEST POINTs

- HDMI LS OE → TP1
- HDMI CT_HPD → TP2
- HDMI1_VDISP → TP3

HDMI_CT_HPD → HDMI_CT_HPD
HDMI_LS_OE → HDMI_LS_OE

VCC3V3_SYS → VCC3V3_SYS
VCC5V_SYS → VCC5V_SYS
GND → GND
CH-GND → CH-GND



Title: HDMI_INTERFACE.SchDoc

File: Carrier-Board-v1.0.PrjPcb

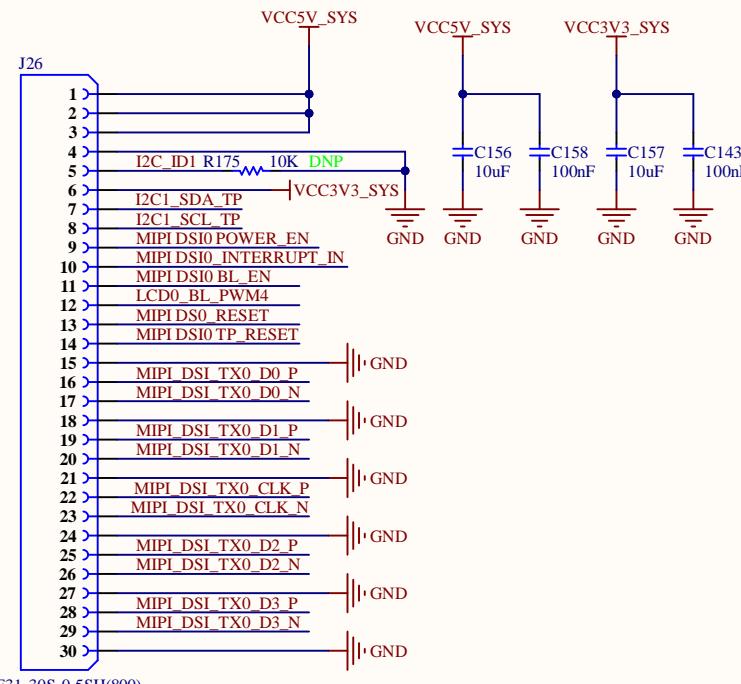
Date: 10/05/2024 Page Num: 8

Drawn By: Huzaifa Ali Page Total: 27

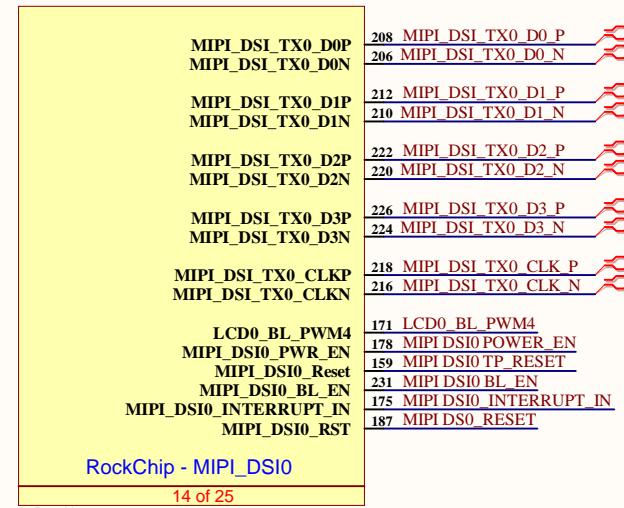
MIPI-DSI DISPLAY

A

A



FireFLY
1280x800 IPS LCD
DM-M10R800 V2



SARADC_VIN2_LCD_ID R116 0R I2C_ID1

B

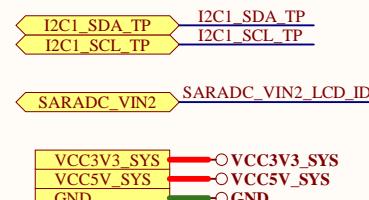
B

C

C

D

D



Title: MIPI-DSI DISPLAY.SchDoc

File: Carrier-Board-v1.0.PrjPcb

Date: 10/05/2024 Page Num: 9

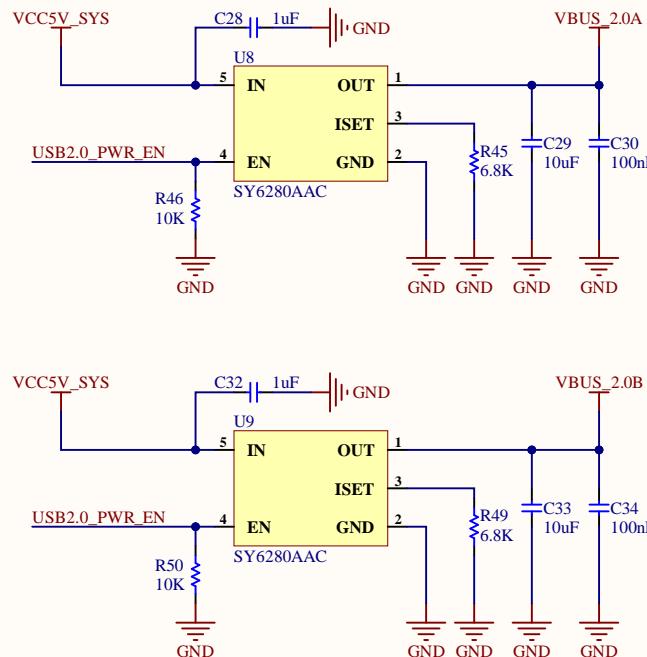
Drawn By: Huzaifa Ali Page Total: 27

USB2.0 INTERFACE

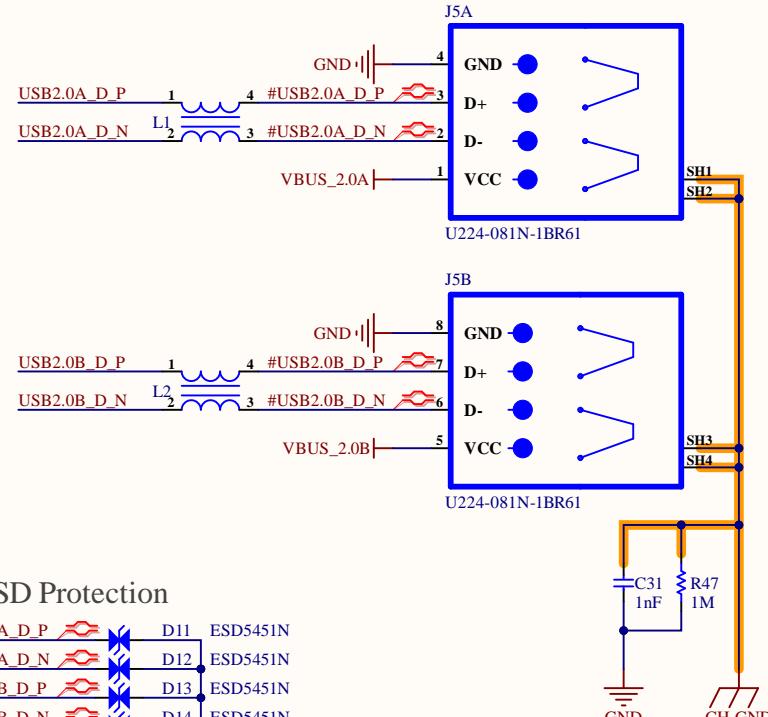
A



B



C



Title: USB2.0_INTERFACE.SchDoc

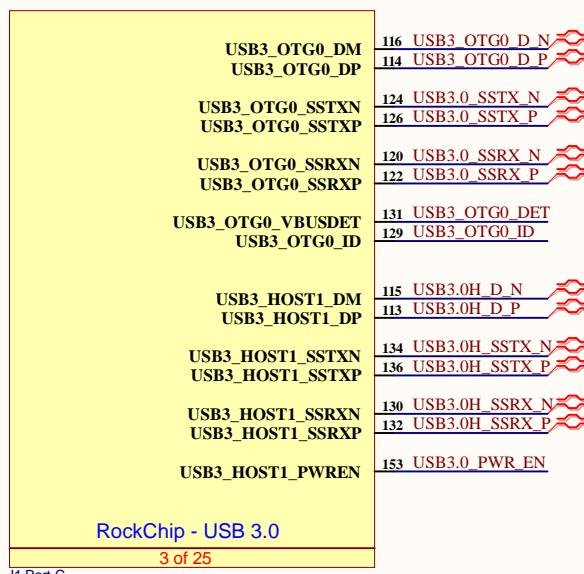
File: Carrier-Board-v1.0.PrjPcb

Date: 20/05/2024 Page Num: 10

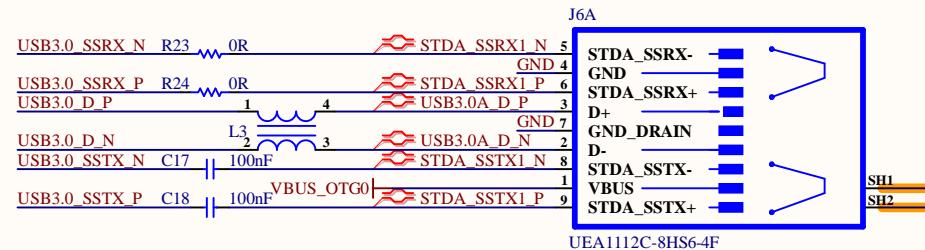
Drawn By: Huzaifa Ali Page Total: 27

USB3.0 INTERFACE

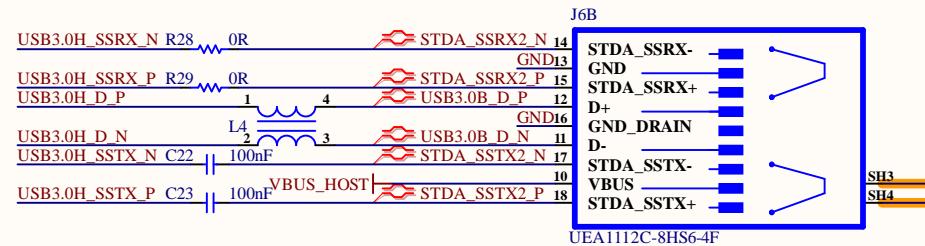
A



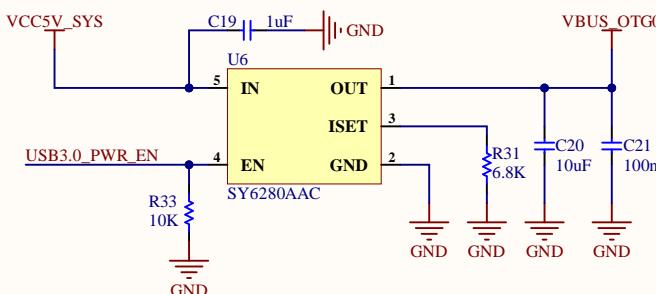
B



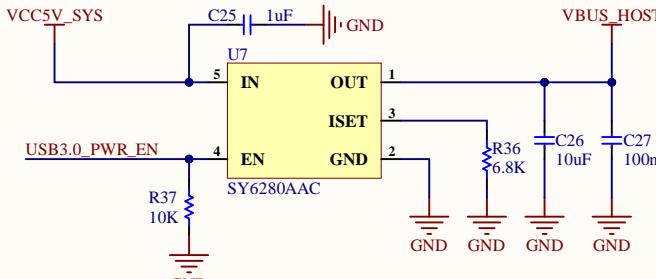
A



B

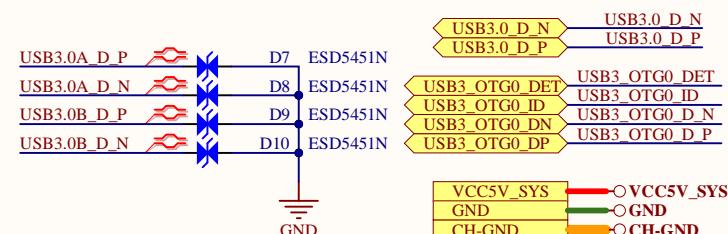
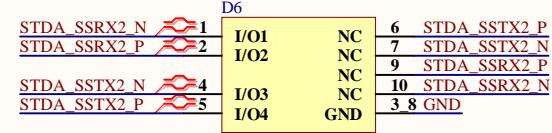
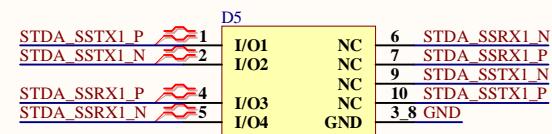


C



D

ESD Protection



TEST POINTs

- TP4: VBUS_OTG0
- TP5: VBUS_HOST



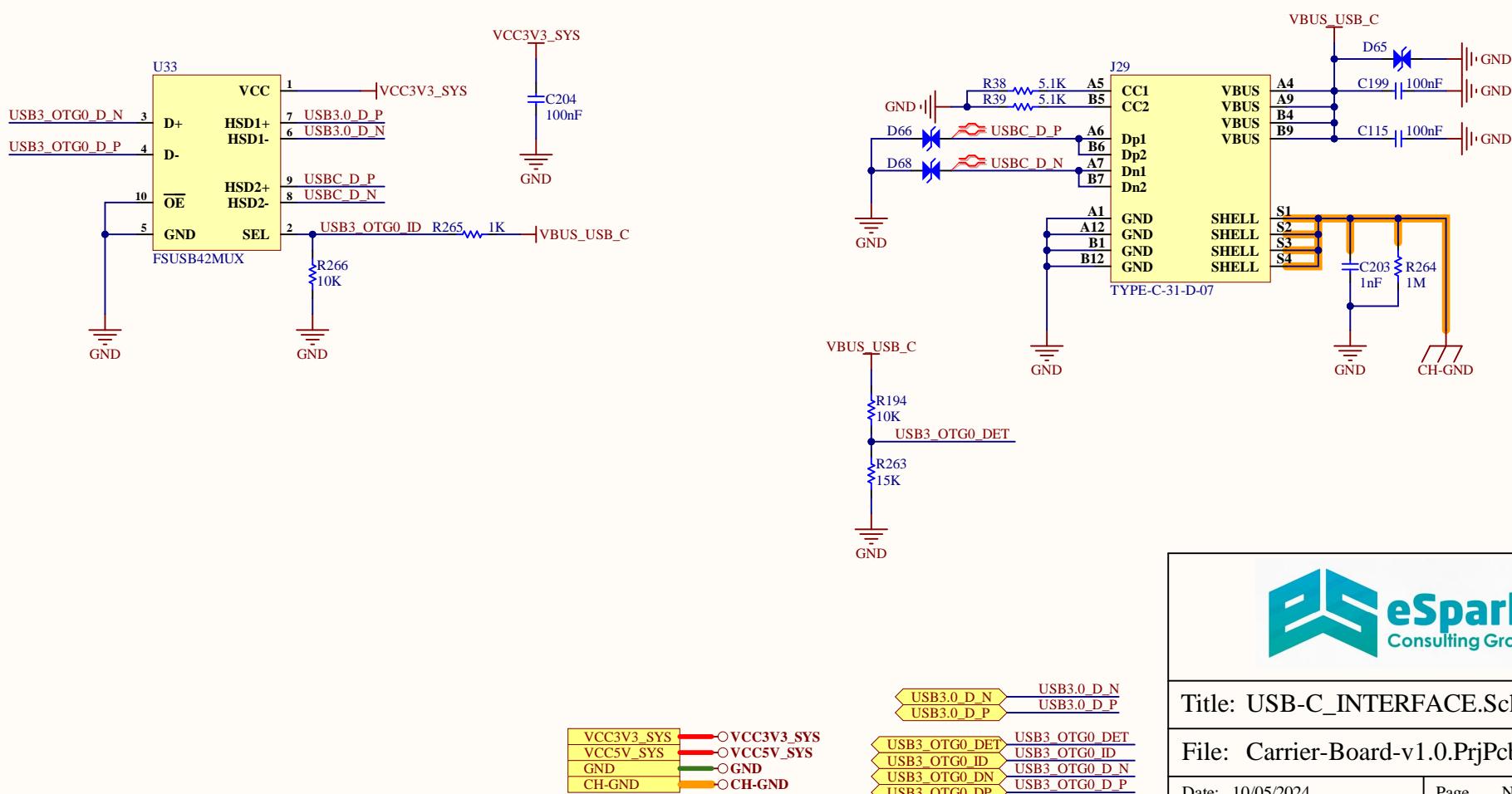
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File: Carrier-Board-v1.0.PrjPcb

Date: 20/05/2024 Page Num: 11

Drawn By: Huzaifa Ali Page Total: 27

USB-C_INTERFACE



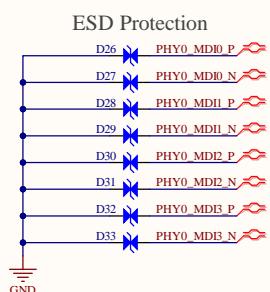
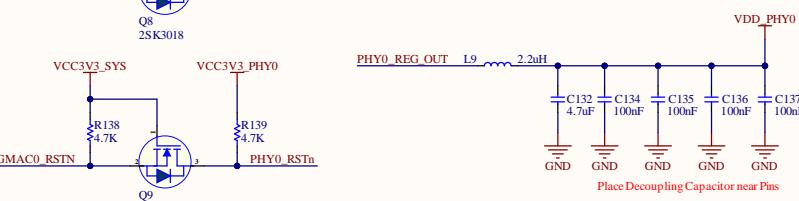
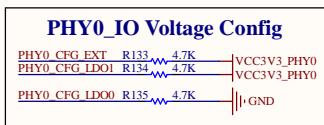
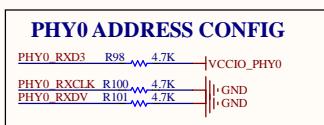
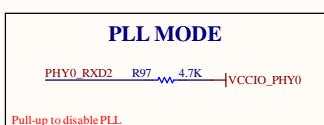
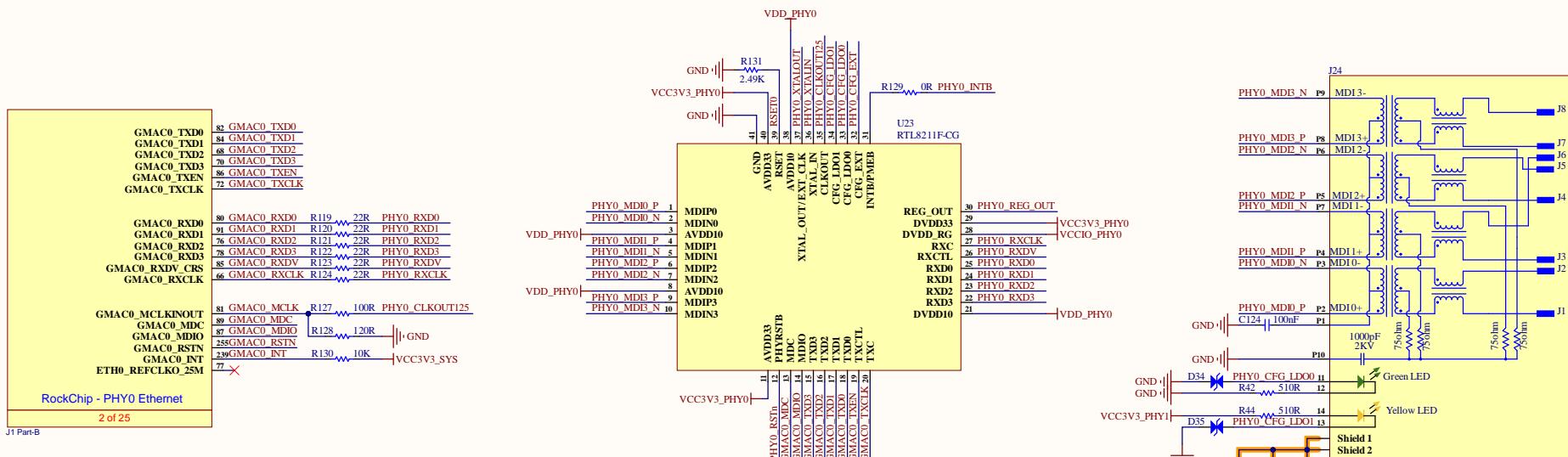
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File: Carrier-Board-v1.0.PrjPcb

Date: 10/05/2024 Page Num: 12

Drawn By: Huzaifa Ali Page Total: 27

ETHERNET PHY0 INTERFACE



Title: ETHERNET PHY0 SchDoc

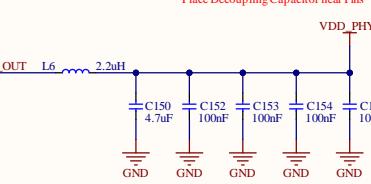
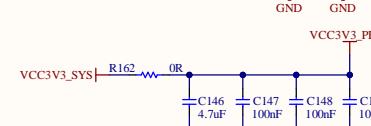
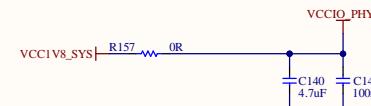
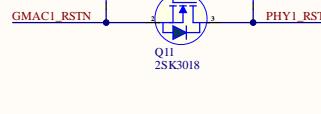
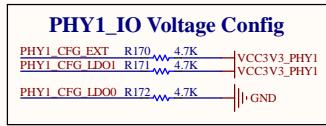
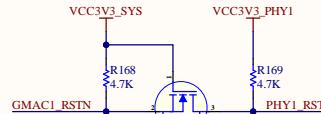
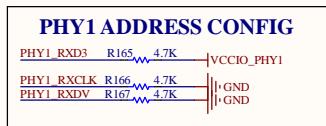
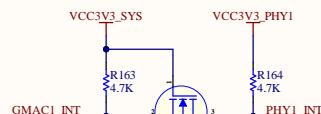
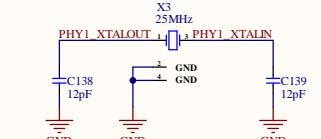
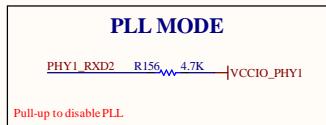
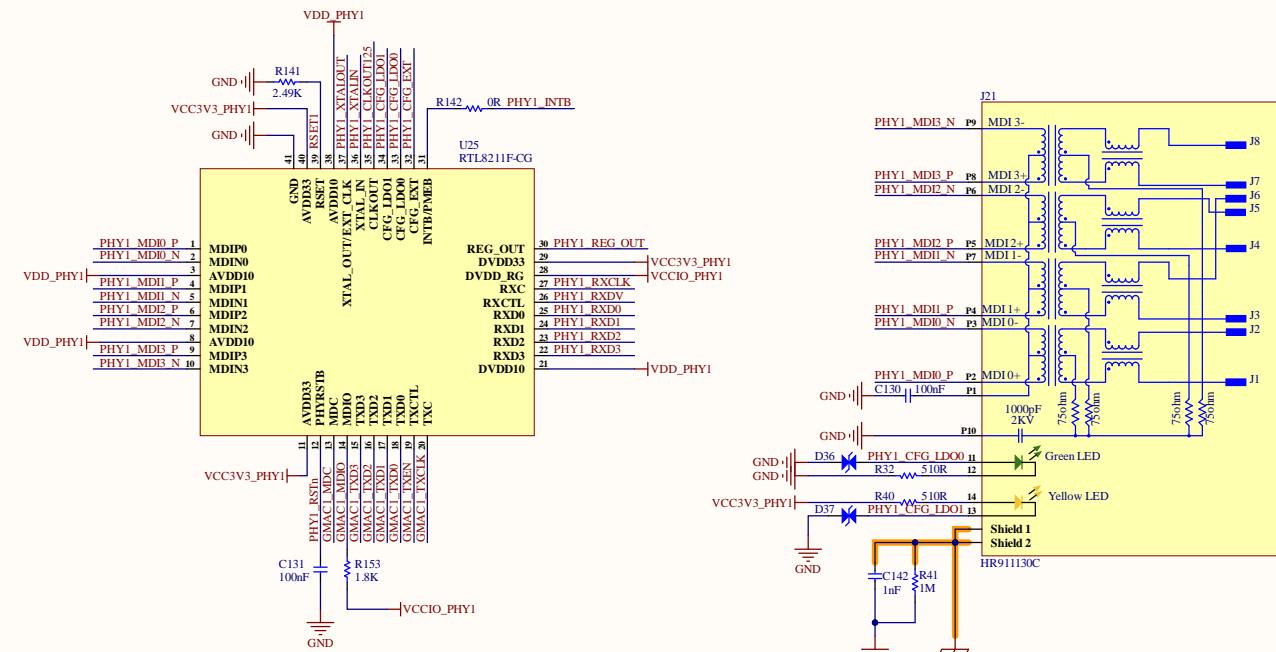
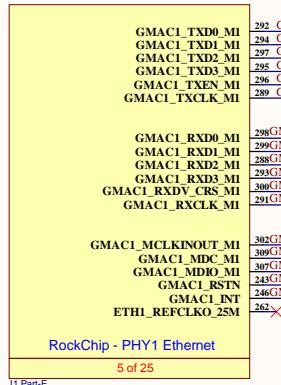
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Date: 24/05/2024 Page Num: 1

Drawn By: Huzaifa Ali Page Total: 2

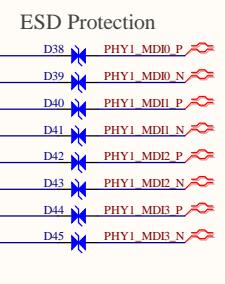
6

ETHERNET_PHY1_INTERFACE



Place Decoupling Capacitor near Pins

Place Decoupling Capacitor near Pins

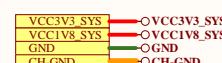


Title: ETHERNET_PHY1.SchDoc

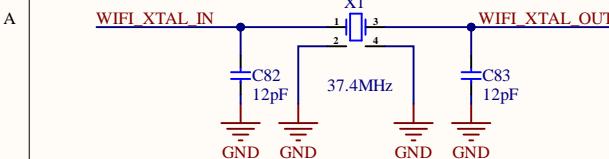
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Date: 10/05/2024 Page Num: 14

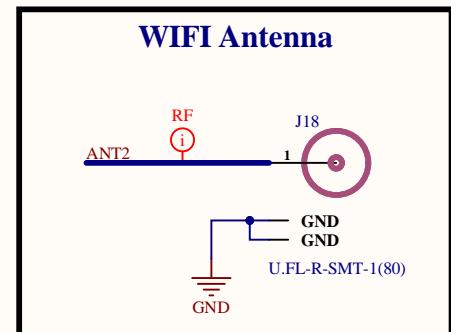
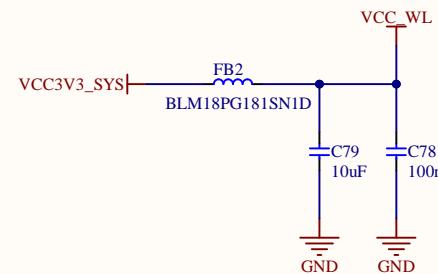
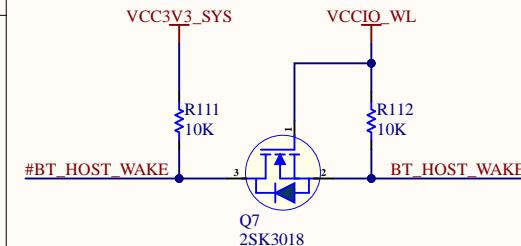
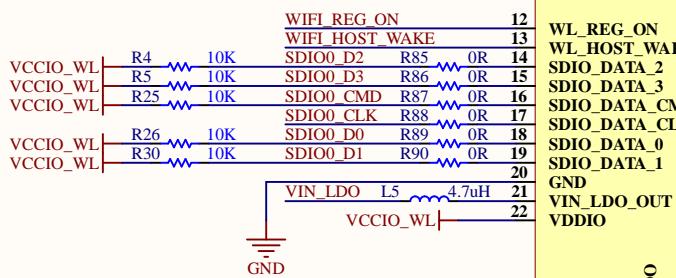
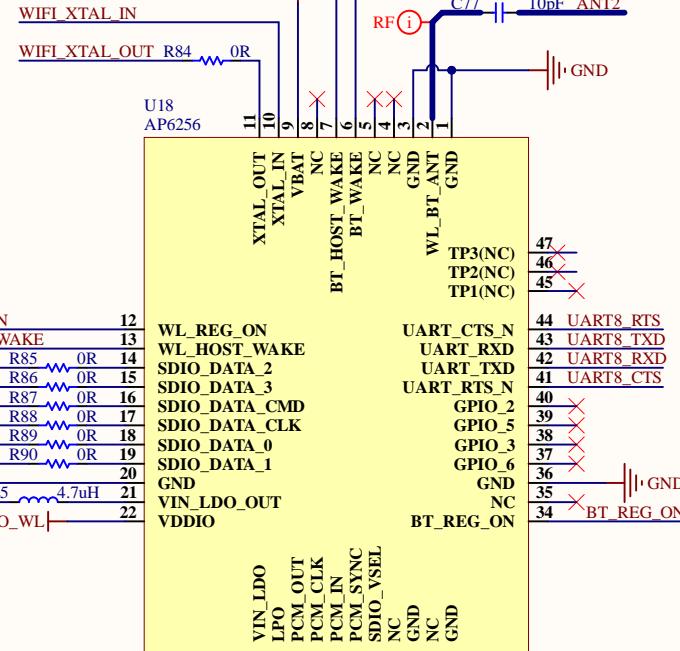
Drawn By: Huzaifa Ali Page Total: 27



WIFI_BLUETOOTH_INTERFACE



Dual Band WiFi



SDMMC2_D0_M0 279
 SDMMC2_D1_M0 281
 SDMMC2_D2_M0 282
 SDMMC2_D3_M0 284
 SDMMC2_CMD_M0 283
 SDMMC2_CLK_M0 280

WIFI_HOST_WAKE 290
 WIFI_REG_ON 285
 WIFI_32KHZ_OUT 275

UART8_CTS 67
 UART8_RXD 69
 UART8_TXD 73
 UART8_RTS 71
 #BT_WAKE 269
 #BT_HOST_WAKE 248
 BT_REG_ON_H 250

RockChip - WIFI/BT-SDIO
 23 of 25
 J1 Part-W

VCC3V3_SYS → VCC3V3_SYS
 VCC1V8_SYS → VCC1V8_SYS
 GND → GND



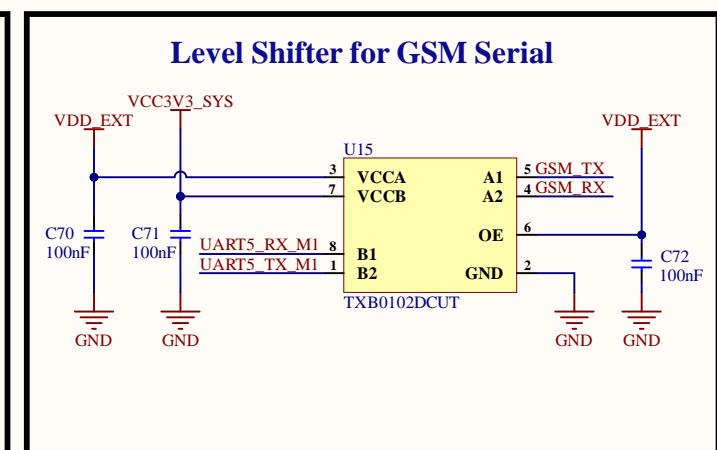
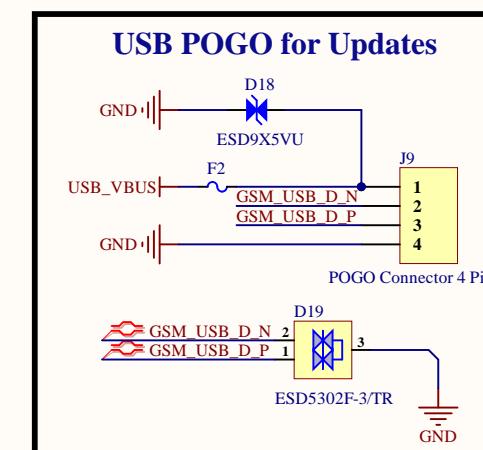
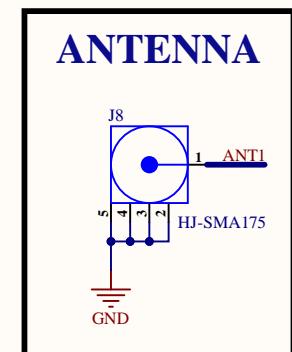
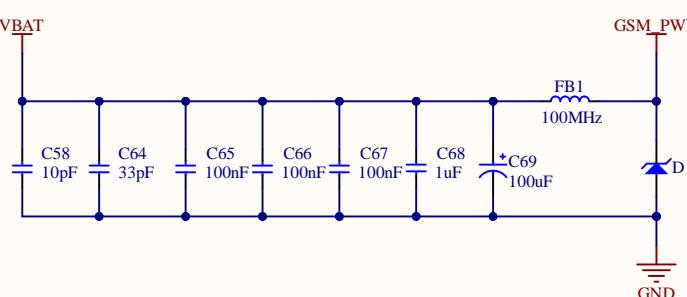
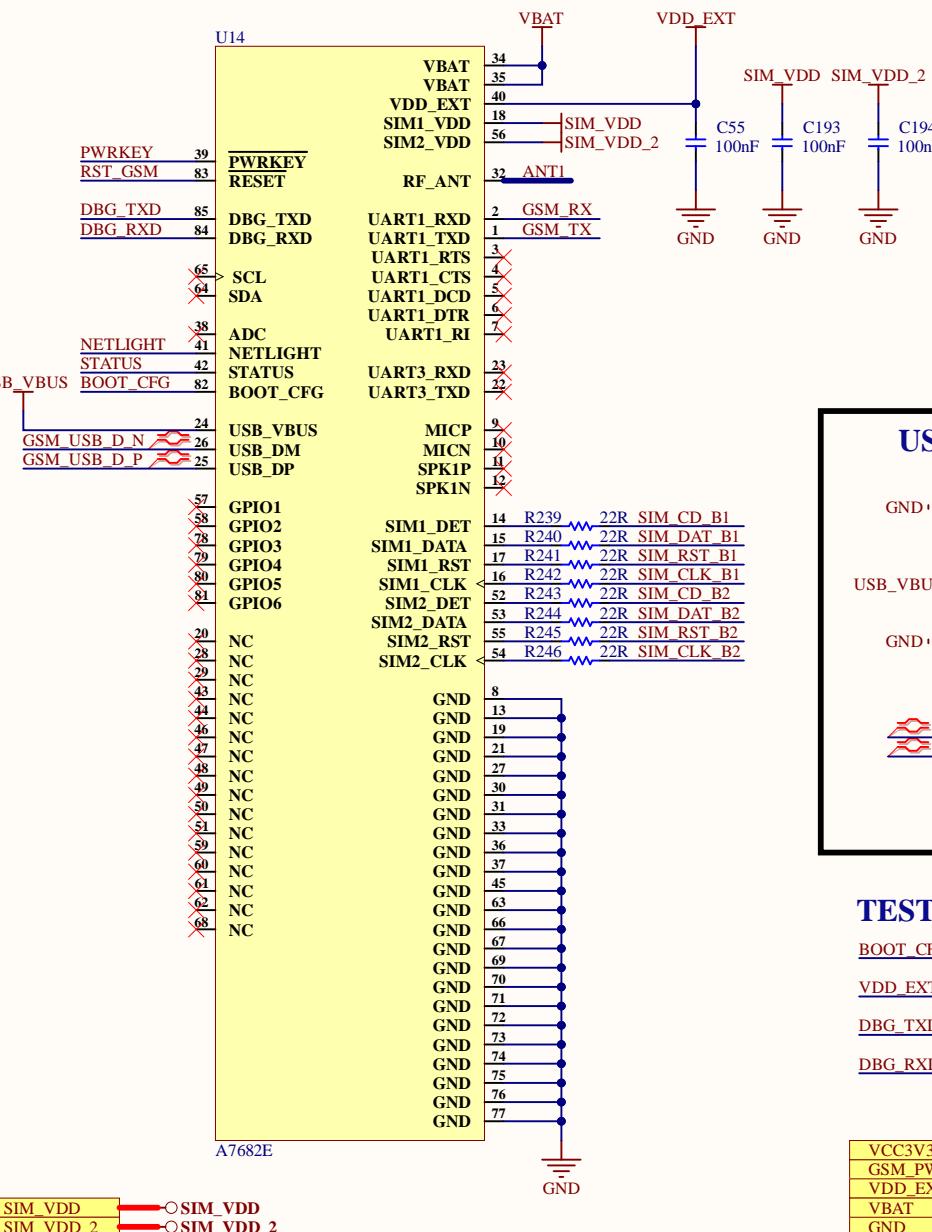
Title: WIFI_BLUETOOTH_SHEET.SchDoc

File: Carrier-Board-v1.0.PrjPcb

Date: 21/05/2024 Page Num: 15

Drawn By: Huzaifa Ali Page Total: 27

GSM_INTERFACE



TEST POINTs

BOOT_CFG — TP21

VDD_EXT — TP22

DBG_TXD — TP23

DBG_RXD — TP24

VCC3V3_SYS — O VCC3V3_SYS
GSM_PWR — O GSM_PWR
VDD_EXT — O VDD_EXT
VBAT — O VBAT
GND — O GND

UART5_RX_M1
UART5_TX_M1

NETLIGHT
STATUS

RST_GSM
PWRKEY

SIM_CLK_B1
SIM_DAT_B1

SIM_RST_B1
SIM_CD_B1

SIM_CLK_B2
SIM_DAT_B2

SIM_RST_B2
SIM_CD_B2



Title: GSM_INTERFACE.SchDoc

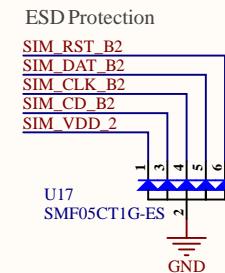
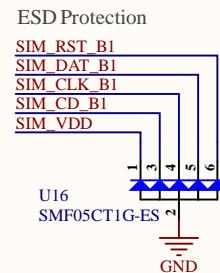
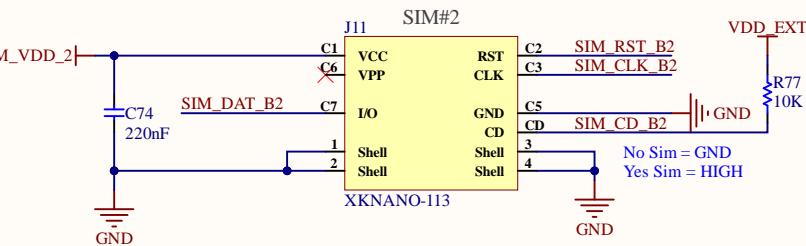
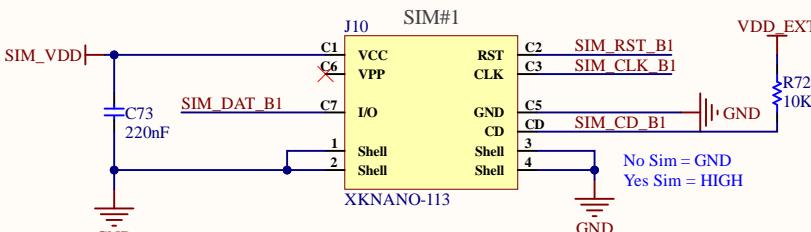
File: Carrier-Board-v1.0.PrjPcb

Date: 20/05/2024 Page Num: 16

Drawn By: Huzaifa Ali Page Total: 27

DUAL_SIM_INTERFACE

DUALSIM WITH MULTIPLEXER



SIM Card Design Guide

SIM card signal could be interfered by some high frequency signal, it is strongly recommended to follow these guidelines while designing:

SIM card holder should be far away from main antenna

SIM traces should keep away from RF lines, VBAT and high-speed signal lines

The traces should be as short as possible

Keep SIM card holder's GND connect to main ground directly

Shielding the SIM card signal by ground well

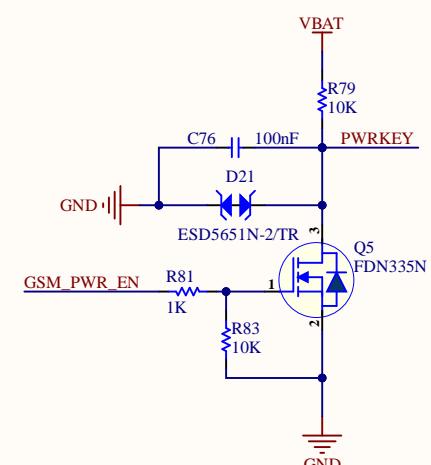
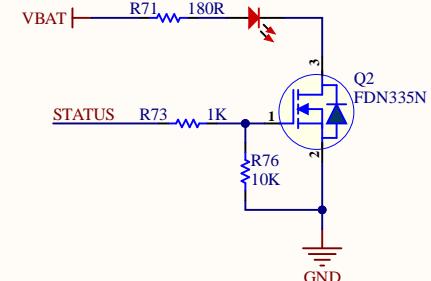
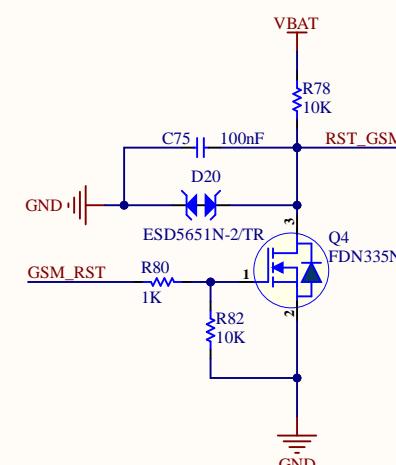
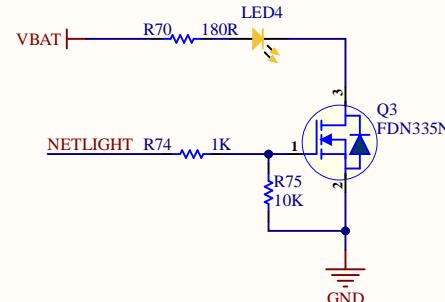
Recommended to place a 100nF capacitor on SIM_VDD line and keep close to the SIM cardholder

Add some TVS which parasitic capacitance should not exceed 50pF

Add 22Ω resistor to (SIM_RST/SIM_CLK/SIM_DATA) signal could enhance ESD protection

Mount 22pF capacitor to (SIM_RST/SIM_CLK/SIM_DATA) signal if having RF signal interference

STATUS LEDs



Title: DUAL_SIM_INTERFACE.SchDoc

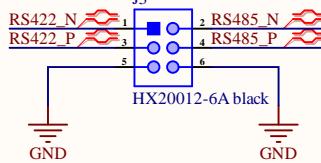
File: Carrier-Board-v1.0.PrjPcb

Date: 10/05/2024 Page Num: 17

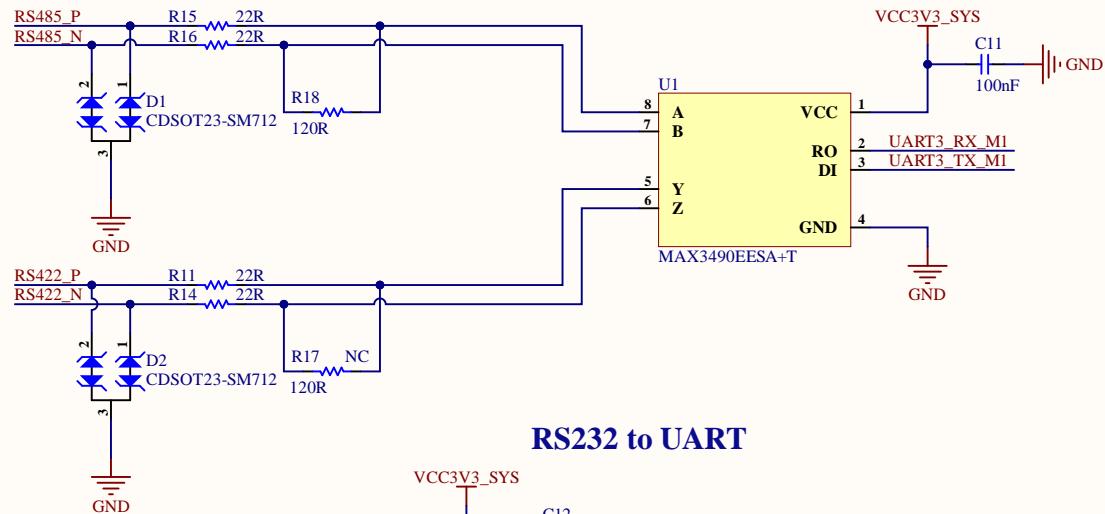
Drawn By: Huzaifa Ali Page Total: 27

RS232_RS485_INTERFACE

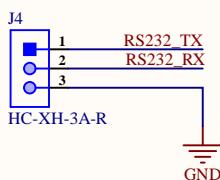
PORT for RS485



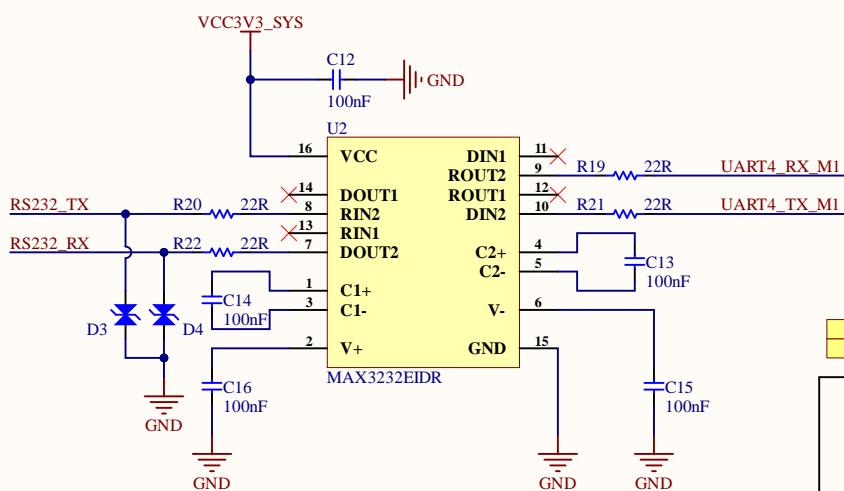
RS485 to UART



PORT for RS232



RS232 to UART



VCC3V3_SYS → VCC3V3_SYS
GND → GND



Title: RS232_RS485_INTERFACE.SchDoc

File: Carrier-Board-v1.0.PrjPcb

Date: 12/06/2024 Page Num: 18

Drawn By: Huzaifa Ali Page Total: 27

DEBUG_UART_INTERFACE

A

A

UART2_RXD_M0_DEBUG
UART2_TXD_M0_DEBUG

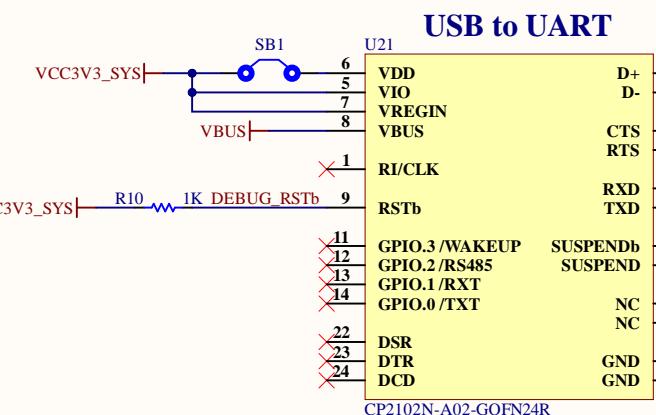
UART3_RXD_M1
UART3_TXD_M1

UART4_RXD_M1
UART4_TXD_M1

UART5_RXD_M1
UART5_TXD_M1

RockChip - UART

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B

B

UART2_RXD_M0_DEBUG
UART2_TXD_M0_DEBUG

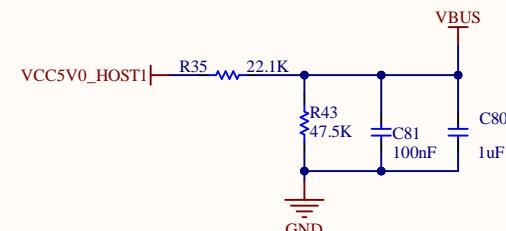
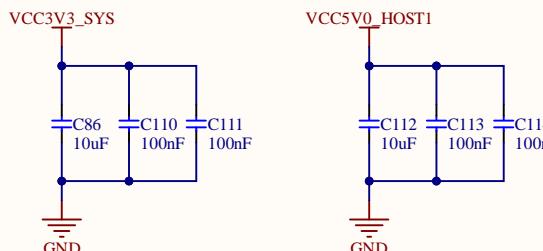
UART3_RXD_M1
UART3_TXD_M1

UART4_RXD_M1
UART4_TXD_M1

UART5_RXD_M1
UART5_TXD_M1

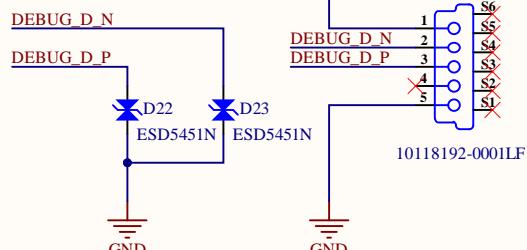
RockChip - UART

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- VCC3V3_SYS → VCC3V3_SYS, GND → GND
- DEBUG_RSTb → DEBUG_RSTb
- UART3_RX, UART3_TX → UART3_RX_M1, UART3_TX_M1
- UART4_RX, UART4_TX → UART4_RX_M1, UART4_TX_M1
- UART5_RX, UART5_TX → UART5_RX_M1, UART5_TX_M1

ESD Protection



Title: DEBUG_UART_INTERFACE.SchDoc

File: Carrier-Board-v1.0.PrjPcb

Date: 10/05/2024 Page Num: 19

Drawn By: Huzaifa Ali Page Total: 27

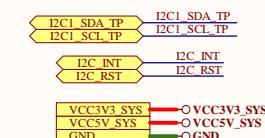
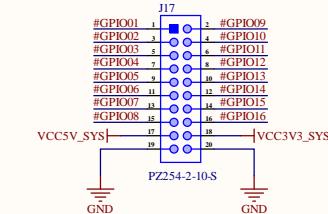
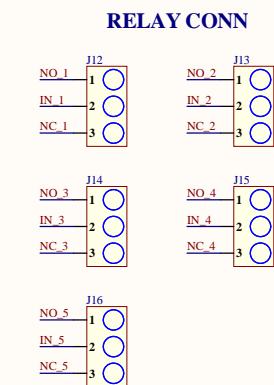
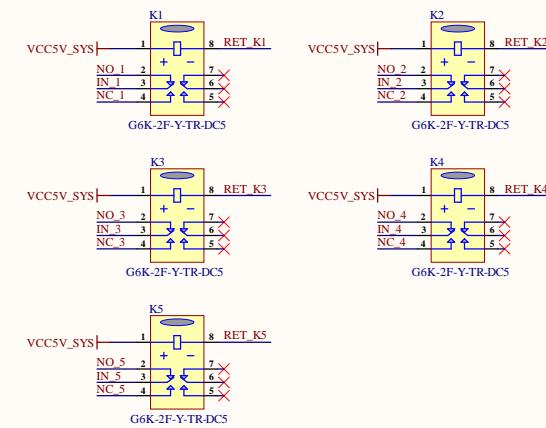
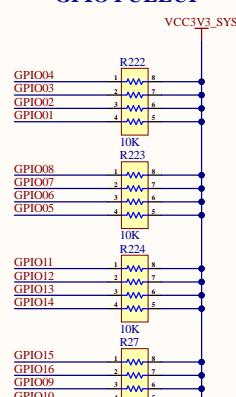
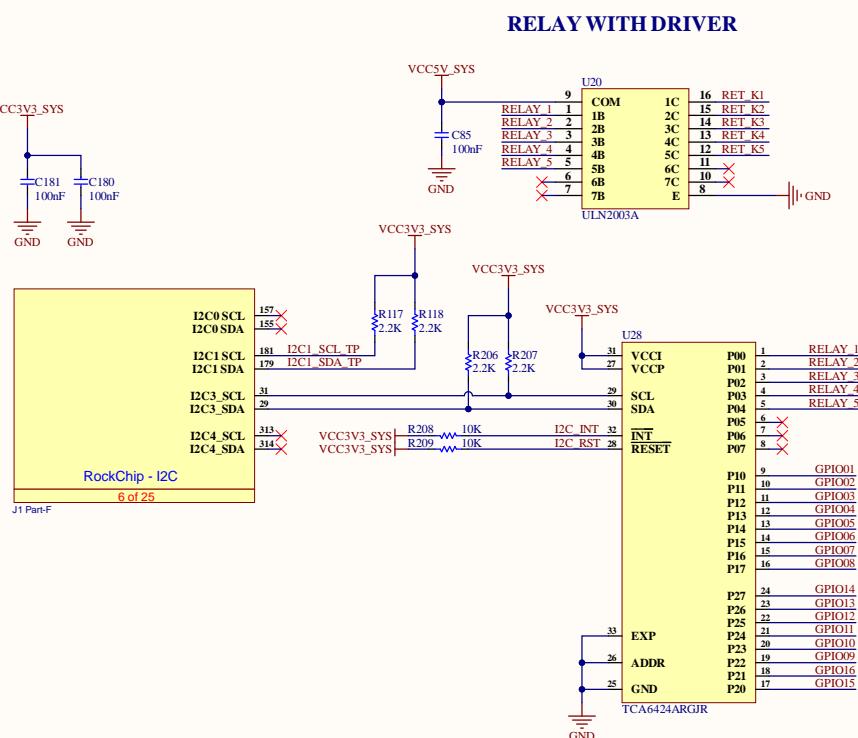
C

C

D

D

DIGITAL IOs_RELAY_INTERFACE



Title: DIGITAL IO RELAY SHEET SchDoc

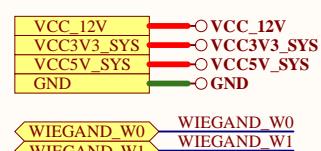
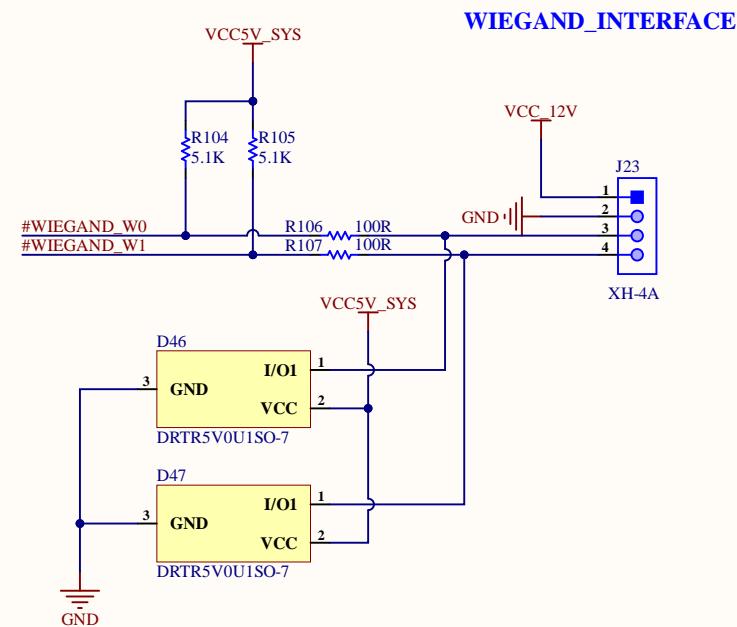
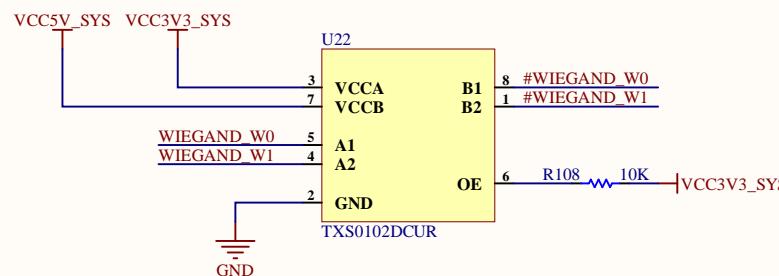
File: Carrier-Board-v1.0.PrjPcb

Date: 10/05/2024 Page Num: 20

Drawn By: Huzaifa Ali Page Total: 27

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WIEGAND_INTERFACE



Title: WIEGAND_INTERFACE.SchDoc

File: Carrier-Board-v1.0.PrjPcb

Date: 10/05/2024 Page Num: 21

Drawn By: Huzaifa Ali Page Total: 27

TEMP/HUMIDITY SENSOR_INTERFACE

A

A

B

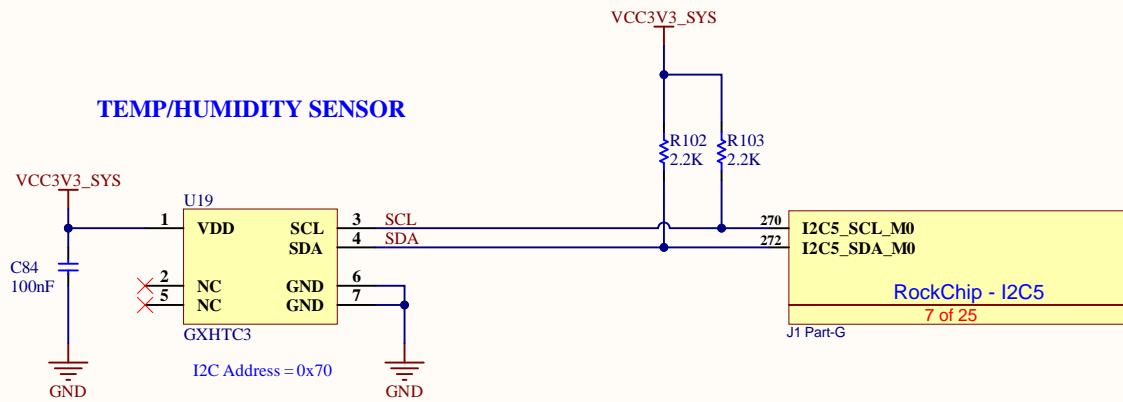
B

C

C

D

D



Title: SENSOR_SHEET.SchDoc

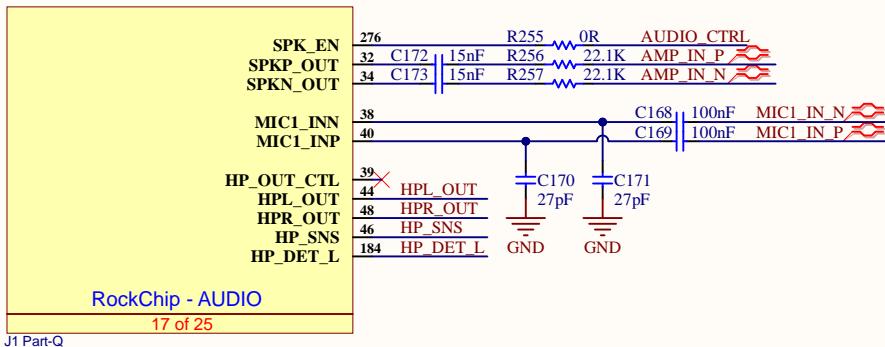
File: Carrier-Board-v1.0.PrjPcb

Date: 10/05/2024 Page Num: 22

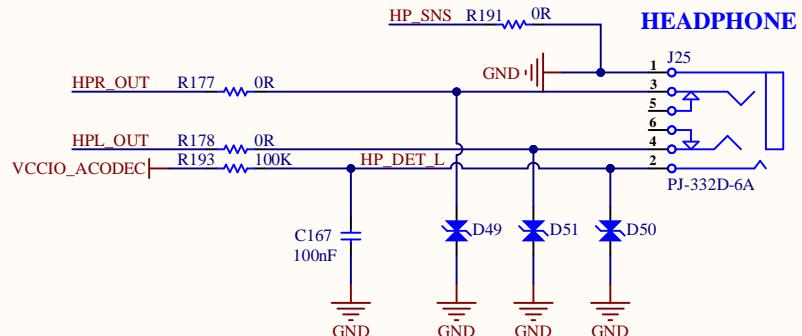
Drawn By: Huzaifa Ali Page Total: 27

AUDIO_INTERFACE

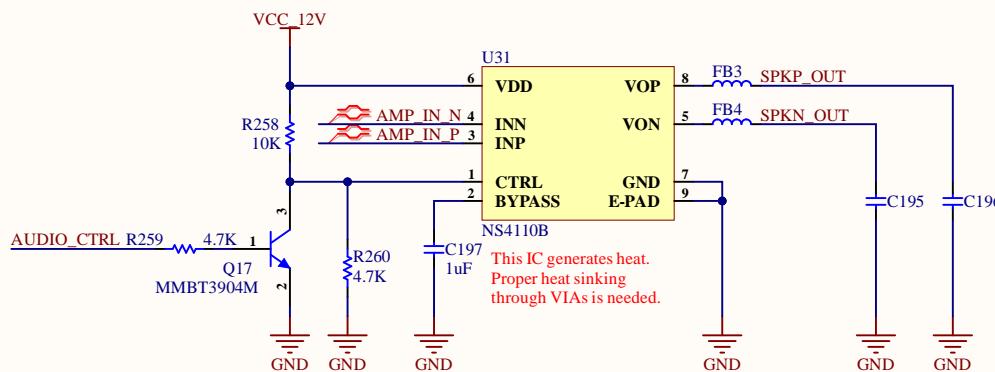
A



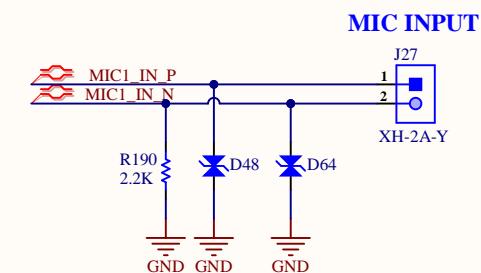
B



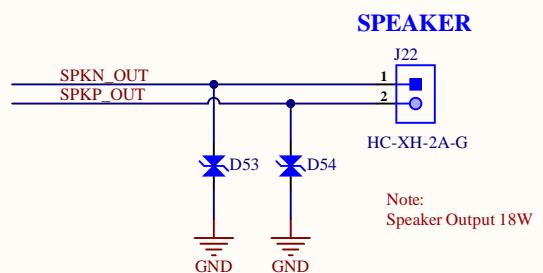
A



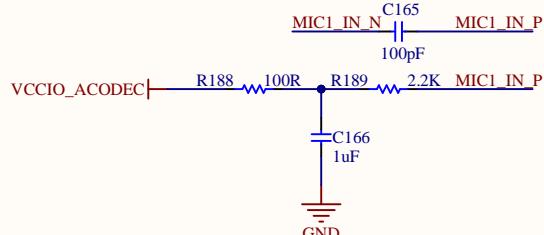
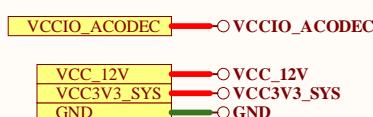
C



B



D



Title: AUDIO_INTERFACE.SchDoc

File: Carrier-Board-v1.0.PrjPcb

Date: 24/05/2024 Page Num: 23

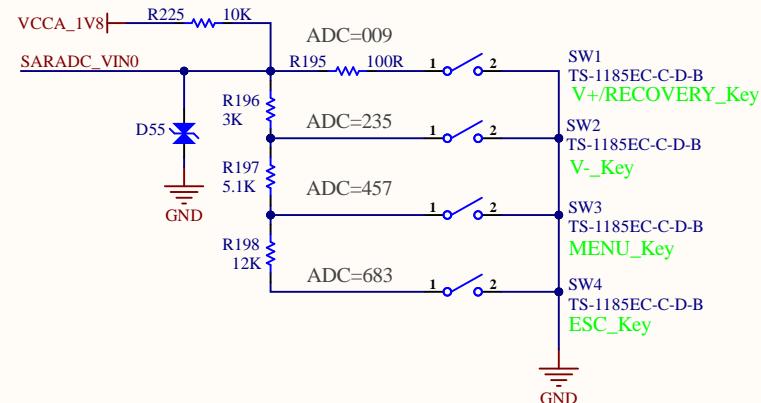
Drawn By: Huzaifa Ali Page Total: 27

PUSH BUTTON_INTERFACE

A

A

ACTION BUTTONS



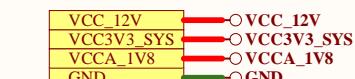
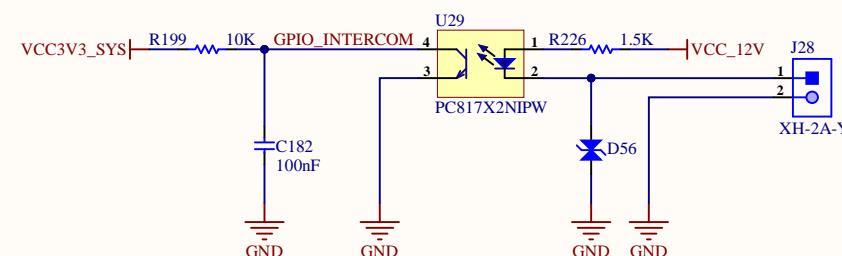
Note:

RECOVERY_Key function:
If SARADC_VIN0=0V
at after power on and reset,
then system will
enter into loader mode.

B

B

INTERCOM ACTION BUTTON



Title: PUSH BUTTONS_INTERFACE.SchDoc

File: Carrier-Board-v1.0.PrjPcb

Date: 20/05/2024 Page Num: 24

Drawn By: Huzaifa Ali Page Total: 27

RGB_LEDs_INTERFACE

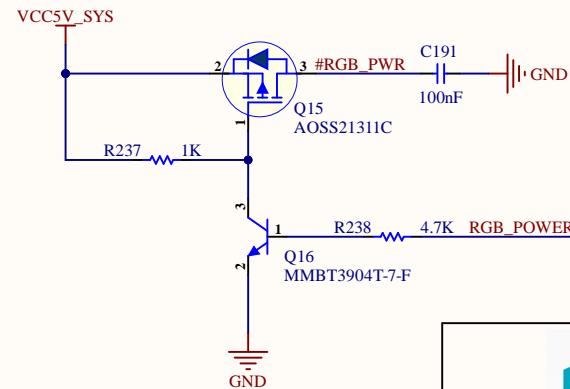
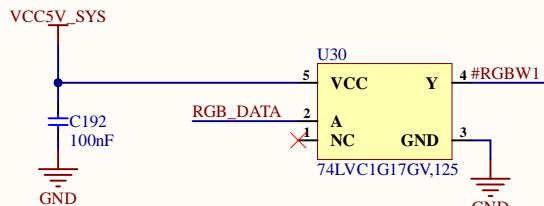
A



B



C



D

VCC5V_SYS → VCC5V_SYS
GND → GND

RGB_DATA → RGB_DATA
RGB_POWER → RGB_POWER



Title: RGB_LEDs_INTERFACE.SchDoc

File: Carrier-Board-v1.0.PrjPcb

Date: 10/05/2024 Page Num: 25

Drawn By: Huzaifa Ali Page Total: 27

ROCKCHIP_GPIOs_NC_PINS

A

PCIE20_REFCLKP
PCIE20_REFCLKN
PCIE30_REFCLKP_IN
PCIE30_REFCLKN_IN

PCIE30_TX0P
PCIE30_TX0N
PCIE30_TX1P
PCIE30_TX1N
PCIE30_RX0P
PCIE30_RX0N
PCIE30_RX1P
PCIE30_RX1N

PCIE30_PERSTn_M0
PCIE30_PERSTn_M1
PCIE_CLK_EN
PCIE_PWR_EN

PCIE30_CLKREQN_M1
PCIE30_WAKEn_M1

RockChip - PCI-EXPRESS

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J1 Part-R

MIPI_DSI_TX1_D0P
MIPI_DSI_TX1_D0N

MIPI_DSI_TX1_D1P
MIPI_DSI_TX1_D1N

MIPI_DSI_TX1_D2P
MIPI_DSI_TX1_D2N

MIPI_DSI_TX1_D3P
MIPI_DSI_TX1_D3N

MIPI_DSI_TX1_CLKP
MIPI_DSI_TX1_CLKN

MIPI_DSI1_BL_EN
MIPI_DSI1_RESET

MIPI_DSI1_INTERRUPT_IN

RockChip - MIPI_DSI1

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J1 Part-O

SATA2_TXP
SATA2_TXN

SATA2_RXP
SATA2_RXN

SATA2_ACT_LED

RockChip - SATA

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J1 Part-S

MIPI_CSI_RX_D0N
MIPI_CSI_RX_D0P
MIPI_CSI_RX_D1N
MIPI_CSI_RX_D1P
MIPI_CSI_RX_D2N
MIPI_CSI_RX_D2P
MIPI_CSI_RX_D3N
MIPI_CSI_RX_D3P

MIPI_CSI_RX_CLK0N
MIPI_CSI_RX_CLK0P
MIPI_CSI_RX_CLK1N
MIPI_CSI_RX_CLK1P

RockChip - MIPI_CSI

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J1 Part-P

EDP_BL
EDP_VCC_EN
EDP_BL_EN

EDP_TX_D0P
EDP_TX_D0N
EDP_TX_D1P
EDP_TX_D1N
EDP_TX_D2N
EDP_TX_D2P
EDP_TX_D3N
EDP_TX_D3P

EDP_TX_AUXN
EDP_TX_AUXP

RockChip - LCM_eDP

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J1 Part-T

BAT_ALRT
HW_LED
PWRON_KEY
nPOR_SYS

EXT_EN
4G_PWR_EN

268 GPIO_INTERCOM
177 HW_LED
43 PWRON_KEY
49 RESET_KEY

8 of 25

J1 Part-H

I2C_INT
I2C_RST

SARADC_VIN0_KEY/RECOVERY
SARADC_VIN3_HW_ID

SARADC_VIN2
SARADC_VIN4
SARADC_VIN5
SARADC_VIN6
SARADC_VIN7

RockChip - SARADC

25 of 25

J1 Part-Y

FSPI_CS
FSPI_CLK

FSPI_D0
FSPI_D1
FSPI_D2
FSPI_D3

RockChip - FSPI

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J1 Part-I

CAN1_RX_M1
CAN1_TX_M1
CAN2_RX_M0
CAN2_TX_M0

RockChip - CAN

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J1 Part-V

SARADC_VIN0
SARADC_VIN2
SARADC_VIN3
SARADC_VIN4
SARADC_VIN5
SARADC_VIN6
SARADC_VIN7

RESET_KEY
PWRON_KEY
HW_LED

GPIO_INTERCOM
DEBUG_RSTb

GSM_BUCK_EN
GSM_RST
GSM_PWR_EN

GSM_RST
GSM_BUCK_EN
GSM_PWR_EN

I2S3_SCLK_M0
I2S3_LRCK_M0
I2S3_SDO_M0
I2S3_SD1_M0

252 GSM_RST
253 GSM_PWR_EN
254 GSM_BUCK_EN
256 DEBUG_RSTb

RockChip - I2S

7 of 25

J1 Part-L

SPI1_MOSI_M1
SPI1_CS_M1

274 I2C_INT
241 I2C_RST

RockChip - SPI

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J1 Part-U

MULTI_PHY0_REFCLKP
MULTI_PHY0_REFCLKN
MULTI_PHY1_REFCLKP
MULTI_PHY1_REFCLKN
PWMO_M0/GPIO0_B7_d
RTCIC_INT_L/GPIO0_D3_d
CIFCLK_OUT/GPIO4_C0_d

119
121
125
123
176
163
303
193
247
261
170
183

HDMI_CT_HPD
HDMI_LS_OE
RGB_DATA
RGB_POWER
WIEGAND_W0
WIEGAND_W1

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SARADC_VIN3_HW_ID C159 1nF || GND
SARADC_VIN2_LCD_ID C160 1nF || GND
SARADC_VIN0 C161 1nF || GND
SARADC_VIN4 C162 1nF || GND
SARADC_VIN5 C163 1nF || GND
SARADC_VIN6 C164 1nF || GND
SARADC_VIN7 C198 1nF || GND



Title: ROCKCHIP_GPIOs_NC_PINS.SchDoc

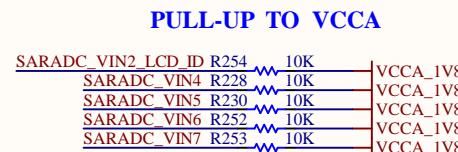
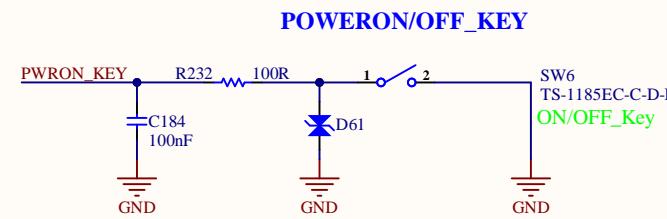
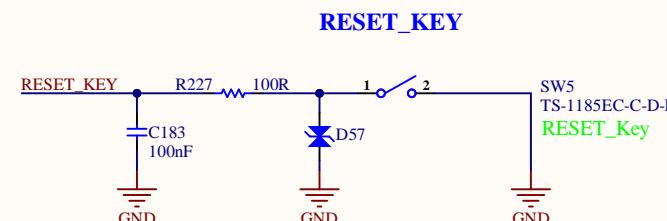
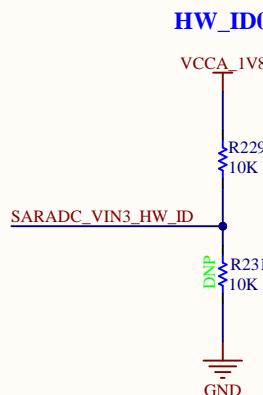
File: Carrier-Board-v1.0.PrjPcb

Date: 10/05/2024 Page Num: 26

Drawn By: Huzaifa Ali Page Total: 27

ROCKCHIP SYSTEM CONTROL

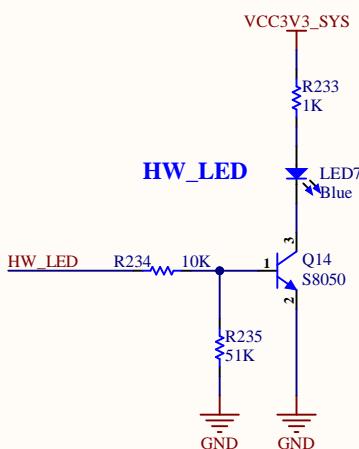
SARADC_VIN1	Up Resistance	Down Resistance
HW ID0	10K	DNP
HW ID1	10K	110K
HW ID2	20K	100K
HW ID3	33K	100K
HW ID4	18K	36K
HW ID5	36K	51K
HW ID6	51K	51K
HW ID7	51K	36K
HW ID8	36K	18K
HW ID9	100K	33K
HW ID10	100K	20K
HW ID11	110K	10K
HW ID12	DNP	10K



SARADC_VIN2	SARADC_VIN2_LCD_ID
SARADC_VIN3	SARADC_VIN3_HW_ID
SARADC_VIN4	SARADC_VIN4
SARADC_VIN5	SARADC_VIN5
SARADC_VIN6	SARADC_VIN6
SARADC_VIN7	SARADC_VIN7

RESET_KEY	PWRON_KEY
PWRON_KEY	HW_LED
HW_LED	

VCC3V3_SYS	VCC3V3_SYS
VCCA_1V8	VCCA_1V8
GND	GND



Title: ROCKCHIP_SYSTEM_CONTROL.SchD

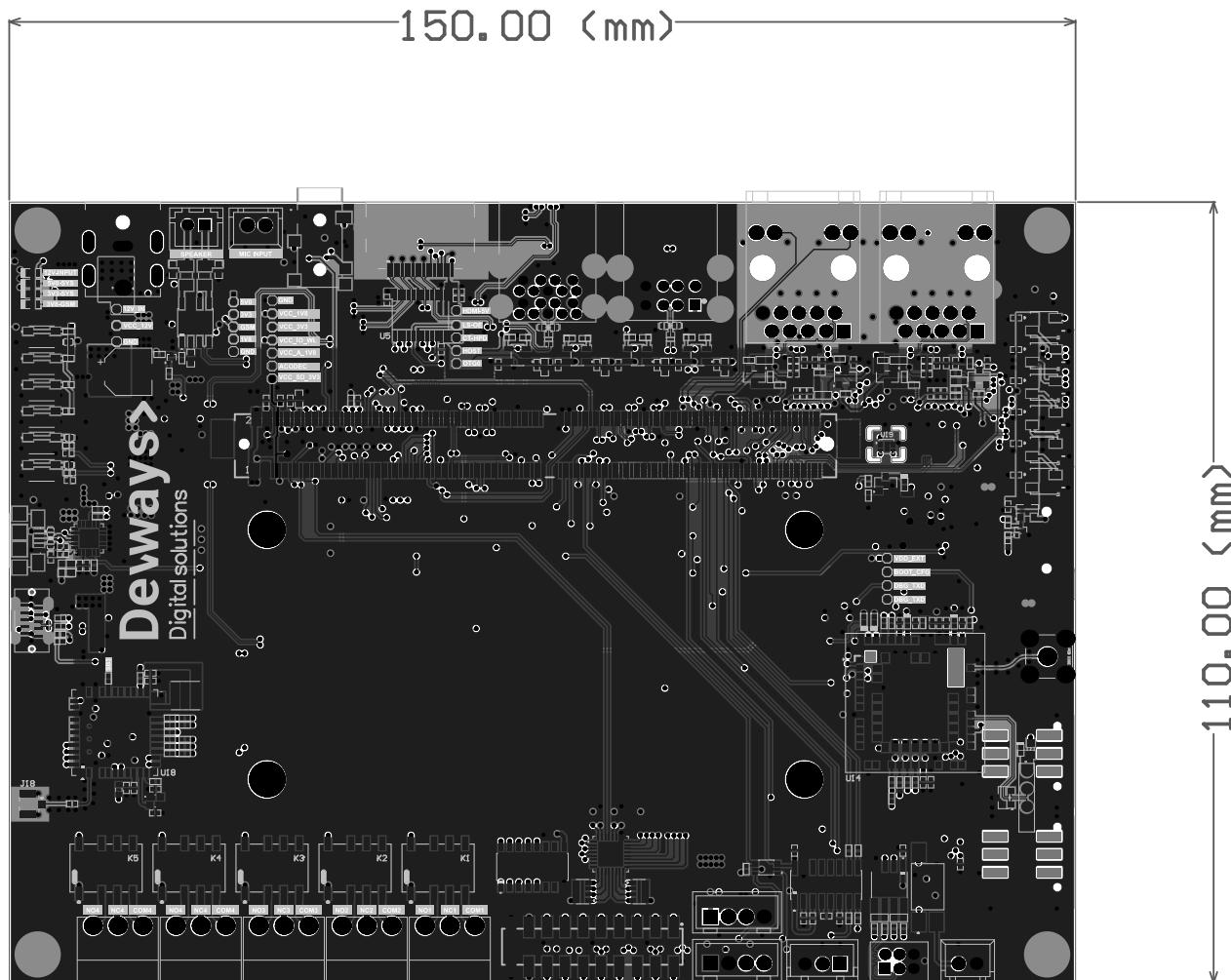
File: Carrier-Board-v1.0.PrjPcb

Date: 10/05/2024 Page Num: 27

Drawn By: Huzaifa Ali Page Total: 27

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.010mm	3.5	
1	Top Layer		0.035mm		
	Dielectric 2	PP-006	0.109mm	4.1	
2	L2_GND1	CF-004	0.030mm		
	Dielectric 4	PP-006	0.250mm	4.1	
3	L3_SIG1	CF-004	0.030mm		
	Dielectric 6	PP-006	0.109mm	4.1	
	Dielectric 8	PP-006	0.109mm	4.1	
4	L4_PWR	CF-004	0.030mm		
	Dielectric 1	FR-4	0.250mm	4.8	
5	L5_GND2	CF-004	0.030mm		
	Dielectric 9	PP-006	0.109mm	4.1	
	Dielectric 7	PP-006	0.109mm	4.1	
6	L6_SIG2	CF-004	0.030mm		
	Dielectric 5	PP-006	0.250mm	4.1	
7	L7_GND3	CF-004	0.030mm		
	Dielectric 3	PP-006	0.109mm	4.1	
8	Bottom Layer		0.035mm		
	Bottom Solder	Solder Resist	0.010mm	3.5	
	Bottom Overlay				

Total board thickness: 1.674mm



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
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