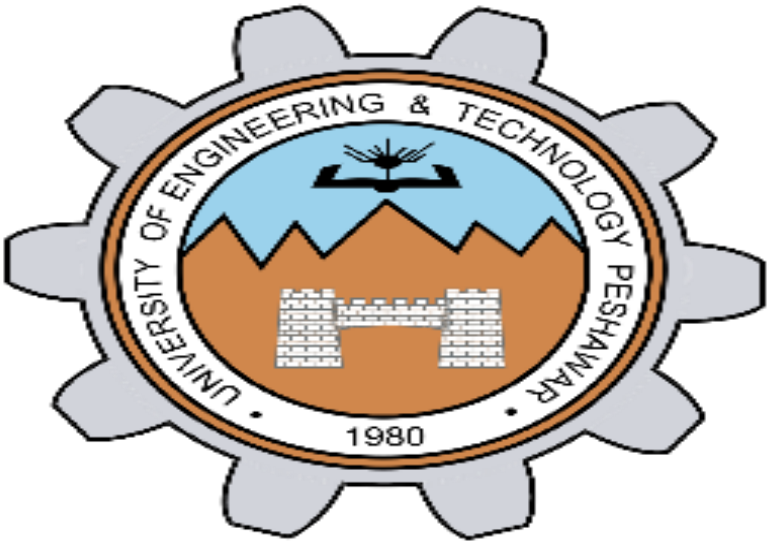
University of Engineering & Technology, Peshawar

DEPARTMENT OF COMPUTER SYSTEM ENGINEERING

Fall 2021



LAB 10 part 2

Muxes,Adder,Subrtracter

(CSE-304L)

Computer Organization and Architecture Lab

Submitted By: Anis Ahmad

Reg NO: 19PWCSE1770

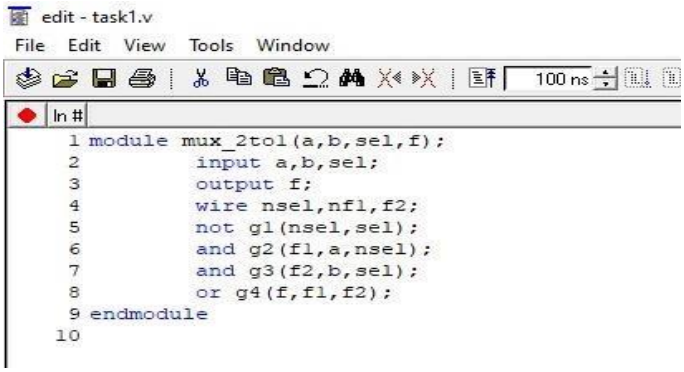
Submitted to: Dr. Ammad Khalil

TASK01: Muxes

Write a Verilog code for 2x1, 4x1 and 8x1 multiplexer using Gate Level modeling.

a) 2x1

Code:



edit - task1b.v

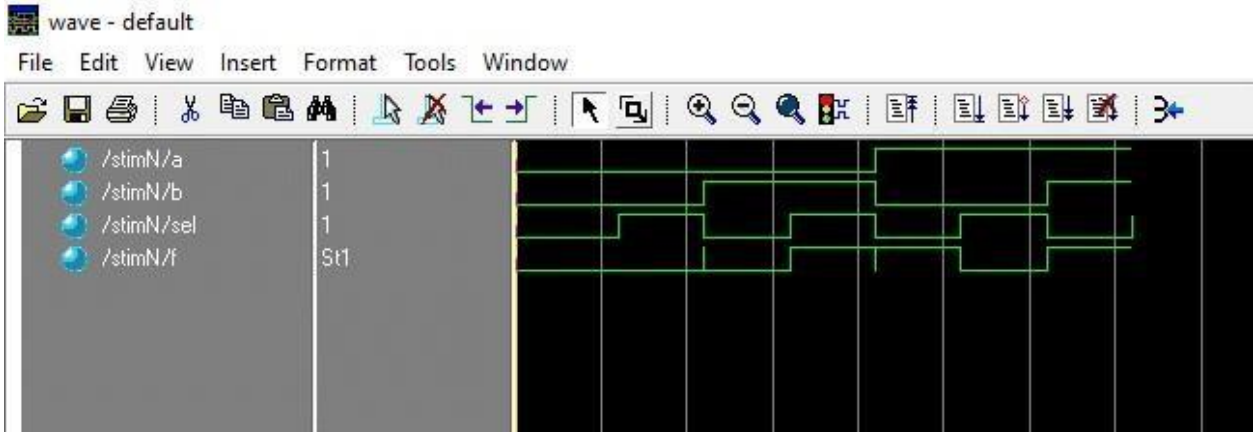
File Edit View Tools Window

100 ns

ln #

```
 1
 2 module stimN();
 3         reg a,b,sel;
 4         wire f;
 5         mux_2to1 M(a,b,sel,f);
 6         initial
 7         begin
 8                 $display("A B SEL F");
 9                 a=0;
10                 b=0;
11                 sel=0;
12                 #1 $display("%b %b %b %b",a,b,sel,f);
13                 #5 a=0;
14                 b=0;
15                 sel=1;
16                 $display("%b %b %b %b",a,b,sel,f);
17                 #5 a=0;
18                 b=1;
19                 sel=0;
20                 $display("%b %b %b %b",a,b,sel,f);
21                 #5 a=0;
22                 b=1;
23                 sel=1;
24                 $display("%b %b %b %b",a,b,sel,f);
25                 #5 a=1;
26                 b=0;
27                 sel=0;
28                 $display("%b %b %b %b",a,b,sel,f);
29                 #5 a=1;
30                 b=0;
31                 sel=1;
32                 $display("%b %b %b %b",a,b,sel,f);
33                 #5 a=1;
34                 b=1;
35                 sel=0;
36                 $display("%b %b %b %b",a,b,sel,f);
37                 #5 a=1;
38                 b=1;
39                 sel=1;
40                 $display("%b %b %b %b",a,b,sel,f);
41         end
42 endmodule
```

Output Wave:



---

b) 4x1

Code:

```
 1
 2 module mux_4to1(s1,s2,d0,d1,d2,d3,f);
 3         input s1,s2,d0,d1,d2,d3;
 4         output f;
 5         wire ns1,ns2,a0,a1,a2,a3,aa0,aa1,aa2,aa3,on1,on2;
 6         not n1(ns1,s1);
 7         not n2(ns2,s2);
 8         and g1(a0,ns1,ns2);
 9         and g11(aa0,a0,d0);
10         and g2(a1,ns1,s2);
11         and g22(aa1,a1,d1);
12         and g3(a2,s1,ns2);
13         and g33(aa2,a2,d2);
14         and g4(a3,s1,s2);
15         and g44(aa3,a3,d3);
16         or o1(on1,aa0,aa1);
17         or o2(on2,aa2,aa3);
18         or o3(f,on1,on2);
19 endmodule
```

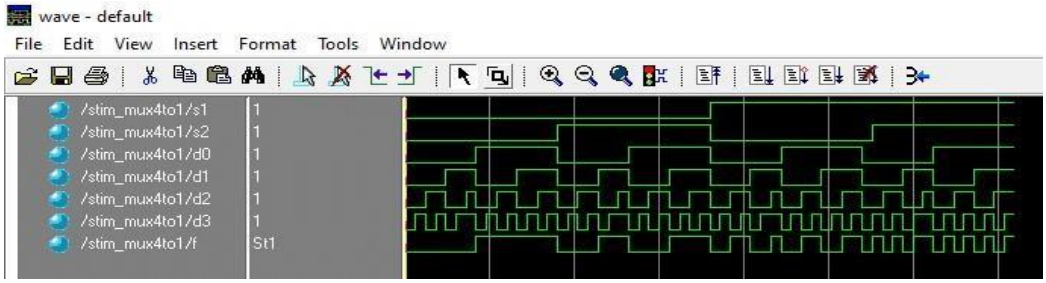
```
module stim_mux4to1();
 reg s1,s2,d0,d1,d2,d3;
 wire f;
          mux_4to1 multi(s1,s2,d0,d1,d2,d3,f);   initial
          begin
                    $display("SEL1 SEL2 D0 D1 D2 D3");

                    s1=0; s2=0;  d0=0;d1=0;d2=0;d3=0;
                     #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

                    s1 = 0;              s2 = 0; d0 = 0; d1 = 0; d2 = 0; d3 = 1;
                     #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);
                    s1 = 0;              s2 = 0;d0 = 0; d1 = 0; d2 = 1; d3 = 0;
                     #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

                    s1 = 0;              s2 = 0;  d0 = 0; d1 = 0; d2 = 1; d3 = 1;
                      #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

                    s1 = 0;              s2 = 0;  d0 = 0; d1 = 1; d2 = 0; d3 = 0;
                      #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

                    s1 = 0;              s2 = 0; d0 = 0; d1 = 1; d2 = 0; d3 = 1;
                      #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);
                    s1 = 0;              s2 = 0;  d0 = 0; d1 = 1; d2 = 1; d3 = 1;
                     #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

           s1 = 0; s2 = 0;  d0 = 1; d1 = 0; d2 = 0; d3 = 0;
            #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);
              s1 = 0; s2 = 0;  d0 = 1; d1 = 0; d2 = 0; d3 = 1;
            #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

                    s1 = 0;              s2 = 0;  d0 = 1; d1 = 0; d2 = 1; d3 = 0;
                     #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

                    s1 = 0;              s2 = 0; d0 = 1; d1 = 0; d2 = 1; d3 = 1;
                     #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

                    s1 = 0;              s2 = 0;
                    d0 = 1; d1 = 1; d2 = 0; d3 = 0;
                     #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);
                    s1 = 0;              s2 = 0;
                    d0 = 1; d1 = 1; d2 = 0; d3 = 1;
                     #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

                    s1 = 0;              s2 = 0;  d0 = 1; d1 = 1; d2 = 1; d3 = 0;
                     #10 $display("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

                    s1 = 0;              s2 = 0; d0 = 1; d1 = 1; d2 = 1; d3 = 1;
                     #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

                    s1 = 0;              s2 = 1;d0 = 0; d1 = 0; d2 = 0; d3 = 0;
```

```
          #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

          s1 = 0;  s2 = 1;  d0 = 0; d1 = 0; d2 = 0; d3 = 1;
#10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

s1 = 0; s2 = 1;  d0 = 0; d1 = 0; d2 = 1; d3 = 0;
#10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

          s1 = 0;               s2 = 1; d0 = 0; d1 = 0; d2 = 1; d3 = 1;
          #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

          s1 = 0;               s2 = 1;
          d0 = 0; d1 = 1; d2 = 0; d3 = 0;
          #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

          s1 = 0;               s2 = 1;
          d0 = 0; d1 = 1; d2 = 0; d3 = 1;
          #10 $display("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

          s1 = 0;               s2 = 1;  d0 = 0; d1 = 1; d2 = 1; d3 = 1;
          #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

          s1 = 0;               s2 = 1; d0 = 1; d1 = 0; d2 = 0; d3 = 0;
          #10 $display("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

          s1 = 0;               s2 = 1; d0 = 1; d1 = 0; d2 = 0; d3 = 1;
          #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

          s1 = 0;               s2 = 1; d0 = 1; d1 = 0; d2 = 1; d3 = 0;
          #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);
          s1 = 0;               s2 = 1;  d0 = 1; d1 = 0; d2 = 1; d3 = 1;
#10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

s1 = 0; s2 = 1;  d0 = 1; d1 = 1; d2 = 0; d3 = 0;
#10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);
  s1 = 0;            s2 = 1; d0 = 1; d1 = 1; d2 = 0; d3 = 1;
          #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

          s1 = 0;               s2 = 1;
          d0 = 1; d1 = 1; d2 = 1; d3 = 0;
          #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

          s1 = 0;               s2 = 1;
          d0 = 1; d1 = 1; d2 = 1; d3 = 1;
          #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

          s1 = 1;               s2 = 0;
          d0 = 0; d1 = 0; d2 = 0; d3 = 0;
          #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

          s1 = 1;               s2 = 0;
```

```
        d0 = 0; d1 = 0; d2 = 0; d3 = 1;
         #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

        s1 = 1;          s2 = 0;
        d0 = 0; d1 = 0; d2 = 1; d3 = 0;
         #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

        s1 = 1;          s2 = 0;
        d0 = 0; d1 = 0; d2 = 1; d3 = 1;
         #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

        s1 = 1;          s2 = 0;
        d0 = 0; d1 = 1; d2 = 0; d3 = 0;
#10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);
  s1 = 1; s2 = 0; d0 = 0; d1 = 1; d2 = 0; d3 = 1;
#10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);
       s1 = 1; s2 = 0; d0 = 0; d1 = 1; d2 = 1; d3 = 1;
         #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);
        s1 = 1;          s2 = 0;
        d0 = 1; d1 = 0; d2 = 0; d3 = 0;
         #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

        s1 = 1;          s2 = 0;
        d0 = 1; d1 = 0; d2 = 0; d3 = 1;
         #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

        s1 = 1;          s2 = 0;
        d0 = 1; d1 = 0; d2 = 1; d3 = 0;
         #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

        s1 = 1;          s2 = 0;
        d0 = 1; d1 = 0; d2 = 1; d3 = 1;
         #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

        s1 = 1;          s2 = 0;
        d0 = 1; d1 = 1; d2 = 0; d3 = 0;
         #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

        s1 = 1;          s2 = 0;
        d0 = 1; d1 = 1; d2 = 0; d3 = 1;
         #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

        s1 = 1;          s2 = 0;  d0 = 1; d1 = 1; d2 = 1; d3 = 0;
         #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);
  s1 = 1; s2 = 0;  d0 = 1; d1 = 1; d2 = 1; d3 = 1;
#10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);
  s1 = 1; s2 = 0;  d0 = 0; d1 = 0; d2 = 0; d3 = 0;
         #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

        s1 = 1;          s2 = 1;
```

```
                d0 = 0; d1 = 0; d2 = 0; d3 = 1;
                 #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

                s1 = 1;              s2 = 1;  d0 = 0; d1 = 0; d2 = 1; d3 = 0;
                 #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

                s1 = 1;              s2 = 1;  d0 = 0; d1 = 0; d2 = 1; d3 = 1;
                 #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

                s1 = 1;              s2 = 1;                          d0 = 0; d1 = 1; d2 = 0; d3 = 0;
                 #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

                s1 = 1;              s2 = 1;  d0 = 0; d1 = 1; d2 = 0; d3 = 1;
                 #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

                s1 = 1;              s2 = 1; d0 = 0; d1 = 1; d2 = 1; d3 = 1;
                 #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

                s1 = 1;              s2 = 1;  d0 = 1; d1 = 0; d2 = 0; d3 = 0;
                 #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

                 s1 = 1; s2 = 1;  d0 = 1; d1 = 0; d2 = 0; d3 = 1;
            #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);
              s1 = 1; s2 = 1;  d0 = 1; d1 = 0; d2 = 1; d3 = 0;
            #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

                s1 = 1;              s2 = 1;  d0 = 1; d1 = 0; d2 = 1; d3 = 1;
                 #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);
                s1 = 1;              s2 = 1; d0 = 1; d1 = 1; d2 = 0; d3 = 0;
                 #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

                s1 = 1;              s2 = 1; d0 = 1; d1 = 1; d2 = 0; d3 = 1;
                 #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

                s1 = 1;              s2 = 1; d0 = 1; d1 = 1; d2 = 1; d3 = 0;
                 #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);

                s1 = 1;              s2 = 1; d0 = 1; d1 = 1; d2 = 1; d3 = 1;
                 #10 $ display ("%b %b %b %b %b %b %b",s1,s2,d0,d1,d2,d3,f);
                        end
endmodule
```

Output Wave:



c) 8x1

Code:

edit - mux8to1a.v

File Edit View Tools Window

100 ns

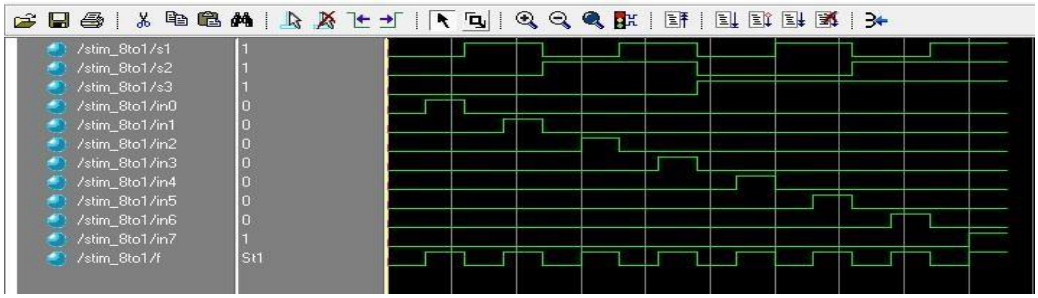
ln #

```
 1
 2 module mux_8to1(s1,s2,s3,in0,in1,in2,in3,in4,in5,in6,in7,f);
 3         input s1,s2,s3,in0,in1,in2,in3,in4,in5,in6,in7;
 4         output f;
 5         wire ns1,ns2,ns3,a0,a1,a2,a3,a4,a5,a6,a7;
 6         not n1(ns1,s1);
 7         not n2(ns2,s2);
 8         not n3(ns3,s3);
 9         and g0(a0,ns1,ns2,ns3,in0);
10         and g1(a1,s1,ns2,ns3,in1);
11         and g2(a2,ns1,s2,ns3,in2);
12         and g3(a3,s1,s2,ns3,in3);
13         and g4(a4,ns1,ns2,s3,in4);
14         and g5(a5,s1,ns2,s3,in5);
15         and g6(a6,ns1,s2,s3,in6);
16         and g7(a7,s1,s2,s3,in7);
17         or o1(f,a0,a1,a2,a3,a4,a5,a6,a7);
18 endmodule
```

```
1
2 module stim_8to1;
3         reg s1,s2,s3,in0,in1,in2,in3,in4,in5,in6,in7;
4         wire f;
5         mux_8to1 multipl(s1,s2,s3,in0,in1,in2,in3,in4,in5,in6,in7,f);
6         initial
7         begin
8                 $display("SEL3 SEL2 SEL1 IN7 IN6 IN5 IN4 IN3 IN2 IN1 IN0 F");
9                 s1 = 0; s2 = 0; s3 = 0;
10                in0=0;in1=0;in2=0;in3=0;in4=0;in5=0;in6=0;in7=0;
11                #1 $display("%b %b %b %b %b %b %b %b %b %b %b %b",s3,s2,s1,in7,in6,in5,in4,in3,in2,in1,in0,f);
12                #5;
13
14                s1 = 0; s2 = 0; s3 = 0;
15                in0=1;in1=0;in2=0;in3=0;in4=0;in5=0;in6=0;in7=0;
16                #1 $display("%b %b %b %b %b %b %b %b %b %b %b %b",s3,s2,s1,in7,in6,in5,in4,in3,in2,in1,in0,f);
17                #5;
18
19                s1 = 1; s2 = 0; s3 = 0;
20                in0=0;in1=0;in2=0;in3=0;in4=0;in5=0;in6=0;in7=0;
21                #1 $display("%b %b %b %b %b %b %b %b %b %b %b %b",s3,s2,s1,in7,in6,in5,in4,in3,in2,in1,in0,f);
22                #5;
23
24                s1 = 1; s2 = 0; s3 = 0;
25                in0=0;in1=1;in2=0;in3=0;in4=0;in5=0;in6=0;in7=0;
26                #1 $display("%b %b %b %b %b %b %b %b %b %b %b %b",s3,s2,s1,in7,in6,in5,in4,in3,in2,in1,in0,f);
27                #5;
28
29                s1 = 0; s2 = 1; s3 = 0;
30                in0=0;in1=0;in2=0;in3=0;in4=0;in5=0;in6=0;in7=0;
31                #1 $display("%b %b %b %b %b %b %b %b %b %b %b %b",s3,s2,s1,in7,in6,in5,in4,in3,in2,in1,in0,f);
32                #5;
33
34                s1 = 0; s2 = 1; s3 = 0;
35                in0=0;in1=0;in2=1;in3=0;in4=0;in5=0;in6=0;in7=0;
36                #1 $display("%b %b %b %b %b %b %b %b %b %b %b %b",s3,s2,s1,in7,in6,in5,in4,in3,in2,in1,in0,f);
37                #5;
38
39                s1 = 1; s2 = 1; s3 = 0;
40                in0=0;in1=0;in2=0;in3=0;in4=0;in5=0;in6=0;in7=0;
41                #1 $display("%b %b %b %b %b %b %b %b %b %b %b %b",s3,s2,s1,in7,in6,in5,in4,in3,in2,in1,in0,f);
42                #5;
```

```
44                s1 = 1; s2 = 1; s3 = 0;
45                in0=0;in1=0;in2=0;in3=1;in4=0;in5=0;in6=0;in7=0;
46                #1 $display("%b %b %b %b %b %b %b %b %b %b %b %b",s3,s2,s1,in7,in6,in5,in4,in3,in2,in1,in0,f);
47                #5;
48
49                s1 = 0; s2 = 0; s3 = 1;
50                in0=0;in1=0;in2=0;in3=0;in4=0;in5=0;in6=0;in7=0;
51                #1 $display("%b %b %b %b %b %b %b %b %b %b %b %b",s3,s2,s1,in7,in6,in5,in4,in3,in2,in1,in0,f);
52                #5;
53
54                s1 = 0; s2 = 0; s3 = 1;
55                in0=0;in1=0;in2=0;in3=0;in4=1;in5=0;in6=0;in7=0;
56                #1 $display("%b %b %b %b %b %b %b %b %b %b %b %b",s3,s2,s1,in7,in6,in5,in4,in3,in2,in1,in0,f);
57                #5;
58
59                s1 = 1; s2 = 0; s3 = 1;
60                in0=0;in1=0;in2=0;in3=0;in4=0;in5=0;in6=0;in7=0;
61                #1 $display("%b %b %b %b %b %b %b %b %b %b %b %b",s3,s2,s1,in7,in6,in5,in4,in3,in2,in1,in0,f);
62                #5;
63
64                s1 = 1; s2 = 0; s3 = 1;
65                in0=0;in1=0;in2=0;in3=0;in4=0;in5=1;in6=0;in7=0;
66                #1 $display("%b %b %b %b %b %b %b %b %b %b %b %b",s3,s2,s1,in7,in6,in5,in4,in3,in2,in1,in0,f);
67                #5;
68
69                s1 = 0; s2 = 1; s3 = 1;
70                in0=0;in1=0;in2=0;in3=0;in4=0;in5=0;in6=0;in7=0;
71                #1 $display("%b %b %b %b %b %b %b %b %b %b %b %b",s3,s2,s1,in7,in6,in5,in4,in3,in2,in1,in0,f);
72                #5;
73
74                s1 = 0; s2 = 1; s3 = 1;
75                in0=0;in1=0;in2=0;in3=0;in4=0;in5=0;in6=1;in7=0;
76                #1 $display("%b %b %b %b %b %b %b %b %b %b %b %b",s3,s2,s1,in7,in6,in5,in4,in3,in2,in1,in0,f);
77                #5;
78
79                s1 = 1; s2 = 1; s3 = 1;
80                in0=0;in1=0;in2=0;in3=0;in4=0;in5=0;in6=0;in7=0;
81                #1 $display("%b %b %b %b %b %b %b %b %b %b %b %b",s3,s2,s1,in7,in6,in5,in4,in3,in2,in1,in0,f);
82                #5;
83                s1 = 1; s2 = 1; s3 = 1;
84                in0=0;in1=0;in2=0;in3=0;in4=0;in5=0;in6=0;in7=1;
85                #1 $display("%b %b %b %b %b %b %b %b %b %b %b %b",s3,s2,s1,in7,in6,in5,in4,in3,in2,in1,in0,f);
86                #5;
87        end
88 endmodule
```

Output Wave:



TASK01:
Write a Verilog code for Half Adder using Gate Level modeling

Code:

edit - halfadder1.v

File Edit View Tools Window

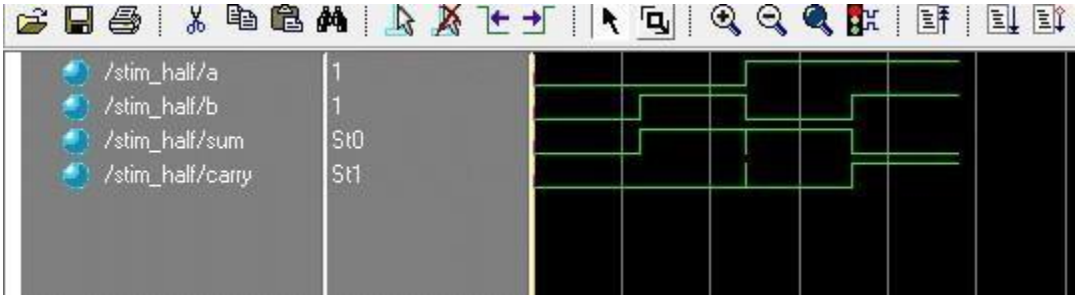
```
1
2 module half_adder(a,b,sum,carry);
3         input a,b;
4         output sum,carry;
5         xor g1(sum,a,b);
6         and g2(carry,a,b);
7 endmodule
```

edit - halfadder2.v

File Edit View Tools Window

```
1
2 module stim_half;
3         reg a,b;
4         wire sum,carry;
5         half_adder HA(a,b,sum,carry);
6         initial
7         begin
8                 $display("A B   Difference Barrow");
9                 a = 0; b = 0;
10                #1 $display("%b %b %b   %b",a,b,sum,carry);
11                #5;
12                a = 0; b = 1;
13                #1 $display("%b %b %b   %b",a,b,sum,carry);
14                #5;
15                a = 1; b = 0;
16                #1 $display("%b %b %b   %b",a,b,sum,carry);
17                #5;
18                a = 1; b = 1;
19                #1 $display("%b %b %b   %b",a,b,sum,carry);
20                #5;
21        end
22 endmodule
```

Output Wave:



TASK02:

Write a Verilog code for Full Adder using Gate Level modeling.

Code:

edit - Fulladder1.v

File Edit View Tools Window

100 ns

ln #

```
 1
 2 module full_adder(a,b,c,sum,carry);
 3         input a,b,c;
 4         output sum,carry;
 5         wire a1,a2,a3;
 6
 7         xor g1(sum,a,b,c);
 8         xor g2(a1,a,b);
 9         and g3(a2,a,b);
10         and g4(a3,a1,c);
11         or g5(carry,a2,a3);
12 endmodule
```

edit - Fulladder2.v

File Edit View Tools Window

100 ns

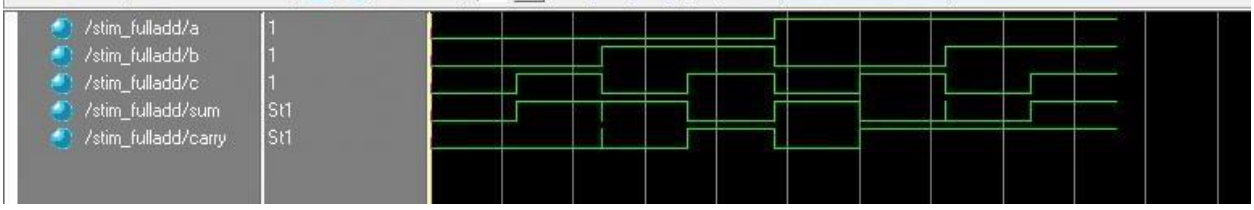
ln # E:/5TH SE

```
 1
 2 module stim_fulladd;
 3         reg a,b,c;
 4         wire sum,carry;
 5         full_adder fulad(a,b,c,sum,carry);
 6         initial
 7         begin
 8                 $display("A B   Cin     Sum     carry");
 9                 a = 0; b = 0; c = 0;
10                 #1 $display("%b %b %b   %b      %b",a,b,c,sum,carry);
11                 #5;
12                 a = 0; b = 0; c = 1;
13                 #1 $display("%b %b %b   %b      %b",a,b,c,sum,carry);
14                 #5;
15                 a = 0; b = 1; c = 0;
16                 #1 $display("%b %b %b   %b      %b",a,b,c,sum,carry);
17                 #5;
18                 a = 0; b = 1; c = 1;
19                 #1 $display("%b %b %b   %b      %b",a,b,c,sum,carry);
20                 #5;
21                 a = 1; b = 0; c = 0;
22                 #1 $display("%b %b %b   %b      %b",a,b,c,sum,carry);
23                 #5;
24                 a = 1; b = 0; c = 1;
25                 #1 $display("%b %b %b   %b      %b",a,b,c,sum,carry);
26                 #5;
27                 a = 1; b = 1; c = 0;
28                 #1 $display("%b %b %b   %b      %b",a,b,c,sum,carry);
29                 #5;
30                 a = 1; b = 1; c = 1;
31                 #1 $display("%b %b %b   %b      %b",a,b,c,sum,carry);
32                 #5;
33         end
34 endmodule
```

Output Wave:

wave - default

File Edit View Insert Format Tools Window



TASK03:

Write a Verilog code for Half Subtractor using Gate Level modeling.

Code:

edit - halfaub1.v

File Edit View Tools Window

100 ns

ln #

```
 1
 2 module half_sub(a,b,sum,carry);
 3         input a,b;
 4         output sum,carry;
 5         wire na;
 6         not n1(na,a);
 7         xor g1(sum,a,b);
 8         and g2(carry,na,b);
 9 endmodule
10
```

edit - halfsub2.v

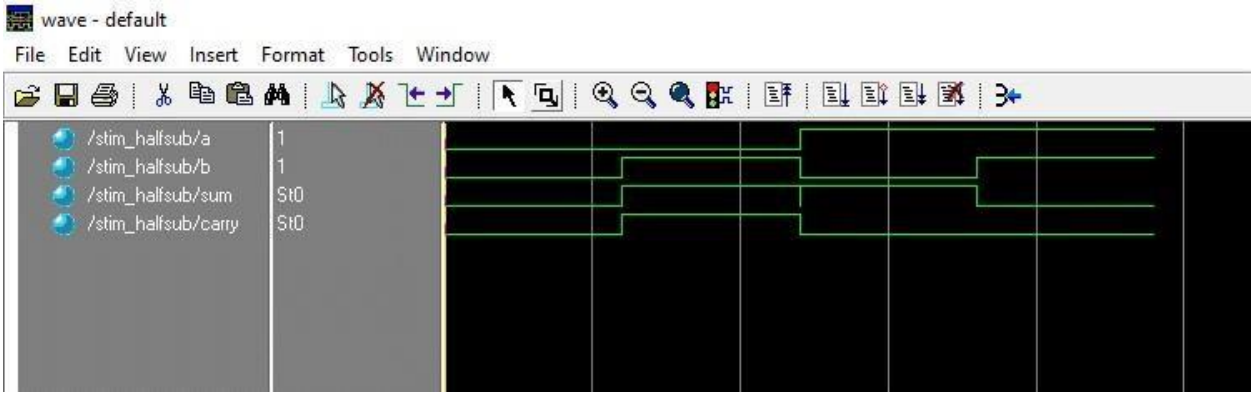
File Edit View Tools Window

100 ns

ln #

```
 1
 2 module stim_halfsub;
 3         reg a,b;
 4         wire sum,carry;
 5         half_sub HS(a,b,sum,carry);
 6         initial
 7         begin
 8                 $display("A B   SUM     Carry");
 9                 a = 0; b = 0;
10                 #1 $display("%b %b %b   %b",a,b,sum,carry);
11                 #5;
12                 a = 0; b = 1;
13                 #1 $display("%b %b %b   %b",a,b,sum,carry);
14                 #5;
15                 a = 1; b = 0;
16                 #1 $display("%b %b %b   %b",a,b,sum,carry);
17                 #5;
18                 a = 1; b = 1;
19                 #1 $display("%b %b %b   %b",a,b,sum,carry);
20                 #5;
21         end
22 endmodule
23
24
```

Output Wave:


wave - default
File Edit View Insert Format Tools Window
/stim_halfsub/a
/stim_halfsub/b
/stim_halfsub/sum
/stim_halfsub/carry
1
1
St0
St0