LAB # 12

Fall 2020

CSE304L Computer Organization & Architecture Lab

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Class Section: **A**

"On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work."

Student Signature: _____

Submitted to:

Engr. Amaad Khalil

March 18, 2021 (Thursday)

Department of Computer Systems Engineering

University of Engineering and Technology, Peshawar

Lab Tasks:

Task:

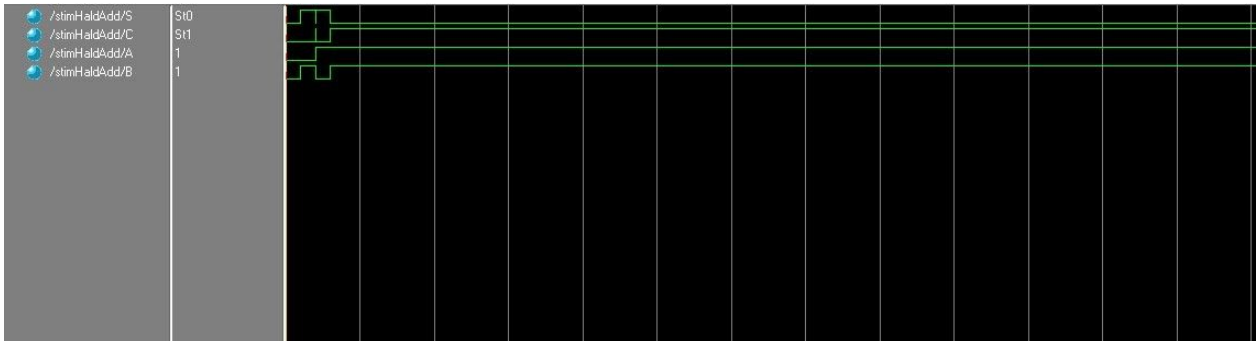
Write a Verilog code for Half Adder using Gate Level modeling.

Code:

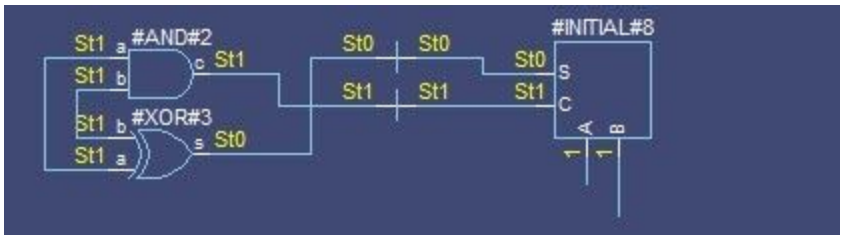
```
module halfAdder( output s,c,input a,b);

and(c,a,b);

xor(s,a,b);

endmodule




module stimHaldAdd();

wire S,C;

reg A,B;



halfAdder ha(S,C,A,B);



initial

begin
```

```
$display("A     B       S       C");

A=0;

B=0;

#1 $display("%b     %b      %b      %b",A,B,S,C);



A=0;

B=1;

#1 $display("%b     %b      %b      %b",A,B,S,C);



A=1;

B=0;

#1 $display("%b     %b      %b      %b",A,B,S,C);



A=1;

B=1;

#1 $display("%b     %b      %b      %b",A,B,S,C);



end
```

```
endmodule
```




```
vsim ash.stimHaldAdd
# vsim ash.stimHaldAdd
# Loading ash.stimHaldAdd
# Loading ash.halfAdder
run
#A   B    S    C
# 0   0    0    0
# 0   1    1    0
# 1   0    1    0
# 1   1    0    1
destroy .wave
```



Task:

Write a Verilog code for Full Adder using Gate Level modeling.

Code:

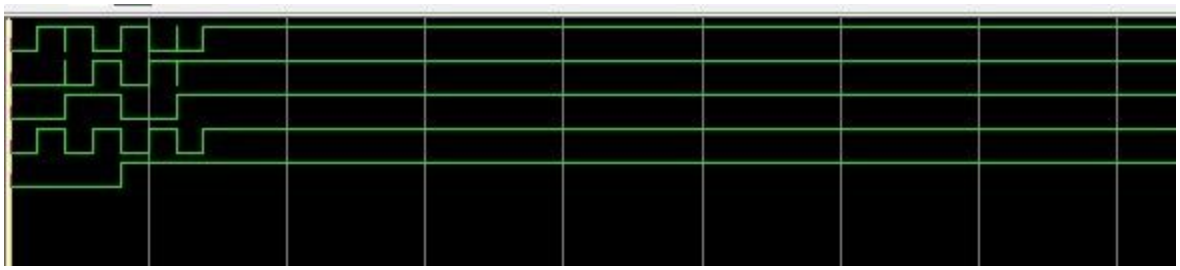
```
module fullAdder( output s,cOut,input a,b,cIn);

xor(n1,a,b),(s,cIn,n1);

and(n2,n1,cIn),(n3,a,b);

or(cOut,n2,n3);
```

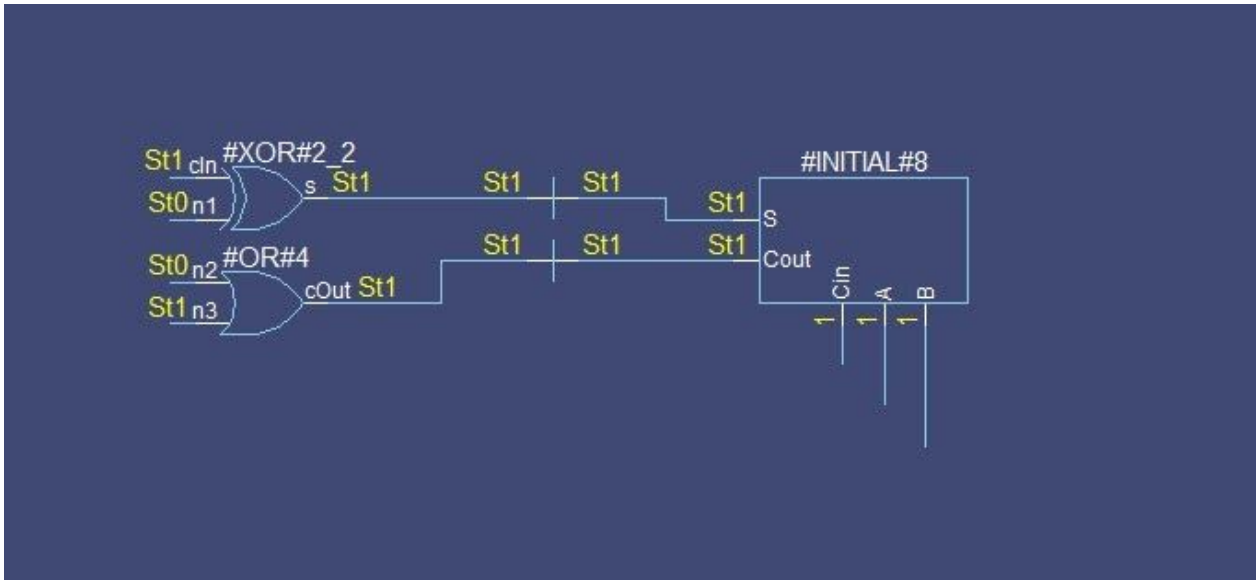
```
endmodule




module stimFullAdd();

wire S,Cout;

reg A,B,Cin;



fullAdder fa(S,Cout,A,B,Cin);



initial

begin



$display("Cin    A      B    S     Cout");

Cin=0;

A=0;

B=0;

#1 $display("%b     %b      %b      %b      %b",Cin,A,B,S,Cout);

Cin=0;
```

```
A=0;

B=1;

#1 $display("%b     %b      %b      %b      %b",Cin,A,B,S,Cout);

Cin=0;

A=1;

B=0;

#1 $display("%b     %b      %b      %b      %b",Cin,A,B,S,Cout);

Cin=0;

A=1;

B=1;

#1 $display("%b     %b      %b      %b      %b",Cin,A,B,S,Cout);

Cin=1;

A=0;

B=0;

#1 $display("%b     %b      %b      %b      %b",Cin,A,B,S,Cout);

Cin=1;

A=0;

B=1;
```

```
#1 $display("%b     %b      %b      %b      %b",Cin,A,B,S,Cout);

Cin=1;

A=1;

B=0;

#1 $display("%b     %b      %b      %b      %b",Cin,A,B,S,Cout);

Cin=1;

A=1;

B=1;

#1 $display("%b     %b      %b      %b      %b",Cin,A,B,S,Cout);




end

endmodule
```

```
vsim ash.stimFullAdd
# vsim ash.stimFullAdd
# Loading ash.stimFullAdd
# Loading ash.fullAdder
run
# Cin   A    B   S   Cout
# 0    0    0    0    0
# 0    0    1    1    0
# 0    1    0    1    0
# 0    1    1    0    1
# 1    0    0    1    0
# 1    0    1    0    1
# 1    1    0    0    1
# 1    1    1    1    1

VSIM 7>
```





Task:

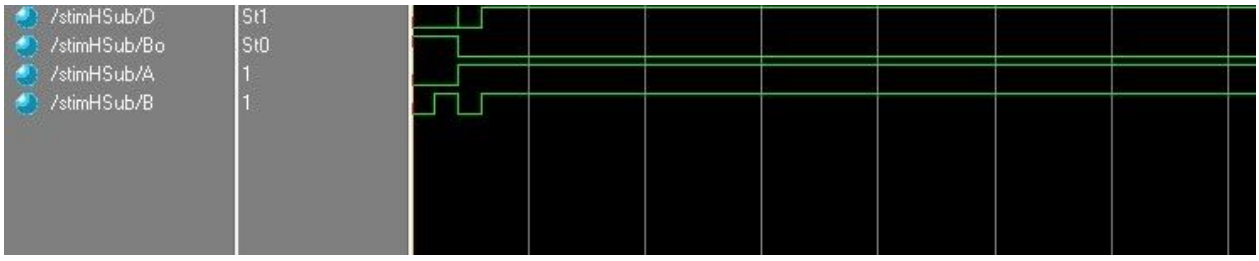
Write a Verilog code for Half Subtractor using Gate Level modeling.

Code:

```
module halfSubractor(output d,bo,input a,b);

xor(d,a,b);

not(a_,a);

and(bo,a_);
```

```
endmodule




module stimHSub();

wire D,Bo;

reg A,B;



halfSubractor hs(D,Bo,A,B);



initial

begin



$display("A     B       D       B");

A=0;

B=0;

#1 $display("%b     %b      %b      %b",A,B,D,Bo);
```

```
A=0;

B=1;

#1 $display("%b     %b      %b      %b",A,B,D,Bo);



A=1;

B=0;

#1 $display("%b     %b      %b      %b",A,B,D,Bo);



A=1;

B=1;

#1 $display("%b     %b      %b      %b",A,B,D,Bo);



end

endmodule
```



/sim ash.stimHSub
vsim ash.stimHSub
Loading ash.stimHSub
Loading ash.halfSubractor
un
#A B D B
#0 0 0 1
#0 1 1 1
#1 0 1 0
#1 1 0 0

/SIM 33>