University of Engineering & Technology, Peshawar

DEPARTMENT OF COMPUTER SYSTEM ENGINEERING

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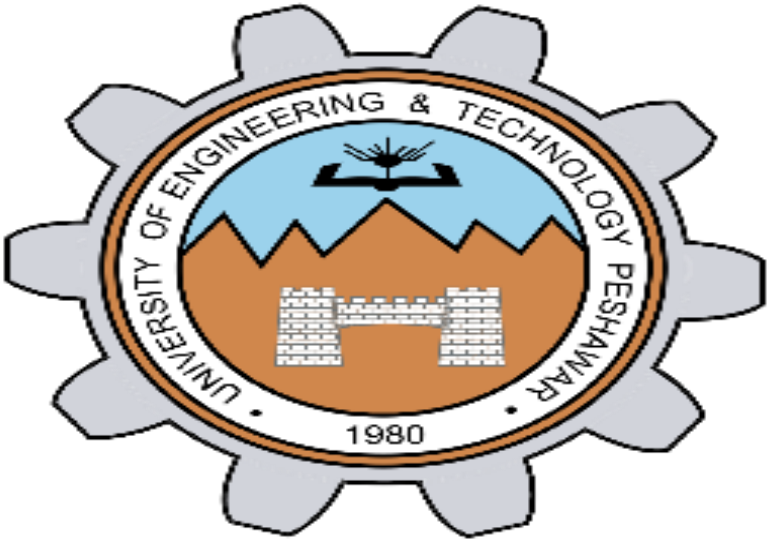

LAB 08

Introduction to Modelsim

Computer Organization and Architecture Lab

Submitted By: Anis Ahmad

Reg NO: 19PWCSE1770

Submitted to: Dr. Ammad Khalil

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MODELSIM*:*

MODELSIM is used to simulate HDL and VHDL.

Steps of Installation:

1) Unzip, unRAR or use the installer

2) Install using "setup.exe"

3) After installation, copy "mgls.dll", "modeltech.exe" and "vlm.exe" into your

   "<installdir>\Win32" dir, overwrite when prompted

4) Copy "license.dat" into your "<installdir>\Win32" dir and into "C:\FlexLM", overwrite when prompted.

5) Done

How to use ModelSim?

Step 1
Create a new project:
Select **File** > **New** > **Project** (Main window) to create a new project. This opens the **Create Project** dialog. The dialog includes these options:

• **Project Name**
The name of the new project.

• **Project Location**
The directory in which the *.mpf* file will be created.

• **Default Library Name**
The name of the working library.

You can generally leave the **Default Library Name** set to "work." The name you specify will be used to create a working library subdirectory within the Project Location. After selecting OK, you will see a blank Project tab in the workspace area of the Main window and the **Add Items to the Project** dialog.

Step 2
Adding items to the project
The **Add Items to the Project** dialog includes these options:

- **Create New File**
  Create a new VHDL, Verilog, Tcl, or text file using the Source window. See below for details.
- **Add Existing File**
  Add an existing file. See below for details.
- **Create Simulation**
  Create a Simulation Configuration that specifies source files and simulator options.
- **Create New Folder**
  Create an organization folder.
- **Create New File**
  The **Create New File** command lets you create a new VHDL, Verilog, Tcl, or text file using the Source window. You can also access this command by selecting **File** > **Add to Project** > **New File** (Main window) or right-clicking (2nd button in Windows; 3rd button in UNIX) in the Project tab and selecting **Add to Project** > **New File**.
- The **Create Project File** dialog includes these options:
- **File Name**
  The name of the new file
- **Add file as type**
  Add the type of the new file. Select VHDL, Verilog, TCL, or text.