Store -> addi , x0 , zero , 3

- Must write zero

X0 -> Constant
S0-S11 -> Variables

- Instructions work on 12 bits by default

LUI -> Lower Upper Immediate

- To add 32 bits, upper 20 bits are stored using lui command and rest 12 using addi
- add only works on 12 bits

0.) lui s0 , 0x12345
1.) addi s0 , s0 , 0x12345
-s0 twice to order 32 bits into s0

LI -> Load Immediate

Memory
1.) Word Addressable -> 32 bits
2.) Byte Addressable -> 8 bits

2.) lw -> Load 1 word
2.) lb - > Load 1 byte
3.) lh -> Load half word(16 bits)

- RISC-V architecture is byte addressable

Data Transfer
1.) lw -> Load word (Takes a word from memory and stores it into register)
2.) rd -> Destination Register (specifies register to store in)

- lw , rd , imm (base register)

3.) sw -> Store word (Stores a word into memory from register)

- sw , rd , address (base register)

Logical Instruction

1. AND
2. OR
3. XOR
4. Left shift
5. Right Shift