Experiment # 9

Objective: To understand FET basic operation and plot its drain and transfer characteristics curves.

Name: ……. **Registration No: …….**

Date: ……. **Grade and Signature: ……**

CLO2, CLO4	Record and sketch the basic amplifier biasing techniques of BJTs and MOSFETs Use basic commands in the circuit simulator (PROTEUS) for analysis of electronic circuits			
Psychomotor/Affective	**Level1 (1)**	**Level 2 (2-3)**	**Level3 (4-5)**	**Level4 (6-7)**
Report Marks (3)			**Total marks (10)**	

Abstract:

The JFET (junction field-effect transistor) is a type of FET that operates with a reverse-biased pn junction to control current in a channel. Depending on their structure, JFETs fall into either of two categories, n channel or p channel. To illustrate the operation of a JFET, Figure 1 shows dc bias voltages applied to an n-channel device. V_{DD} provides a drain-to-source voltage and supplies current from drain to source. V_{GG} sets the reverse-bias voltage between the gate and the source, as shown in Figure 1. The drain current (ID) of the JFET is controlled by the application of reverse-biased voltage between gate and source terminals (V_{GS}). The relationship between I_D and V_{GS} is defined by the well-known Shockley's equation:

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

Where V_P is called the pinch-off voltage and I_{DSS} is known as the drain saturation current. When $V_{GS} = V_P$ then $I_D = 0$, and the FET is in the cut-off region.

From figure 2, it is seen that the gate is directly connected to source to achieve $V_{GS} = 0V$, this is similar to no bias condition. The instant the voltage V_{DD} (=V_{DS}) is applied, the electrons will be drawn to the drain terminal, causing I_D & I_S to flow (i.e. $I_D = I_S$).

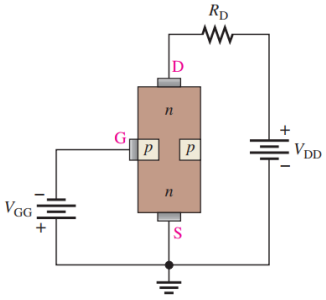
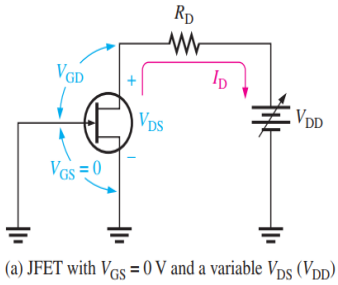


Figure 1



(a) JFET with $V_{GS} = 0$ V and a variable V_{DS} (V_{DD})

Figure 2

Required Material:

- Two resistors of 560 ohms.
- An n-channel JFET (2N5484).

Required Equipment:

- Breadboard
- VOAM
- DC power supply
- Variable voltage supply

Step 1: For Drain Characteristics

a. Connect the circuit as per given in figure 2 properly.
b. Keep V_{GS} = 0V by varying V_{GG}
c. Vary V_{DS} in step of 1V up to 10 volts and measure the drain current I_D.
d. Tabulate all the readings in Table 1.
e. Repeat the above procedure for V_{GS} as -0.5, -1V, -1.5V, -2V, -2.5V, -3V, -3.5V etc.

Table 1

V_{GS} = 0 V		V_{GS} = -1 V		V_{GS} = -2 V		V_{GS} = -3 V		V_{GS} = -4 V	
V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)
0									
1									
2									
3									
4									
5									
6									
7									
8									
9									
10									

Step 2: For Transfer Characteristics

a. Connect the circuit as per given in figure 2 properly.
b. Set the value of V_{DD} so that the voltage V_{DS} is constant at 10 V.
c. Vary V_{GS} by varying V_{GG} in the step of 0.5 up to 3.5V and note down value of drain current I_D.
d. Tabulate all the readings in Table 2.
e. Plot the output characteristics V_{DS} vs I_D and transfer characteristics V_{GS} vs I_D.
f. Calculate I_{DSS} and V_P from the graphs and verify it from the data sheet.

Table 2

	R = 47K	
S.No.	V_{GS} (V)	I_D (mA)
1.		
2.		
3.		
4.		
5.		
6.		
7.		
8.		
9.		
10.		

Questions

1. What are different terminals of FET?

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2. What are advantages of FET?

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3. What are disadvantages of FET?

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4. What is the difference between n- channel FET and p-channel FET?