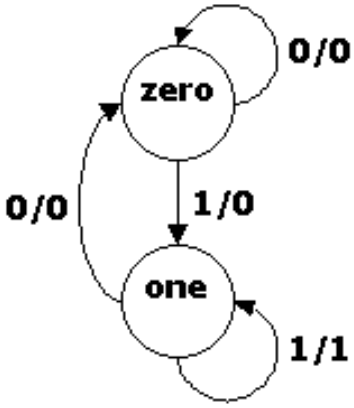
CSE 308: Digital System Design

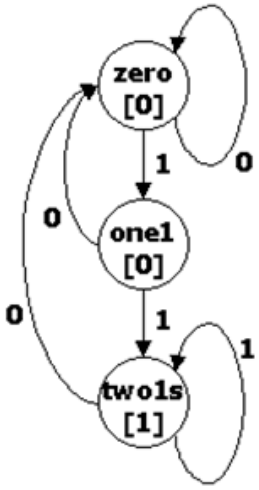
(a) State whether the following FSM is a Moore/Mealy FSM. Explain why?
(b) Convert the FSM to its other form.
(c) Implement the FSM in (a) in Verilog.



Solution:

(a) The given FSM is a Mealy FSM because the output depends on present state as well as input.

(b) Mealy ➔ Moore.



(c)

```
module FSM_mealy (clk, reset, in, out);
     input clk, reset, in;
     output out;
     parameter zero = 0, one = 1;
     reg out;
     reg PRSNT_STATE, NXT_STATE;

     // Implement the state register
     always @ (posedge clk)
          if (reset) PRSNT_STATE <= zero;
          else PRSNT_STATE <= NXT_STATE;

     // Implement the combinational logic
     always @ (in or PRSNT_STATE)
          case (PRSNT_STATE)
               zero: begin
                    out = in ? 0 : 0;
                    NXT_STATE = in ? one : zero;
               end
               one: begin
                    out = in ? 1 : 0;
                    NXT_STATE = in ? one : zero;
               end
               default: begin
                    out = 0;
                    NXT_STATE = zero;
               end
          endcase
endmodule;
```