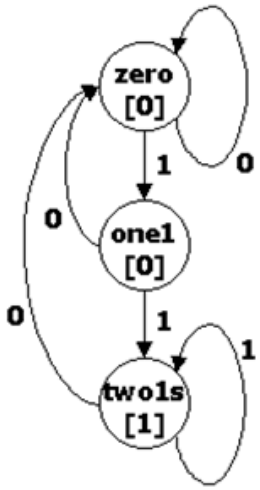
CSE 308: Digital System Design

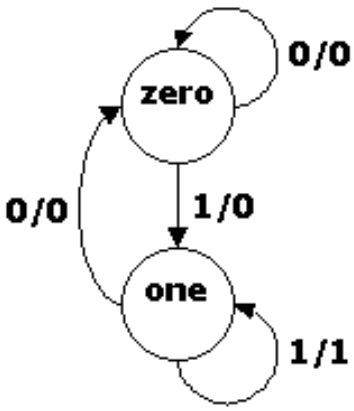
(a) State whether the following FSM is a Moore/Mealy FSM. Explain why?
(b) Convert the FSM to its other form.
(c) Implement the FSM in (a) in Verilog.



Solution:

(a) The given FSM is a Moore FSM because the output depends on present state only.

(b) Moore ➔ Mealy.



(c)

```
module reduce (clk, reset, in, out);
  input clk, reset, in;
  output out;
  parameter zero = 0, one1 = 1, two1s = 2; // states
  reg out;
  reg [1:0] state;       // state register
  reg [1:0] next_state;  // always block needs reg

// Implement the state register
  always @(posedge clk)
    if (reset) state = zero; //can put in next state logic
    else       state = next_state;

  always @(in or state) // combinational logic
    case (state)
      zero: begin // last input was a zero
        out = 0;
        if (in) next_state = one1;
        else    next_state = zero;
      end
      one1: begin // we've seen one 1
        out = 0;
        if (in) next_state = two1s;
        else    next_state = zero;
      end
      two1s: begin // we've seen at least 2 ones
        out = 1;
        if (in) next_state = two1s;
        else    next_state = zero;
      end
      default: begin // in case we reach a bad state
        next_state = zero;
        out = 0;
    endcase
endmodule
```

must include all signals that are input to state and output equations