Monolithically integrated UTC-PD with an RF-choke on InP for V-band communications

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***Abstract*—This work reports on the first monolithic integration of a planar bias circuit directly integrated with a uni-traveling carrier photodetector in an InP membrane platform. The bias circuit is optimized for V-band using first order approximations and numerical optimizations. Simulations demonstrate transmission loss below −3 dB and RF to DC isolation of at least 15 dB for a frequency range of 20 GHz around the center of the V-band. Fabricated integrated devices show external responsivities up to 0.035 A/W with measured RF to DC isolation of at least 25 dB between 40 GHz to 65 GHz.**

***Index Terms*—UTC-PD, monolithic integration, V-band, beyond-5G, microwave photonics**

I. Introduction

In microwave photonics and beyond-5G applications, integrated devices play a key role in miniaturization allowing massive system deployment [1]. More specifically, high speed photodetectors such as uni-traveling carrier photodiodes (UTC-PDs) [2] are a crucial component since they interface both the optical and electrical domain. The photodetector is required to be biased without the need of an external bias-tee, to best meet the requirement of miniaturization. This can be achieved by an on-chip bias circuit that allows for separate DC and RF connections interfacing with the UTC-PD.

InP based UTC-PDs demonstrate high responsivity and bandwidth simultaneously, in combination with high current operation due to a reduced space charge effect [2]. Various bias-free UTC-PDs have demonstrated decent performance [3]–[5] however, UTC-PDs generally show increased bandwidths and responsivities when a bias voltage is applied due to the increased internal electric field.
Although a discrete DC bias circuit can be assembled with a UTC-PD through wirebonding or by means of silver-filled epoxy [6], [7], this may cause additional RF losses and impedance mismatches, as well as high costs from component assembly. This can be evaded by means of monolithic integration [8].

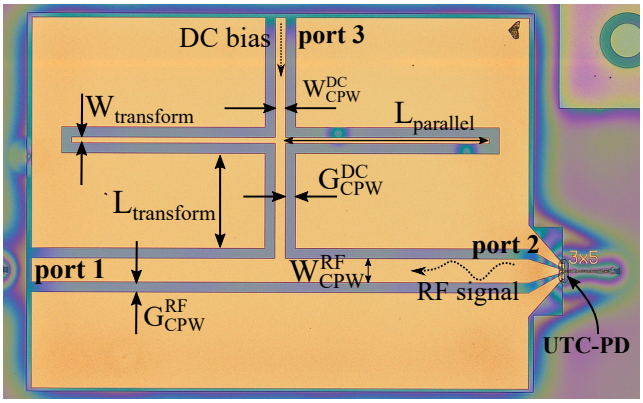

Fig. 1. Fabricated V-band bias circuit integrated with UTC-PD.

This work reports on the monolithic integration of a bias circuit and a UTC-PD [9] in the nanophotonic InP-Membrane On Silicon (IMOS) platform [10]. The bias circuit is designed based on a co-planar waveguide (CPW) RF-choke suitable to operate in V-band (40 GHz to 75 GHz). The component dimensions are numerically optimized to limit transmission loss, RF reflections and leakage from the RF to DC path. The monolithic integration of the bias circuit is realized during the final metallization step of the IMOS fabrication process. The external responsivity and electrical RF to DC isolation of the fabricated devices have been measured and analysed.

II. Design & Fabrication

A T-shaped RF-choke is used to apply the DC bias to the RF path of the UTC-PD. To prevent leakage of the RF signal (port 2 to 1) towards the DC path (port 3), an RF filter is placed in the DC path, as can be seen in Fig. 1. The RF-filter consists of a quarter wavelength transformer leading to a virtual RF open circuit, blocking the RF signal to be passed through the DC line [11], [12]. Capacitive decoupling of the RF line found in

TABLE I
MATERIAL PROPERTIES AND LAYER THICKNESSES

Material	ϵ_r	t [µm]
BCB (bonding)	2.5	1.8
BCB (planarization)	2.5	0.65
SiO_2 (cladding)	3.6	0.1
Si (substrate)	11.9	300
Gold (bias circuit)	-	0.4

a conventional bias-tee is not present in this design, and can be added as part of external circuitry e.g., capacitive input of an RF amplifier. The DC and RF CPW lines are optimized to achieve a 50 Ω characteristic impedance in V-band whilst being compatible with an RF probe with a 100 µm pitch for measurement purposes.

The bias circuit is designed based on a material stack consisting of a high resistivity 300 µm thick silicon substrate, followed by a combination of SiO_2 and BCB layers. The implemented layerstack is listed in Table I. The distance between RF signal line and the stub in the DC path $L_{\text{transform}}$ is designed to match the V-band center frequency f_0, and is calculated according to:

$$L_{\text{transform}} = \frac{c}{4 f_0 \sqrt{\epsilon_{\text{eff}}}}. \quad (1)$$

The parameters $W_{\text{transform}}$, L_{parallel} and $L_{\text{transform}}$ (Fig. 1) have been numerically optimized using EM simulation software based on performance targets for the reflections, transmission and RF to DC isolation.

The final device with a size of $1.5 \times 1.1\,\text{mm}^2$ is realized in the final metallization layer which directly connects to the p- and n-contacts of previously patterned UTC-PDs as can be seen in Fig. 1. The bias circuit is fabricated in combination with two active area variations of the UTC-PD being $5 \times 2\,\mu\text{m}^2$ and $5 \times 3\,\mu\text{m}^2$ (length x width), as well as a standalone device.

III. RESULTS

A. Simulation results

The simulated S-parameter results are shown in Fig. 2 excluding and including the UTC-PD. The S-parameters show optimal performance around the designed center frequency. Excluding the UTC-PD, transmission (S_{12}) remains below −3 dB, and RF to DC isolation (S_{13}) remain below −15 dB between 40 GHz to 65 GHz. Adding the UTC-PD results in slightly reduced RF to DC isolation. This difference is due to the presence of a potential impedance mismatch between the UTC-PD and the bias circuit.

B. Measurement results

Electrical S-parameter measurements of the fabricated devices have been performed using a VNA at frequencies up to 65 GHz. For the individual bias circuit, both transmission (S_{21}) and RF to DC isolation (S_{31}) are measured. For devices including a UTC-PD, only RF to DC isolation is measured. The measurement results are shown in Fig. 3, and clearly

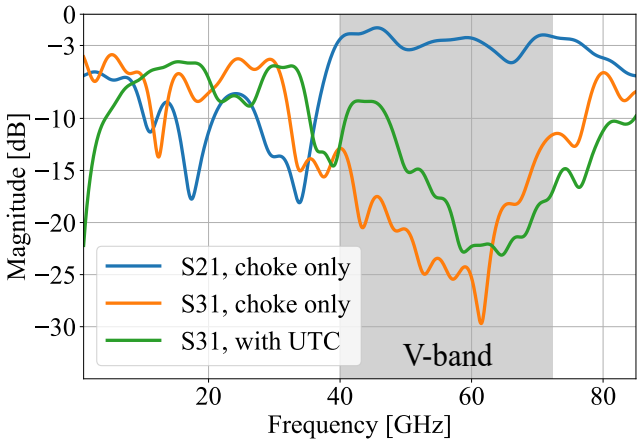

Fig. 2. Simulated S_{21} and S_{31} excluding and including a UTC-PD.

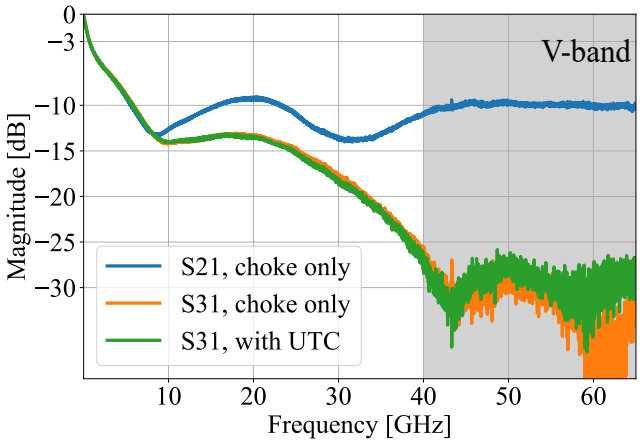

Fig. 3. Measured S_{21} and S_{31} excluding and including a UTC-PD.

demonstrate RF to DC isolation of at least −25 dB around the frequency band of interest. However, the measured S_{21} transmission curve also shows significant losses of around 10 dB compared to only 3 dB in the simulation results. This is likely caused by leakage paths towards highly doped contact layers, which were not removed properly during fabrication. This also explains the relatively high measured RF to DC isolation, which is effectively increased by the signal leakage.

In addition, the DC photocurrent of the fabricated devices was measured for various optical input powers while applying a bias of −4 V through the bias circuit. The results are shown in Fig. 4 and demonstrate linear behaviour with a calculated external responsivity of 0.024 A/W for the smaller PD and 0.035 A/W for the larger PD, while including fiber to chip coupling losses.

These measurement results demonstrate successful operation of the device, including increased RF to DC isolation in the frequency range of interest. Additional characterisation such as bandwidth measurements will be performed to further analyse the capabilities of the monolithically integrated device.

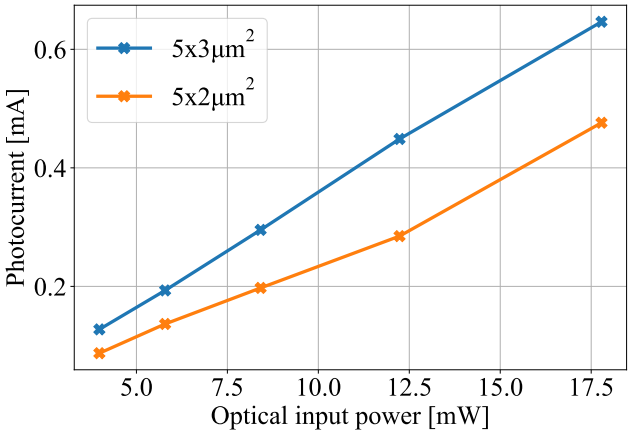

Fig. 4. Measured photocurrent as function of optical input power at −4 V applied through the bias circuit.

IV. Conclusions

Miniaturization of high speed opto-electronic integrated components operating in millimeter wave bands for beyond-5G applications will be a fundamental requirement to enable massive deployment. Therefore, monolithic integration of a bias circuit and UTC-PD is required as it can avoid losses, potential impedance mismatches caused by additional wirebonds as well as high costs from device fabrication and assembly, compared to discrete component integration. A monolithically integrated bias circuit based on a coplanar waveguide RF-choke using a quarter wavelength RF filter in the DC line is designed and fabricated in the nanophotonic InP-membrane on silicon platform.

The bias circuit is designed based on first order approximations and numerical optimizations to operate in V-band (40 GHz to 75 GHz). Simulation results of the bias circuit demonstrate transmission loss below −3 dB and RF to DC isolation of at least 15 dB for a frequency range of 20 GHz around the selected center frequency.

The fabricated bias circuits monolithically integrated with a UTC-PD demonstrate external responsivities up to 0.035 A/W. Additionally, electrical S-parameter reflection measurements of all fabricated devices demonstrate RF to DC isolation of −25 dB between 40 GHz to 65 GHz, with similar characteristics compared to the simulated results.

Acknowledgment

This work was supported by the Institute of Design, Optoelectronics and Sensing (IDEAS) Project INTENSE and it is partially funded by 5G STEP FWD (grant no. 722429) project as part of the European Union's Horizon 2020 research and innovation programme.

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