Co-integrated Non-Volatile Charge Trap Memory with III-V/Si Photonics

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***Abstract*— We review results on non-volatile charge-trap memory (CTM) integrated with III-V/Si photonics. The III-V/Si CTM cell facilitates non-volatile functionality for a variety of devices such as Mach-Zehnder Interferometers (MZIs), asymmetric MZI lattice filters, and ring resonators.**

Keywords—Silicon photonics, non-volatile, heterogeneous integration, memory, neuromorphic

I. Introduction

The ability to co-locate photonic computing elements and non-volatile memory provides an attractive path towards eliminating the von-Neumann bottleneck. We have leveraged our heterogeneous III-V/So optical interconnect platform to demonstrate integrated charge-trap memory (CTM) cells based on advanced metal-oxide-semiconductor capacitors (MOSCAP) [1]–[3]. These can be integrated with lasers [4], modulators [5], [6], and optical filters [7], [8] which are useful for high-speed optical modulation or matrix-vector-multiplication [9] with memory. The memory effect involves charge trapping in the dielectric stacks and triggers non-volatile optical phase shifts due to the overlap of photonics and carriers induced by the stored charges.

II. Design and Discussion

Our optical CTM cell is based on an engineered n-GaAs/Al_2O_3/HfO_2/Al_2O_3/HfO_2/Al_2O_3/Si heterogeneous MOSCAP structure, where the Al_2O_3 and HfO_2 serve as the tunneling/blocking oxide and charge trap respectively. In addition to high potential barriers, HfO_2 was chosen because of reported deep energy level traps (E_t = 1.5 eV) and high electron density traps ranging from 10^{19} – 10^{21} cm^{-3}. The center Al_2O_3 layer is inserted in between the HfO_2 for the convenience and compatibility of our bonding process. The single-mode waveguide structure is defined by a width, height, and etch depth of 500, 300, and 170 nm, respectively, as indicated in Fig. 1 (a-b). The wafer-bonded III-V region is primarily 150 nm-thick n-GaAs doped at 3×10^{18} cm^{-3}. Based on measured respective dielectric thicknesses of 1.7/4.0/2.0/4.0/0.5 nm (Fig. 1 (d)) and refractive indices of 1.75/1.90/1.75/1.90/1.75 at 1310 nm for Al_2O_3/HfO_2/Al_2O_3/HfO_2/Al_2O_3, the calculated optical confinement factors are Γ_{Si} = 64.49 %, Γ_{HfO2} = 1.637 %, and Γ_{Al2O3} = 0.82 % with an overall TE_{00} effective index of n_{eff} = 3.0971 and group index of n_g = 3.7914.

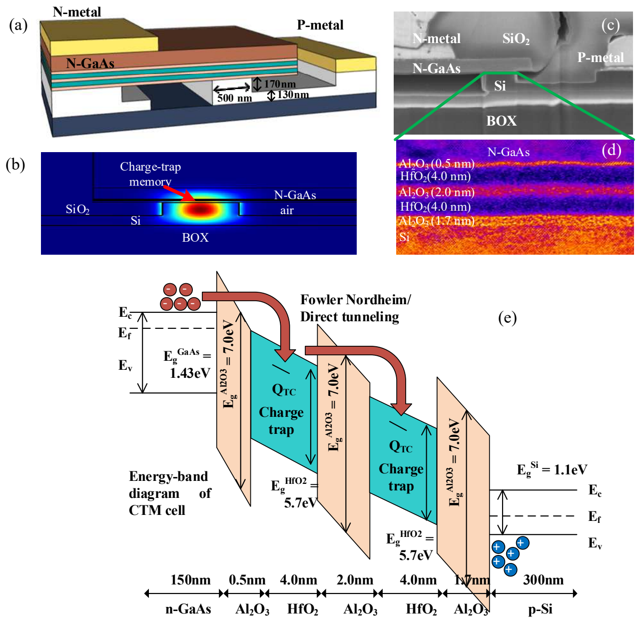

Fig. 1. 3-D schematic of the heterogeneous III-V/Si CTM cell with (b) SEM cross section and HRTEM image of CTM dielectric stacks. (c) Blown up material layer view and respective dimensions. (d) Energy band diagram during write process.

During the write process in this CTM, a positive bias is applied to the p-Si region which injects electrons from the highly doped n-GaAs into the high-k HfO_2 where carriers are trapped due the presence of charge traps (Q_{TC}) as shown in Fig. 1 (e). Once the HfO_2 region is fully charged, holes will accumulate at the p-Si/Al_2O_3 interface, thus altering the effective index of the optical mode due to the plasma dispersion effect. During the erase process, a reverse bias is applied to sweep out the trapped electrons, thus returning the optical CTM cell back to the initial electrical and optical state. Fig. 2 shows the non-volatile ring resonators transmission for the (a) write process and (b) erase process.

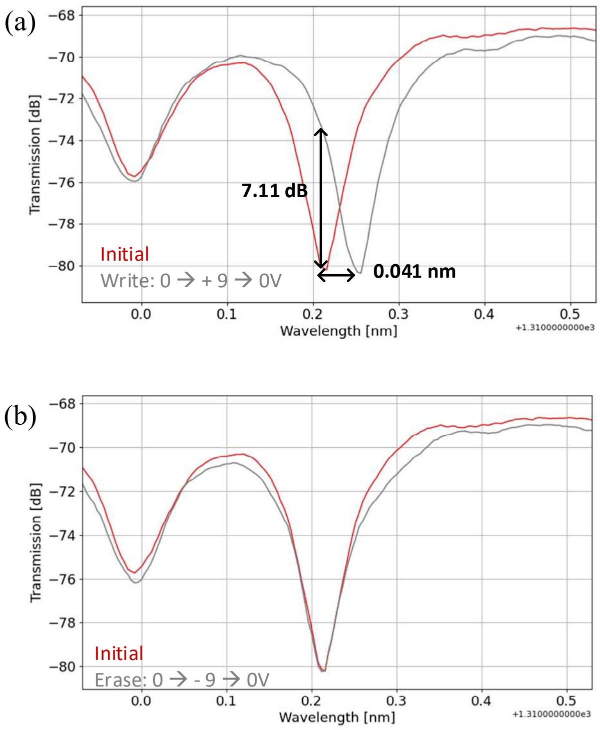

Fig. 2. Measured non-volatile ring resonator transmission for (a) write process and (b) erase process.

III. Conclusion

Our III-V/Si platform allows for seamless heterogeneous integration of a large family of co-mingled, high-quality actives, passives, and non-volatile elements for both novel interconnect and computing applications. Combined with continuous innovations in architecture [9], device physics and materials, our solution offers an avenue towards energy-efficient and scalable photonic neuromorphic computing.

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