Nanoseconds CDR Enabled by Clock Distribution and Protection Sequence Insertion in Optical Switching Networks

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***Abstract*—The scheme combining clock distribution and protection sequence insertion from the network perspective is proposed and experimentally investigated to implement a 3.1 nanoseconds clock and data recovery in optical switching networks without deploying burst-mode receivers.**

Keywords—clock and data recovery, optical switching network, clock distribution, protection sequence insertion

I. INTRODUCTION

With the fervently developing momentum of Metaverse, 5G services and cloud applications, the traffic explosion promotes the evolution from the electrical switching to high-capacity optical switching in data center networks (DCNs) [1]. However, implementing an optical switching system induces the frequent clock and data recovery (CDR) process because the optical switches break the optical links every time the incoming data changes [2]. There is no valid data received before the CDR procedure accomplished at the receiver side. The longer the CDR time spends, the lower throughput of the optical switching network is.

Researchers have focused on the device perspective to shorten the CDR time, where the burst-mode receiver is extensively evaluated. There are three typical methods for burst-mode CDR implementation in passive optical networks, 1. the fast-locked PLL, 2. oversampling CDR, 3. voltage-controlled oscillator type CDR [3]. However, the burst-mode receiver evolution presents a bottleneck on the transmission speed while the dedicated component is expensive. Moreover, with the optical switching techniques developing, such as the three dimension micro-electro-mechanical systems-based switch [4], the Liquid Crystal on Silicon-based switch [5] advanced to Mach-Zehnder interferometer-based switch [6], semiconductor optical amplifier (SOA)-based switch [1] and arrayed waveguide grating routers-based switches [7], the switching time cost from hundreds microseconds to nanoseconds. In light of these fast optical switches, a new fast CDR scheme implemented from the network perspective without deploying the burst-mode receivers is required to be compatible with the fast optical switching techniques.

As shown in Fig. 1(a), the excessive time consumed on the CDR derives from two aspects. First, when the optical link is enabled, clock frequency recovery embraced frequency detector (FD) costs most of the CDR time [8]. The deviation between the received signal clock and the local reference clock exerts a significant impact on the CDR time. Second, when the optical channel switches, the optical link suffers interruption with the absence of an optical signal in contrast to the continuous channel. After a certain period of time, the locking frequency in the phase-locked loop (PLL) module will shift and the lock lost at the receiver.

In this paper, we propose a scheme combining the clock distribution and protection sequence insertion from the network perspective to specifically address the above two aspects, respectively. Without dedicated circuits and high-cost

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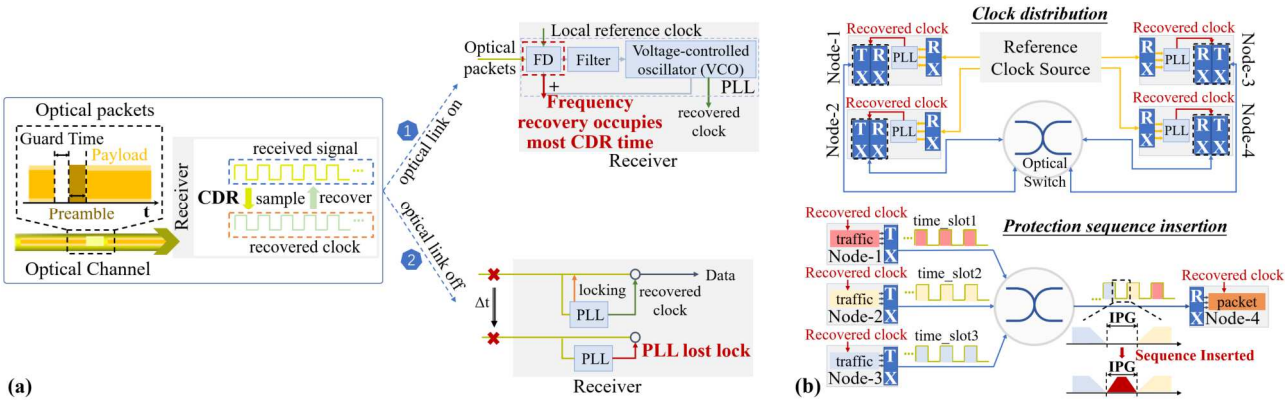

Fig. 1. (a) Two aspects of impacting the CDR time, (b) Scheme of clock distribution and protection sequence insertion.

burst-mode receiver deployments, the network clock is distributed to synchronize all the network nodes' clock frequency on the physical layer to avoid the time-consuming frequency recovery step. The protection sequence insertion between optical packets is applied in the network perspective to maintain the locking state of PLL. The experimental investigations validate the 3.1ns fast CDR enabled by the proposed scheme in a SOA-based 4*4 optical switching system. Enhanced by the nanoseconds CDR, the network achieves 2.5Mb/s packet granularity switching with zero packet loss.

II. Clock Distribution and Protection Sequence Insertion

To solve the problem of long-time cost on CDR in optical switching networks, we propose schemes to reduce the time without burst-mode receiver deployment. The clock distribution and the protection sequence insertion respectively surmount the long time spent on clock frequency locking and the PLL lost lock.

A. Clock Distribution

To reduce the PLL lock-in time, we distribute a unified clock frequency to all nodes at the physical layer in the optical switching network. There is a clock source deployed in the network. The clock is transmitted to every node via optical fiber link as shown in Fig. 1(b). The clock is recovered by the PLL in CDR module of these various nodes. The recovered clock is regenerated as the driven clock to apply on the communication to other nodes. Consequently, with the procedure of clock distribution, the clock frequency information contained in the received data is analogous to the CDR module driven clock. The execution can effectively decrease the time spent on the process from the frequency detector measurement to the voltage-controlled oscillator feedback. In virtue of the physical layer clock distribution, receivers can reduce CDR time in optical switching networks, while the impact from the network layer can be minimized.

B. Protection Sequence Insertion

In the transmission of optical switching networks, the optical link is shut down when it is switching. To guarantee the data signal integrity, the transmitter inserts the protection interval in front of optical packets and after the transmission accomplishment. The protection interval between optical packets constitutes the inter-packet gap (IPG) with a default zero optical intensity. This manifests the cessation of laser emission at the transmitter, as well as the optical link down. Subsequently, the frequency lock of PLL on receivers will gradually deteriorate to unlocked frequency with no valid signal input. Hence, the prolonged absence of data reception at the destination node can cause the loss of lock, while on the other hand, excessively long IPG exhibits analogous outcomes. To this end, we fill IPG with the protection sequence designed as binary "11001100" to maintain the PLL locked state. To be specific in the optical switching network, it is highly probable that many nodes send data to the same destination node. The protection sequence insertion is executed after optical packets of Node-1 and ,when the optical link switches, before the optical packets transmission of Node-2 as Fig. 1(b) illustrated. With series protection sequences inserted, the PLL module sustains locked state, while it tracks clock frequency faster and thus decreased the time consumed on CDR process.

III. Experiment Setup and Results

We demonstrate the proposed scheme clock distribution and protection sequence insertion on the field programmable gate array (FPGA) evaluation board based network nodes. These boards are FPGA board, while the small form pluggable plus (SFP+) optical module is 10 Gb/s FINISAR FTLX1471D3BCL-ZX (setup-A/B) and 25Gb/s SFP28 module FTLF1436P3BCL (setup-C). The wavelength of these modules is 1310nm. The preamble designed in our experiment is 9600bit, which corresponds to approximately 930ns as 300 clock cycles. The length of our payload in every packet is 1600 cycles (approximate 50kilo-bit). The gap length is the length of IPG between received optical packets. These packets are transmitted by Gigabit transceiver series Y (GTY) on FPGA boards [9].

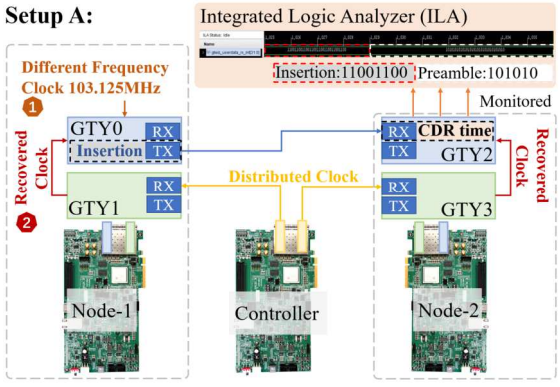

Fig. 2. The influences evaluation on clock frequency distribution and protection sequence insertion.

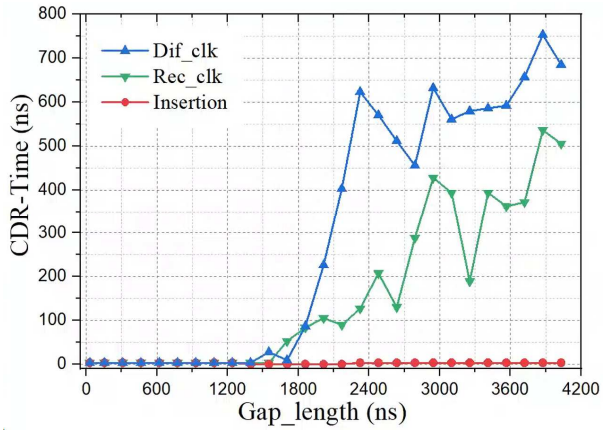

Fig. 3. CDR time of 3 experiment scenarios.

A. *Inherent Influences Evaluation*

To probe inherent influences from clock frequency distribution and protection sequence insertion, the experiment setup A is designed without switching as illustrated in Fig.2. The impact on clock distribution is evaluated with the time cost on CDR for packets driven by different frequency reference clock (Dif_clk) and the recovery clock (Rec_clk). In our experiment, the frequency of Dif_clk is set at 103.125MHz, while the reference clock operates on 156.25MHz. Moreover, the reference clock are supplied from the oscillator on the controller board, while the recovery clock is regenerated from the GTY1 and GTY3 receiver side on Node-1 and Node-2 depicted as Fig. 2. The recovery clock on both boards drive GTY0 and GTY2 to communicate with the other side. Furthermore, the CDR time is measured at GTY2 by means of the tool named Integrated Logic Analyzer (ILA) in Vivado.

As shown in the Fig.3, the CDR time of Dif_clk has obviously increased when the gap exceed 1500ns. The CDR time of recovered clock exhibits a gradual increase commencing at approximate 1700ns of the gap length. When the gap is more than 1800ns, the CDR time of Dif_clk intensely deteriorates. Until the gap length exceeds 3255ns, the CDR time is more than 362ns, irrespective of which clock drives the transmission. With the physical layer clock distribution, the CDR time has reduced 53% in average. The inherent influences of protection sequence insertion is also investigated in this scenario. The red curve in Fig. 3 also exhibits the result of protection sequence insertion driven by the Rec_clk. It shortens the time spent on CDR to 0ns and 3.1ns at the range from 30ns to 4030ns of gap length. The reduction of time cost on CDR is obvious, which greatly demonstrates the significant impact from the protection sequence insertion .

B. *Effectiveness evaluations in a SOA-based 4*4 Optical Swithcing System*

Based on the fundamental performance research of proposed schemes, setup B is planned to explore the CDR time cost of our scheme in the 4*4 semiconductor optical amplifier (SOA)-based 10Gb/s optical switching network. The SOA is Anritsu 1.3μm SOA module AA3F215CA. Fig. 4(a) presents the 4*4 optical switching system with the different set on the FPGA boards. FPGA-1, FPGA-2, FPGA-3, FPGA-4 are set as data source nodes while the FPGA-5 is set as the controller. The enable signals of the data transmission and SOA switch on are generated from controller. Moreover, optical packets forward to the same destination are aggregated by a 1*4 coupler in the system.

To protect the data integrity, the interval after SOA switching on and before the switching off is stable when it is set more than 120ns (approximate 40 clock cycles). In the experiment, the time spent on CDR of time-division multiplexing flows from Node-1, Node-2 and Node-3 is collected on Node-4. As Fig. 5 illustrated, the CDR time values are shown in average for many sample points on the same gap length. The measured CDR time of the transmitter driven by Rec_clk is relatively deteriorated to 331.7ns on the CDR time cost in the optical switching system. Along with the protection sequence binary “11001100…” inserted, the CDR time measured at Node-4 achieves 3.1ns. The results demonstrate the capability and feasibility of clock distribution and protection sequence insertion on nanosecond CDR time cost in the optical switching networks.

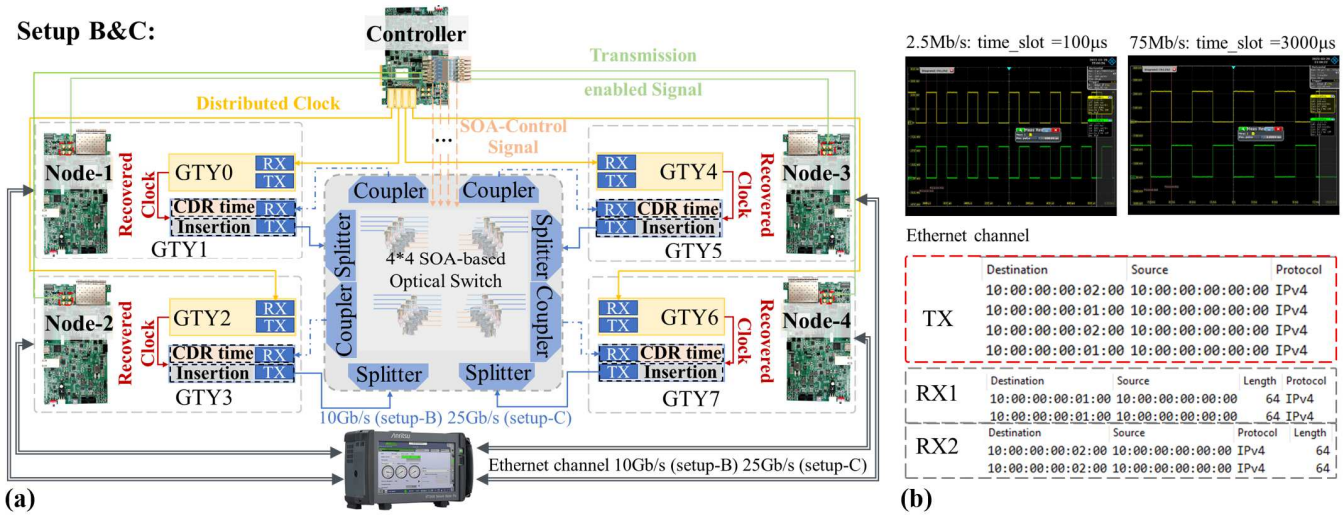

Fig. 4. (a) A 4*4 SOA-based switching to evaluate the fast CDR scheme (b) Monitored experimental parameters.

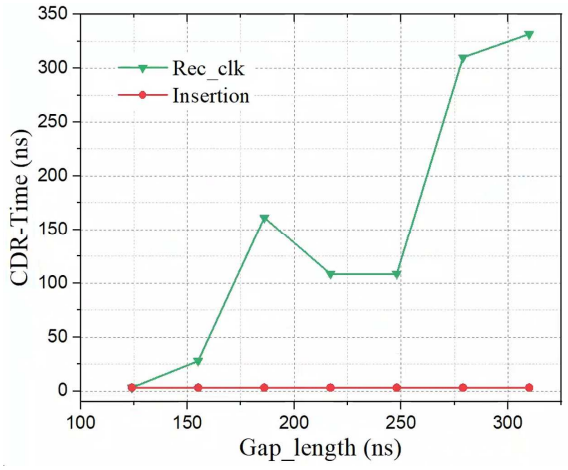

Fig. 5. The CDR time in SOA-based switching network

C. *Switching Capability Evaluations in the 4*4 Optical Swithcing System*

Enhanced with the time consumed reduction on CDR and fast SOA switching capability, the switching granularity of time-slot based optical switching network is measured as Fig. 4(a) depicted. The experiment uses Anritsu Ethernet Testing Center to generate data flows of two different destination addresses with a bandwidth of 25Gbps flowing to Node-4. With the switching program transmitting, data packets are forward by the identification with different Media Access Control Address (MAC) to the corresponding output port according the time_slot1, time_slot2 and time_slot3. Optical packets are distinguished in the time_slot1, time_slot2 and time_slot3 versus different optical link to Node-1, Node-2 and Node-3. The transmission is controlled by the controller with transmission enabled signal. The monitored experimental parameters are illustrated in Fig. 4(b). As presented in Fig. 6, the switching results of different time slot length which indicates the various packet granularities is measured. The data size of packets of 100 microsecond time slot is 2.5Mb, where the packet loss is zero even at the traffic load of 1.0. However, the performance deteriorates when the time slot length increased, corresponding to the high packet loss ratio exceed 47%.

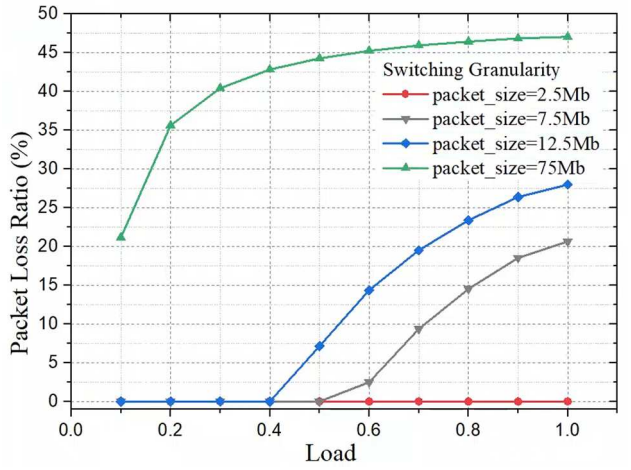

Fig. 6. The packet loss ratio versus different optical packet size.

IV. Conclusions

To sustain the optical switching technology evolution, the long CDR time takes crucial impact on the data reception. This paper proposed the application of clock distribution and protection sequence insertion to decline the CDR time cost to nanoseconds magnitude. The nanoseconds CDR time is verified in a SOA-based 4*4 optical switching system, while it is measured statistically with three transmitted nodes and a received node. Thereafter the scheme was implemented, the receiver achieves 3.1ns fast CDR, while the switching granularity achieves 2.5Mb/s with zero packet loss.

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