Inverse-designed Ultra-compact Polarization Splitter–Rotator in 180 nm CMOS Process

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***Abstract*—We presented an inverse-designed ultra-compact polarization splitter–rotator (PSR) fabricated in a 180 nm commercial silicon photonic foundry. The proposed PSR displays a low insertion loss (<1.3 dB) and low crosstalk (<−17.8 dB) over 80 nm wavelength by measurements.**

Keywords—Polarization splitter-rotator (PSR), inverse design, adjoint method, silicon-on-insulator (SOI)

I. INTRODUCTION

Silicon photonics is becoming a revolutionary technology enabling new applications in a wide variety of product areas, such as optical transceivers, optical computing, radio-over-fiber (ROF) and LiDAR (Light Detection And Ranging). The key to the success of silicon photonics is that it leverages standard complementary metal-oxide-semiconductor (CMOS) fabrication processes, allowing high-performance optical systems to be produced in large volumes at very low cost [1].

The traditional silicon photonic devices are usually designed based on physical intuition and engineering experience assisted with repetitive parameter sweeping. These traditional designs have long hampered the progress of high-density integration in silicon photonics because of their quite large size usually ranging from tens to hundreds of microns for even basic functions. Inverse design, which harnesses intelligent optimization algorithms [2-6] to explore the full design space of fabricable devices, is supposed to be a promising way to realize silicon photonic devices with both unprecedented footprint and relatively high performance. However, the devices generated by inverse design are often confronted with the problem of irregular small features that are difficult to fabricate reliably using photolithography, the mainstay of commercial CMOS fabrication. Generally speaking, most of the experimentally reported inverse-designed photonic devices have used either electron-beam lithography or focused ion beam machining, which have considerably higher resolution, but cannot be used for massive manufacturing [4-8].

In this work, we successfully demonstrate an inverse-designed ultra-compact silicon polarization splitter–rotator (PSR) in a commercial 180 nm CMOS process. The device was fabricated as part of the Chongqing United Microelectronics Center (CUMEC) 200 mm wafer multi-project wafer (MPW) foundry offering. The design methodology was based on our previous work [9]. The proposed PSR has a small footprint of 3×17 μm, which was optimized by the adjoint method [10]. Combined with geometric-constraint algorithm [11] and robust-optimization strategies [12], the fabrication feasibility and tolerance of the device was greatly promoted. Through additional layout post-processing, our design becomes fully-complied to the foundry's design rule checks (DRCs) without requiring any DRC waivers. The measured results show that our PSR has decent insertion losses (ILs) less than 1.3 dB and crosstalks (CTs) less than −17.8 dB within 80 nm wavelength range.

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II. DEVICE DESIGN

Our proposed PSR is based on 200 mm silicon-on-insulator (SOI) substrate with 2 μm BOX (Buried Oxide) and 220 nm top silicon. As shown in Fig. 1(c), it mainly consists of a bi-level polarization rotator and a fully-etched mode demultiplexer. The function of the polarization rotator is to convert a fundamental TM mode (TM0) input into a first-order TE mode (TE1) output while keeping a fundamental TE mode (TE0) input unchanged. The function of the mode demultiplexer is to demultiplex a combined TE0 and TE1 signal from the input waveguide to the two single-mode output waveguides.

Fig. 1(f) shows the top-view of our designed bi-level polarization rotator with Fig. 1(a) showing part of its cross-section view. The silicon slab height (denoted as H_{slab}) was restricted to 70 nm by the foundry. The boundaries of the rib and slab layers are defined by smooth quadratic splines, where the vertical position of each spline node can be optimized through our bi-level shape adjoint method [9]. We adopted a multi-figure of merits (FOMs) strategy in which we not only focus transmission performance with the ideal slab height (70 nm), but also consider the performance of slab height deviation groups ($\Delta H_{slab} = \pm 10$nm). In this way, the device robustness against the partially etching depth could be strengthened. More detail of the design flow could be found in [9].

Fig. 1(g) illustrates the comparison of our inverse-designed mode demultiplexer before/after layout post-processing with Fig. 1(b) showing part of its cross-section view. This part was designed by topology adjoint method with worst-case optimization strategy [12], where the FOM at each iteration took the worst one from three unique designs (namely

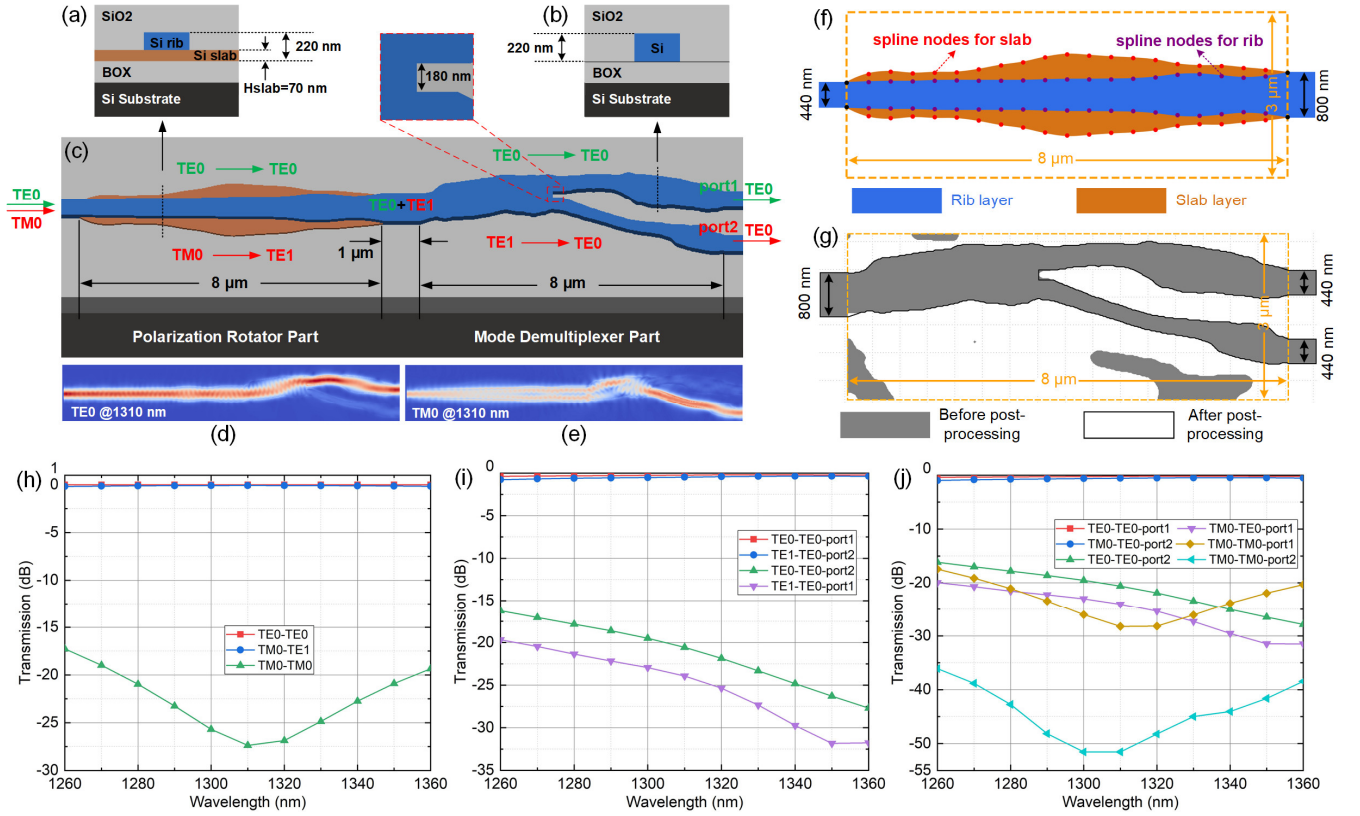

Fig. 1. Cross-section views of (a) the polarization rotator part and (b) the mode demultiplexer part. (c) Schematic of the inverse-designed PSR. The enlarged part shows the detail with 180 nm minimum feature size. (d) and (e) show the simulated electric fields through the PSR at 1310 nm when TE0 and TM0 modes input, respectively. (f) Final design for the polarization rotator. (g) Comparison of the designs before/after layout post-processing for the mode demultiplexer. Simulated transmission performance (h) for the polarization rotator, (i) for the mode demultiplexer and (j) for the assembled PSR, respectively.

ideal-etched, over-etched, and under-etched). This kind of strategy could improve fabrication tolerance against the variation of etching widths and implement minimum feature size control as well. The originally optimized design is filled in gray shown in Fig. 1(g). To make our structure more concise, we manually removed some physical meaningless islands. Next, we manually mended all illegal details to make our design obey the foundry's DRCs. Note that the minimum space was restricted to be 180 nm. The mended contour of the final design is plotted with black line in Fig. 1(g). Thanks to the implement of robust-optimization, the device performance does not degrade obviously after all the above post-possessing.

Fig. 1(h)-1(j) display the simulated transmission performances for the designed polarization rotator, the mended mode demultiplexer and for the assembled PSR, respectively. Our inverse-designed polarization rotator exhibits excellent ILs (TM0 < 0.18 dB, TE0 < 0.01 dB) and a low CT (< -17.3 dB) over the entire O band. Our mode demultiplexer after post-possessing exhibits decent ILs (< 0.78 dB) and CTs (< -16.3 dB) for both TE0/TM0 input over the entire O band. The assembled PSR also exhibits low ILs (TE0 < 0.4dB, TM0 < 1 dB) and low CTs (< -16.1 dB) over the entire O band. Fig.1(d)-1(e) show the simulated electric fields through the proposed PSR at 1310 nm when TE0 and TM0 modes input, respectively.

III. Experimental Results

The microscopic images of the fabricated PSR test groups with TE/TM grating couplers (GCs) input are shown in Fig. 2(a)-(b), respectively, while the enlarged profile of the PSR is shown in Fig. 2(c). Since the fabrication of the PSR needs two steps of etching, the misalignment between different masks for photolithography may deteriorate the performance of the polarization rotator. To better investigate this impact, three sets of PSRs with different mask offset were fabricated together. Fig. 2(d) exemplifies a +40 nm mask offset between the rib and the slab layers. Note that we only focus on the mask misalignment perpendicular to the light propagation direction, and the mask offset here is a kind of preset in the layout, not the actual misalignment during fabrication. The device measurements were conducted with a tunable laser, a polarization controller, fiber alignment stages and an optical power meter. TE and TM GCs, which also work as TE and TM type on-chip polarizers, respectively, were used to receive or transmit light from/into the fibers.

Fig. 2(e) displays the spectra of the TE and TM grating coupler references for calibration with the inset showing their microscopic images. It can be observed that TE/TM GCs have similar peak insertion losses and close peak wavelengths around 1300 nm.

Fig. 2(f)-2(h) show the measured IL and CT performance for the fabricated PSR with no mask offset, -40 nm mask offset and +40 nm mask offset, respectively. All spectra have been normalized to the GC references. The ripples in the measured spectra, are mainly due to the Fabry-Perot effect created by reflections between the input and output grating couplers. It can be seen that the PSR with no mask offset exhibits the best performance with ILs below 0.8 dB/1.3 dB and CTs below -17.8 dB/-21.6 dB for TE0/TM0 input over a wide wavelength range from 1260-1340 nm, which coincide quite well with the simulation results. For PSRs with ±40 nm mask offset, the IL for TM mode deteriorates more obviously than that for TE mode, and the CTs for both modes

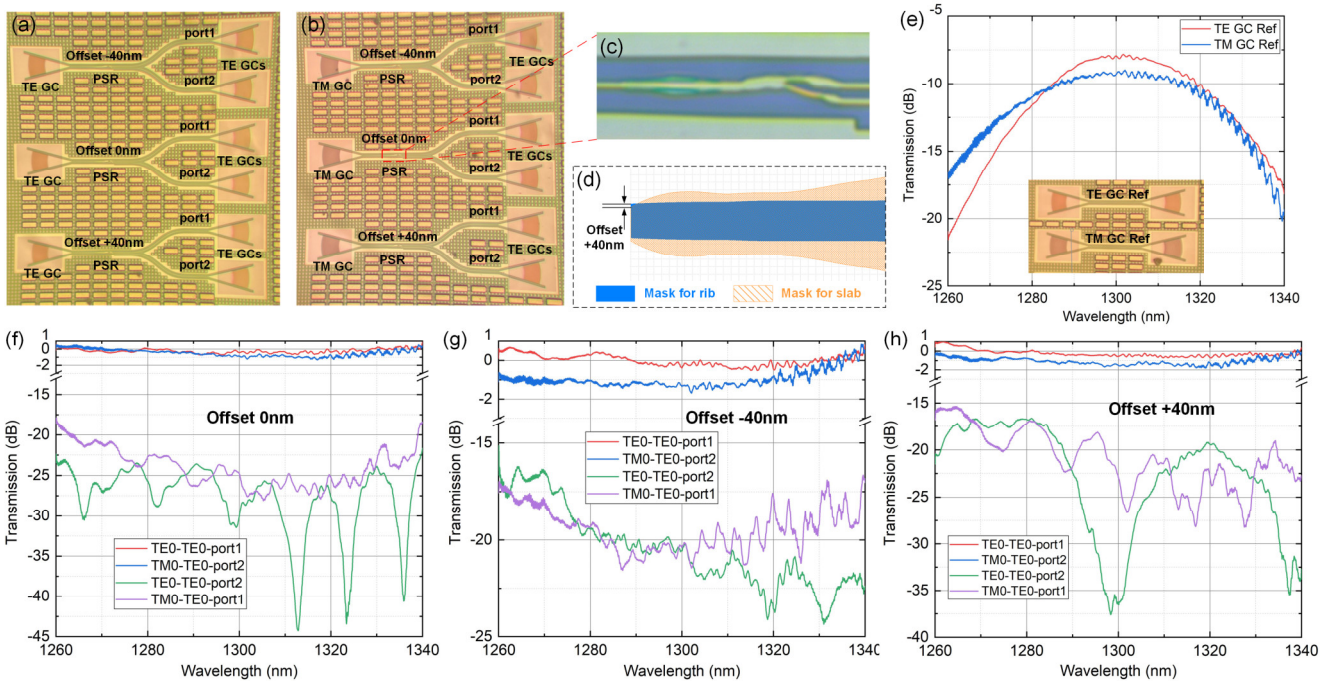

Fig. 2. Microscopic images of the fabricated PSR test groups with different layer offsets when (a) TE and (b) TM grating couplers input. (c) Enlarged profile of the proposed PSR. (d) Sketch map to show a +40 nm mask offset between the rib and the slab layers. (e) Spectra for the TE and TM grating coupler references. The inset shows the microscopic images of the fabricated TE/TM grating coupler references. Measured IL and CT performance for the fabricated PSR with (f) no mask offset, (g) -40 nm mask offset and (h) +40 nm mask offset, respectively.

deteriorates slightly. More specifically, the PSRs within ±40 nm mask offset still exhibit acceptable ILs below 0.8 dB/1.8 dB for TE/TM and CTs below 15 dB for both modes over 80 nm wavelength range, which proves that our proposed PSR has decent tolerance against mask misalignment.

IV. Conclusions

In summary, we have experimentally demonstrated an inverse-designed SOI-based PSR fabricated by 180 nm commercial silicon photonic foundry. Our proposed PSR has an ultra-compact footprint of 3×17 μm with acceptable insertion losses (< 1.3 dB) and crosstalks (< −17.8 dB) in a wavelength range of 80 nm with no extra layers or an air cladding. By using the multi-FOMs and the worst-case optimization strategies, the device fabrication tolerance is promoted. The implement of geometric-constraint and layout post-processing also guarantees the CMOS compatibility of the design. We believe, our design methodology can be applied to a wide variety of nanophotonic devices suitable for massive CMOS manufacturing.

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