Calibration-free reconfigurable silicon optical signal processor

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***Abstract*—Reconfigurable silicon optical signal processors using interferometer meshes are essential in optical interconnection and optical computing systems. However, due to random phase errors in the tuning elements, most of the pervious demonstrations either require hundreds of self-configuration iterations or calibration of all the tuning elements. Here, we propose and demonstrate a calibration-free silicon optical signal processor based on 5×5 interferometer mesh using low-phase-error Mach-Zehnder interferometer (MZI). The proposed processor can be tuned easily to achieve various functions, including multi-channel optical switch and matrix multiplications. Our work paves the way towards large-scale calibration-free silicon photonic MZI-based processors.**

Keywords—silicon photonics, optical signal processing, integrated optics, optical switches, matrix multiplication

I. Introduction

The past few years have seen high growth in areas such as artificial intelligence, resulting in an increasing global demand for computing power[1]. With electronic processors approaching their limits and Moore's Law slowing down or even failing, emerging optical computing is seen as one of the possibilities that can surpass the performance bottleneck of electronic processors. One of the mainstream solutions is implementing integrated optical signal processors thanks to their advantages of low energy consumption, low cost and system stability [2]. Among various integrated materials, silicon-based optical signal processors show great superiority in terms of footprint compactness, complementary metal-oxide-semiconductor (CMOS) compatibility, high thermo-optic efficiency and have the potential to fabricate large-scale signal processing networks[3].

To date, numerous silicon-based optical signal processors based on interferometer meshes have been demonstrated. A programmable hexagon signal processor has been demonstrated to realize over 20 different functionalities through self-configuring programming[4]. A 8×8 silicon-based linear optical network (LON) was proposed and can be tuned to achieve various functions, including multichannel optical switching and tunable optical filter [5]. A similar interferometer mesh-based optical neural chip (ONC) has been demonstrated for complex-valued optical computing, achieving strong learning capabilities compared to real-valued counterpart[6].

To reconfigure these optical signal processors, one of the keys is to control the tunable basic building block: Mach-Zehnder interferometers (MZIs). However, due to the manufacturing errors, traditional singlemode MZIs have significant random phase errors, which make the initial state deviate seriously, wasting extra heating power for calibration[7]. Therefore, the system power consumption and complexity are significantly increased, thus limiting the applications of optical signal processors in optical interconnection and optical computing systems.

In this paper, we implement a silicon optical signal processor based on 5 × 5 multiport interferometer mesh using low-random-phase-errors MZIs. Without calibration of the tuning elements, the device can be tuned to achieve various functions, including reconfigurable multichannel optical switch and 3 × 3 matrix multiplications. Our work enables the control of the reconfigurable silicon optical signal processor, making large-scale silicon optical signal processor based on MZIs more viable.

II. Principle and Expeimental Setup

The optical transformation of an ideal *N*-channel multiport interferometer can be described as an $N \times N$ unitary scattering matrix U acting on electric fields. The transformation between channels n and m ($n = m$-1) using lossless MZIs is[8]

$$T_{n,m}(\theta,\phi) = \begin{bmatrix} 1 & 0 & & & & & & 0 \\ 0 & 1 & & & & & & \\ & & \ddots & & & & & \\ & & & e^{i\phi}\cos\theta & -\sin\theta & & & \\ & & & e^{i\phi}\sin\theta & \cos\theta & & & \\ & & & & & \ddots & & \\ & & & & & & 1 & 0 \\ 0 & & & & & & 0 & 1 \end{bmatrix} \quad (1)$$

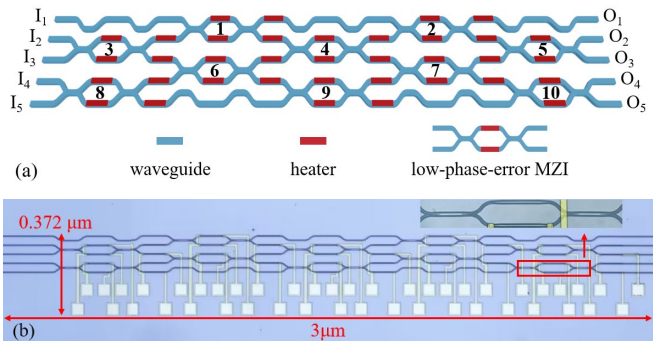

Fig. 1. (a) The structure of 5 × 5 multiport interferometer; (b) The picture of the fabricated chip.

where $\theta \in [0,\ \pi/2]$, $\phi \in [0,\ 2\pi]$. Noting that the U matrix can be decomposed into the product of multiple $T_{n,m}$. Thus by adjusting each $T_{n,m}$ (i.e. MZI), U (i.e. multiport interferometer) can be set to an arbitrary unitary matrix.

Fig. 1(a) shows the schematic of 5 × 5 multiport interferometer mesh based on MZIs. There are 10 MZIs (#1−#10) with 20 heaters on the upper and lower arms for configuring the optical path. Here, MZI with low random phase error is used. With phase shifters width increased to 2 μm, the random phase errors of the MZI are less than a third of those of the conventional MZI with 0.45-μm-wide single-mode phase shifters[9].

Fig. 1(b) shows the picture of the fabricated chip in silicon. The silicon-on-insulator (SOI) wafer has a 220-nm-thick silicon core layer and a 2-μm-thick buried oxide (BOX) layer. The chip's area is 3 μm × 0.372 μm. All the heaters are led to the bottom side of the chip for wire-bonding to a printed circuit board (PCB). For multiport coupling of the chip, a seven-channel fiber array is used, and the measured in-and out-coupling loss is about 13 dB.

III. Chip Characterization

The basic building block of the 5 × 5 multiport interferometer mesh is the low-phase-error MZI. To verify the performance of the MZI, we measure the cross-port and bar-port transmission spectra from 1530 to 1570 nm in the off and on states. The characterization results of the representative device (MZI#1 in Fig. 1(a)) are shown in Fig. 2(a), which exhibit low excess losses (ELs) (~0.35 dB) and high extinction ratios (ERs) (>30 dB).

The transmissions at the cross- and bar-ports of this MZI is then measured by sweeping the heating power from 0 to 80 mW when it operates at 1550 nm, as shown in Fig. 2(b). It can be seen that a heating power of 25 mW is needed to generate a phase shifting of π. The switch speed was also characterized, as shown in Fig. 2(c). It can be seen that the rise/fall time of the optical switching is about 20 μs.

Fig. 2(d) shows the measured results for the ratio Q_0/Q_π for all MZIs on the device, where Q_π is the power to generating an additional phase shifting of π needed for the ON state, and Q_0 for the OFF state. It can be seen that the ratios Q_0/Q_π for all MZIs are smaller than 0.2, which is much lower than those conventional MZIs with 0.45-μm-wide single-mode phase shifters [9]. Such a property can help reduce the calibration complexity and the power consumption greatly, particularly for a signal processor with numerous MZI elements.

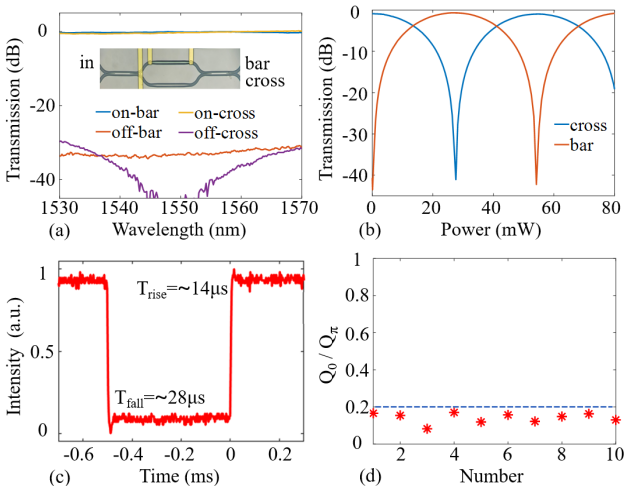

Fig. 2. Measurement results of a representative MZI: (a) Transmissions at the cross- and bar-ports of the MZI; (b) Transmissions at the cross and bar-ports for the central wavelength as a function of the heating power; (c) The switching time; (d) Q_0/Q_π for all MZIs in the device.

IV. System Demonstration

A. Multichannel Optical Switch

To verify the reconfigurability of the signal processor, we first configure it into a multi-channel optical switch. In this case, the power from port I_1 is switched into different outputs O_1 - O_5, separately. Fig. 3(a) shows the maximum (switch on, solid line) and minimum (switch off, dashed line) transmission of different output ports when the power is input from I_1. For example, the black solid line in Fig. 3(a) shows the transmission at port O_5 when the power in I_1 is only switched to the output O_5, while black dashed line shows the transmission at the same output port (O_5) when the power in I_1 is not switched to that output port. As we can see from Fig. 3(a), the crosstalk is higher than 20 dB, which means the power from I_1 can be successfully switched into different outputs O_1 - O_5.

To be more specifically, Fig. 3(b) shows the transmission at each output port O_1 - O_5 when the power form I_1 is only switched to O_1 within the wavelength range of 1530−1570 nm. Most of the power is output at port O_1, while the power in other output ports are all below −20 dB. This demonstrates a low-crosstalk optical switch.

B. Universal Unitary Matrix

We then configure the device into a 3×3 matrix multiplier, as shown in Fig. 4(a), where the thick yellow line being the used optical path and the thin black line being the unused part. Each intersection corresponds to a MZI.

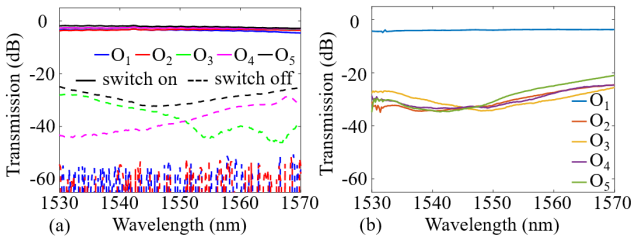

Fig. 3. Measurement results for multichannel optical switching. (a) The maximum and minimum power at each output port when only the power is input into port I_1. (b) Transmission at each output port when the power from I_1 is only swithced into O_1.

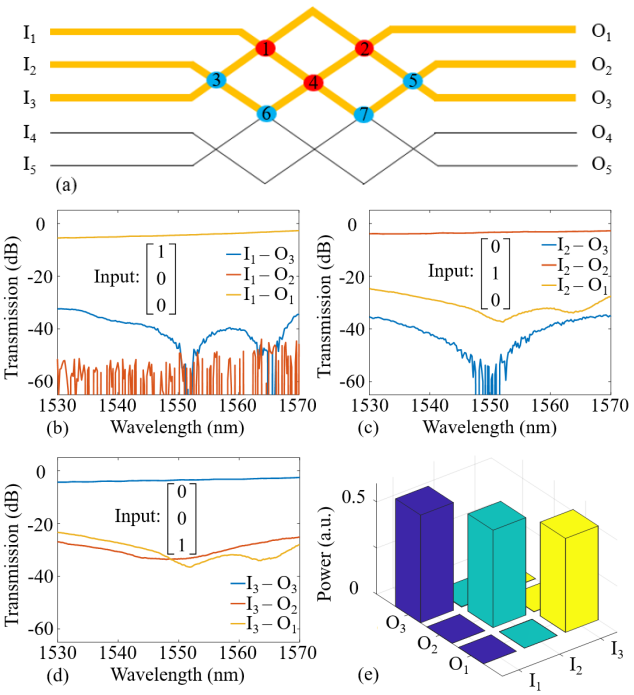

Fig. 4. Statistic scheme for the anti-diagonal matrix. (a) Mesh configuration for 3 × 3 matrices. (b) - (d) Transmissions of each output port with different input matrices. (e) The power distribution of each outport with different input power.

The 3 × 3 matrix multiplier is firstly configured to achieve an anti-angle matrix as follows:

$$\begin{bmatrix} 0 & 0 & 1 \\ 0 & 1 & 0 \\ 1 & 0 & 0 \end{bmatrix} \tag{2}$$

Fig. 4(b) - (d) shows the transmissions of each output port when the input matrix is [1 0 0], [0 1 0], and [0 0 1], respectively. In fact the function of this matrix is easy to understand: when the input is [1 0 0], after multiplied with the anti-angle matrix programmed by 3×3 matrix multiplier chip, the output matrix is [0 0 1], which means the power from I_1 is only switches to port O_3, the same principle can be used when the input is [0 1 0], or [0 0 1]. The corresponding power distribution at the output ports when the input matrix is [1 0 0], [0 1 0], and [0 0 1] are shown in Fig. 4(e).

Then we configure the device into a more complex 3 × 3 matrix in (3). When the input power is [1 0 0], the output power should be [1/4 1/4 1/2]. Fig. 5(a) shows the output power at different outputs when the input power is [1 0 0], indicates that the ratio of O_1, O_2 and O_3 output power is 1:1:2. Fig. 5(b) shows the corresponding power distribution at the output ports.

$$\begin{bmatrix} \frac{1}{2} & -\frac{1}{2} & -\frac{\sqrt{2}}{2} \\ -\frac{1}{2} & \frac{1}{2} & -\frac{\sqrt{2}}{2} \\ \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & 0 \end{bmatrix} \tag{3}$$

Table 1 lists the theoretical and experimental voltages applied to each MZI to achieve the matrix multiplication in Fig. 5. As we can see from Table 1, with the help of the low-phase-error MZI technique, the experimental voltages on all

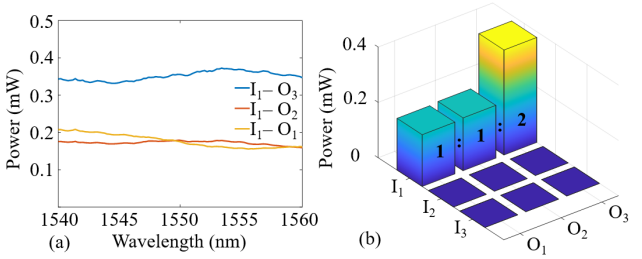

TABLE I. VOLTAGE FOR CALIBRATION

Number	1	2	3	4	5	6	7
Theoretical	2.77	2.90	2.15	3.16	2.33	2.21	2.15
Experimental	2.35	2.88	2.15	3.16	2.33	2.21	2.15

Fig. 5. Statistic scheme for the general matrix. (a) Output power at different outputs when the input is [1 0 0]. (b) Power distribution at the output ports at 1550 nm when the input is [1 0 0].

MZIs to achieve the desirable function is almost the same as the theoretical one. For the present chip, low-phase-error MZSs, which not only relieves the calibration complexity but also reduces the total power consumption. As a result, the optical signal processor can be easily configured to achieve different matrix multiplication.

V. CONCLUSION

We have designed, fabricated and demonstrated a silicon optical signal processor based on multiport interferometer mesh using low-phase-error MZI. This processor is reconfigured as a multichannel optical switch and 3 × 3 matrix multiplier without calibration of the tuning elements. This work opens a new solution for calibration-free large-scale silicon optical signal processors with many tuning elements.

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