Monolithic Integration of III-V Quantum Dot Lasers and Silicon Waveguides on SOI Platforms

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***Abstract*—We embedded InAs QD lasers on trenched SOI, enabling monolithic integration with butt-coupled waveguides. High-performance lasers with max output power of 6.8 mW and -6.7 dB coupling efficiency achieved.**

Keywords—silicon photonic integration, quantum dot laser, SOI platforms

I. INTRODUCTION

One of the main methods for achieving power-efficiency, high optical interconnect integration, and densely integrated optical interconnects is the integration of photonics chips and on-chip lasers[1-4]. External laser coupling has been achieved on a silicon-based integrated chip using a 200mm silicon-on-insulator (SOI) wafer[5,6]. Bonding III-V/Si heterogeneous integration is considered the most promising way to achieve on-chip light sources[7-10]. However, with the rapid development of silicon photonics in fields such as artificial intelligence, data centers, high-performance computing, light-detection and ranging(LIDAR), and microwave photonics[11], fully integrated light sources are beginning to demonstrate more advantages as a higher integration and lower power consumption technology. From the perspective of silicon photonics integration, integrating active and passive devices on the same SOI platform can more efficiently couple light into silicon waveguide devices.

This study demonstrates a method for embedding QD lasers in pre-fabricated laser grooves and silicon waveguides (WGs), enabling laser on-chip coupling to silicon waveguides and providing huge potential for achieving fully integrated silicon photonics chips.

II. DESIGN AND FABRICATION OF SOI TEMPLATE

The complete process of embedding laser is shown in Fig. 1, including the growth of III-V gain material in the trench and the subsequent fabrication of the laser. As shown in the figure, an oxide layer is grown on top of the waveguide section in a pre-fabricated SOI substrate with the waveguide. The area for embedding the laser diode is formed by etching a groove, and it should be noted that the horizontal alignment accuracy between the laser diode and the waveguide is an important factor affecting the coupling efficiency. Therefore, in order to obtain higher coupling efficiency, the etching depth of the

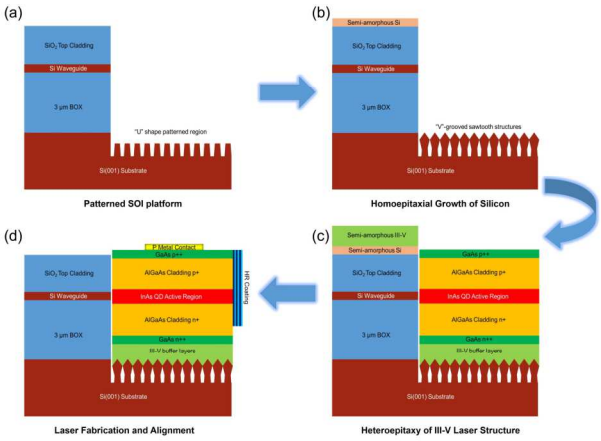

Fig. 1 Schematic diagram of patterned SOI trenches and design of edge coupler. Step 1: The exposed silicon substrate patterned with silicon gratings. Step 2: Homoepitaxially formed Si V-groove structures over the top of silicon gratings. Step 3: InAs/GaAs QD laser epi-structures directly grown inside the SOI trench. Step 4:Fabricated narrow ridge laser with one-side as-cleaved

trench needs to be precisely controlled, so that the active region of the laser is at the same height as the silicon waveguide. As shown in step 1 and step 2 in the Fig. 1, in order to avoid crack formation caused by anti-phase domains (APDs), threading dislocations (TDDs), and thermal mismatch[12,13], we first etched a U-shaped grating on the silicon substrate, and then grew a layer of silicon on the grating to form a silicon (111)-faceted. As shown in step 3 of the Fig. 1, another important issue is that during the growth of silicon and III-V materials in the trench, they will also deposit in polycrystalline form outside the trench. This will cause a large height difference between the inside and outside of the trench. Due to the existence of this height difference, the uneven distribution of photoresist at the edge of the trench will affect the photolithography of the laser structure in subsequent fabrication processes. To solve this problem, before starting the laser fabrication process, we used a wet etching method of H_3PO_4: H_2O_2: H_2O (1:2:20) to remove excess polycrystalline

material, as shown in step 4 of the Fig. 1. After removing the excess III-V material, the standard edge-emitting laser fabrication process was used to obtain the laser diode structure, which was then thinned to 100μm. The two facets of the laser, one away from the waveguide, were formed into cavity facet by cleaving. The laser facet near the waveguide cannot form a reflective cavity surface through cleaving. Therefore, we used focused ion beam (FIB) etching to form the reflective cavity surface of the laser. The facet with cleaved was coated with HR coating to improve the performance of the laser.

III. Monolithic Epitaxial Growth and Fabrication of III-V Lasers on Trenched SOI Substrate.

Fig. 2a shows the comprehensive schematic diagram of the laser epitaxial structure on the SOI template. Initially, a 10nm AlAs nucleation layer is deposited to optimize the GaAs/Si interface and suppress the formation of APD. Subsequently, a 2100nm III-V buffer layer is grown, which includes an InGaAlAs/GaAs quantum well defect filter (DLFs) and a GaAs/AlGaAs superlattice layer (SL)[14], to achieve a flat and APD-free GaAs surface. The surface is characterized by atomic force microscopy (AFM), and in a 5×5 μm² area, the root-mean-square roughness (RMS) of 0.8 nm as shown in Fig 2b.

Using the high-quality GaAs/SOI substrate, a standard InAs/GaAs QD laser is grown[15,16]. The active region of the laser consists of 7 layers of InAs quantum dots with a 400 nm N-/P-doped GaAs contact layer above and below, and a 1400 nm N-/P-doped $Al_{0.4}Ga_{0.6}As$ cladding layer. To characterize the optical gain properties of the InAs QD laser grown within the trench, the room temperature photoluminescence (PL) spectra of the InAs QD laser grown on both the trench GaAs/SOI substrate and the GaAs substrate are tested as shown in Fig 2c. The PL spectrum of the trench GaAs/SOI substrate has a half-width of 33 nm, which is smaller than that of the PL spectrum on the GaAs substrate. Moreover, the peak intensity of the two PL spectra is almost identical.

Fig. 2d shows the inclined InAs QD laser of prefabricated silicon waveguide microscope images. As mentioned earlier, the horizontal offset between the laser ridge and the silicon waveguide is less than 250 nm. At the coupling tip of silicon WGs, fork-like spot-size converter is implemented to increase dimensional tolerance of laser-waveguide alignment offsets, as shown in Fig 2e. The FIB processing is also used here to further polish to form a high gain cavity, as shown in Fig. 4g. The smoothness of the cavity is one of the most important factor affecting the performance of laser. Therefore, the initial separation of large-current etching III-V materials and silicon materials is used when the FIB is etching. Subsequently, the smaller current FIB opposite wall was finely polished to obtain a smooth laser facet. In Fig. 4f and Fig. 4g, we compared the wet etched laser facet and FIB polished laser facet. The Fig. 4f showed the wet etched laser facet of about 5 μm wide coupled between the laser and the silicon waveguide. It can be observed that the steepness and roughness of the wet carved laser surface are not perfect. After the FIB is polished in the SEM image below Fig. 4g, the laser facet become more smooth, similar to the cleaved facet.

IV. Characterizations of On-Chip Integrated Lasers

In order to examine the coupling efficiency of laser to WGs, we selected a laser that grows directly in the SOI trench, both facet are cleaved, and the light-current (L-I) is

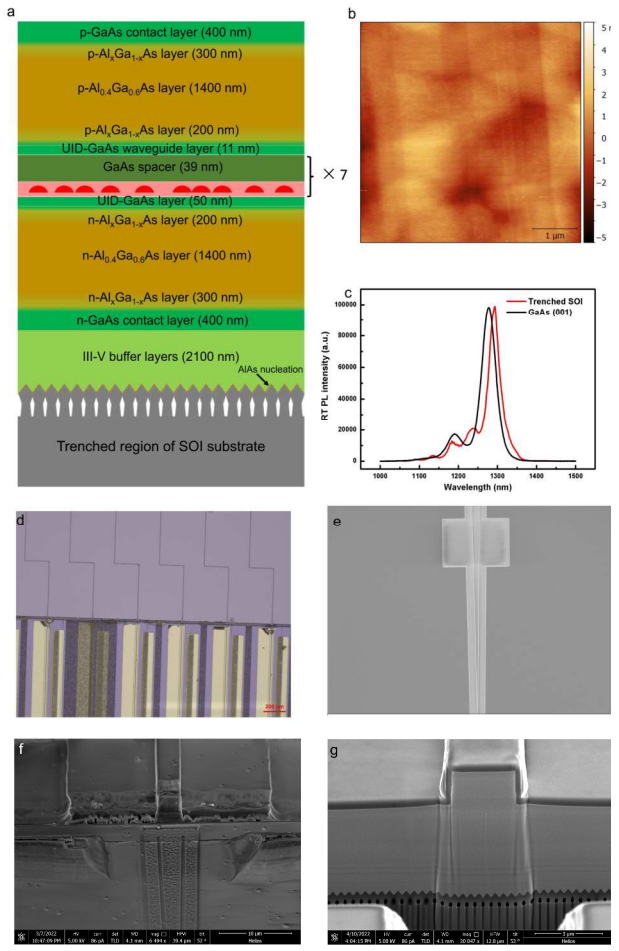

Fig. 2 Epitaxial growth structures, material characterization and fabricated monolithically integrated InAs QD lasers coupled to silicon waveguides. a Schematic of the laser epi-structures. **b** Surface AFM image of 2100 nm thick III-V buffer layers grown on trenched SOI before epitaxial growth of laser structures (RMS ~ 0.8 nm). **c** PL spectra comparison between InAs QDs grown on trenched SOI substrate and standard GaAs substrate under identical conditions. **d** microscope image of fabricated narrow ridge laser directly coupled with silicon waveguides using fork-like mode converter. **e** SEM image of silicon waveguide mode converter. **f** SEM image of monolithically integrated laser and silicon WG. **g** SEM image of the embedded lasers with FIB etched facet.

measurements as a reference. For the trench laser with silicon WG, we test the L-I curves and optical spectra by collecting laser from silicon WGs. The temperature dependent L-I curves of embedded laser without silicon WG (so-named as reference laser) are measured in Fig. 3a, which manages to lase up to 95 °C in continuous-wave (CW) current operation. At room temperature, the threshold current is 50 mA, and the maximum output power is 37 mW at injection current of 250 mA. The threshold of the laser that coupled with the silicon WG is 65 mA under the CW mode as shown in Fig 3b. The maximum working temperature is reduced to 85 °C. The relatively higher threshold current and lower maximum working temperature are caused by increased thermal accumulation inside the laser trench with surrounding BOX layer. Inset of Fig. 3b compares the L-I characteristics of an

embedded laser before and after FIB. Through additional FIB etching, the facet can be more smooth, and the reflectance is higher. The threshold current decreases from 92 mA to 65 mA. Under the injection of 210 mA current, the optical power obtained by the coupling of silicon WGs is increased from 5.3 mW to 6.8 mW. Among them, the cavity length of the reference laser and the on-chip integrated laser is 3mm and the ridge width is 3μm. By comparing their L-I characteristics, the coupling loss of laser and silicon WG in the trench is -6.7dB. In addition, we collected the laser from the waveguide with a lens fiber and analyze the spectrum. At room temperature, the injection current is shown in Fig. 3c from the spectrum of 70 mA-160 mA, and the laser wavelength range is from 1270 nm-1283 nm. Fig 3d shows that the laser changes from the range of 20 °C-70 °C when the injection current is 175mA. To the best of our knowledge, this is the first demonstration of the InAs/GaAs QD laser was epitaxially grown on a trenched SOI

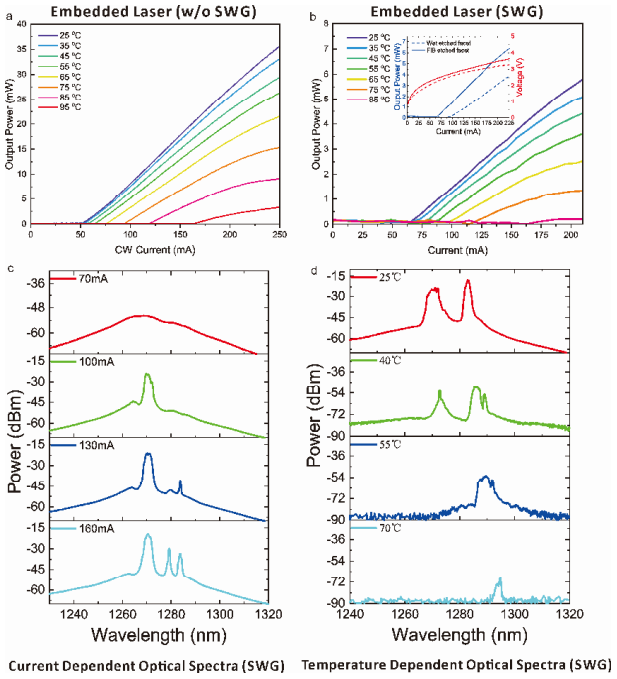

Fig. 3 Continuous-wave characterizations of embedded InAs QD laser on SOI with and without coupling into silicon waveguide. a Continuous-wave temperature-dependent L-I measurements of double-side cleaved III-V laser inside SOI trench as reference laser. **b** Continuous-wave temperature-dependent L-I measurements of integrated laser with one cleaved facet and FIB etched for the other. **inset** room-temperature L-I comparison between single-side wet etched facet and FIB etched facet. **c** Optical spectral analysis of integrated laser versus increased injection current. **d** Optical spectral analysis of integrated laser versus temperature variation.

template with a butt-coupling silicon waveguide.

V. Discussion

In summary, monolithic integrated III-V lasers on SOI substrate with silicon waveguide output have been realized by directly growing InAs QD lasers inside pre-patterned SOI trenches. Homoepitaxial formation of (111)-faceted Si V-grooves and heteroepitaxial growth of InGaAs/GaAs defect trapping techniques are implemented in this work to achieve high quality III-V gain materials on SOI. Our results demonstrate that monolithic integration of III-V laser with silicon photonic components will no longer be a design-level hypothesis. Overall, the monolithically integrated lasers can operate over 85 ºC with low threshold current of 65 mA at room temperature and silicon WG coupled maximum output power of 6.8 mW. One more step forward, the performance of on-chip integrated InAs QD lasers can be further improved by including advanced silicon spot-size converter with accurate control of laser-waveguide coupling distance during process. Once the coupling efficiency issue is resolved, many selections of silicon photonic components can all be integrated monolithically on a single wafer, such as modulators, wavelength de-multiplexers and photodetectors, just to name a few. Meanwhile, QD laser growth on a 300 mm patterned (001) silicon wafer with butt-coupled configuration has also been recently demonstrated[17], which leads to a great prospect for achieving dense on-chip integration. The next major step towards functional integration shall be including single longitudinal mode operation with high side mode suppression ratio (SMSR), which shall require implementing surface gratings or on-chip distributed bragg reflectors[17]. Overall, we believe that this monolithic integration techniques of on-chip lasers would offer a promising approach towards high-density and large-scale silicon photonic integration, especially in the application fields such as on-chip optical interconnect and integrated optical ranging.

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