Low-Power Multi-Step PDLUT Implementation for Transmitter Nonlinearity Compensation

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***Abstract*—A low-power multi-step pattern-dependent look-up table (PDLUT) implementation approach is proposed to compensate transmitter hardware nonlinearities. Compared to the conventional PDLUT, the proposed multi-step PDLUT reduces power consumption by 47% without performance degradation and by 53% with 0.2 dB required optical signal to noise ratio (ROSNR) degradation.**

Keywords—multi-step PDLUT, transmitter nonlinearity

I. Introduction

The nonlinear effect of transmitter components including digital-to-analog converter (DAC), modulator driver amplifier and optical modulator, severely distorts the transmitter signals especially for high-order modulation formats at high baud rates, which highly limits the transceiver performance. The nonlinear distortion shows a strong dependence on data patterns [1]. Normally, a nonlinear digital pre-distortion (DPD) algorithm is required in the transmitter digital signal processing (DSP) to mitigate the nonlinear distortion. Many DPD methods are published, such as Volterra algorithm [2], pattern-dependent look-up table (PDLUT) method [3], neural network (NN) method [4], and so on. Volterra algorithm doesn't perform as well as PDLUT or NN, and the complexity is high; while NN has good performance but it requires large resources and/or long calibration time. Among them, PDLUT approach draws great attention due to the good performance and low power consumption. A typical PDLUT application scheme is shown in Fig. 1. The LUT correction errors Δ, which are obtained based on a calibration process by comparing the data after receiver DSP and the ideal symbols transmitted at the transmitter, are applied to ideal symbols in transmitter DSP before linear pre-compensation (such as pulse shaping, data skew compensation and pre-transmitter bandwidth compensation, etc).

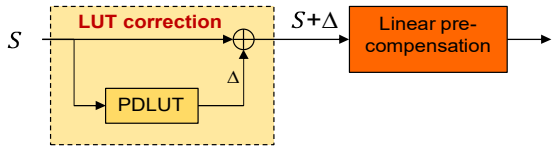

Fig. 1. Illustration diagram of PDLUT application at transmitter DSP.

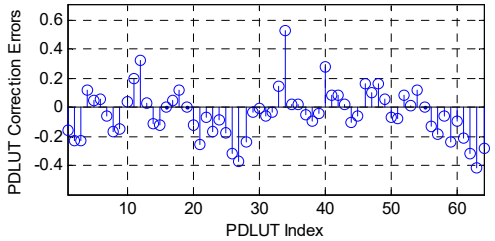

Fig. 2: A typical PDLUT of 16QAM with memory length of 3.

For ultra-high-speed (800Gbps and beyond) data center interconnection (DCI) applications, the power consumption of transceiver modules, including DSP modules, must comply with a strict standard. For such a low-power application-specific integrated circuit (ASIC) implementation, a time-domain finite impulse response (FIR) equalizer is normally employed in transmitter DSP to reduce power consumption for linear pre-compensation. Although the PDLUT itself is a low-power approach, it however causes a large power consumption increase for the following FIR linear equalizer pre-compensation. That is because correction errors (Δ) are normally small decimals and the corrected symbols (S+Δ) require a much higher bit resolution compared to the symbols themselves (normally integer numbers).

Fig. 2 shows a typical 16QAM PDLUT of one channel (xi, xq, yi or yq) with memory length of 3 symbols. The LUT errors (Δ) are 'normalized' to the symbol constellation. Compared with symbol values [-3, -1, 1, 3], Δ are mostly small values. As a result, the PDLUT nonlinear pre-distortion increases the input bit resolution of the following FIR linear equalizer, which causes a significant power increment for the transmitter DSP implementation. This large power increment is not acceptable in ultra-low-power ASIC design. Therefore, a newly-designed low-power PDLUT implementation approach is highly desired.

In this paper, we propose a feasible multi-step PDLUT approach to reduce PDLUT introduced power consumption in ultra-low-power ASIC implementation. The performance of the proposed PDLUT is verified with experiment. Compared to the conventional PDLUT, the proposed PDLUT reduces the

power consumption up to 53% with negligible performance degradation.

II. Principle

A. Main idea of the proposed multi-step PDLUT

Since the PDLUT introduced power consumption is mainly due to the increased bit resolution of the corrected symbols, to reduce the PDLUT caused power consumption, the bit resolution of PDLUT output (FIR input) should be reduced. In the proposed multi-step PDLUT scheme, symbols and correction errors go through FIRs separately. The correction errors are scaled and quantized to integer numbers before going through FIR equalizer. The residual errors can be further scaled and quantized, and go through another FIR, until a good performance is achieved. In addition, the number of FIR taps for quantized correction errors is reduced for further power reduction. By this means, the original long-bit-resolution-input FIR is divided into several short-bit-resolution-input FIRs with smaller tap number, which greatly reduces power consumption.

We take a 2-step PDLUT as an example to illustrate the principle of the proposed approach. The illustration diagram is shown in Fig. 3. PDLUT correction errors (Δ) are scaled and quantized (with level number of *Nlevel1*) to obtain Δ1, and then the residual correction errors are scaled and quantized (with level number of *Nlevel2*) to obtain Δ2. Quantization level numbers *Nlevel1* and *Nlevel2* are not necessarily equal. After the 2-step scaling and quantizing, Δ1 and Δ2 are all integers. Symbols (*S*) and quantized correction errors (Δ1 and Δ2) go through FIRs (which are denoted as *FIR0*, *FIR1* and *FIR2,* respectively) independently. Since the quantized errors are scaled, the corresponding FIR coefficients should be re-scaled as well to make the final compensation correct. It should be noted that Δ1, Δ2, and the FIR coefficients rescaling could be pre-calculated without additional power consumption.

The scaling and quantization could be extended to one or more steps as required to achieve better performance and/or lower power consumption, and the detailed quantization method is described in section *B*.

B. Quantization method

The quantized errors Δ1 can be obtained by the following equations:

$$scaleFactor1 = \frac{\max(\Delta)-\min(\Delta)}{Nlevel1-1} \quad (1)$$

$$\Delta 1 = round(\frac{\Delta}{scaleFactor1}) \quad (2)$$

Since Δ1 are integers and much larger than Δ, to ensure correct compensation, the *FIR1* coefficients should be rescaled by multiplying the scale factor, as follows.

$$FIR1coef = FIR0coef \cdot scaleFactor1 \quad (3)$$

Similarly, the residual errors *rErr*= Δ-Δ1·*scaleFactor1* are scaled and quantized again by the equation (4) and (5) to obtain quantized error Δ2. Accordingly, the *FIR2* coefficients needs to be rescaled, as shown in equation (6).

$$scaleFactor2 = \frac{scaleFactor1}{Nlevel2} \quad (4)$$

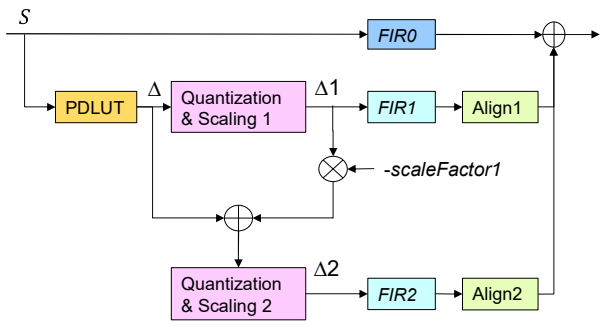

Fig. 3. Illustration diagram of the proposed 2-step PDLUT.

$$\Delta 2 = round(\frac{rErr}{scaleFactor2}) \quad (5)$$

$$FIR2coef = FIR0coef \cdot scaleFactor2 \quad (6)$$

It should be noted that, the denominator *Nlevel2* used in equation (4) to calculate *scaleFactor2*, is different from *scaleFactor1*. This is because the LUT errors Δ are usually not symmetric with respect to the symbols under correction, the denominator of *Nlevel1*-1 can ensure that the quantization has no more than *Nlevel1* output. However, the residual errors *rErr* in the second step are always symmetric, therefore, the denominator is *Nlevel2* to get a better resolution and to ensure an exact *Nlevel2* output levels.

It can be proved that the accuracy of a 2-step PDLUT with quantization levels of (*Nlevel1*, *Nlevel2*) is equivalent to 1-step PDLUT with (*Nlevel1*-1)×*Nlevel2* levels. However, their power consumption might be quite different. If more than six quantization levels are required, a 2-step PDLUT could be employed instead of a 1-step PDLUT to further save power. Similarly, under extreme conditions where the LUT correction errors have a larger peak-to-peak value, three steps or more could be considered.

C. FIRs outputs alignment

To further save power, the smaller number of taps could be used for the error paths (*FIR1* and *FIR2*). In this case, the outputs of FIRs need to be carefully aligned. For example, if the tap number for data path is 32 and for error paths are 8, the delay between them is (32-8)/2=12 symbols. After FIRs with 1.25 up-sampling rate, the delay between them becomes 12×1.25=15 samples. The *FIR1* and *FIR2* outputs need to be shifted by 15 samples to be aligned with the data path output.

However, if the tap number of the error paths is 12 instead, the delay between *FIR0* output and *FIR1* (or *FIR2*) output are (32-12)/2×1.25=12.5 samples, which is not an integer. In this case, the integer-sample delay (12 samples) can be achieved by simply shifting sample output of the error path, while the residual fractional-sample delay (0.5 sample) can be achieved by adding the corresponding delay to FIR coefficients for further alignment.

It should be noted that the delay and the delayed coefficients can be pre-calculated based on FIR tap number difference, which causes no extra power consumption.

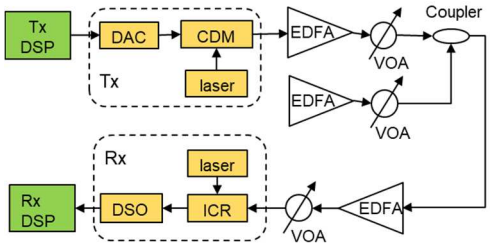

Fig. 4. Experimental setup.

III. Performance Verification

A 91GBd 16QAM signal is employed to evaluate experimentally the performance of different PDLUT configurations. The experimental setup is shown in Fig. 4. The digital signals are pre-compensated in transmitter DSP, and then converted to analogue signals by a four-channel DAC at a sampling rate of 120GS/s. A coherent driver modulator (CDM) is used to modulate the data signal at wavelength of 1548.5nm. In the experiment, the signal OSNR at the Rx is varied by adjusting the attenuation of a variable optical attenuator (VOA). After being detected by integrated coherent receiver (ICR), the signals are sampled digitally by a digital storage real-time oscilloscope (DSO) at a sampling rate of 200GS/s. An offline DSP platform is used to process the received digital data. The PDLUT is calibrated based on the comparison between the compensated received signals and the transmitted symbols. Then the proposed multi-step PDLUT is applied to the transmitted symbols in the transmitter DSP for nonlinearity pre-compensation.

The dependence of BER on OSNR performance with different PDLUT structures are shown in Fig. 5. The results show that all the PDLUT approaches improve the ROSNR (at a BER threshold of 1.25e-2) by more than 3dB, as compared to the case without PDLUT. The ROSNR of the proposed 1-step PDLUT (*Nlevel1*=5) is degraded by 0.2dB compared to the conventional PDLUT. For the 2-step PDLUT (*Nlevel1*=5, *Nlevel2*=3), the performance is comparable to the conventional PDLUT. In multi-step PDLUT schemes, 32 taps are used for *FIR0* while 8 taps are used for both *FIR1* and *FIR2*, respectively.

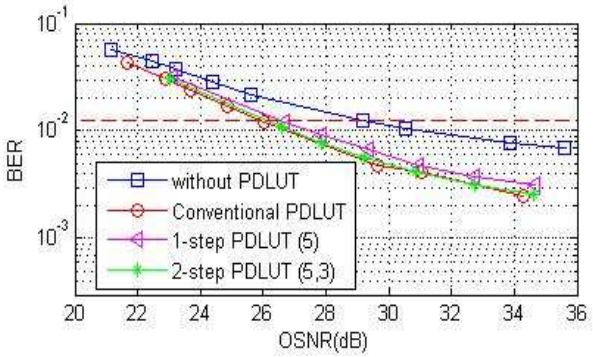

Fig. 5. the dependence of BER on OSNR performance.

TABLE I. Complexity Comparison

	FIR input bit resolution	Number of FIR taps	Power Reduction
Conventional PDLUT	8×8	32	Reference
1-step PDLUT (*Nlevel1*=5)	3×8 3×8	32 8	53%
2-step PDLUT (*Nlevel1*=5, *Nlevel2*=3)	3×8 3×8 2×8	32 8 8	47%

IV. Complexity Analysis

The complexity of the conventional PDLUT, 1-step DPLUT (*Nlevel1*=5), and 2-step PDLUT (*Nlevel1*=5, *Nlevel2*=3) are shown in Table 1. 16QAM symbols $S \in \{\pm1,\pm3\}$ in each channel (xi, xq, yi and yq) after the conventional PDLUT correction ($S+\Delta$) require a typical 8-bit resolution, while FIR coefficients also require 8-bit resolution. The FIR input bit resolution of the conventional PDLUT is denoted as 8×8. For 1-step PDLUT (*Nlevel1*=5), both symbols S and quantized errors $\Delta1$ require only 3-bit resolution. While for 2-step PDLUT (*Nlevel1*=5, *Nlevel2*=3), the quantized errors $\Delta2$ require 2-bit resolution. Since the power consumption roughly increases linearly with bit resolution and number of taps, the proposed 1-step and 2-step PDLUT reduce the power consumption by about 53% and 47%, respectively. In addition, the power introduced by extra adders after FIR filters is negligible. Therefore, with the proposed multi-step PDLUT approach, the implementation of PDLUT in ultra-low-power chip implementation becomes feasible.

V. Conclusions

We propose a low-power multi-step PDLUT implementation approach for transmitter nonlinear compensation. In the proposed multi-step PDLUT scheme, the FIR with high bit resolution input is divided into several FIRs with lower-bit-resolution input and with lower tap number. The experimental results show that the 2-step PDLUT (*Nlevel1*=5, *Nlevel2*=3) reduces power consumption by 47% without performance degradation, while 1-step PDLUT (*Nlevel1*=5) reduces power consumption by 53% with a ROSNR degradation of 0.2dB.

References

[1] P. J. Winzer, "High-Spectral-Efficiency Optical Modulation Formats", J. Lightwave Tech., Vol.30, No.24, pp.3824-3835, 2012.

[2] L. Guan and A. Zhu., "Low-Cost FPGA Implementation of Volterra Series-Based Digital Predistorter for RF Power Amplifiers", IEEE Trans. Microw. Theory Techn., vol. 58, no. 4, pp. 866–872, 2010.

[3] J. Ke, Y. Gao, and J. C. Cartledge, "400 Gbit/s single-carrier and 1 Tbit/s three carrier superchannel signals using dual polarization 16-QAM with look-up table correction and optical pulse shaping", Optics Express, Vol. 22, pp.71-83, 2014.

[4] V. Bajaj, F. Buchali, M. Chagnon, S. Wahls, and V. Aref, 'Deep Neural Network-Based Digital Pre-distortion for High Baudrate Optical Coherent Transmission', J. Lightw. Techn., vol. 40, no. 3, pp. 597-606, 2022.