A Selective Binary Search-assisted Digitized Adjoint Method for Photonic Device Design

Xiaoke Ruan
Research Institute of Intelligent Networks
Zhejiang Laboratory
Hangzhou, China
xkruan@zhejianglab.com

Ruiqi Luo
Research Institute of Intelligent Networks
Zhejiang Laboratory
Hangzhou, China
luoruiqi0202@zhejianglab.com

Nan Liu
Research Institute of Intelligent Networks
Zhejiang Laboratory
Hangzhou, China
liunan812@zhejianglab.com

Wei Ma
College of Information Science and Electronic Engineering
Zhejiang University
Hangzhou, China
ma_wei@zju.edu.cn

Kun Yin
Research Institute of Intelligent Networks
Zhejiang Laboratory
Hangzhou, China
yink@zhejianglab.com

***Abstract*—A digitized adjoint method assisted by selective binary search is proposed for photonic device design. Based on this approach, an ultra-compact 130 nm CMOS compatible polarization-insensitive power splitter is designed and fabricated on SOI.**

Keywords—Power splitter, inverse design, adjoint method, silicon-on-insulator (SOI)

I. INTRODUCTION

Optical inverse design, which explores the full design space of fabricable devices, is supposed to be a promising way to realize nanophotonic devices with multiple functionalities, high performances and unprecedented footprints [1-3]. In general, inverse-designed nanophotonic devices can be classified into two categories: digital and analog. The former consists of a limited number of pixels with fabrication-friendly dimensions. However, this type of structure is usually optimized by brute-force methods such as direct-binary search (DBS) [3-4] or heuristic methods [5-6], both of which lack computing efficiency especially when the number of pixels is quite large. On the contrary, the analog structure has numerous pixels with much smaller dimension and with the help of adjoint method [7], the gradient information of all these pixels could be efficiently calculated at one time by using only a forward and an adjoint (backward) simulation. The design freedom of this type of structure is much larger than the digital counterpart, but the irregular device geometry often makes the fabrication difficult. This problem can be partially alleviated by additional geometrical constraints algorithms [8-9], which would increase the computing complexity and cause further performance loss.

Recently, several schemes have been reported to implant efficient adjoint method in the design of digital photonic devices [10-12]. In 2020, Wang et al. [10] proposed a digitized adjoint method assisted with multi-level digital pattern, which requires a quite small minimum feature size of 70 nm. In [11] and [12], the digital topology optimization processes were successfully facilitated by the adjoint method, but they still need several rounds of DBS as supplementary.

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In this paper, we propose a new design approach for digital nanophotonic devices called the selective binary search (SBS)-assisted digitized adjoint method, which comprises a continuous optimization stage, a slowly discretization stage and a selective binary search stage. Based on this approach, a polarization-insensitive power splitter (PIPS) is designed and fabricated on silicon-on-insulator (SOI) with acceptable losses for both TE0/TM0 modes from 1500 nm to 1600 nm. The footprint of the device is only 3.168 μm × 3.168 μm and the minimum feature size is 132 nm, which is compatible with 130 nm complementary metal-oxide-semiconductor (CMOS) process. This algorithm maintains relatively high optimization efficiency and easily adjustable feature size, which is suitable for digital devices with larger footprints.

II. DEVICE DESIGN

Fig. 1 illustrates the optimization processes for the PIPS based on our design approach. The initial structure diagram of the PIPS is shown in Fig. 1(a) and the cross-section views of input and output waveguides are shown in Fig. 1(f). The device was designed on standard SOI substrate with 220 nm top silicon, 2 μm buried oxide, and 2 μm-thick oxide cladding. The PIPS consists of an input, two outputs, and a designed region with a dimension of 3.168 μm × 3.168 μm. The width of the input and output waveguides were all chosen to be 0.5 μm. The gap distance between the two output waveguides was set to 1 μm. The designed region was divided into a 24 × 24 pixel matrix with each pixel dimension of 132 nm × 132 nm, which is compatible with 130 nm CMOS process. The design objective was to achieve high transmission efficiency for both TE0 and TM0 modes input. Since the PIPS is a complete symmetrical structure, we only need to consider the transmission of one output waveguide. Therefore, the figure of merit (FOM) of the optimization can be expressed as: FOM=T_{TE0}+T_{TM0}. Here, T_{TE0} and T_{TM0} are the transmittances of the upper-output at wavelength 1550 nm for TE0/TM0 modes, respectively.

In the first continuous optimization stage, the permittivity of each pixel in the design region was allowed to vary continuously between the silicon (ε_{Si}) and the cladding (ε_{SiO_2}) and we obtained an initial design by starting with a uniform permittivity of $\varepsilon_{initial} = (\varepsilon_{Si} + \varepsilon_{SiO_2})/2$ in the entire design region. Due to the symmetrical structure, we only need to determine the states of half of the pixels. The

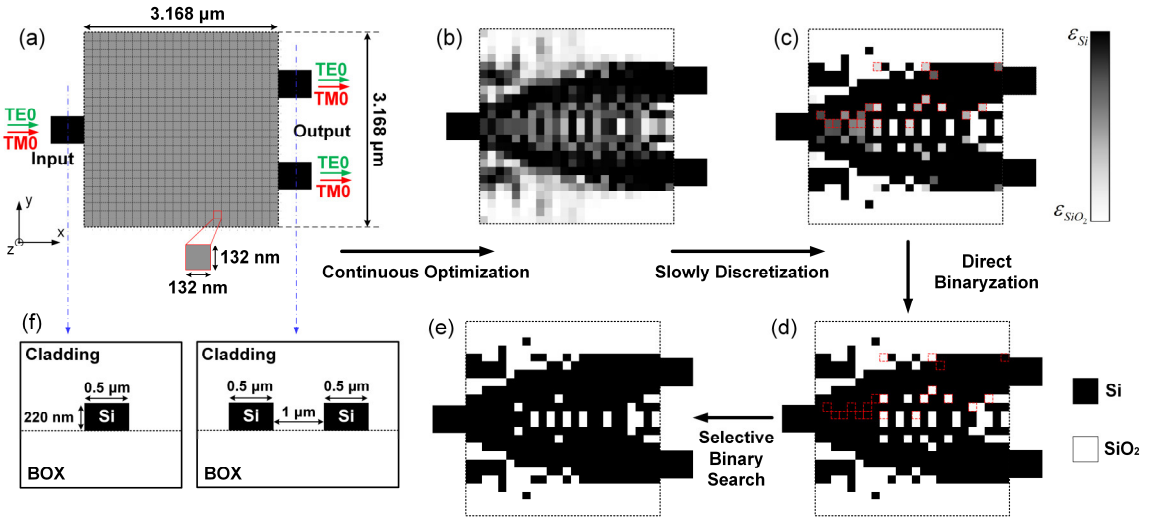

Fig. 1. The illustration of all optimization processes. (a) The initial structure diagram of the PIPS. (b) Design after the continuous optimization stage. (c) Design after the slowly discretization stage. The right-side colorbar is for (a)-(c). (d) Design after the direct binarization process. The right-side legend is for (d)-(f). (e) Design after the selective binary search. (f) The cross-sections of input and output waveguides.

permittivity of each pixel would be updated based on our digitized adjoint method. In the simulations by Lumerical 3D finite difference time domain (FDTD), the mesh grid size in the designed region was set to 22 nm × 22 nm, which means each pixel occupies a 6 × 6 mesh grid. Therefore, the original gradient matrix obtained by the adjoint method has a size of 72 × 144 (due to symmetry). To get the gradient matrix the same size of the designed pixel array, we averaged the gradient values in every 6 × 6 mesh grid occupied by the corresponding pixel. The design structure at the end of the first stage is shown in Fig. 1(b).

In the next stage, the digitized adjoint method was accompanied by slowly discretization operation. We slowly converted the "gray" pattern from the first stage to a "quasi-binary" one in which the permittivities of most pixels were close to the silicon or the cladding. This could be easily realized by using the Heaviside projection function [7] with slowly increased discreteness relevant coefficient. At each iteration, we counted the number of pixels that had not reached "quasi-binary" states (also named gray-state pixel), whose permittivity was in the range of $\varepsilon_{SiO_2} + (\varepsilon_{Si} - \varepsilon_{SiO_2}) \cdot 10\%$ to $\varepsilon_{SiO_2} + (\varepsilon_{Si} - \varepsilon_{SiO_2}) \cdot 90\%$. When the number of gray-state pixels decreased to a preset threshold (set 20 here), the digitized adjoint method stopped. The design structure at the end of this stage is shown in Fig. 1(c) and all of the remained gray-state pixels (highlighted by red dashed line) were recorded.

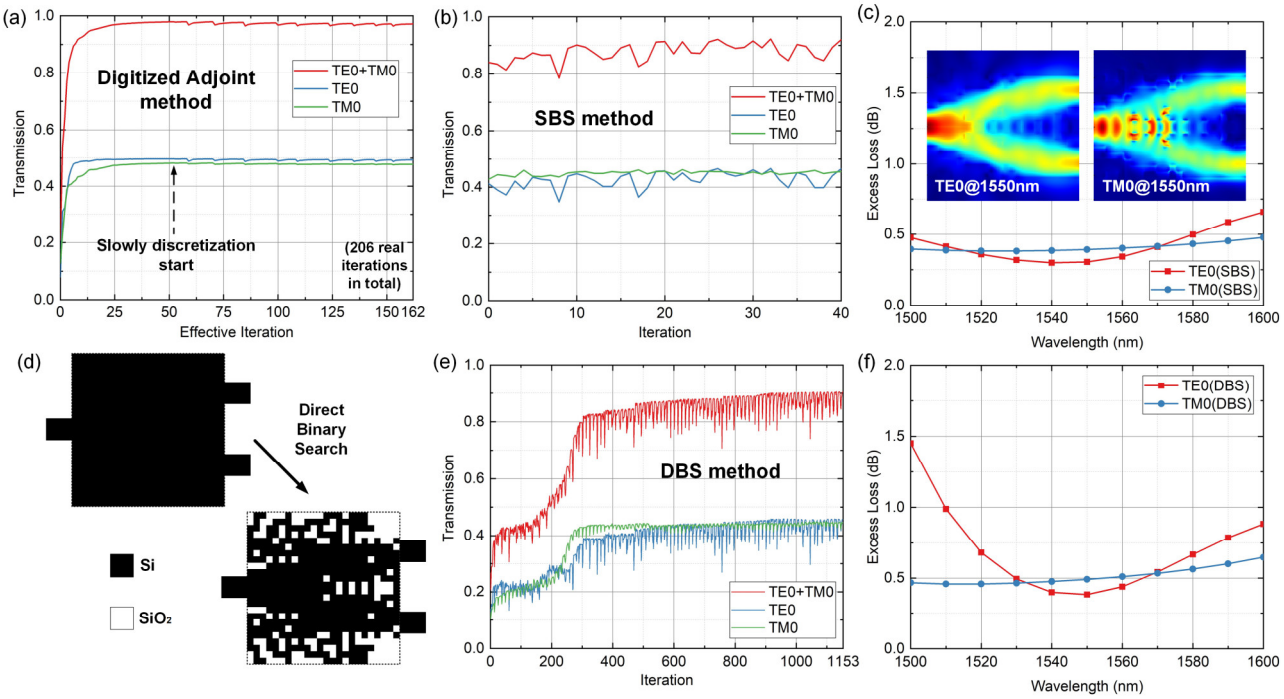

Fig. 2. Simulated transmission of the PIPS versus the iteration number optimized by (a) digitized adjoint method (b) and SBS method. (c) Simulated excess loss spectra of the designed PIPS for TE0/TM0 modes optimized after the SBS. The insets show the simulated electric fields through the final designed device at 1550 nm when TE0/TM0 modes input. (d) Designs before/after the DBS method. (e) Simulated transmission of the PIPS versus the iteration number for the DBS method. (f) Simulated excess loss spectra of the designed PIPS optimized by the DBS method.

The final stage is called the selective binary search. We first directly converted the "quasi-binary" pattern in Fig. 1(c) to a real-binary one in Fig. 1(d) through hard-decision with a permittivity threshold of $(\varepsilon_{Si} + \varepsilon_{SiO_2}) / 2$. Then the binary search method would be implemented over the recorded pixels only. Compared to applying complete DBS over all designed pixels after the adjoint method in [11-12], our SBS method could also further improve the ultimate performance of the device without consuming too much computing resources. The final optimized structure after SBS is shown in Fig. 1(e).

Fig. 2(a) shows the simulated transmission performance of the PIPS versus the effective iteration number optimized by digitized adjoint method, which includes the first and second stages. Note that the effective iteration number here did not count in unsuccessful pattern updating without total FOM improving. The first continuous optimization got converged after 52 effective iterations and the whole digitized adjoint optimization took about 162 effective iterations (206 groups of forward/adjoint simulations). Fig. 2(b) shows that due to abrupt direct binarization, the FOMs experienced a little bit loss, while after two rounds of SBS (41 groups of simulations), the FOMs improved a lot and got converged. The whole 3-stage optimization took about 453 groups of TE0/TM0 3D-FDTD simulations ($206 \times 2 + 41$). For comparison, traditional DBS method was implemented over the same design region and the designs before/after the DBS are shown in Fig. 2(d). Fig. 2(e) displays the FOM evolution of traditional DBS method. We can see that the total FOM did not get converged until four rounds of DBS, with up to 1153 groups of TE0/TM0 3D-FDTD simulations ($24 \times 12 \times 4 + 1 = 1153$). It can be safely concluded that our new proposed optimization method is much more efficient than traditional DBS method.

Fig. 2(c) and 2(f) compare the simulated excess loss spectra of the designed PIPS for both TE0/TM0 modes optimized by our new approach and by DBS, respectively. It can be observed that the devices optimized by different methods exhibit quite similar performance at the targeted wavelength (1550 nm). Especially, the PIPS designed by our new approach exhibits a low loss of <0.7 dB for both modes over a broadband wavelength range from 1500 nm to 1600 nm. The insets in Fig. 2(c) also show the simulated electric fields through the device designed by our new approach at 1550 nm when TE0/TM0 modes input.

III. Experimental Results

To experimentally validate the functionality of our inverse-designed PIPS, a series of devices were fabricated and the cutback method was used. The electron beam lithography (EBL), inductively coupled plasma (ICP), and plasma-enhanced chemical vapor deposition (PECVD) processes were used to fabricate the devices. The microscopic images of the fabricated PIPS cutback groups as well as TE/TM grating coupler (GC) references are shown in Fig. 3(a). Fig. 3(b) shows the scanning electron microscope (SEM) image of the PIPS designed by our new approach. The fabricated structure has good agreement with the algorithm-determined design. The measurements were conducted with a tunable laser, a polarization controller, fiber alignment stages and an optical power meter. TE and TM GCs, which also work as TE and TM type on-chip polarizers, respectively, were used to receive or transmit light from/into the fibers.

The measured cutback spectra of the PIPS for TE/TM modes are shown in Fig. 3(d)-3(e) and the insets show the linear fit results at a wavelength of 1550 nm. The curves labeled with "num=0" represent the spectra for TE/TM GC references. Non-negligible ripples can be observed in TE but not in TM mode cutback spectra, which could be partially illustrated by the simulated reflection difference between TE and TM modes as shown in Fig. 3(c). The extracted excess loss of the PIPS from cutback measurements are shown in Fig. 3(f). It can be seen that our PIPS exhibits an acceptable excess loss of < 0.9 dB over 100

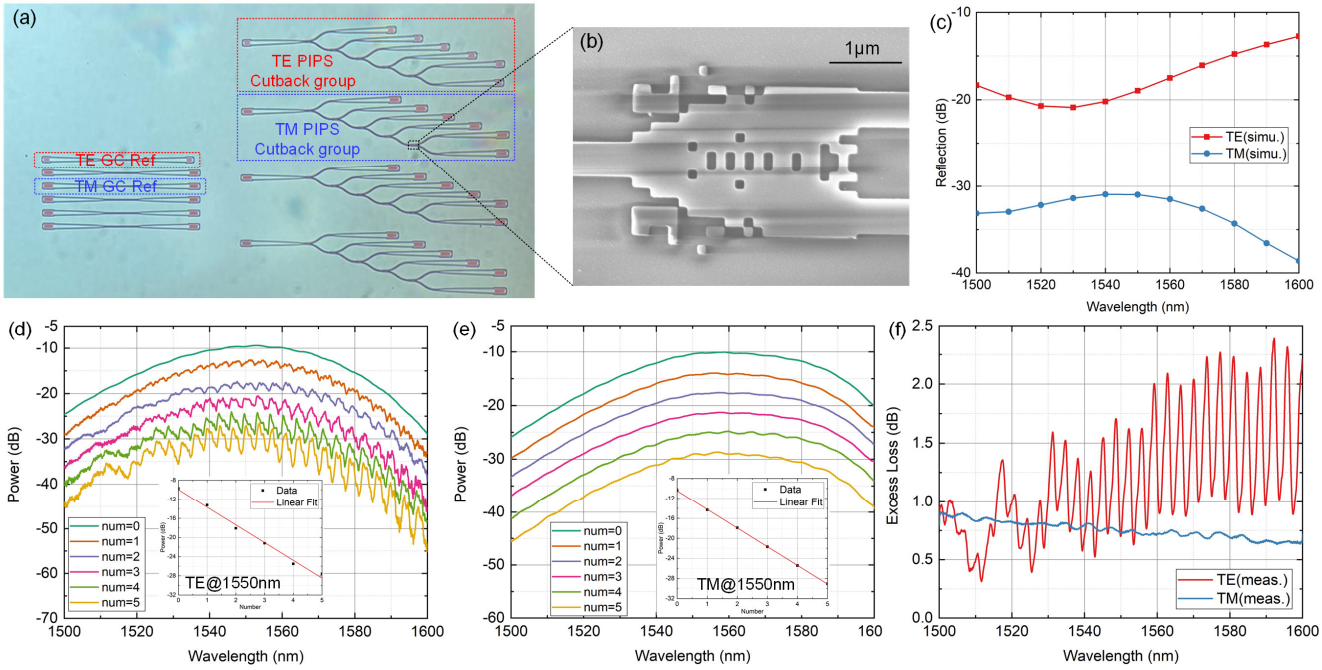

Fig. 3. (a) Microscopic images of the fabricated PIPS cutback groups as well as TE/TM grating coupler references. (b) SEM image of the fabricated PIPS. (c) Simulated reflection performance of the designed PIPS. Measured cutback spectra of the designed PIPS for (d) TE and (e) TM modes input. Insets: Linear fit results for TE/TM cutback measurements at a wavelength of 1550 nm. (f) Extracted excess loss spectra of our PIPS for TE/TM modes input.

nm wavelength range for TM mode. For TE mode, however, accurate estimation could not be performed due to the severe reflection. To alleviate this problem, in the future version, reflectance of the device will also be added to the total FOM during the SBS process.

IV. Conclusions

In conclusion, we propose a selective binary search-assisted digitized adjoint method for the design of digital nanophotonic devices. This algorithm combines the easily adjustable feature size of digital structure and the high efficiency of adjoint method. Assisted by SBS process, the device performance could be further improved without wasting much computing resources. Based on this algorithm, a polarization-insensitive power splitter is designed and fabricated on SOI with acceptable excess losses for both TE0/TM0 modes over 100 nm broadband wavelength range. The device footprint is only 3.168 μm × 3.168 μm and the minimum feature size is 132 nm, which makes it compatible with 130 nm CMOS process. This method can be applied to a wide variety of nanophotonic devices with larger footprints.

References

[1] A. Y. Piggott, J. Lu, K. G. Lagoudakis, J. Petykiewicz, T. M. Babinec, and J. Vučković, "Inverse design and demonstration of a compact and broadband on-chip wavelength demultiplexer," Nat. Photonics, vol. 9, pp. 374-377, 2015.

[2] S. Molesky, Z. Lin, A. Y. Piggott, W. Jin, J. Vucković, and A. W. Rodriguez, "Inverse design in nanophotonics," Nat. Photonics, vol. 12, pp. 659-670, 2018.

[3] B. Shen, P. Wang, R. Polson, and R. Menon, "An integrated-nanophotonics polarization beamsplitter with $2.4 \times 2.4\ \mu m^2$ footprint," Nat. Photonics, vol. 9, pp. 378-382, 2015.

[4] K. Xu, L. Liu, X. Wen et al., "Integrated photonic power divider with arbitrary power ratios," Opt. Lett., vol. 42, no. 4, pp. 855–858, 2017.

[5] Z. Yu, H. Cui and X. Sun, "Genetic-algorithm-optimized wideband on-chip polarization rotator with an ultrasmall footprint," Opt. Lett., vol. 42, no.16, pp. 3093-3096, 2017.

[6] Z. Xie, T. Lei1, F. Li et al., "Ultra-broadband on-chip twisted light emitter for optical communications," Light: Science & Applications, vol. 7, no.3, pp. 18001, 2018.

[7] J. S. Jensen and O. Sigmund, "Topology optimization for nanophotonics," Laser Photon. Rev., vol. 5, no. 2, pp. 308–321, 2011.

[8] M. Zhou, B. S. Lazarov, F. Wang, and O. Sigmund, "Minimum length scale in topology optimization by geometric constraints," Comput. Methods Appl. Mech. Engrg., vol. 293, pp. 266-282, 2015.

[9] X. Qian and O. Sigmund, "Topological design of electromechanical actuators with robustness toward over- and under-etching," Comput. Methods Appl. Mech. Engrg., vol. 253, pp. 237-251, 2013.

[10] K. Wang, X. Ren, W. Chang et al., "Inverse design of digital nanophotonic devices using the adjoint method," Photonics Res., vol. 8, no. 4, pp. 528–533, 2020.

[11] H. Chen, H. Jia, T. Wang and J. Yang, "A Gradient-Oriented Binary Search Method for Photonic Device Design," J. Lightwave Technol., vol. 39, no. 8, pp. 2407–2412, 2021.

[12] J. Xu, Y. Liu, X. Guo, Q. Song and K. Xu, "Inverse design of a dual-mode 3-dB optical power splitter with a 445 nm bandwidth," Opt. Express, vol. 30, no. 15, pp. 26266-26274, 2022.