Faculty of Engineering and Technology
Department of Electrical and Computer Engineering

ENCS 5131 Project

Hardware design Lab
Sec-Sem 2023-2024

Please find below project/term paper description. We need paper written in the template attached and explained below.

The project Title:

" Implementation of Spiking Neural Networks for IoT Devices using 32nm or lower process Process"

Due dates : Tuesday Jun 21 Paper and ppt discussion that day.

Tools: You can use electric or ICC2 for implementation and Verdi or Playground for Verifications.

Number of students per project: **Max of two in each group**

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Refrence examples:

Majority of the Refrence paper should be from the last 3-4 years .

- https://www.sciencedirect.com/science/article/pii/S1474667015404562
- Watch to understand: https://www.youtube.com/watch?v=9dYZXQl4ozk
- https://www.youtube.com/watch?v=FDefITq14T0&list=PLJePd8QU_LYKZwJnByZ8FHDg5l1rXtcIq&index=5
- Codes:
    - https://github.com/vipinkmenon/neuralNetwork/tree/master/Tut-1
    - https://www.youtube.com/watch?v=1YnyNAxaJIg
- https://www.mdpi.com/1424-8220/23/14/6275
- https://www.researchgate.net/profile/Mohamed-Mourad-Lafifi/post/I-want-to-built-a-spiking-behavior-of-a-neural-network-using-a-vlsi-ckt-can-you-plz-provide-some-help/attachment/59d63ee079197b807799b6a5/AS%3A425748612816896%401478517787126/download/VLSI+Implementation+of+a+agruebl_diss_kip.pdf

Template: You can use any IEEE two column template

Project Requirements: VLSI Design Lab - Implementation of Spiking Neural Networks for IoT Devices using 32nm Process

1. Project Overview:

- **Develop a VLSI design project focusing on implementing Spiking Neural Networks (SNN) tailored for IoT devices.**
- **Utilize a cutting-edge 32nm process technology to optimize power consumption and performance.**

2. Objectives:

- **Design and implement SNN architecture suitable for IoT applications.**
- **Leverage the benefits of the 32nm process to enhance energy efficiency.**
- **Evaluate the trade-offs between power consumption, area utilization, and processing speed.**

3. System Architecture:

- **Define the overall architecture of the Spiking Neural Network for IoT.**
- **Specify the integration of sensory input, synaptic processing, and spike generation components.**

4. Design Considerations:

- **Optimize the SNN design for low-power operation, crucial for IoT devices.**
- **Consider the constraints of IoT environments, such as limited resources and intermittent connectivity.**

5. Hardware Description Language (HDL):

- **Utilize industry-standard HDLs (Verilog or VHDL) for the hardware description of the SNN components.**

6. Power Analysis:

- **Conduct thorough power analysis at different stages of the SNN operation.**
- **Explore power reduction techniques specific to the 32nm process.**

7. Performance Metrics:

- **Define performance metrics, including latency, throughput, and energy efficiency.**
- **Establish benchmarks for comparison with existing SNN implementations.**

8. Integration with IoT Devices:

- **Investigate and incorporate communication interfaces suitable for IoT connectivity.**
- **Ensure compatibility with common IoT communication protocols.**

9. Validation and Testing:

- **Develop a comprehensive testing strategy to validate the SNN functionality.**
- **Simulate and verify the design using appropriate tools and methodologies.**

10. Project Deliverables:

- **Complete hardware description of the SNN using Verilog/VHDL.**
- **Power analysis report highlighting efficiency gains in the 32nm process.**
- **Performance evaluation results based on defined metrics.**
- **Integration guide for deploying SNN on IoT devices.**

Paper Structure:

1. Introduction:

- **Background and motivation for implementing SNN in IoT devices.**
- **Overview of the chosen 32nm process technology.**

2. Literature Review:

- **Survey of existing SNN implementations for IoT and their limitations.**
- **Discussion of the advantages of the 32nm process in VLSI design.**

3. System Architecture:

- **Detailed description of the proposed SNN architecture.**
- **Explanation of the integration of sensory input, synaptic processing, and spike generation.**

4. Design Methodology:

- **Overview of the hardware description using Verilog/VHDL.**
- **Discussion on design considerations for low-power operation.**

5. Power Analysis:

- **Detailed power analysis at different stages of SNN operation.**
- **Comparison with power consumption in other process technologies.**

6. Performance Evaluation:

- **Presentation of performance metrics, including latency, throughput, and energy efficiency.**
- **Benchmarking against existing SNN implementations.**

7. Integration with IoT Devices:

- **Discussion on communication interfaces and protocols for IoT connectivity.**
- **Demonstration of compatibility with common IoT devices.**

8. Verification and Validation and Testing:

- **Description of the testing strategy and simulation results.**
- **Verification of SNN functionality and performance.**

9. Results and Discussion:

- **Analysis of the obtained results and their implications.**
- **Comparison with expectations and potential areas for improvement.**

10. Conclusion:

- **Summary of key findings and contributions.**
- **Implications for the broader field of IoT and neuromorphic computing.**

11. Future Work:

- **Suggestions for further enhancements and research directions.**

12. References:

- **Citations of relevant literature, tools, and methodologies used in the project.**