Lab 1: Power Management & Bootloading

ESE519/IPD519: Introduction to Embedded Systems
University of Pennsylvania

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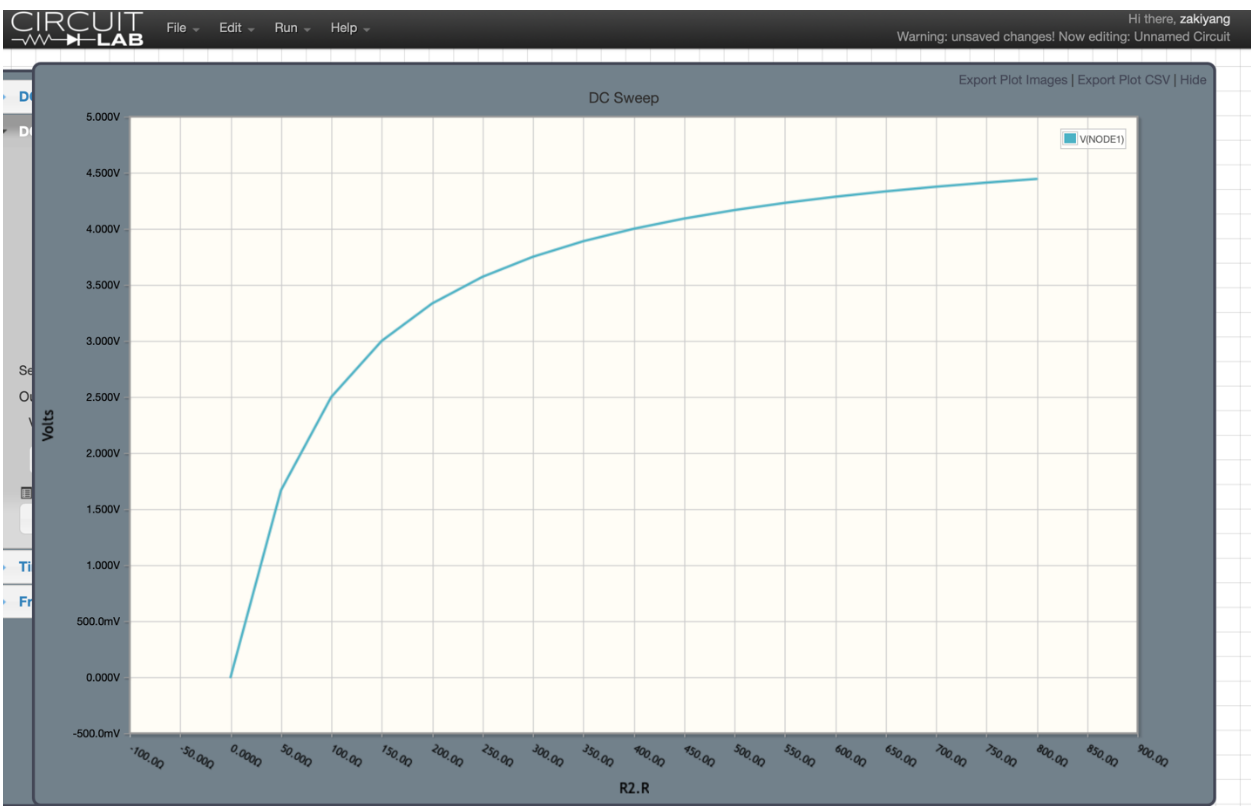
GitHub Repository: https://github.com/Zakiyanggg/ESE519/

Par1: Voltage Regulator

Voltage divider

1. In the loop:
   V1-I*R1-I*R2 = o
   $I = \frac{V1}{R1+R2}$
   Vnode1 = VR2 = I*R2 = (5v/(100Ω+100Ω))*100Ω = 2.5v
2. Change R2 to 850Ω
   Vnode1 = VR2 = I*R2 = (5v/(100Ω+850Ω))*850Ω = 4.47v
3.



Yes, this graph matches the equation I derived in 1)

Vnode1 = VR2 = $\frac{V1}{R1+R2}$*R2

4. 1) User would be able to get a lower voltage from a higher voltage source.
   2) A voltage divider circuit is handy and convenient to design and build, only resistors are involved.
   3) Can be used to measure a voltage source that too high to be directly measured.

Buck Converter

5.

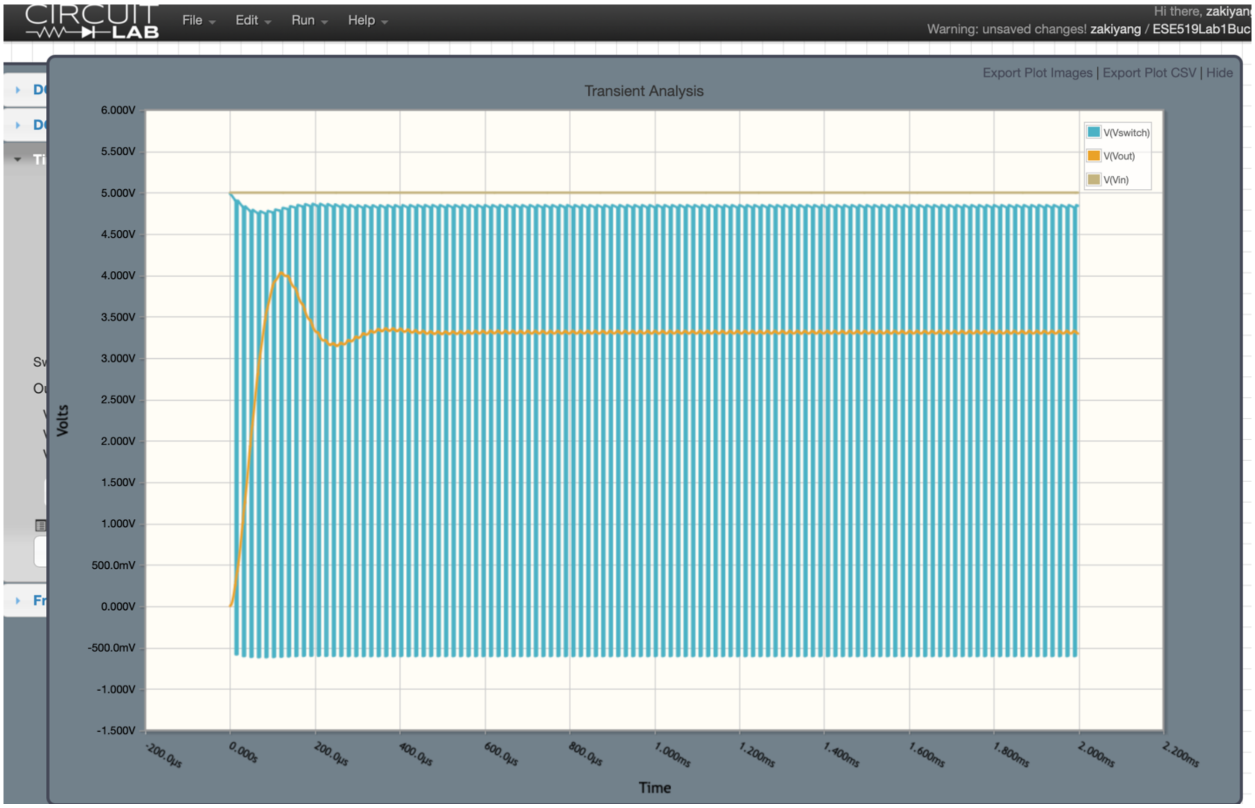
The duty cycle represents the fraction of one period in which a signal or system is active. It represents the low time of the pulse. The MOSFET is active when the pulse is low.

6.

In simulation, When Vout = 3.3v the duty cycle is 0.266. Vout = 2v, the duty cycle is 0.54

This does make sense since if the duty cycle decrease which will lead the on time of MOSFEP longer. So, the output voltage would be higher since the RC circuit oscillates more. The components in the circuit such as the diode and the inductor would slightly affect the result.

7. Plot of Vout = 3.3v

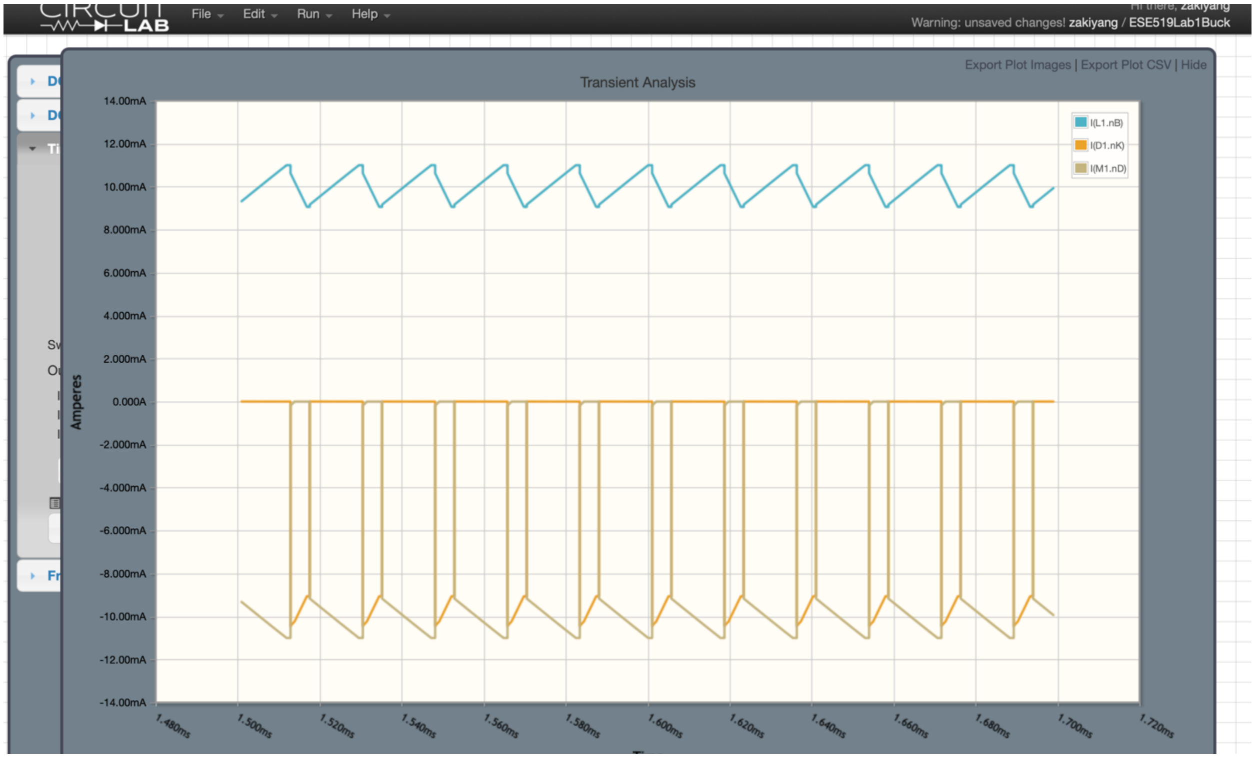


8.

Because in the circuit there is a capacitor and an inductor. Both takes a while to charge and discharge then reach to a steady point.

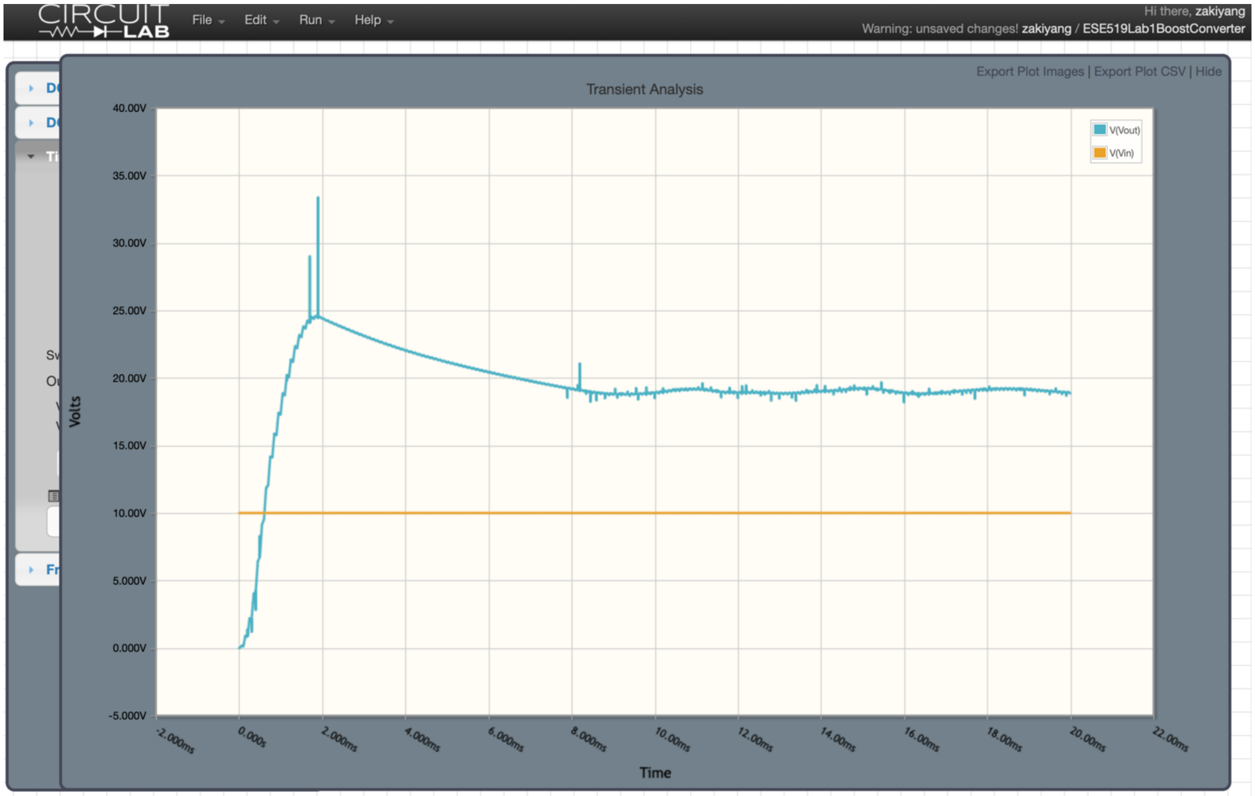
The reason why the steady state output is not a straight horizontal line is because the PWM signal oscillation between high and low state. So, the capacitor and inductor is continuously switching between charging and discharging. Thus, the Vout would oscillating in a certain range, and it can be count as steady output.

9.



10.
KCL: Id1+Il1 = Im1
The sum of the currents trough out one node is always zero. The graph matches this behavior.

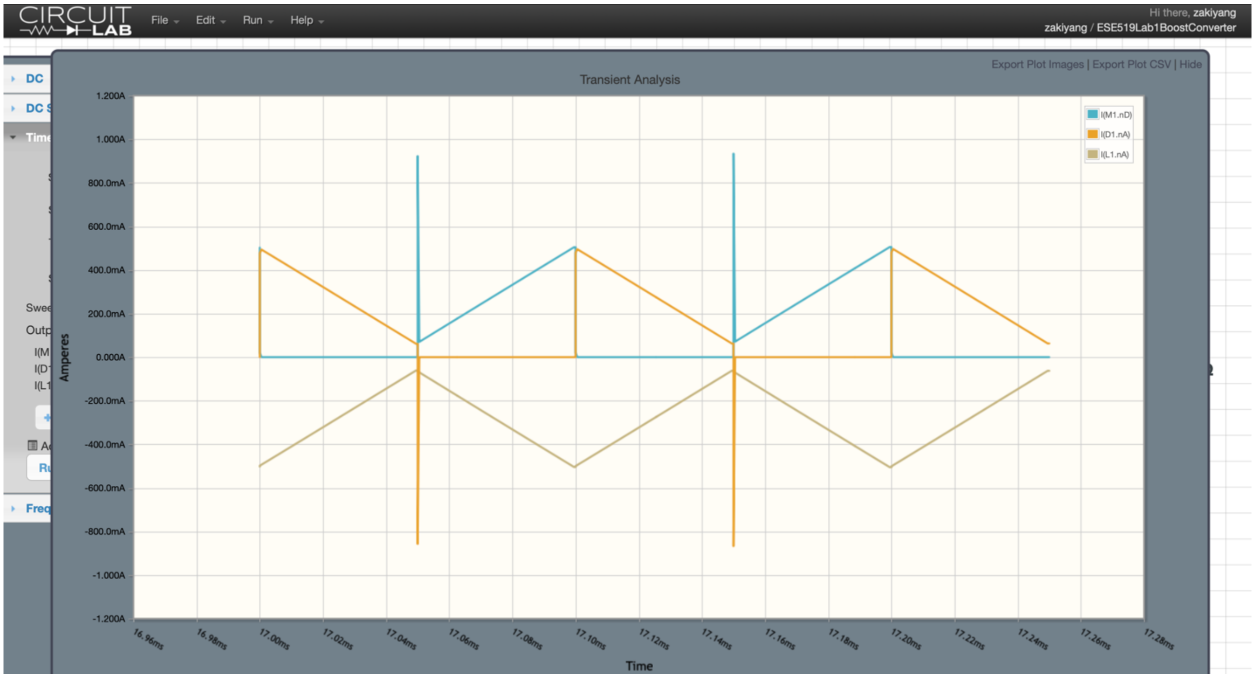
Boost Converter
11.



12.

Ideal output = Vin/(1-D), as the duty cycle is 0.5 the output should be 10/0.5 = 20v
As shown in the graph the steady state gives around 19v output voltage. The result is close to the ideal situation, so it is what I expected. The difference might be caused by the diode or other components in the circuit.

13.
For buck regulator the simulation plots for 2ms but for boost convertor it plots for 20ms. And the two clk frequencies are different. Also the output voltage of boost converter is much higher than buck regulator, this may cause more time to plot.



15.
According to KCL, the sum of the three current should always be zero. The graph matches the expectation.

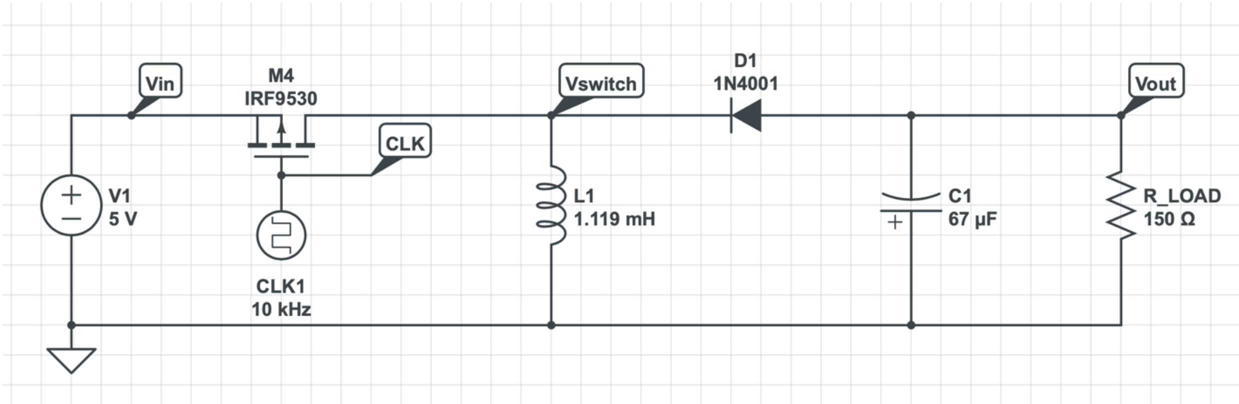
Part B: Adruino Power Management

16.

Jack	USB	Power Source?	NODE1	NODE2	NODE3
0V	5V	USB	-928.8uV	4.999v	3.300v
10V	0V	Barrel Jack	5.001v	5.000v	3.300v
10V	5V	Barrel Jack	5.001v	5.000v	3.300v
3V	3V	USB	-928.8uV	4.999v	3.300v

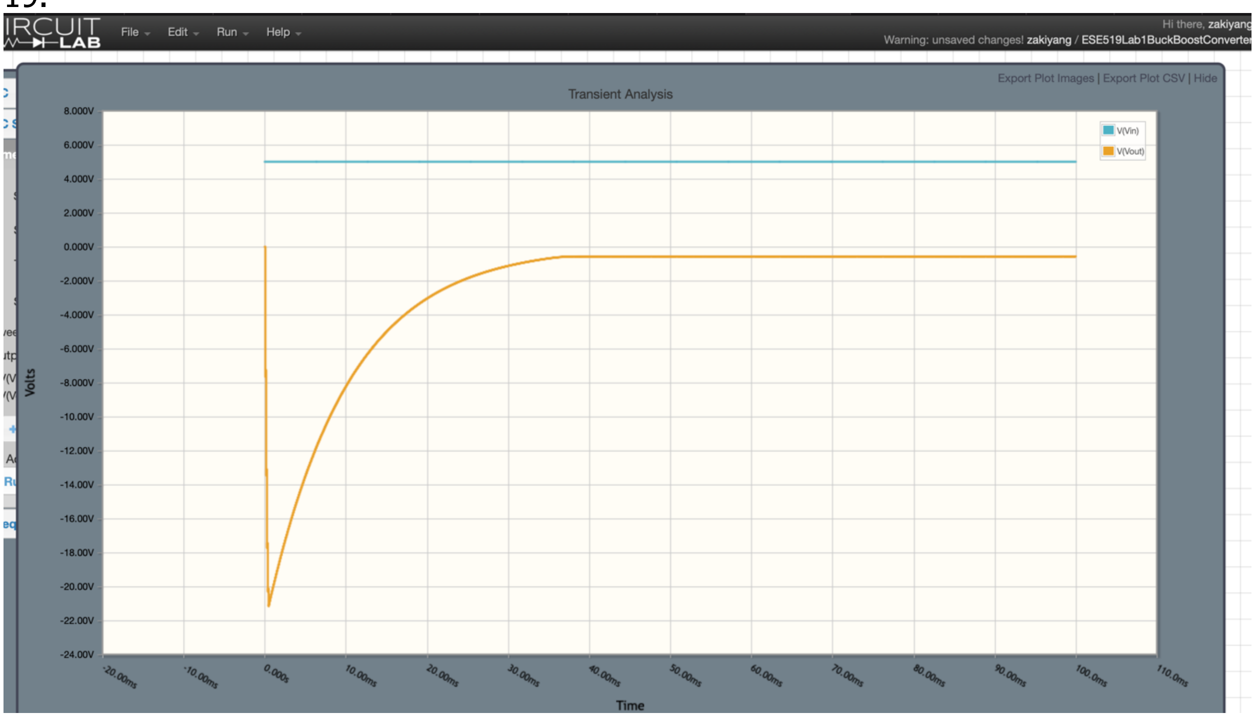
17.
In this set up the system has a priority to use the USB as the voltage source. As the inverting input is 3.3v since there is a regulator. The barrel jack mush has a voltage input greater than 3.3/1/2 = 6.6v to deactivate usb power input. So, if the divider is removed, the non-inverting input is always greater than 3.3v so the barrel jack will be the priority power input.

18.



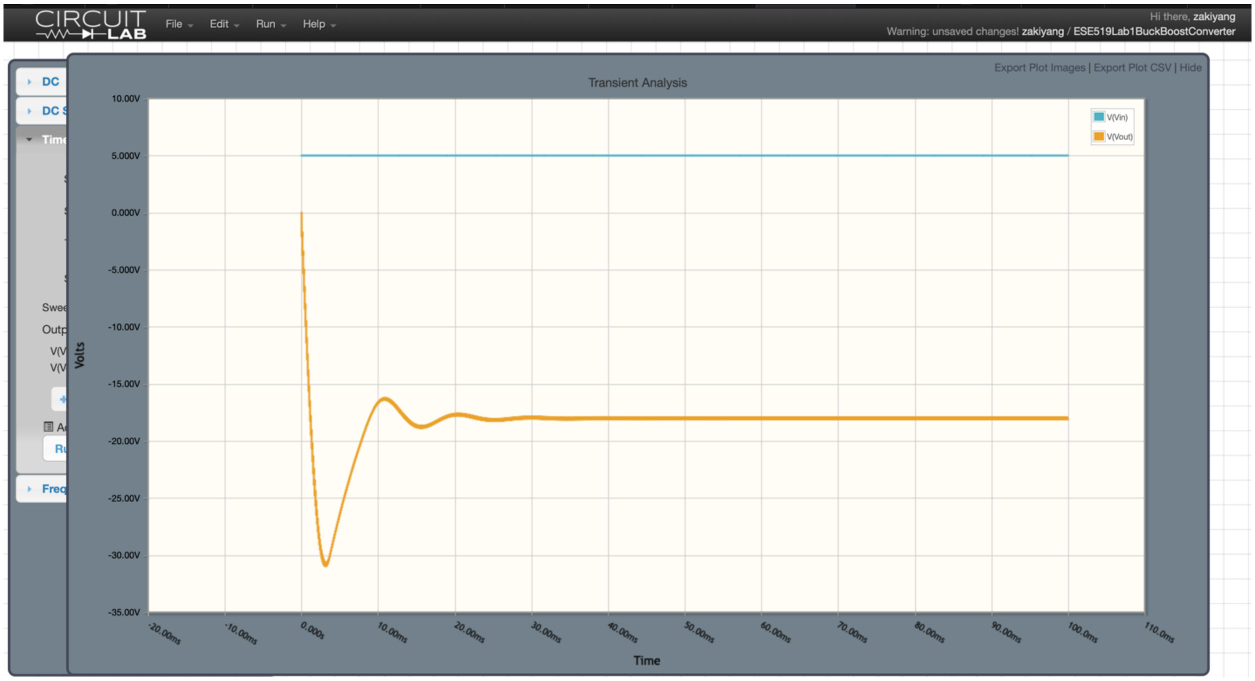
https://www.circuitlab.com/circuit/kcf4hj77pe5y/ese519lab1buckboostconverter/#menu_file_link_and_share

19.



0.2 Duty cycle (step Down)

20.



0.8 Dury cycle(step Up)

21.

BJT is a bipolar junction transistor and it's driven by current. MOSFET is filed effect transistor that's driven by voltage. BJT may cause current leak and waste power. So for a system with smaller power consumption, BJT is a better choice. MOSFET is suitable for high power system so it usually has a higher cost than BJTs.