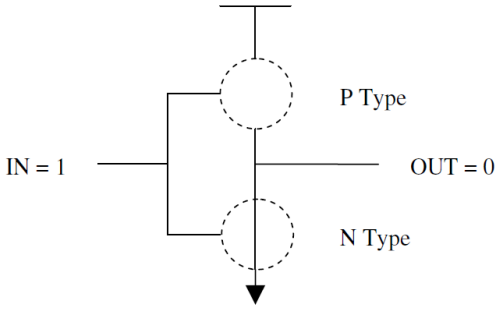
3.1

	N-Type	P-Type
Gate=1	closed	open
Gate=0	open	closed

3.2



3.9

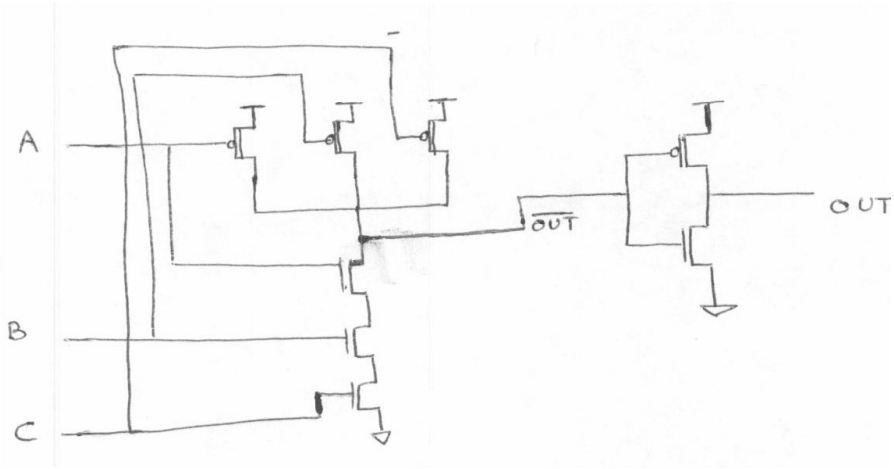
A	B		NOT(NOT(A) OR NOT(B))
0	0		0
0	1		0
1	0		0
1	1		1

AND gate has the same truth table.

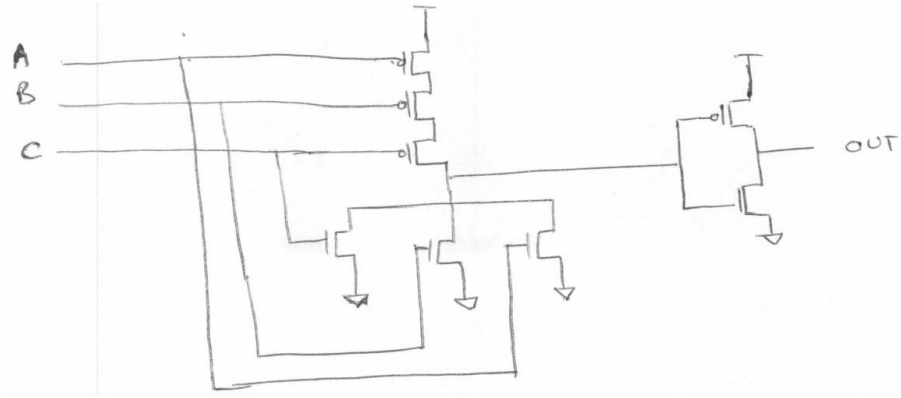
3.10

A	B		A NOR B
0	0		1
0	1		0
1	0		0
1	1		0

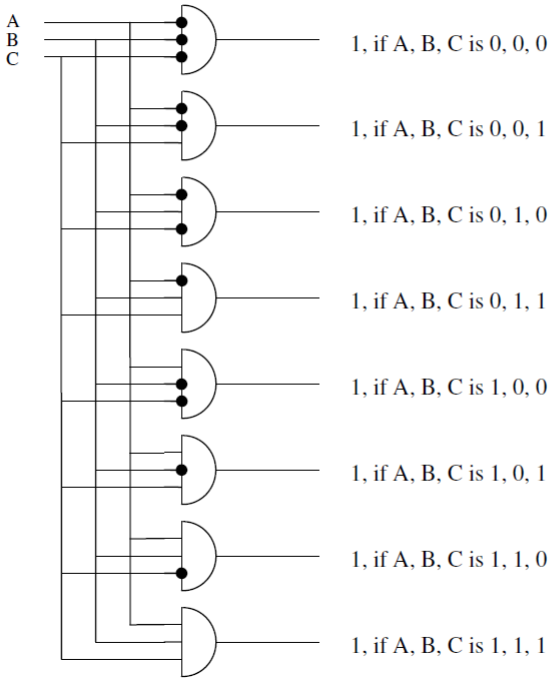
3.11 a. Three input And-Gate



Three input OR-Gate



3.12



3.13 A five input decoder will have 32 output lines.

3.14 A 16 input multiplexer will have one output line (ofcourse!). It will have 4 select lines.

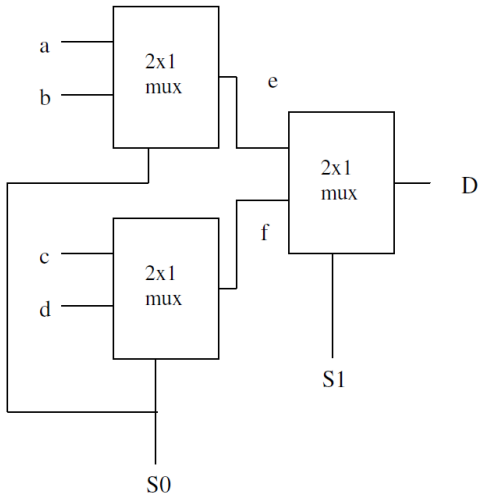
3.15

C_{in}	1	1	1	0
A	0	1	1	1
B	1	0	1	1
S	0	0	1	0
C_{out}	1	1	1	1

A = 7, B = 11, A + B = 18.
In the above calculation, the result (S) is 2 !! This is because 18 is too large a number to be represented in 4 bits. Hence there is an overflow - Cout[3] = 1.

3.19 Figure 3.36 is a simple combinational circuit. The output value depends ONLY on the input values as they currently exist. Figure 3.37 is an R-S Latch. This is an example of a logic circuit that can store information. That is, if A, B are both 1, the value of D depends on which of the two (A or B) was 0 most recently.

3.21 $2 * 2^{14} = 2^{15} = 32768$ nibbles
3.22



S1	S0		e	f	D
0	0		a	c	a
0	1		b	d	b
1	0		a	c	c
1	1		b	d	d

3.24 (a) X=0 => S = A+B, X=1 => S = A+C

3.31. 8 * (2^3) = 64 bytes

3.32 A memory address refers to a location in memory. Memory's addressability is the number of bits stored in each memory location.

3.34

a) 4 locations
b) 4 bits
c) 0001

3.35 Total bits of storage = 2^22 * 3 = 12582912

3.44