CS3339

Homework 3

Fall 2018

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SHOW YOUR WORK

I will be much harsher on neatness, lack of work, marking answers this time around

Instructions: Print the homework out single sided and answer the problems in sharp pencil, SHOWING YOUR WORK, in the space provided. Use the back of page if you run out of room but be sure to say " continued on back". Put your name below, staple all pages together and turn in at the beginning of class on the due date. Suggest putting name on all pages. Make sure all parts of question are answered. Make sure to underline or circle answer if it is not obvious.

NAME:		
. */ \! *! 	 	

Assume 32 bit address. You have a 8K byte direct mapped cache. Each block has 8 words. Identify the number of bits for the following:

Tag Index	
Index	
Block Address	
Tag	
Index	
Block Offset	

Assume 64 bit address. You have a 64K byte direct mapped cache. Each block has 32 words. Identify the number of bits for the following:

Tag	
Index	
Block Offset	

Assume 32 bit address. You have a 4-way set associative cache with a total capacity of 64 kB. There are 32 words per block and 8 bytes per word. Identify the set index, tag, block offset in the physical memory address below. Put bit pattern in table.

i.e. sample

Tag	1111 1111 11

0011 0101 1111 1001 1010 0101 1100 0011

	Bits	Bit Pattern
Tag		
Set Index		
Block Offset		

4. 8 points

One way associativity is the same as:?

If you have 8 blocks and you have 8 way associativity you have what kind of cache?

5. 10 Points

In a 5 stage ARM pipeline with each stage taking one cycle, how many cycles to fully execute 8 instructions with no hazards?

Use following pipelines and show hazards and indicate for each line what would need to be done in terms of forwarding or bubbles. On one set of boxes draw arrows showing the initial hazards. On another set show forwarding arrows, or where you would add bubbles. If you add a bubble add boxes and show the stalled stage like in the lecture, showing effect on following instructions also.

It must be very NEAT!

Use following pipelines and show hazards and indicate for each line what would need to be done in terms of forwarding or bubbles. On one set of boxes draw arrows showing the initial hazards. On another set show forwarding arrows, or where you would add bubbles. If you add a bubble add boxes and show the stalled stage like in the lecture, showing effect on following instructions also.

It must be very NEAT!

STOR R1,[R6, #4] IM ID EX MEM WB
LDUR R8,[R1, #4]
LDUR R7,[R8, #4]
ADD R2,R7,R3
SUB R9,R7,R3
STOR R1, [R6, #4] IM ID EX WB
LDUR R8,[R1, #4]
LDUR R7,[R8, #4]
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8. 3 Points

A program consists of two nested loops, with a branch instruction at the end of each loop and no other branch instruction anywhere. The outer loop is executed 20 times and the inner loop 10 times. Determine the prediction accuracy percentage for the two prediction strategies: (a) always predict branch not taken, (b) always predict branch taken

9. 2 Points

What is a capacity cache miss:

10. 2 Points

A control hazard can occur from what type of instruction?