

CS3339

Homework 2

Fall 2018

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SHOW YOUR WORK

SHOW UNITS

**I will be much harsher on neatness, lack of work,
marking answers this time around**

Instructions: Print the homework out single sided and answer the problems in sharp pencil, **SHOWING YOUR WORK**, in the space provided. Use the back of page if you run out of room but be sure to say " continued on back". Put your name below, staple all pages together and turn in at the beginning of class on the due date. Suggest putting name on all pages. Make sure all parts of question are answered. Make sure to underline or circle answer if it is not obvious.

NAME: _____

1.(20 points)

What is the binary representation of 53.25 assuming IEEE754 single precision?

Double Precision?

2.(20 pts) Evaluate the following ARM code line by line and show the state of each of the following registers in radix 16 after each instruction executed. X1 , X2 , X3.

Precondition:

X1 => 0x1000 mem loc 0x1004 => 0x8, mem loc 0x1008 => 0xb

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	X1	X2	X3
At Start	0x1000	0x0	0x0
LDUR X2, [X1, #1]			
LDUR X3, [X1, #2]			
ADD X3, X2, X3			
ADDI X3, X2, #12			
EOR X1, X2, X3			

3. (10 pts) Convert the following binary floating point to decimal

IEEE 32-bit floating point format.

0 10000100 000 0100 1101 0000 0000 0000

4. (5 pts) Take the following 32 bit words in hex and express them in little and big endian forms. Separate bytes and orient the lowest memory address on the left as shown. Convert the hex to decimal. It better be neat!!!!

Treat the memory layout as follows:

Memory Addr xxxxxx0 xxxxxx1 xxxxxx2 xxxxxx3

0x90AB12CD

0xDEADBEEF (used by all CE coders for some reason) I like it

0xCAFEBAFE (starts every java class file)

0xDA7ABA5E

	Byte 1:0		Byte 3:2		Byte 5:4		Byte 7:6	
BIG								
LITTLE								
BIG								
LITTLE								
BIG								
LITTLE								
BIG								
LITTLE								

5. (20 pts) Amazon Microprocessor (the former Intel company) has just come out with a new 32 core super duper tanium processor. It has a clock speed of 2.2 Ghz, compared to the current four core processor machines running at 3.0 Ghz that you have in your companies current servers and lab machines and this has confused your boss. You boss has asked you, the smart looking, sharply dressed, well groomed, recently bathed, polite, inquisitive, and informed newbie dude or dudette, to come into his office in 30 minutes and tell him how you are going to evaluate the new computers that Amazon Computer (the former Dell company) has just announced (available in 2 days from now) since if Amazon did it there must be a reason and he wants to look smart.

This is your big chance to show me, I mean your boss, how good of an engineer you are. You are to prepare one killer power point slide that explains to your boss the complexities of evaluating processor and system performance tradeoffs. Once finished. you will use this to tell him you will need at least a week to get him an answer on how long its going to take you to get him the final evaluation. Your slide will be evaluated both on the information it contain as well as how professional it looks.

If you have no clue what professional slides look like, I suggest spending some time studying this. I will pick the five best slide sets from my perspective and you will then all vote on the best of best and runner up before we go over the midterm. The winner will receive **a bag of snickers** or **twix miniature candy bars** for their efforts. Second place gets whatever first place didn't want.

You are to print out the slidesand attach it to your homework. Please, no names on the slides!!!! If color is important, print it out in color.

6. (25 pts) Evaluate the following ARM code line by line and show the state of each of the following registers after each instruction executed: \$t0 , \$t1 , \$t2 , PC after instruction executes, memory location 0x40001004, memory location 0x40001008

Precondition:

PC (initial) = 0x 4000 0000 X4 = 0x4000 1000

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	X0	X1	X2	PC	0x4000 1004	0x4000 1008
Start	0	0	0	0x4000 0000	0	0
ADDI X0, #5						
STUR X0, [X4 , #1]						
LDUR X1, [X4, #1]						
ADD X0, X1, X0						
STUR X0, [X4, #2]						
B Exit						
Exit						
ADD X2, X1, X0						