

(Insert in 618-205, MJS77
Functional Requirements Book)
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MJS77-3-100

Functional Requirements, Saturn 1977 Spacecraft Requirements and Constraints

MJS77-3-110

Functional Requirement, Mariner Jupiter/Saturn 1977 Functional Block Diagrams and Interface Listings

MJS77-3-180

Functional Requirements, Mariner Jupiter/Saturn 1977 Configuration

MJS77-3-210

Functional Requirement, Mariner Jupiter/Saturn 1977 Criteria for Spacecraft Temperature Control

No. MJS77-4-2006-1A

20 March 1978

MJS77-3-220

Functional Requirement, Mariner Jupiter/Saturn 1977 Electronic Equipment

Supersedes
7 July 1975

MJS77-3-230

FUNCTIONAL REQUIREMENT, Mariner Jupiter/Saturn 1977 Equipment List and Mass
MARINER JUPITER/SATURN 1977 FLIGHT EQUIPMENT

FLIGHT DATA SUBSYSTEM

MJS77-3-240

Functional Requirement, Mariner Jupiter/Saturn 1977 Environmental Design
Requirements

MJS77-3-250

Functional Requirements, Mariner Jupiter/Saturn 1977 Power Profile and Allocation

1.0 SCOPE

The functional requirements for the Mariner Jupiter/Saturn 1977 (MJS77) flight data subsystem (FDS) are met by FDS hardware and FDS software. This document establishes the general FDS functional requirements and those associated with the FDS hardware. The functional requirements for FDS software are established in MJS77-4-2006-2, Flight Data Subsystem Software.

2.0 APPLICABLE DOCUMENTS

Functional Requirement, Mariner Jupiter/Saturn 1977 Telemetry Measurements and

The following documents form a part of this Functional Requirement.

MJS77-3-290

NOTE

Functional Requirement, Mariner Jupiter/Saturn 1977 Command Structure and

MJS77-3-100, Spacecraft Requirements and Constraints, applies to this document. Requirements of other MJS77 level three documents may also be applicable. It is the responsibility of the user to adequately acquaint himself with the organization and pertinent content of the level three documents, as well as with the material contained herein.

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REQUIREMENTS

Jet Propulsion Laboratory

MJS77-3-100

Functional Requirement, Mariner Jupiter/Saturn 1977 Support Equipment Functional Block Diagrams and Interface Listings

Jet Propulsion Laboratory

MJS77-3-110

Functional Requirement, Mariner Jupiter/Saturn 1977 Spacecraft Requirements and Constraints

1006740

Functional Requirement, Mariner Jupiter/Saturn 1977 Functional Block Diagram and Interface Listings

OTHER MJS77-3-180

Functional Requirements, Mariner Jupiter/Saturn 1977 Configuration

Jet Propulsion Laboratory

MJS77-3-210

Functional Requirement, Mariner Jupiter/Saturn 1977 Design Criteria for Spacecraft Temperature Control Plan

3.0

FUNCTIONS

Functional Requirement, Mariner Jupiter/Saturn 1977 Electronic Equipment Design

The Major Functions

Functional Requirement, Mariner Jupiter/Saturn 1977 Equipment List and Mass Allocations

a) Collect engineering data from modules.

Functional Requirement, Mariner Jupiter/Saturn 1977 Environmental Design Requirements

b) Perform 8-bit analog-to-digital conversion of digital data.

Functional Requirement, Mariner Jupiter/Saturn 1977 Power Profile and Allocation

c) Format engineering and science data through the modulator.

Functional Requirement, Mariner Jupiter/Saturn 1977 Electrical Grounding and Interfacing

d) Accept commands from the computer command subsystem (CCS).

Functional Requirement, Mariner Jupiter/Saturn 1977 Telemetry and Command Handling

e) MJS77-3-270 data mode specified in MJS77-3-280, Telemetry

Functional Requirement, Mariner Jupiter/Saturn 1977 Telemetry Measurements and Data Formats

MJS77-3-290

Functional Requirement, Mariner Jupiter/Saturn 1977 Command Structure and Assignments

MJS77-4-2006-1A

MJS77-3-1110 Functional Requirement, Mariner Jupiter/Saturn 1977 Support Equipment Functional Block Diagrams and Interface Listings
DRAWINGS
Lunar and planetary subsystems (LPS), radio frequency subsystem (RFS), radio frequency interface (RFI), astronomy subsystem (AS), low noise electronic equipment (LNE), infrared interferometer subsystem (LIPS), plasma subsystem (PS), ultraviolet spectrometer and radiometer subsystem (URS), photopolarimeter subsystem (PPS), modulation demodulation subsystem (MDS).

Jet Propulsion Laboratory

10063288 Circuit Data Sheet Index and Guide

10062408 FDS Interface Control Drawing

OTHER DOCUMENT

618-232 Voyager, Spacecraft System Configuration Management Plan

3.0 FUNCTIONAL REQUIREMENTS

The MJS77 FDS shall:

- a) Collect engineering data from the mission and propulsion modules.
- b) Collect data from, and control the operation of, the science instruments.
- c) Perform 8-bit analog-to-digital conversion of engineering and science analog data having low sample rate requirements.
- d) Format engineering and science data for on-board storage by the data storage subsystem (DSS) and/or real-time transmission through the modulation demodulation subsystem (MDS).
- e) Accept commands from the computer command subsystem (CCS) and provide commands to the science instruments according to the bit patterns as specified in MJS77-3-290, Command Structure and Assignments.
- f) Provide the data modes, rates, formats, and conditioning as specified in MJS77-3-270, Telemetry and Command Handling, and MJS77-3-280, Telemetry Measurements and Data Formats.

Normal operation uses a single processor and both memories. The prime memory contains the executing program and scratch pad for data buffering. Secondary memory usually contains a redundant program but can be used for data buffering and parameter storage. A new program can be loaded into secondary memory without effecting the

MJS77-4-2006-1A

- g) Provide frequency references to MDS, DSS, power subsystem (PWR), radio frequency subsystem (RFS), CCS, planetary radio astronomy subsystem (PRA), low energy charged particle subsystem (LECP), plasma subsystem (PLS), infrared interferometer spectrometer and radiometer subsystem (IRIS), photopolarimeter subsystem (PPS), and magnetometer subsystem (MAG).
- h) Be mechanized such that no single failure shall cause the loss of data from more than one science instrument or more than one-half of all engineering data.
- i) Retain its memory contents as long as the 50 V, 2.4 kHz power is present, or the 30 V bus is greater than 15 V.
- j) Provide the capability to control the recording and playback of the DSS. The FDS shall be capable of synchronizing playback data from DSS in order to perform processing of that data if the telecom performance should become degraded.
- k) Provide the capability to update memory contents via the umbilical lines.
- l) Provide the capability for commandable telemetered readout of each of its memories.
- m) Provide the capability to encode the general science and engineering data using a Golay (24, 12) code with an interleaved depth of 36 and a Reed-Solomon (J=8, E=16) code with an interleaving depth of 4 for transmission to MDS on the high rate channel.
- n) Provide the capability of encoding the MDS high rate data using a Viterbi (K=7, R=1/3) code for transmission to MDS on the low rate channel.

4.0 FUNCTIONAL DESCRIPTION

4.1 Functional Block Diagram

A block diagram of the FDS is shown in Figure 1. The basic approach is similar to standard computer applications having a computer (FDS processor) interfacing with several peripheral devices (FDS I/O units). The processor uses a single interrupt for periodic synchronization which is not part of the interface with the I/Os. This synchronization allows automatic recovery from changes in unprotected memory should they occur.

Normal operation uses a single processor and both memories. The prime memory contains the executing program and scratch pad for data buffering. Secondary memory usually contains a redundant program but can be used for data buffering and parameter storage. A new program can be loaded into secondary memory without effecting the

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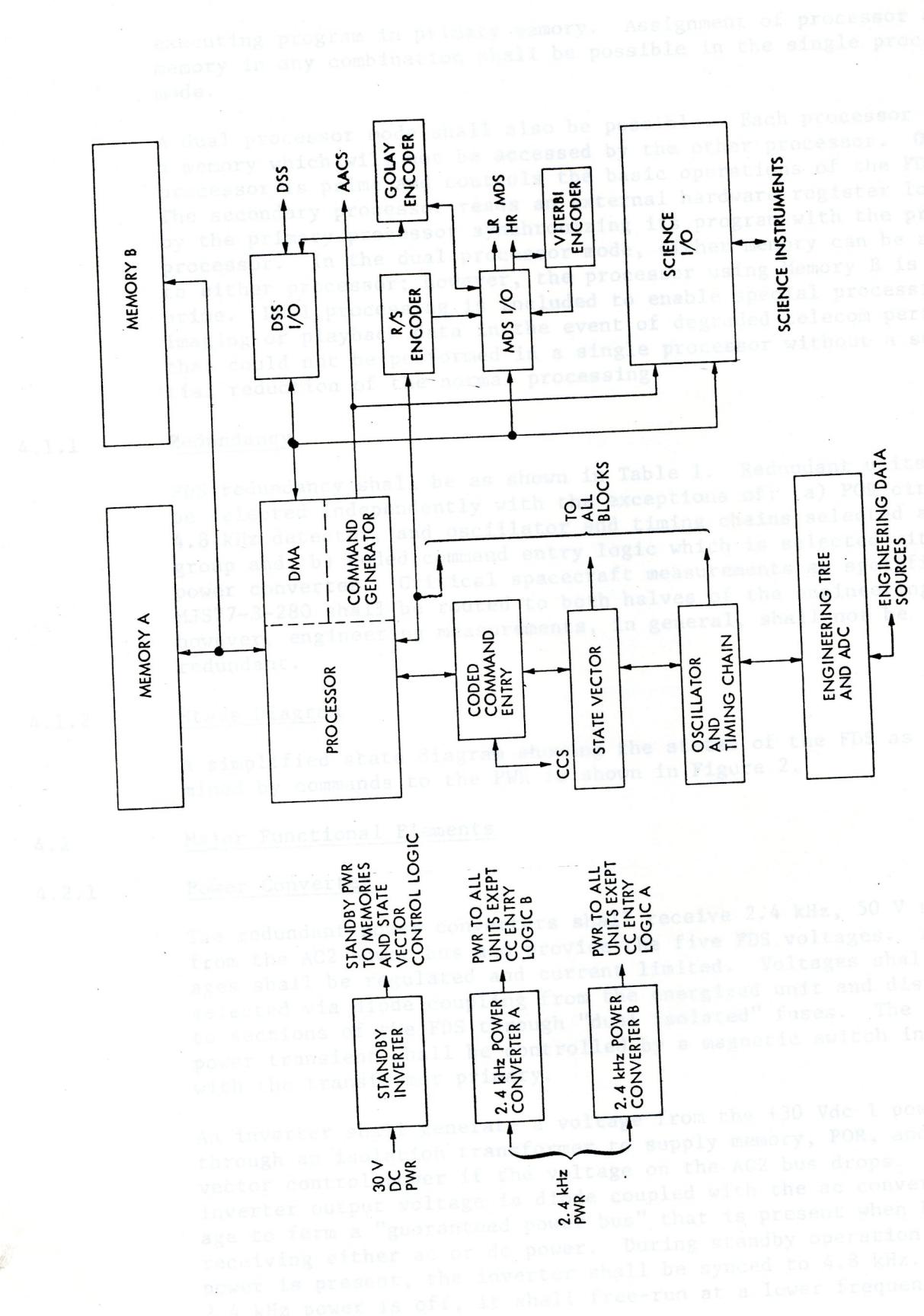


Figure 1: FDS Hardware Functional Block Diagram

MJS77-4-2006-1A

executing program in primary memory. Assignment of processor and memory in any combination shall be possible in the single processor mode.

A dual processor mode shall also be possible. Each processor uses a memory which will not be accessed by the other processor. One processor is prime and controls the basic operations of the FDS. The secondary processor reads an external hardware register loaded by the primary processor synchronizing its program with the primary processor. In the dual processor mode, either memory can be assigned to either processor; however, the processor using Memory B is always prime. Dual processing is included to enable special processing of imaging or playback data in the event of degraded telecom performance that could not be performed in a single processor without a substantial reduction of the normal processing.

4.1.1 Redundancy

FDS redundancy shall be as shown in Table 1. Redundant units shall be selected independently with the exceptions of: a) POR circuits, 4.8 kHz detector, and oscillator and timing chains selected as a group and, b) coded command entry logic which is selected with the power converter. Critical spacecraft measurements as specified in MJS77-3-280 shall be routed to both halves of the engineering trees; however, engineering measurements, in general, shall not be redundant.

4.1.2 State Diagram

A simplified state diagram showing the states of the FDS as determined by commands to the PWR is shown in Figure 2.

4.2 Major Functional Elements

4.2.1 Power Converter

The redundant power converters shall receive 2.4 kHz, 50 V rms power from the AC2 power bus and provide the five FDS voltages. All voltages shall be regulated and current limited. Voltages shall be selected via diode coupling from the energized unit and distributed to sections of the FDS through "dual isolated" fuses. The turn-on power transient shall be controlled by a magnetic switch in series with the transformer primary.

An inverter shall generate a voltage from the +30 Vdc 1 power bus through an isolation transformer to supply memory, POR, and state vector control power if the voltage on the AC2 bus drops. The inverter output voltage is diode coupled with the ac converter voltage to form a "guaranteed power bus" that is present when FDS is receiving either ac or dc power. During standby operation when main power is present, the inverter shall be synced to 4.8 kHz. When 2.4 kHz power is off, it shall free-run at a lower frequency.

MJS77-4-2006-1A

Table 1. FDS Redundancy Table

Nonredundant Units	Redundant Units
Memory standby inverter	Power converter
Reed-Solomon Encoder	POR circuits
State vector control	Oscillator and timing chain
Viterbi Encoder	4.8 kHz detector
DSS I/O	CC entry logic
ENG A	Processor
ENG B	Memory
IRIS I/O	CRS I/O
ISS NA I/O	LECP I/O
ISS WA I/O	MAG I/O
PLS I/O	Golay coder
PPS I/O	MDS I/O
PRA I/O	
PWS I/O	
UVS I/O	

The power converter shall supply a logic level 2.4 kHz sync signal that provides the basic timing for the CCS coded command interface. Voltages necessary to load commands can be supplied from the FDS SE. This method shall be used to load the FDS memories prior to main power turn-on during system level testing.

Excitation power for 11 external pressure transducers shall be provided with the capability to remove power from 5 pressure transducers during periods of the mission when these measurements are not required. The power to these subsystems shall not be inhibited by the detector circuit. The detector circuit performance shall be as characterized in paragraph 6.2.

4.2.3

Coded Command Entry Logic

This redundant logic shall receive coded commands from the CCS or FBS S/C and process them in hardware. Each unit shall be capable of receiving commands from either one of the two CCS coded command interfaces. The A unit shall be powered from power converter A and the B unit from power converter B. Switching to the redundant set of command logic shall be accomplished by switching power converters.

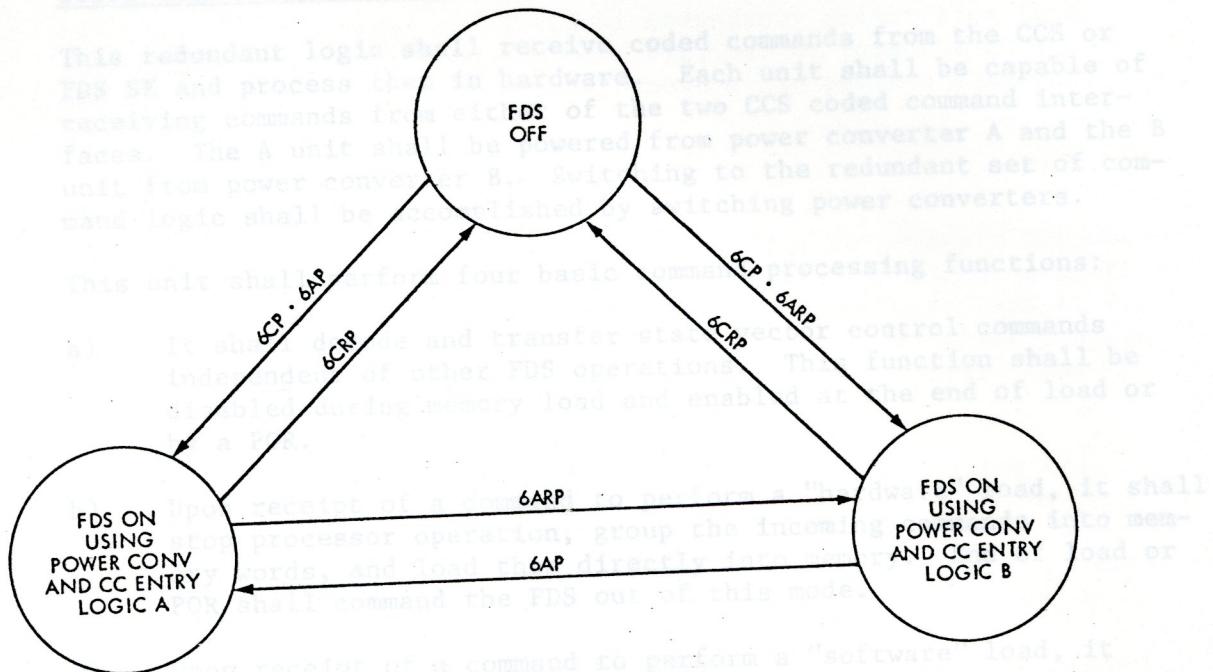


Figure 2. Simplified FDS State Diagram

The power converter shall have redundant POR circuits that initialize and inhibit operations during power turn-on or power outages. They are powered from the guaranteed bus and selected by the state vector control timing chain select signal. The circuit performance shall be as characterized in paragraph 6.3.

4.2.2

Oscillator and Timing Chain

The basic FDS timing shall be generated from a 4.8384 MHz (210.33.52.7) crystal controlled oscillator. The processor cycle time frequency of 403.2 kHz and other required frequencies shall be derived by dividing down from the master oscillator frequency. Both the oscillator and the countdown chain shall be redundant; however, only the oscillator and countdown chain selected by the state vector control shall be powered. The oscillator performance shall be as described in paragraph 6.4.

4.2.4

A 4.8 kHz signal shall be generated and sent to PWR for synchronizing the spacecraft 2.4 kHz inverters. A detector circuit in the FDS shall inhibit this signal when out of tolerance. Frequency references supplied by the FDS to other subsystems shall not be inhibited by the detector circuit. The detector circuit performance shall be as characterized in paragraph 6.2.

4.2.3

Coded Command Entry Logic

This redundant logic shall receive coded commands from the CCS or FDS SE and process them in hardware. Each unit shall be capable of receiving commands from either of the two CCS coded command interfaces. The A unit shall be powered from power converter A and the B unit from power converter B. Switching to the redundant set of command logic shall be accomplished by switching power converters.

4.2.5

This unit shall perform four basic command processing functions:

- a) It shall decode and transfer state vector control commands independent of other FDS operations. This function shall be disabled during memory load and enabled at the end of load or by a POR.
- b) Upon receipt of a command to perform a "hardware" load, it shall stop processor operation, group the incoming commands into memory words, and load them directly into memory. End of load or POR shall command the FDS out of this mode.
- c) Upon receipt of a command to perform a "software" load, it shall pass subsequent command words to the processor for grouping into memory words. This loading shall be performed without interfering with a running program. When the program recognizes the end of a load, the coded command logic shall be reset. POR shall allow recovery from this mode in the event of a processor malfunction. The memory protect logic is momentarily overridden when writing into protected memory. Commands will be separated by greater than 60 ms in this mode.
- d) It shall send commands that are not associated with the state vector control logic or a software load to the processor where they can be software decoded. This will enable the changing of several functions by a single 12-bit command if the software load technique is not efficient for some changes.

4.2.4

State Vector Control Logic

This single unit shall control all FDS redundancy except the power converters and the CC ENTRY logic which are selected together through PWR. State vector commands shall be decoded in the energized CC ENTRY logic and fed directly to this unit. Only a working power converter and CC ENTRY logic unit shall be required to change the state vector. Recovery shall be possible from any failure outside this unit including the FDS timing chain. The state vector control logic shall be powered from the guaranteed bus and shall be independent of the POR. It must be set at initial turn-on.

The state vector control logic shall be designed so that a single failure will not leave any critical redundancy select line in an indeterminate state. This includes blowing the fuse for this unit which will select all A units and remove write protect from both memories.

4.2.5

Processor

The FDS processor shall provide the capability to generate sequences of control signals to the instrument I/O units, to collect data from I/O units, to perform simple data processing algorithms, and to format and output data to the MDS and DSS I/O units, all under program control. Processor functions fall into five general areas (see Figure 3). These are:

- a) The execution of instructions by a central processing unit (CPU).
- b) Direct access to memory (DMA) for high speed transfer of data to and from consecutive memory locations.
- c) Periodic restarting of the program based on a timing "interrupt" occurring every 2.5 ms.
- d) The provision for a data path, and control logic, which allow direct loading of blocks of data into the FDS memories by the CCS command entry logic.
- e) Memory access gating which allows either processor to be used alone with both memories, or each processor to be used with a single memory.

4.2.5.1

Instruction Execution. The FDS instruction set shall provide for:

- a) Moving data between special memory registers, general memory, and I/O units using serial and parallel word transfers along with a 5-bit bus used for high speed discrete commanding.
- b) Performing arithmetic, logical, and shifting operations on data in special registers.
- c) Modifying the program sequence by unconditionally jumping or by skipping conditionally based on the contents of special registers or arithmetic operation results.
- d) Controlling which half of the 8 K memory the program is executing in through a pair of special OUT instructions; SETJU for set jump up and SETJD for set jump down. The program operates in the lower 4K until SETJU occurs which causes the next jump to transfer control to the given 12-bit address in the upper 4 K. Subsequent JUMP's continue to transfer control with upper

Figure 3. FDS Processor Functional Block Diagram

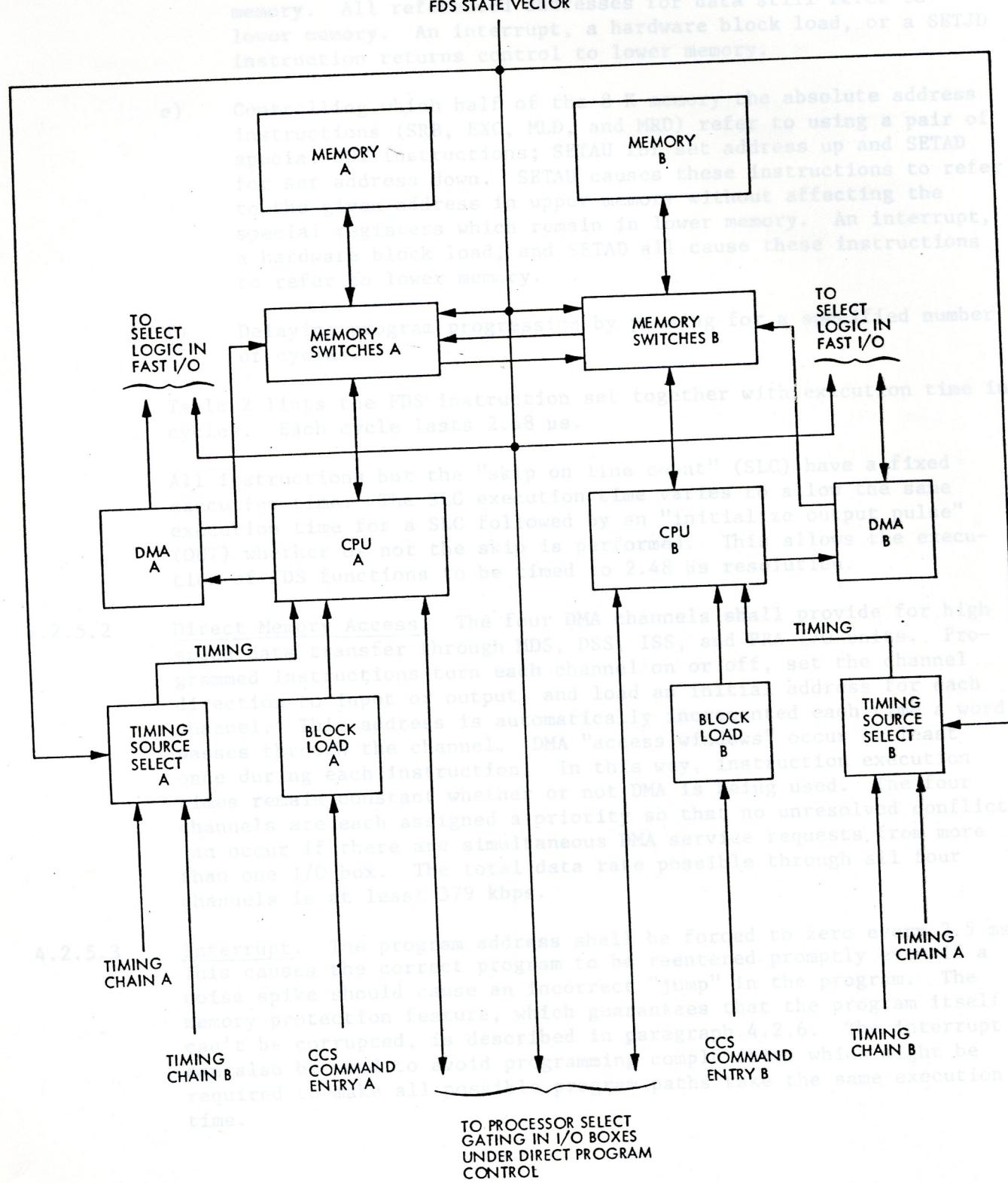


Figure 3. FDS Processor Functional Block Diagram

memory. All referenced addresses for data still refer to lower memory. An interrupt, a hardware block load, or a SETJD instruction returns control to lower memory.

- 1. INPUT/OUTPUT
 - e) Controlling which half of the 8 K memory the absolute address instructions (SRB, EXC, MLD, and MRD) refer to using a pair of special OUT instructions; SETAU for set address up and SETAD for set address down. SETAU causes these instructions to refer to the given address in upper memory without affecting the special registers which remain in lower memory. An interrupt, a hardware block load, and SETAD all cause these instructions to refer to lower memory.
 - f) Delaying program progression by pausing for a specified number of cycles.
- 2. MEMORY ALTER
 - 3. BRANCHING
 - 4. DIRECT MEMORY READ
 - 5. INDEX MODIFICATION
 - 6. CONDITIONAL MODIFY INDEX
 - 7. TIMING
 - 8. INDEX MODIFICATION

Table 2 lists the FDS instruction set together with execution time in cycles. Each cycle lasts 2.48 μ s.

All instructions but the "skip on line count" (SLC) have a fixed execution time. The SLC execution time varies to allow the same execution time for a SLC followed by an "initialize output pulse" (OUT) whether or not the skip is performed. This allows the execution of FDS functions to be timed to 2.48 μ s resolution.

- #### 4.2.5.2
- Direct Memory Access. The four DMA channels shall provide for high speed data transfer through MDS, DSS, ISS, and PRA I/O units. Programmed instructions turn each channel on or off, set the channel direction to input or output, and load an initial address for each channel. This address is automatically incremented each time a word passes through the channel. DMA "access windows" occur at least once during each instruction. In this way, instruction execution times remain constant whether or not DMA is being used. The four channels are each assigned a priority so that no unresolved conflict can occur if there are simultaneous DMA service requests from more than one I/O box. The total data rate possible through all four channels is at least 379 kbps.

- #### 4.2.5.3
- Interrupt. The program address shall be forced to zero every 2.5 ms. This causes the correct program to be reentered promptly even if a noise spike should cause an incorrect "jump" in the program. The memory protection feature, which guarantees that the program itself can't be corrupted, is described in paragraph 4.2.6. The interrupt can also be used to avoid programming complexities which might be required to make all possible program paths take the same execution time.

Table 2. FDS Instruction Set

MNEMONIC	CYCLES	FUNCTION
1. INPUT/OUTPUT		
OUT	3	INITIALIZE OUTPUT PULSE
PWD	4	PARALLEL WORD TRANSFER
SWO	11	SERIAL WORD OUT
SWI	11	SERIAL WORD IN
2. MEMORY REFERENCE		
AMR	6	AUTO INDEXED MEMORY READ
AML	6	AUTO INDEXED MEMORY LOAD
MRD	4	DIRECT MEMORY READ
MLD	4	DIRECT MEMORY LOAD
SRB	3	STORE RB (RETURN ADDRESS)
3. BRANCHING		
JMP	2	JUMP
SLC	3 OR 6	SKIP ON LINE COUNT NOT EQUAL TO VALUE
SKP	3	SKIP ON POSITIVE
ISP	4	INCREMENT AND SKIP ON POSITIVE
DSP	4	DECREMENT AND SKIP ON POSITIVE
SKZ	3	SKIP ON ZERO
ISZ	4	INCREMENT AND SKIP ON ZERO
DSZ	4	DECREMENT AND SKIP ON ZERO
SKO	3	SKIP ON OVERFLOW
SKE	3	SKIP IF INDEX IS EQUAL TO VALUE
EXC	2	EXECUTE
SKC	3	SKIP ON CARRY
4. SHIFTING		
LRS	9	LONG RIGHT SHIFT (ARITHMETIC)
LLS	9	LONG LEFT SHIFT
LRR	9	LONG RIGHT ROTATE
SRS	6	SHORT RIGHT SHIFT
SLS	6	SHORT LEFT SHIFT
SRR	6	SHORT RIGHT ROTATE
ARS	6	SHORT RIGHT SHIFT (ARITHMETIC)
5. ARITHMETIC AND LOGIC		
ADD	6	ADD
SUB	6	SUBTRACT
AND	6	LOGICAL AND
LOR	6	LOGICAL OR
LXR	6	LOGICAL EXCLUSIVE OR
6. CONSTANTS		
ABS	3	LOAD ABSOLUTE
7. TIMING		
WAT	2-4097	WAIT
8. INDEX MODIFICATION		
MCX	4	CONDITIONALLY MODIFY INDEX

4.2.5.4 Hardware Block Load. The initial FDS memory load and subsequent substitutions for large blocks of FDS memory are performed by stopping the normal CPU sequencing and giving control of the memory to the CCS command entry logic. This logic will load a starting address into the CPU and then supply a series of data words to be loaded into consecutive locations. The address is automatically incremented by the CPU after each word is loaded.

4.2.5.5 Memory Access Switching. In normal operation only one processor will be operating. The FDS state vector selects the operating processor and selects one 8192 word memory as prime and one as secondary. Operating programs will reside in the prime memory. The secondary memory can be accessed for storage and retrieval of data blocks. A possible alternate mode of operation is that in which both processors operate with all access confined to a single 8192 memory for each processor.

4.2.6 Memories

The FDS shall contain two 8192 word x 16 bit/word memories using 256 x 1 bit CMOS random access memories (RAMs). Each memory is constructed using four large scale digital hybrid modules. Each hybrid module has a 2048 word x 16 bit/word organization and provides adequate mission radiation shielding by means of the hybrid package design.

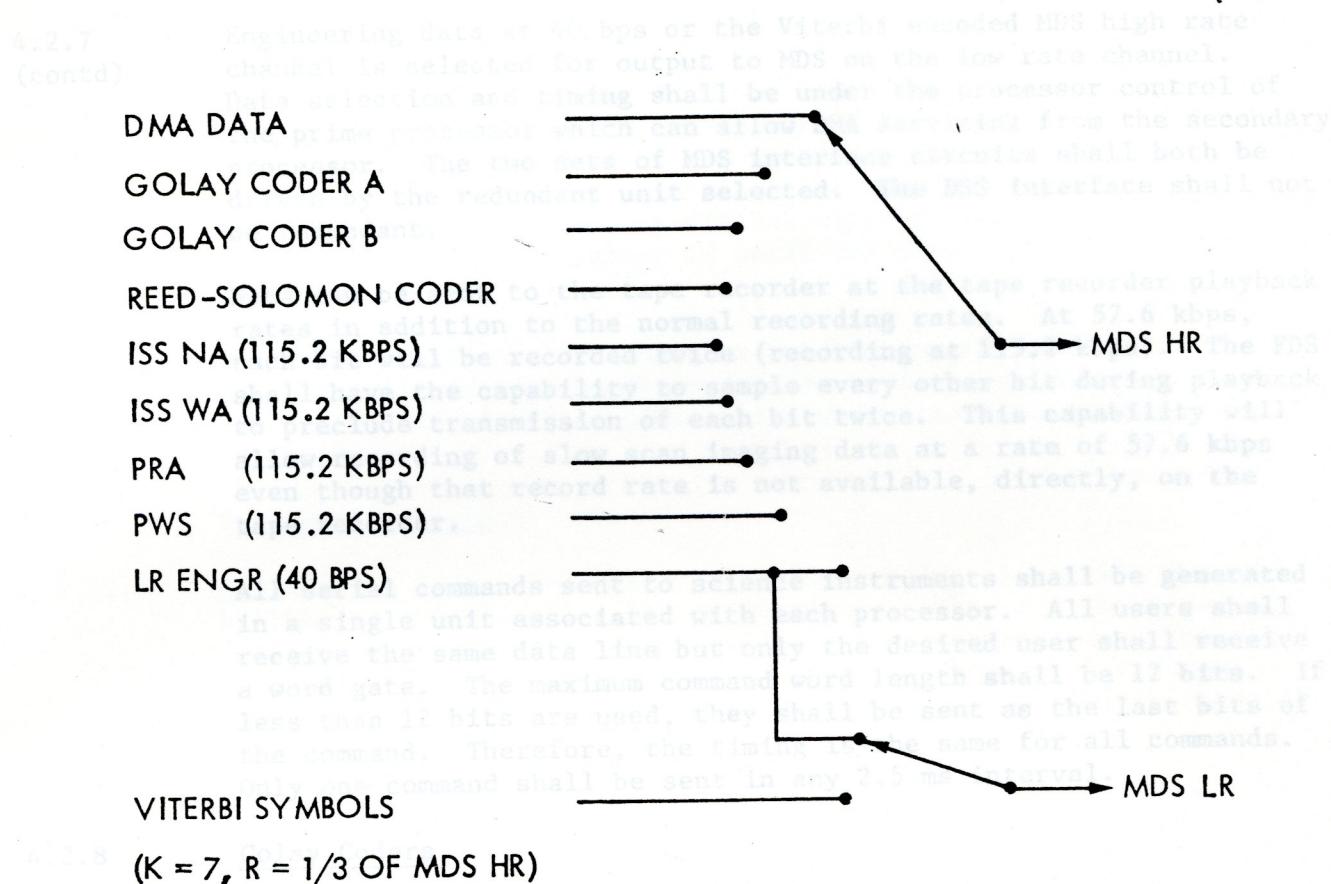
The state vector control logic shall assign one memory as prime and the other as secondary. Programs are executed from the prime memory only. Unused primary memory and the secondary memory can be used for buffering and parameter storage. The state vector also has a bit that controls which half of the 8 K memory is actually accessed by inverting the 13th address bit. This allows recovery from failures in the special register locations by relocating them and redefining the failed locations to be in upper memory.

Each memory shall have write protect circuitry used to protect the program storage during transient conditions. Protection is contiguous in a single block for each 4 K of memory starting from address "000" to 9FF (2560 decimal), to BFF (3072 decimal), or DFF (3584 decimal). This protect must be overridden to write into these areas during memory loads. The memory contents shall be retained as long as either power converter is receiving 50 V rms, 2.4 kHz power, or the 30 V bus is greater than 15 V.

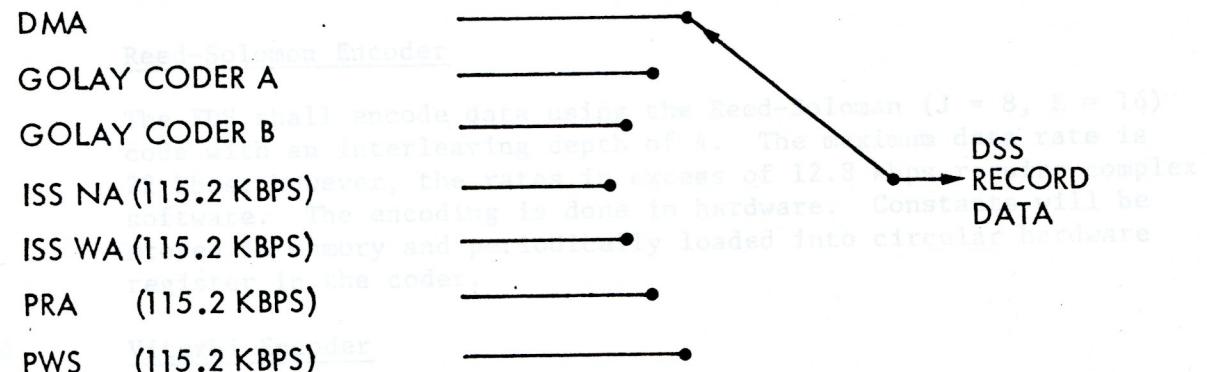
4.2.7 Data and Command I/O

The FDS shall output data to the DSS for temporary storage and to MDS for real-time transmission. Both units shall receive data from memory using DMA, from the Golay coders or directly from the ISS, PRA, and PWS I/O units. In addition, MDS receives Reed-Solomon coded data and engineering data at 40 bps as shown in Figure 4.

Figure 4. Data Output Functional Diagram



The FSS shall code 3600 bps general science and engineering (GSE) data and 40 bps engineering data (24, 12) code interleaved to depth 36. The MDS I/O data output shall be as specified in MDS I/O Data Selection. The Golay coders shall be redundant with the exception that both coders are required to generate telemetry modes in which Golay coded outputs are sent to the DSS and MDS at the same time at different rates.



The FSS shall encode the MDS HR data stream using K = 7, R = 1/3 code interleaved to the capability to transmit this data to the MDS data line. When this encoder is being used, the MDS HR data line to MDS will be unusable (MDS symbol sync is 3 times the data rate rather than 7 times as required by the MDS).

Figure 4. Data Output Functional Diagram

- 4.2.7 (contd) Engineering data at 40 bps or the Viterbi encoded MDS high rate channel is selected for output to MDS on the low rate channel. Data selection and timing shall be under the processor control of the prime processor which can allow DMA servicing from the secondary processor. The two sets of MDS interface circuits shall both be driven by the redundant unit selected. The DSS interface shall not be redundant.
- 4.2.12 Data can be sent to the tape recorder at the tape recorder playback rates in addition to the normal recording rates. At 57.6 kbps, each bit will be recorded twice (recording at 115.2 kbps). The FDS shall have the capability to sample every other bit during playback to preclude transmission of each bit twice. This capability will allow recording of slow scan imaging data at a rate of 57.6 kbps even though that record rate is not available, directly, on the tape recorder.
- 4.2.12.1 All serial commands sent to science instruments shall be generated in a single unit associated with each processor. All users shall receive the same data line but only the desired user shall receive a word gate. The maximum command word length shall be 12 bits. If less than 12 bits are used, they shall be sent as the last bits of the command. Therefore, the timing is the same for all commands. Only one command shall be sent in any 2.5 ms interval.
- 4.2.8 Golay Coders
The FDS shall code 3600 bps general science and engineering (GS&E) data with a Golay (24, 12) code interleaved to depth 36. The format of the coded data output shall be as specified in MJS77-3-280. The Golay coders shall be redundant with the exception that both coders are required to generate telemetry modes in which Golay coded outputs are sent to the DSS and MDS at the same time at different rates.
- 4.2.9 Reed-Solomon Encoder
The FDS shall encode data using the Reed-Solomon ($J = 8, E = 16$) code with an interleaving depth of 4. The maximum data rate is 22 kbps; however, the rates in excess of 12.8 kbps require complex software. The encoding is done in hardware. Constants will be stored in memory and periodically loaded into circular hardware register in the coder.
- 4.2.10 Viterbi Encoder
The FDS shall encode the MDS HR data stream using $K = 7, R = 1/3$ code and provide the capability to transmit this data to the MDS via the low rate data line. When this encoder is being used, the MDS HR data line to MDS will be unusable (MDS symbol sync is 3 times the data rate rather than 2 times as required by the MDS).

- 4.2.11 Science I/O Units employed cancels the small errors due to integrator saturation and commutator offset voltages.
- These units shall perform two basic functions. They shall receive instruction words from memory via the processors that specify when each signal is to be sent to the science instruments. The I/O unit shall decode that word and initiate the appropriate action. Secondly, they shall receive digital data from the science instruments and temporarily buffer it until the processor picks up the data under program control.
- 4.2.12 UVS and PPS Measurements. The MDS will shift UVS and PPS I/Os shall both contain hardware that performs a floating point compression on their data as it is being shifted into the FDS. All UVS and PPS samples shall be compressed and cannot be bypassed.
- 4.2.12.1 Engineering Tree. The FDS engineering tree shall provide the capability for accommodating 243 measurements. The tree shall be divided into two nonredundant halves. Three types of measurements shall be made: 1) temperature, 2) digital, and 3) 0-3 V analog. The number of each type available in the A and B halves shall be as shown below:
- | | | |
|--------------|----|----|
| Temperature | 45 | 45 |
| Digital | 32 | 16 |
| 0-3 V Analog | 45 | 60 |
- Measurements shall be 8 bits each and can be taken at a maximum rate of one each 6-2/3 ms, (equivalent to a data rate of 1200 bps). Assignment of measurements to specific locations on the FDS engineering tree shall be as specified in MJS77-3-280. The electrical interface constraints for the tree are specified in MJS77-3-260, Electrical Grounding and Interfacing.
- 4.2.12.2 Engineering ADC. The redundant Engineering ADC shall be the dual integrating type with word conversion timing based upon an 8-bit engineering word at 1200 bps (833-1/3 μ s/bit). The convert time is always the same, i.e., it is independent of the engineering data rate. The integration period is selected to provide heavy rejection to sinusoidal components of the 2.4 kHz power. The type of ADC and

conversion cycle employed cancels the small errors due to integrator time constant variations and commutator offset voltages.

4.2.12.3 Engineering Readout Structure. The engineering readout structure shall be as specified in MJS77-3-280. This structure is generated by FDS software via a parameter look-up table stored in FDS memory.

4.2.12.4 Special Telemetry Interfaces

4.2.12.4.1 MDS Signal-to-Noise Ratio (SNR) Measurement. The MDS will shift a 20-bit serial word, MSB first, to the FDS every 62.5 ms which is related to the ST_B/No at the input to the command detector unit (CDU). The FDS shall transfer the 16 LSBs of the 20-bit SNR word into a storage register upon receipt on an alert pulse supplied by the MDS. The contents of this storage register are inserted into the telemetry stream with the next two samples of the SNR measurement. The storage register shall be reset to zero upon being read out.

4.2.12.4.2 MDS Oscillator Monitor. The MDS will provide the FDS a 1638.4 Hz squarewave signal which is related to the command detector unit oscillator frequency. The FDS shall count this signal over intervals of 96 s and generate an 8-bit word which defines the signal frequency. The oscillator monitor frequency and counter interval are chosen so that each count represents a frequency change of 6.35 ppm; and so that the residue remaining in the 7 LSBs of the register is centered at midrange when the MDS and FDS oscillator frequencies are at their design values. The MSB of the register shall be set to "1" when the correct number of overflows have occurred and "0" otherwise. At the end of the count interval, the data in the counting register shall be transferred to an 8-bit storage register and the count register shall be reset. The storage register shall hold the telemetry sample until readout or updated with a later sample. The storage register shall be reset upon readout. If the storage register is interrogated after being read, but prior to being updated with a new sample, the telemetry word shall be all zeros.

4.2.10.4.3 Propulsion IPU and TCAPU Pressure Measurements. The FDS shall provide four 16-bit counters to accumulate pulses supplied by selected IPU or TCAPU thrusters. These registers are POR'ed to 0 and count the pulses on the input lines thereafter. Data is sampled in the FDS at the time of occurrence of the data word gate of the most significant byte.

4.3 Data Rates and Modes

Data rates and modes shall be as specified in MJS77-3-270. Table 3 shows the data rates possible to MDS.

Table 3. Possible MDS Data Rates

0.010 kbps	4.800 kbps
0.020	5.400
0.023 1/3	5.600
*0.40	5.973 1/3
0.046 2/3	6.300
*0.080	6.400
0.093 1/3	*7.200
0.100	7.466 2/3
*0.160	8.400
0.186 2/3	9.600
0.200	10.800
0.233 1/3	11.200
b) 0.300	12.600
*0.320	12.800
0.373 1/3	14.400
0.400	14.933 1/3
0.466 2/3	16.800
c) 0.525	19.200
0.600	*21.600
*0.640	22.400
0.700	25.200
0.746 2/3	28.800
0.800	*29.866 2/3
0.900	33.600
0.933 1/3	38.400
1.050	43.200
*1.200	*44.800
*1.280	50.400
1.400	57.600
1.493 1/3	*67.200
1.600	86.400
1.800	*89.600
b) 1.866 2/3	100.800
2.100	*115.200
2.400	134.400
*2.560	172.800
2.700	201.600
2.800	268.800
2.986 2/3	345.600
3.200	403.200
*3.600	
3.733 1/3	
4.200	
<u>Engineering Analog Measurement Accuracies</u>	
* rates used in standard mission	

Engineering analog measurements are engineering measurements as read from the analog-to-digital converter. The following table lists the output of the converter below:

- a) 0-3-V measurement at 1 percent of full scale, $\pm 1/2$ DN quantization error.

4.4

Data Formats

Data formats shall be as specified in MJS77-3-280.

5.0

INTERFACE DEFINITION

5.1

Electrical Interfaces

The electrical interface shall be:

- a) Basic requirements are contained in MJS77-3-260 for electrical grounding, electrical bonding, electrical interface circuits, and electromagnetic compatibility.
- b) Specific system level requirements for electrical interface circuits and grounding are contained in the applicable circuit data sheets. For additional information, refer to JPL Drawing 10063288, Circuit Data Sheet Index and Guide.
- c) All spacecraft flight and umbilical interface circuits, e.g., subsystem-subsystem, subsystem-launch vehicle, and subsystem-support equipment through the umbilical connector are listed in MJS77-3-110, Functional Block Diagram and Interface Listings. All such circuits interfacing with this subsystem are reproduced for reference in Table 4 herein.
- d) All spacecraft nonflight circuits, including direct access circuits, are listed in MJS77-3-1110, Support Equipment Functional Block Diagrams and Interface Listings.
- e) Details of each interface are described in MJS77-3-270.

5.2

Mechanical Interfaces

Mechanical interfaces with the spacecraft shall be as specified on the JPL Drawing 10062408, FDS Interface Control Drawing, and in MJS77-3-180, Configuration.

5.3

Thermal

There are no special FDS thermal requirements. The FA temperature range is 0 to +55°C.

6.0

PERFORMANCE

6.1

Engineering Analog Measurement Accuracies

The accuracy of analog engineering measurements as read from the input of the FDS to the engineering ADC output shall be as specified below:

- a) 0-3 V measurements: ± 1 percent of full scale, $\pm 1/2$ DN quantization error.

Table 4. Electrical Interface Circuits
MJS77

KEY: Only S/C system level electrical interface circuits are listed.		
Heading	Code	Explanation
<u>Item:</u>	1,2	Items are numbered consecutively for quick reference
<u>Subsystem (SUB):</u>	001	Structure subsystem
	002	Radio frequency subsystem
	003	Modulation/demodulation subsystem
	004	Power subsystem
	005	Computer command subsystem
	007	Attitude and articulation control subsystem
	008	Pyrotechnic subsystem
	009	Cabling subsystem
	010	Propulsion subsystem
	011	Temperature control subsystem
	012	Mechanical devices subsystem
	016	Data storage subsystem
	017	S/X-band antenna subsystem
	021	Cosmic ray subsystem
	022	Planetary radio astronomy subsystem
	023	Plasma wave subsystem
	025	Low energy charged particle subsystem
	027	Photopolarimeter subsystem
	032	Plasma subsystem
	034	Ultraviolet spectrometer subsystem
	035	Magnetometer subsystem
	036	Imaging science subsystem
	039	Infrared interferometer and radiometer subsystem
<u>Flow:</u>	>	Signal flow is to the right (relative to the Sub-SUB code)
	<	Signal flow is to the left
	-	Signal flow may be either left or right
<u>Circuit Name</u>		Listed exactly as in MJS77-3-110.

TABLE 4. ELECTRICAL INTERFACE CIRCUITS
MJS77 (CONT)

ITEM	SUB	SUB	NO FLOW	CIRCUIT NAME

ITEM	SUB	SUB	NO FLOW	CIRCUIT NAME
STRU	-			FDS

1. 001-006- 01 > TLM RAY 1 TEMP
2. 001-006- 02 > TLM RAY 3 TEMP US SHIFT CLOCK
3. 001-006- 03 > TLM RAY 5 TEMP WORD GATE
4. 001-006- 04 > TLM RAY 7 TEMP WORD GATE
5. 001-006- 05 > TLM RAY 9 TEMP US 1 OUTPUT
6. 001-006- 06 > TLM RAY 2 TEMP US 2 OUTPUT
7. 001-006- 07 > TLM RAY 4 TEMP HYBRID TEMP
8. 001-006- 08 > TLM RAY 6 TEMP TEMP
9. 001-006- 09 > TLM RAY 8 TEMP TEMP
10. 001-006- 10 > TLM RAY 10 TEMP TEMP

002-006- 20 > TLM S-BAND TWT/SSA BASE TEMP

ITEM	SUB	SUB	NO FLOW	CIRCUIT NAME
RFS	-			FDS

11. 002-006- 01 < 14.4KHZ, S&X BAND TWTA/SSA
12. 002-006- 02 > TLM X-BAND TWT CATHODE CUR
13. 002-006- 03 > TLM X-BAND TWT REG V
14. 002-006- 04 > TLM X-BAND HGA DR
15. 002-006- 05 > TLM X-BAND TWT HFLIX CUR
16. 002-006- 06 > TLM S-TWT CATHODE/SSA INPUT CUR
17. 002-006- 07 > TLM S-BAND TWT/SSA REG V
18. 002-006- 08 > TLM S-BAND TWT HFLIX CUR
19. 002-006- 09 < 50.4KHZ, SEX-1, XEX-1, & RCVR 1
20. 002-006- 10 < 50.4KHZ, SEX-2, XEX-2, & RCVR 2

TABLE 4. ELECTRICAL INTERFACE CIRCUITS
MJS77 (CONT)

ITEM	SUB	SUB	NO FLOW	CIRCUIT NAME
	RFS	-	FDS	
21.	002-006-	11	>	14.4KHZ STATUS SHIFT CLOCK
22.	002-006-	12	<	RFS STATUS 1 WORD GATE
23.	002-006-	13	<	RFS STATUS 2 WORD GATE
24.	002-006-	14	>	TLM RFS STATUS 1 OUTPUT
25.	002-006-	15	>	TLM RFS STATUS 2 OUTPUT
26.	002-006-	16	>	TLM X-BAND HYBRID TEMP
27.	002-006-	17	>	TLM RCVR VCO TEMP
28.	002-006-	18	>	TLM AUX OSC TEMP
29.	002-006-	19	>	TLM X-BAND EX TEMP
30.	002-006-	20	>	TLM S-BAND TWT/SSA BASE TEMP
31.	002-006-	21	>	TLM X-BAND TWT BASE TEMP
32.	002-006-	22	>	TLM X-BAND RF MONITOR TEMP
33.	002-006-	23	>	TLM X-BAND EX CUR
34.	002-006-	24	>	TLM RCVR LO DR
35.	002-006-	25	>	TLM RCVR 1 AGC;XR
36.	002-006-	26	>	TLM RCVR 1 OR 2 VCO V COARSE
37.	002-006-	27	>	TLM S-BAND EX CUR
38.	002-006-	28	>	TLM RCVR 2 AGC;XR
39.	002-006-	29	>	TLM RCVR RANGING AGC V
40.	002-006-	30	>	TLM RCVR 1 OR 2 VCO V FINE
41.	002-006-	31	>	TLM RCVR CUR

TABLE 4. ELECTRICAL INTERFACE CIRCUITS
MJS77 (CONT)

ITEM	SUB	SUB	NO FLOW	CIRCUIT NAME
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RFS	-	FDS	
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- | | | | | |
|-----|----------|----|---|------------------------|
| 42. | 002-006- | 32 | > | TLM S-BAND HGA DRIVE |
| 43. | 002-006- | 33 | > | TLM X-BAND TWT DRIVE |
| 44. | 002-006- | 34 | > | TLM S-BAND TWT DR |
| 45. | 002-006- | 35 | > | TLM LGA DRARRIER LOCK |
| 46. | 002-006- | 36 | > | TLM USO INNER OVFN CUR |
| 47. | 002-006- | 37 | > | TLM S-BAND HYBRID TEMP |
| 48. | 002-006- | 38 | > | TLM XMTR RF ASW TEMP |

MDS	-	FDS	
-----	---	-----	--

- | | | | | |
|-----|----------|----|---|---------------------------------|
| 49. | 003-006- | 01 | < | TMU-A SYMBOL SYNC |
| 50. | 003-006- | 02 | < | HIGH RATE CHANNEL DATA TO TMU-A |
| 51. | 003-006- | 03 | < | LOW RATE CHANNEL DATA TO TMU-A |
| 52. | 003-006- | 04 | < | TMU-A 14.4KHZ SHIFT CLOCK |
| 53. | 003-006- | 05 | < | TMU-A STATUS WORD GATE 1 |
| 54. | 003-006- | 06 | < | TMU-A STATUS WORD GATE 2 |
| 55. | 003-006- | 07 | > | TMU-A STATUS DATA |
| 56. | 003-006- | 08 | < | TMU-B SYMBOL SYNC |
| 57. | 003-006- | 09 | < | HIGH RATE CHANNEL DATA TO TMU-B |
| 58. | 003-006- | 10 | < | LOW RATE CHANNEL DATA TO TMU-B |
| 59. | 003-006- | 11 | < | TMU-B 14.4KHZ SHIFT CLOCK |
| 60. | 003-006- | 12 | < | TMU-B STATUS WORD GATE 1 |

TABLE 4. ELECTRICAL INTERFACE CIRCUITS
MJS77 (CONT)

ITEM	SUB	SUB	NO	FLOW	CIRCUIT NAME
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	MDS	-	FDS		
61.	003-006-	13	<	TMU-B STATUS WORD GATE	2
62.	003-006-	14	>	TMU-B STATUS DATA	P 2
63.	003-006-	15	>	TMU-B ACTIVE UNIT IND	
64.	003-006-	16	>	CDU-A SUBCARRIER LOCK	
65.	003-006-	17	>	CDU-A BIT SYNC LOCK	3
66.	003-006-	18	>	CDU-A OSC MONITOR	P 1
67.	003-006-	19	>	CDU-A SNR DATA	TEMP 2
68.	003-006-	20	>	CDU-A SNR ALERT PULSE	P 1
69.	003-006-	21	>	CDU-A SNR CLOCK	OR TEMP 2
70.	003-006-	22	>	CDU-B SUBCARRIER LOCK	
71.	003-006-	23	>	CDU-B BIT SYNC LOCK	
72.	003-006-	24	>	CDU-B OSC MONITOR	
73.	003-006-	25	>	CDU-B SNR DATA	V
74.	003-006-	26	>	CDU-B SNR CLOCK	V
75.	003-006-	27	>	CDU-B SNR ALERT PULSE	
76.	003-006-	28	>	CDU-B ACTIVE UNIT IND	
76.	004-006-	17	>	30VDC RTG 3 OUTPUT I	
	PWR	-	FDS		
77.	004-006-D07		>	30VDC BUS VOLTAGE	
78.	004-006-D08		>	2.4KHZ PWR TO CONV A	
79.	004-006-Q12		>	2.4KHZ PWR TO CONV B	
	100+		>	30VDC FDS MEMORY PWR	
	100+		>	30VDC 2.4KHZ DIV. INPUT I	
	100+		>	30VDC 2.4KHZ DIV. INPUT I	

TABLE 4. ELECTRICAL INTERFACE CIRCUITS
MJS77 (CONT)

ITEM	SUB	SUB	NO	FLOW	CIRCUIT NAME
	PWR	-			FDS
80.	004-006-	01	<	4.8KHZ REFERFNCE FREQ	
81.	004-006-	02	>	TLM RTG 1 CASE TFMP 2	
82.	004-006-	03	>	TLM RTG 1 CASE TFMP 3	
83.	004-006-	04	>	TLM RTG 2 CASE TFMP 1	
84.	004-006-	05	>	TLM RTG 2 CASE TEMP 3	
85.	004-006-	06	>	TLM RTG 3 CASE TEMP 1	
86.	004-006-	07	>	TLM RTG 3 CASE TFMP 2	
87.	004-006-	08	>	TLM SHUNT RADIATOR TFMP 1	
88.	004-006-	09	>	TLM SHUNT RADIATOR TEMP 2	
89.	004-006-	10	>	TLM BATTERY TEMP	
90.	004-006-	11	>	TLM SHUNT REG TEMP	
91.	004-006-	12	>	TLM RTG 1 OUTPUT V	
92.	004-006-	13	>	TLM RTG 2 OUTPUT V	
93.	004-006-	14	>	TLM RTG 3 OUTPUT V	
94.	004-006-	15	>	TLM RTG 1 OUTPUT I	
95.	004-006-	16	>	TLM RTG 2 OUTPUT I	
96.	004-006-	17	>	TLM RTG 3 OUTPUT I	
97.	004-006-	18	>	TLM DC BUS VOLTAGE	
98.	004-006-	19	>	TLM RDM VOLTAGE	
99.	004-006-	20	>	TLM SHUNT REGULATOR INPUT I	
100.	004-006-	21	>	TLM 2.4KHZ INV. INPUT I	

TABLE 4. ELECTRICAL INTERFACE CIRCUITS
MJS77 (CONT)

ITEM	SUB	SUB	NO FLOW	CIRCUIT NAME
	PWR	-		FDS
101.	004-006-	22	>	TLM 2.4KHZ INV. OUTPUT I
102.	004-006-	23	>	TLM 2.4KHZ INV. OUTPUT V
103.	004-006-	24	>	TLM DC BUS I
104.	004-006-	25	>	TLM 2.4KHZ INV STATUS
123.	006-007-	06	>	AACS ADDRESS DATA B;XR
	CCS	-		FDS
105.	005-006-	01	>	CC STROBE;XR
106.	005-006-	02	>	CC DATA;XR
107.	005-006-	03	>	CC ENABLE;XR
108.	005-006-	04	>	TLM CCS OUT 1
109.	005-006-	05	>	TLM CCS OUT 2
110.	005-006-	06	<	CCS BIT SYNC 1
111.	005-006-	07	<	CCS BIT SYNC 2
112.	005-006-	08	<	CCS ALERT 1
113.	005-006-	09	<	CCS ALERT 2
114.	005-006-	10	<	FDS SEQUENCE SYNC 1;XR
115.	005-006-	11	<	FDS SEQUENCE SYNC 2;XR
116.	005-006-	12	<	FDS LO RATE DATA;XR
117.	005-006-	13	<	FDS LO RATE BIT SYNC;XP
	FDS	-		AACS
118.	006-007-	01	>	AACS ADDRESS DATA A;XR

TABLE 4. ELECTRICAL INTERFACE CIRCUITS
MJS77 (CONT)

ITEM	SUB	SUB	NO FLOW	CIRCUIT NAME
	FDS	-	AACS	
119.	006-007-	02	>	AACS ADDRESS WORD GATE A;XR R PRES
120.	006-007-	03	>	AACS 14.4KHZ SHIFT CLOCK A;XR PRES
121.	006-007-	04	>	AACS DATA WORD GATE A;XR PAPER PRES
122.	006-007-	05	<	AACS DATA 1;XR ENG 2 CHAMBER PRES
123.	006-007-	06	>	AACS ADDRESS DATA B;XR
124.	006-007-	07	>	AACS ADDRESS WORD GATE B;XR
125.	006-007-	08	>	AACS 14.4KHZ SHIFT CLOCK B;XP
126.	006-007-	09	>	AACS DATA WORD GATE B;XR
127.	006-007-	10	<	AACS DATA 2;XR POSITION BR1
128.	006-007-	11	<	TLM CST 1 TEMP POSITION BR2
129.	006-007-	12	<	TLM CST 2 TEMP
130.	006-007-	13	<	TLM SUN SENSOR TEMP
131.	006-007-	14	<	TLM SCAN AZ TEMP
132.	006-007-	15	<	TLM A GYRO TEMP
133.	006-007-	16	<	TLM B GYRO TEMP
134.	006-007-	17	<	TLM C GYRO TEMP
135.	006-007-	18	>	MAM 14.4KHZ SHIFT CLOCK A
136.	006-007-	19	>	MAM DATA WORD GATE A
137.	006-007-	20	<	MAM DATA A LINE TEMP 2
138.	006-010-	07	<	TLM IPU +ROLL ENGINE 1 TEMP
139.	006-010-	08	<	TLM IPU +ROLL ENGINE 2 TEMP

TABLE 4. ELECTRICAL INTERFACE CIRCUITS
MJS77 (CONT)

ITEM	SUB	SUB	NO FLOW	CIRCUIT NAME
	FDS	-	PYRO	
138.	006-008-	01	< +P THRUST 1/+A ENG 1 CHAMBER PRES	
139.	006-008-	02	< -P THRUST 1/-A ENG 1 CHAMBER PRES	
140.	006-008-	03	< +Y THRUST 1/+B ENG 2 CHAMBER PRES	
141.	006-008-	04	< +R THRUST 1/-B ENG 2 CHAMBER PRES	
142.	006-008-	05	< TLM CAP BANK A VOLTS	TEMP 1
143.	006-008-	06	< TLM CAP BANK B VOLTS	TEMP 2
144.	006-008-	07	< TLM PYRO AMP IND A	TEMP 1
145.	006-008-	08	< TLM PYRO AMP IND B	TEMP 2
146.	006-008-	09	< TLM ISO VALVE POSITION BR1	
147.	006-008-	10	< TLM ISO VALVE POSITION BR2	
148.	006-010-	19	< TLM TCAPU +YAW THR 2 TEMP	
	FDS	-	CABL	
149.	006-010-	20	< TLM TCAPU -YAW THR 1 TEMP	
148.	006-009-	01	< S/C-LV SEPARATION INDICATION	
149.	006-009-	02	< PM-MM SEPARATION INDICATION	
150.	006-010-	23	PROP LIM TCAPU +ROLL THR 2 TEMP	
150.	006-010-	01	< TLM IPU SOLID MOTOR TEMP 1	
151.	006-010-	02	< TLM IPU SOLID MOTOR TEMP 2	PRESXP
152.	006-010-	05	< TLM IPU LINE TEMP 1	PRESSURE 1
153.	006-010-	06	< TLM IPU LINE TEMP 2	PRESSURE 2
154.	006-010-	07	< TLM IPU +ROLL ENGINE 1 TEMP	PRES
155.	006-010-	08	< TLM IPU +ROLL ENGINE 2 TEMP	PRES

TABLE 4. ELECTRICAL INTERFACE CIRCUITS
MJS77 (CONT)

ITEM	SUB	SUB	NO FLOW	CIRCUIT NAME
	FDS	-	PROP	
156.	006-010-	09	<	TLM IPU -ROLL ENGINE 1 TEMP
157.	006-010-	10	<	TLM IPU -ROLL ENGINE 2 TEMP
158.	006-010-	11	<	TLM TCAPU TANK TFMP 1
159.	006-010-	12	<	TLM TCAPU TANK TFMP 2
160.	006-010-	13	<	TLM TCAPU FEED SYSTEM TEMP 1
161.	006-010-	14	<	TLM TCAPU FEED SYSTEM TEMP 2
162.	006-010-	15	<	TLM TCAPU SURFACE TEMP 1
163.	006-010-	16	<	TLM TCAPU SURFACE TEMP 2
164.	006-010-	17	<	TLM TCAPU +PITCH THR 2 TEMP
165.	006-010-	18	<	TLM TCAPU -PITCH THR 2 TEMP
166.	006-010-	19	<	TLM TCAPU +YAW THR 2 TEMP
167.	006-010-	20	<	TLM TCAPU -YAW THR 1 TEMP
168.	006-010-	21	<	TLM TCAPU -YAW THR 2 TEMP
169.	006-010-	22	<	TLM TCAPU -ROLL THR 1 TEMP
170.	006-010-	23	<	TLM TCAPU +ROLL THR 2 TEMP
171.	006-010-	24	<	TLM TCAPU -ROLL THR 2 TEMP
172.	006-010-	25	<	TLM IPU SOLID MOTOR CHMBR PRES:XR
173.	006-010-	26	<	TLM TCAPU N2H4 PRESSURE 1
174.	006-010-	27	<	TLM TCAPU HE PRESSURE
175.	006-010-	28	<	TLM TCAPU +PITCH TCM THR CH PRES
176.	006-010-	29	<	TLM TCAPU -PITCH TCM THR CH PRES

TABLE 4. ELECTRICAL INTERFACE CIRCUITS
MJS77 (CONT)

ITEM	SUB	SUB	NO FLOW	CIRCUIT NAME
	FDS	-	PROP	
177.	006-010-	30	<	TLM TCAPU +YAW TCM THR CH PRES
178.	006-010-	31	<	TLM TCAPU -YAW TCM THR CH PRES
195.	006-016-	10	>	2.4192 MHZ REFERENCE
	FDS	-	TEMP	
196.	006-016-	11	<	TLM SCI PLUMF SHIELD TEMP 1
179.	006-011-	01	<	TLM SCI PLUME SHIELD TEMP 2
180.	006-011-	02	<	TLM DSS MOTOR V
198.	006-016-	13	<	TLM DSS TRANSPORT PRESSURE
199.	FDS-016-	14	<	DEV DSS TRANSPORT PRESSURE
181.	006-012-	02	<	TLM RTG BOOM DEPLOY STATUS
182.	006-012-	04	<	TLM SCI ROOM DEPLOY STATUS
183.	006-012-	05	<	TLM MAG BOOM DEPLOY STATUS
184.	006-012-	06	<	TLM MAG ROOM RELEASE STATUS
185.	006-012-	07	<	TLM SCIENCE LATCH PRESSURE
203.	006-017-	04	<	TLM DSS BODY TEMP
	FDS	-	DSS	
186.	006-016-	01	>	CC DATA 2
187.	006-016-	02	>	CC STROBE 2
188.	006-016-	03	>	RECORD DATA
189.	006-016-	04	>	DSS STATUS BIT SYNC
190.	006-016-	05	>	DSS MODE STATUS ALERT
191.	006-016-	06	>	DSS PLAYBACK STATUS ALERT
192.	006-016-	07	>	RECORD BIT SYNC
210.	006-021-	07	>	CRC PHA DATA WG R

TABLE 4. ELECTRICAL INTERFACE CIRCUITS
MJS77 (CONT)

ITEM	SUB	SUB	NO FLOW	CIRCUIT NAME
	FDS	-		DSS
193.	006-016-	08	>	PLAYBACK BIT SYNC A
194.	006-016-	09	>	CC ENABLE 2
195.	006-016-	10	>	2.4192 MHZ REFERENCE
196.	006-016-	11	<	PLAYBACK DATA
197.	006-016-	12	<	TLM DSS STATUS RESET
198.	006-016-	13	<	TLM DSS MOTOR V STEP
199.	006-016-	14	<	TLM DSS TRANSPORT PRESSURE
200.	006-021-	16		CRS REDUNDANCY SELECT
	FDS	-		SXA
200.	006-017-	01	<	TLM HGA MAIN REFLECTOR TEMP
201.	006-017-	02	<	TLM HGA S-BAND FEED TEMP
202.	006-017-	03	<	TLM X-BAND FEED HORN TEMP
203.	006-017-	04	<	TLM LGA BODY TEMP
204.	006-021-	01	>	CRS 14.4KHZ SHIFT CLOCK A
205.	006-021-	02	>	CRS 14.4KHZ SHIFT CLOCK B
206.	006-021-	03	>	CRS CMD WG
207.	006-021-	04	>	CRS CMD WORD
208.	006-021-	05	>	CRS HV ON
209.	006-021-	06	>	CRS PHA DATA WG A
210.	006-021-	07	>	CRS PHA DATA WG B

TABLE 4. ELECTRICAL INTERFACE CIRCUITS
MJS77 (CONT)

ITEM	SUB	SUB	NO FLOW	CIRCUIT NAME
	FDS	-		CRS
211.	006-021-	08	>	CRS RATE DATA WG A
212.	006-021-	09	>	CRS RATE DATA WG B
213.	006-021-	10	>	CRS DIG STATUS WG
214.	006-021-	11	>	CRS SYNC DATA
215.	006-021-	12	>	CRS ANALOG MUX RESET
216.	006-021-	13	>	CRS ANALOG MUX STEP
217.	006-021-	14	>	CRS CALIB START TEMP
218.	006-021-	15	>	CRS REDUNDANCY SELECT
219.	006-021-	16	<	CRS DIG DATA A
220.	006-021-	17	<	CRS DIG DATA B
221.	006-021-	18	<	CRS ANALOG DATA
222.	006-021-	19	<	CRS TELESCOPE TEMP
223.	006-021-	20	<	CRS ELECTRONICS TEMP
	006-023-	04	>	PWS INPUT RANGE CONTROL
	FDS	-	05	PRA
224.	006-022-	01	>	PRA ADC BIT SYNC
225.	006-022-	02	>	PRA ADC START
226.	006-022-	03	>	PRA STATUS WG
227.	006-022-	04	>	PRA 76.8KHZ CLOCK
228.	006-022-	05	>	PRA MUX STEP
229.	006-022-	06	>	PRA MIJX RESET

TABLE 4. ELECTRICAL INTERFACE CIRCUITS
MJS77 (CONT)

ITEM	SUB	SUB	NO FLOW	CIRCUIT NAME
	FDS	-		PRA
230.	006-022-	07	>	PRA CMD WG
231.	006-022-	08	>	PRA CMD WORD
232.	006-022-	09	>	PRA 14.4KHZ SHIFT CLOCK
233.	006-022-	10	<	PRA ADC DATA
234.	006-022-	11	<	PRA DIG STATUS DATA
235.	006-022-	12	<	PRA ANALOG MUX DATA
236.	006-022-	13	<	PRA ELECTRONIC TFMP
237.	006-022-	14	<	PRA B ANT DEPLOY
238.	006-022-	15	<	PRA A ANT DEPLOY
	FDS	-		PWS
239.	006-023-	01	>	PWS FREQ STEP
240.	006-023-	02	>	PWS CLOCK RESFT
241.	006-023-	04	>	PWS INPUT RANGE CONTROL
242.	006-023-	05	<	PWS INPUT RANGE STATE
243.	006-023-	07	<	PWS TEMP
244.	006-023-	08	<	PWS ANALOG OUTPUT A
245.	006-023-	09	<	PWS ANALOG OUTPUT B
246.	006-023-	10	<	PWS PWR SUPPLY VOLTAGE
247.	006-023-	11	<	PWS WAVEFORM DATA
248.	006-023-	12	>	PWS ADC BIT SYNC

TABLE 4. ELECTRICAL INTERFACE CIRCUITS
MJS77 (CONT)

ITEM	SUB	SUB	NO FLOW	CIRCUIT NAME
	FDS	-	PWS	
249.	006-023-	13	>	PWS ADC START
250.	006-023-	14	>	PWS WAVEFORM PWR
270.	006-025-	20	<	LECP LEMPA TEL TEMP
	FDS	-	LECP	
251.	006-025-	01	>	LECP 14.4KHZ SHIFT CLOCK A
252.	006-025-	02	>	LECP 14.4KHZ SHIFT CLOCK B
253.	006-025-	03	>	LECP CMD WORD A
254.	006-025-	04	>	LECP CMD WORD B
255.	006-025-	05	>	LECP CMD WG A
256.	006-025-	06	>	LECP CMD WG B
257.	006-025-	07	>	LECP PHA WG A
258.	006-025-	08	>	LECP PHA WG B
259.	006-025-	09	>	LECP REDUNDANCY SELECT
260.	006-025-	10	>	LECP RATE CMD WG
261.	006-025-	11	>	LECP RATE/STATUS WG A
262.	006-025-	12	>	LECP RATE/STATUS WG B
263.	006-025-	13	>	LECP MOTOR STEP
264.	006-025-	14	>	LECP MUX STEP
265.	006-025-	15	>	LECP MUX RESET
266.	006-025-	16	>	LECP ADC CLOCK
267.	006-025-	17	<	LECP DATA A

TABLE 4. ELECTRICAL INTERFACE CIRCUITS
MJS77 (CONT)

ITEM	SUB SUB NO	FLOW	CIRCUIT NAME
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FDS - LECP

- 268. 006-025- 18 < LECP DATA B
- 269. 006-025- 19 < LECP ANALOG ENGR DATA
- 270. 006-025- 20 < LECP LEMPA TEL TFMP
- 271. 006-025- 21 < LECP LEPT TEL TEMP
- 272. 006-025- 22 < LECP ANALOG CAL DATA

FDS - PPS

- 273. 006-027- 01 > PPS 14.4 KHZ SHIFT CLOCK
- 274. 006-027- 02 > PPS COMMAND WORD GATE
- 275. 006-027- 03 > PPS COMMAND WORD
- 276. 006-027- 04 > PPS DATA/COUNT CONTROL
- 277. 006-027- 06 < PPS DIGITAL SCIENCE DATA
- 278. 006-027- 07 < PPS LVPS MON
- 279. 006-027- 08 < PPS HVPS MON
- 280. 006-027- 09 < PPS SOLAR SENSOR
- 281. 006-027- 10 < PPS FILTER POSITION
- 282. 006-027- 11 < PPS ANALYZER POSITION
- 283. 006-027- 12 < PPS APERTURE POSITION
- 284. 006-027- 13 < PPS OPTICS TEMP
- 285. 006-027- 14 < PPS ELECTRONICS TEMP XDUCER

TABLE 4. ELECTRICAL INTERFACE CIRCUITS
MJS77 (CONT)

ITEM	SUB	SUB	NO FLOW	CIRCUIT NAME
	FDS	-		PLS
286.	006-032-	01	>	PLS 14.4KHZ SHIFT CLOCK
287.	006-032-	02	>	PLS MUX RESET
288.	006-032-	03	>	PLS SAMPLE CLOCK
289.	006-032-	04	>	PLS DATA WG
290.	006-032-	05	>	PLS CMD WG
291.	006-032-	06	>	PLS CMD WORD
292.	006-032-	07	>	PLS MUX STEP
293.	006-032-	08	>	PLS ADC CLOCK
294.	006-032-	09	<	PLS DIG DATA
295.	006-032-	10	<	PLS ANALOG MUX OUT
296.	006-032-	11	<	PLS SENSOR TEMP
297.	006-032-	12	<	PLS ELECTRONICS TEMP
298.	006-032-	13	<	PLS MODULATOR TEMP
317.	FDS	-	>	UVS
299.	006-034-	01	>	UVS 14.4KHZ SHIFT CLOCK
300.	006-034-	02	>	UVS REGISTER LOAD GATE
301.	006-034-	03	>	UVS WORD ADDRESS RESFT
302.	006-034-	04	>	UVS MODE CONTROL
303.	006-034-	05	>	UVS HV CONTROL 1
304.	006-034-	06	>	UVS HV CONTROL 2

TABLE 4. ELECTRICAL INTERFACE CIRCUITS
MJS77 (CONT)

ITEM	SUB	SUB	NO FLOW	CIRCUIT NAME
	FDS	-		UVS
305.	006-034-	07	>	UVS HV CONTROL 3
306.	006-034-	08	<	UVS HV MONITOR
307.	006-034-	09	<	UVS SCIENCE DATA 1
308.	006-034-	10	<	UVS SCIENCE DATA 2
309.	006-034-	11	<	UVS TEMP
	FDS	-		MAG
310.	006-035-	01	>	MAG 14.4KHZ SHIFT CLOCK A
311.	006-035-	02	>	MAG 14.4KHZ SHIFT CLOCK B
312.	006-035-	03	>	MAG CMD WG A
313.	006-035-	04	>	MAG CMD WG B
314.	006-035-	05	>	MAG CMD WORD A
315.	006-035-	06	>	MAG CMD WORD B
316.	006-035-	07	>	MAG SAMPLE A
317.	006-035-	08	>	MAG SAMPLE B
318.	006-035-	09	>	MAG RESET A
319.	006-035-	10	>	MAG RESET B
320.	006-035-	11	>	MAG STATUS WG A
321.	006-035-	12	>	MAG STATUS WG B
322.	006-035-	13	>	MAG SCI DATA WG A
323.	006-035-	14	>	MAG SCI DATA WG B

TABLE 4. ELECTRICAL INTERFACE CIRCUITS
MJS77 (CONT)

ITEM	SUB	SUB	NO FLOW	CIRCUIT NAME
	FDS	-		MAG
324.	006-035-	15	>	MAG IBHFM CLOCK(50.400KHZ)
325.	006-035-	16	>	MAG ORHFM CLOCK(53.760KHZ)
326.	006-035-	17	>	MAG IBLFM CLOCK A(60.480KHZ)
327.	006-035-	18	>	MAG IRLFM CLOCK B(60.480KHZ)
328.	006-035-	19	>	MAG OBLFM CLOCK A(64.512KHZ)
329.	006-035-	20	>	MAG OBLFM CLOCK B(64.512KHZ)
330.	006-035-	22	>	MAG MUX STEP
331.	006-035-	23	>	MAG MUIX RESET
332.	006-035-	24	<	MAG DIG DATA A
333.	006-035-	25	<	MAG DIG DATA B
334.	006-035-	26	<	MAG ANALOG MUIX OUT
335.	006-035-	27	<	MAG IBHFM SENSOR TEMP
336.	006-035-	28	<	MAG ORHFM SENSOR TEMP
337.	006-035-	29	<	MAG IRLFM SENSOR TEMP
338.	006-035-	30	<	MAG OBLFM SENSOR TEMP
	FDS	-		ISS
339.	006-036-	01	>	ISS-NA FRAME GATE
340.	006-036-	02	>	ISS-NA LIGHT FLOOD CONTROL
341.	006-036-	03	>	ISS-NA FRAME ERASE GATE
342.	006-036-	04	>	ISS-NA LINE CONTROL GATE

TABLE 4. ELECTRICAL INTERFACE CIRCUITS
MJS77 (CONT)

ITEM	SUB	SUB	NO FLOW	CIRCUIT NAME
	FDS	-		ISS
343.	006-036-	05	>	ISS-NA G1 V/GAIN CMD WORD
344.	006-036-	06	>	ISS-NA G1 V/GAIN CMD WORD GATE
345.	006-036-	07	>	ISS-NA SHUTTER RFSET
346.	006-036-	08	>	ISS-NA SHUTTER CLOSE IX RESET
347.	006-036-	09	>	ISS-NA SHUTTER OPEN CLOCK
348.	006-036-	10	>	ISS-NA FILTER STEP
349.	006-036-	11	>	ISS-NA FILTER READ/MUX RESET
350.	006-036-	12	>	ISS-NA 14.4KHZ SHIFT CLOCK
351.	006-036-	13	>	ISS-NA MUX STEP
352.	006-036-	14	>	ISS-NA BEAM ON
353.	006-036-	15	>	ISS-NA ELECTRONICS CALIBRATE
354.	006-036-	16	>	ISS-NA OPTICS CALIBRATE
355.	006-036-	17	>	ISS-WA BEAM ON ITION
356.	006-036-	18	>	ISS-WA ELECTRONICS CALIBRATE
357.	006-036-	19	>	ISS-WA FRAME GATE ES TEMP
358.	006-036-	20	>	ISS-WA LIGHT FLOOD CONTROL
359.	006-036-	21	>	ISS-WA FRAME FRASE GATE
360.	006-036-	22	>	ISS-WA LINE CONTROL GATE
361.	006-036-	23	>	ISS-WA G1 V/GAIN CMD WORD
362.	006-036-	24	>	ISS-WA G1 V/GAIN CMD WORD GATE
363.	006-036-	25	>	ISS-WA SHUTTER RFSET FR

TABLE 4. ELECTRICAL INTERFACE CIRCUITS
MJS77 (CONT)

ITEM	SUB	SUB	NO FLOW	CIRCUIT NAME
	FDS	-		ISS
364.	006-036-	26	>	ISS-WA SHUTTER CLOSE
365.	006-036-	27	>	ISS-WA SHUTTER OPEN
366.	006-036-	28	>	ISS-WA FILTER STEP
367.	006-036-	29	>	ISS-WA FILTER READ/MUX RESET
368.	006-036-	30	>	ISS-WA 14.4KHZ SHIFT CLOCK
369.	006-036-	31	>	ISS-WA MUX STEP
370.	006-036-	32	>	ISS-NA ADC BIT SYNC
371.	006-036-	33	>	ISS-WA ADC BIT SYNC
372.	006-036-	34	>	ISS-NA ADC START
373.	006-036-	35	>	ISS-WA ADC START
374.	006-036-	36	<	ISS-NA ADC VIDEO DATA
375.	006-036-	37	<	ISS-WA ADC VIDEO DATA
376.	006-036-	38	<	ISS-NA FILTER POSITION
377.	006-036-	39	<	ISS-WA FILTER POSITION
378.	006-036-	40	<	ISS-NA REAR OPTICS TEMP
379.	006-036-	41	<	ISS-WA OPTICS TEMP
380.	006-036-	42	<	ISS-NA FRONT OPTICS TFMP
381.	006-036-	43	<	ISS-NA VIDICON TFMP
382.	006-036-	44	<	ISS-WA VIDICON TFMP
383.	006-036-	45	<	ISS-NA POWER SUPPLY TFMP
384.	006-036-	46	<	ISS-WA POWER SUPPLY TEMP

TABLE 4. ELECTRICAL INTERFACE CIRCUITS
MJS77 (CONT)

ITEM	SUB	SUB	NO FLOW	CIRCUIT NAME
	FDS	-		ISS
385.	006-036-	47	<	ISS-NA ANALOG ENGR TLM ^{NALOG}
386.	006-036-	48	<	ISS-WA ANALOG ENGR TLM ^{NALOG}
387.	006-039-	16	<	MIRIS STANDBY SUPPLY STATUS
	FDS	-		MIRIS
	403.	006-039-	17	MIRIS C40 WORD GATE
	404.	006-039-	18	MIRIS C40 WORD GATE
	405.	006-039-	19	MIRIS PWR FROM LCE
	406.	006-039-	20	MIRIS DATA FROM LCE
	407.	006-039-	21	MIRIS SIGNAL
387.	006-039-	01	>	MIRIS 14.4KHZ SHIFT CLOCK
388.	006-039-	02	>	MIRIS FRAME START
389.	006-039-	03	>	FDS 480HZ NEON RFF FRQ
390.	006-039-	04	<	MIRIS SCIENCE DATA
391.	006-039-	05	>	MIRIS PLL CARRIER
392.	006-039-	06	<	MIRIS RAD SURFACE TEMP
393.	006-039-	07	<	MIRIS PRI MIRROR TEMP
394.	006-039-	08	<	MIRIS SEC MIRROR TEMP
395.	006-039-	09	<	MIRIS ELECTRONICS TEMP
396.	006-039-	10	<	MIRIS RADIOMETER HIGH GAIN ANALOG
397.	006-039-	11	<	MIRIS RADIOMETER ANALOG
398.	006-039-	12	<	MIRIS NEON ANALOG
399.	006-039-	13	<	MIRIS RAD SURFACE HTR ANALOG

b) TABLE 4. ELECTRICAL INTERFACE CIRCUITS
MJS77 (CONT)

ITEM	SUB	SUB	NO FLOW	CIRCUIT NAME
				FDS - MIRIS
400.	006-039-	14	<	MIRIS PRI MIRROR HTR ANALOG
401.	006-039-	15	<	MIRIS SEC MIRROR HTR ANALOG
402.	006-039-	16	<	MIRIS STANDBY SUPPLY STATUS
403.	006-039-	17	>	MIRIS CMD WORD GATE
404.	006-039-	18	>	MIRIS CMD WORD
				FDS - LCE
405.	006-206-F01		<	+10VDC PWR FROM LCE
406.	006-206-F02		<	+5VDC PWR FROM LCE
407.	006-206-F03		<	-3VDC PWR FROM LCE
408.	006-206-F04		<	CC DATA FROM LCE
409.	006-206-F05		<	CC ENABLE FROM LCE
410.	006-206-F06		<	CC STROBE FROM LCE
411.	006-206-F07		>	2.4KHZ CC SYNC SIGNAL
				FDS - LVS
412.	006-LVS-		>	MJS ENGINEERING DATA

- b) Standard temperature range (-78° to +100°C) measurements:
±3 percent of full scale, ±1/2 DN quantization error.
- c) Nonstandard temperature ranges: ±5 percent of full scale,
±1/2 DN quantization error.

6.2 4.8 kHz Detector

The detector shall inhibit the signal to PWR if the frequency is not 4800 Hz, ±6 percent (± 288 Hz).

6.3 Power on Reset

The FDS shall be in the power reset condition during power up when the AC voltage is below 43.5 V (nominal). During power down, FDS shall undergo a power reset at 42.0 V (nominal).

6.4 Master Oscillator Accuracy

The FDS master oscillators shall operate at 4.8384 MHz ±20 ppm over the TA temperature range for the life of the mission.

7.0 PHYSICAL CHARACTERISTICS AND CONSTRAINTS

7.1 Mass

The mass of the FDS shall be as specified in MJS77-3-230, Equipment List and Mass Allocations, and is given here for reference only: 16.3 kg.

7.2 Power

The maximum power consumed by the FDS shall be as specified in MJS77-3-250, Power Profile and Allocation, and is given here for reference only: 14.0 W.

7.3 Volume

The volume of the FDS shall be as specified in Interface Control Drawing 10062408.

7.4 Environmental

The FDS shall be designed to operate within specification over the type approval (TA) temperature range which is -20°C to +75°C. In addition, the subsystem shall be compatible with the requirements of MJS77-3-240, Environmental Design Requirements, and MJS77-3-210, Design Criteria for Spacecraft Temperature Control.

REVISION LOG

7.5

Packaging

The FDS shall be packaged utilizing planar multilayer laminate packaging technology in accordance with the applicable sections of MJS77-3-220, Electronic Equipment Design.

7.6

Location

The FDS shall be located within the spacecraft in the location specified in MJS77-3-180.

7.7

Identification and Marking

The FDS shall be identified and marked as required in Equipment Identification and Marking, Section VII of 618-232, Configuration Management Plan.

8.0

SAFETY CONSIDERATIONS

The MJS77 FDS shall constitute no unusual safety hazard nor require any special handling other than normal for spacecraft electronic equipment.

O. H. Holler

REVISION LOG

Revision	Date	ECRs Incorporated	Comments
Original	7 July 1975		P. L. 76
A	20 March 1978	36059, 36069, 36077, 36107, 36146, 36172, 36201, 36212, 36353, 36597, 36917	Changes affected by ECRs listed
		JET PROPULSION LABORATORY Functional Requirements Mariner Jupiter/Saturn 1977 Flight Equipment Flight Data Subsystem Hardware	Rev. No. MJS77-4-2006-1A 20 March 1978 Superseded 7 July 1975
1.0	SCOPE	The functional requirements for the Mariner Jupiter/Saturn 1977 flight data subsystem (FDS) are met by FDS hardware and FDS software. This document establishes the general FDS functional requirements and those associated with the FDS hardware. The functional requirements for FDS software are established in MJS77-4-2006-2, Flight Data Subsystem Software.	
2.0	APPLICABLE DOCUMENTS	The following documents form a part of this Functional Requirements Document. NOTE MJS77-3-100, Spacecraft Requirements and Constraints, applies to this document. Requirements of other MJS77 level three documents may also be applicable. It is the responsibility of the user to become familiar himself with the organization and pertinent content of the level three documents, as well as with the material contained herein.	