

Questdata

Volume 2 Issue #12

©

RELOCATOR

by
Enos Jones

It is a near certainty that many Elf owners have found themselves in the position where it is necessary to add some additional code inside an existing machine language program either because during development an omission occurred or just to bring about improvements in an existing program. At that point two options generally exist:

1. Replace two or more bytes with a jump or branch to the new routine which is somewhere else in memory, then restore the last bytes at the end of the new routine and jump back at a point past the patch. This is not always acceptable.
2. Manually relocate the existing code to make space for the new routine. This involves rewriting the program out on paper and adjusting the branch instructions, and then reentering it. Again it is far from optimal.

The solution to this dilemma was to write a machine language program which performs the second type of relocation quickly and painlessly. It requires 11 bytes of information as follows:

- A. Function select 00 – fix references only
 - 01 – move block and fix references
 - 02 – move block only
- B. Starting address of (2 bytes A1–Hi address code to be relocated A2–Lo address).
- C. Ending address of (2 bytes B1–Hi address code to be relocated B2–Lo address).

D. Destination address (2 bytes D1–Hi address for code to be relocated to D2–Lo address).

E. First address to (2 bytes F1–Hi address have references fixed F2–Lo address).

F. Last address to have (2 bytes F3–Hi address references fixed F4–Lo address).

The relocator uses the technique of immediate data display to prompt for each of the various parameters it needs. That is, the output display of the Super Elf will display 'FC' when a function code is required at which time the appropriate keys are pressed followed by '1'. Elf will accept it and delay before prompting for the next parameter.

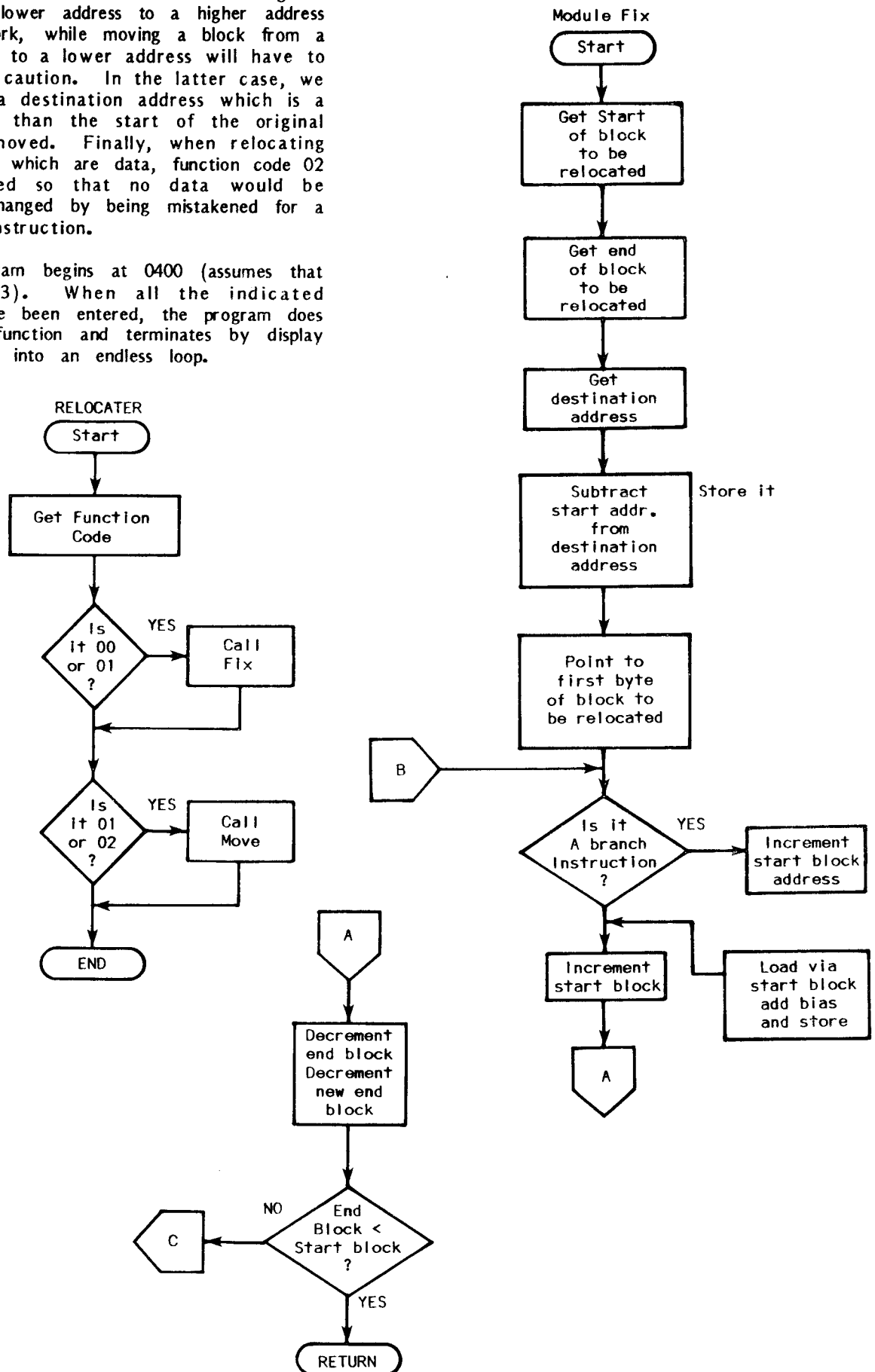
The relocator performs a block move if function code 00 is entered. The relocator both moves the block and fixes branch references if code 01 is selected. If 02 is selected, only the branch references are fixed (i.e. no block move).

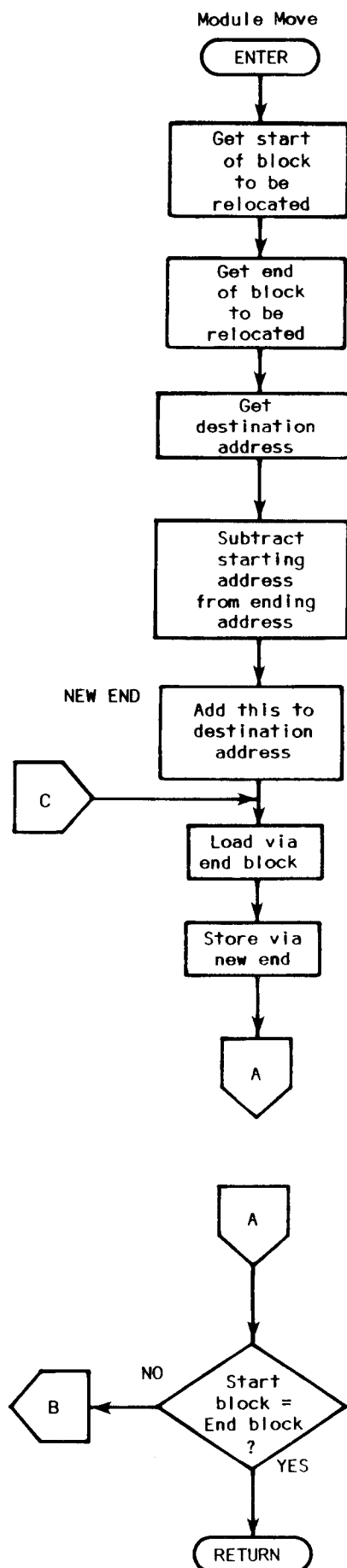
The relocator fixes references by first calculating the offset to add to the branch reference by computing offset equals (b–d). Then, it searches through the specified fix reference range (e through f) for branch instructions and when one is found it adds the offset to the next byte and replaces that byte.

It must be noted that the relocator does not adjust load immediate (F8) instructions so register set-ups using the technique must be manually changed. Additionally, the relocator performs a block move by moving a block end first.

Thus block moves which result in moving the block from a lower address to a higher address will always work, while moving a block from a higher address to a lower address will have to be done with caution. In the latter case, we must specify a destination address which is a lower address than the start of the original block to be moved. Finally, when relocating blocks of code which are data, function code 02 should be used so that no data would be inadvertently changed by being mistaken for a branch type instruction.

The program begins at 0400 (assumes that the PC is R3). When all the indicated parameters have been entered, the program does the indicated function and terminates by display 'AA' and going into an endless loop.





REGISTER USAGE:

R2 - Stack
 R3 - PC
 R4 - First address of block to be relocated
 R5 - Last address of block to be relocated
 R6 - Destination Addr.
 R7 - First address to have references fixed
 R8 - Last addr. to have references fixed.
 R9 - Function Code.
 RA - 2 byte code table
 RB - 3 byte code table
 RC - CALL FIX
 RD - CALL MOVE
 RE - INPUT ROUTINE

ADDR	CODE	LABEL	OPCODE	OPERAND	COMMENT
0400	F8 04	START:			R2 - Stack
0402	B2				
0403	F8 F0 A2				*
0406	F8 05 BE				RE-Input routine
0409	F8 01 AE				*
040C	F8 05 BC				RC-Fix reference
040F	F8 14 AC				*
0412	F8 04 BD				RD-Move routine
0415	F8 5F AD				*
0418	E3 64 FC				Get Function code
041B	DE A9				*
041D	E3 64 A1				Get address of 1st
0420	DE B4				Block to be
0422	E3 64 A2				relocated. . .
0425	DE A4				
0427	E3 64 B1				Get last addr. of
042A	DE B5				block to be
042C	E3 64 B2				relocated.
042F	DE A5				*
0431	E3 64 D1				Get destination
0434	DE B6				address
0436	E3 69 D2				*
0439	DE A6				*
043B	E3 64 F1				Get first address
043E	DE B7				to have ref.
0440	E3 64 F2				fixed and last
0443	DE A7				
0445	E3 64 F3				
0448	DE B8				
044A	E3 64 F4				
044D	DE A8				
044F	89				Get function code
0450	FF 02				
0452	33 5B		BGE	CONT	
0454	F8 05 BA				CALL FIX
0457	F8 D0 AA				
045A	DC				
095B	89		GLO	R9	Get function code
045C	30 87		BR	FINISH	
045E	DE	RETURN:	SEP	R3	
045F	E2 85	MOVE:	SEX	R2	Get low end
					address
0461	52 84		STR	R2	Get low start
					address
0463	F5		SD		Subtract
0464	AF		PLO	RF	Store in RF.0
0465	95 52		GHI	R5 STR 2	
0467	94 75		GHI	R4 SUD B	Sub. high start
					from high GHI
0469	BF		PHI	RF	Store in RF.0
046A	86		GLO	R6	Get low destin-
					ation addr.
046B	52		STR 2		Store
046C	8F		GLO RF		
046D	F4		ADD		
046E	AF		PLO	RF	
046F	96		GHI	R6	Get high destin.

ADDR	CODE	LABEL	OPCODE	OPERAND	COMMENT	ADDR	CODE	LABEL	OPCODE	OPERAND	COMMENT
0470	52		STR	via R2		0544	21 1A	CHECK2:	DEC R1	INC RA	All table entries
0471	9F 74		GHI	RF ADC		0546	81		GLO	R1	Checked?
0473	BF		PHI	RF		0547	3A 25		BNZ	ANOTHER	No branch
0474	26		DEC	R6		0549	F8 0A A1 2 BYTE		LDI	0A PLO R1	Load number no
0475	05	ANOTHER	LD5		Load via end addr.			(NON)			effect 2 byte
0476	5F	STORE	RF		Store via mod.						codes
					"TO" address	054C	EA	AGAIN:	SEX	RA	RA is index
0477	25 2F		DEC R5	DEC RF	Dec. to address	054D	07		LD7		Load from block
0479	96 52		GHI R6	STR 2		054E	F3		XOR		Check if 2 byte
047B	9F F5		GHI RF	SUB							number
047D	3A 75		BNZ	ANOTHER		054F	3A 67		BNZ	CHECK3	No go check other
047F	86 52		GLO R6	STR 2							codes
0481	8F F5		GLO RF	SUB		0551	17		INC	R7	Yes, just
0483	3A 75		BNZ	ANOTHER							increment
0485	30 5E		BR	RETURN		0552	E2 98		SEX R2	GHI R8	At end of
0487	32 8A	FINISH	BZ	SKIP		0554	52 97		STR R2	GHI R7	reference fixing?
0489	DD		CALL	MOVE		0556	F5		XOR		*
048A	F3		SEX	R3	Display end of	0557	33 61		BNZ	N FIN.	
048B	64 AA		OUT4		program	0559	88 52		GLO RS	STR R2	
048D	30 8D	LOOPA:	BR	LOOPA	'AA'	055B	87 F5		GLO R7	XOR	
0500	D3	RETURN:	SEP	R3		055D	33 61		BNZ	N FIN	
0501	3F 01	INPUT:	BN4		Wait for	055F	30 13		BR	END FIX	*Yes return from
0503	37 03		B4		*Input						routine
0505	32 6C 64		SEX R2	INP4 OUT4	Display input	0561	17		INC	R7	Inc. block pointer
0508	22		DEC	R2	*	0562	F8 D0 AA		LDI	XX PLO RA	Reset table
0509	F8 FF B1		LDI FF	PHI R1	Delay before						pointer
0506	91 21		GHI R1	DEC R1	Returning	0565	30 22		BR	CYCLE	Go process
050E	3A 0C		BNZ		*						(through table)
0510	02		LD2		Put input in D	0567	21 1A	CHECK3:	DEC R1	INC RA	All table entries
					register	0569	81		GLO	R1	checked?
0511	30 00		BR	RETURN	Return	056A	3A 4C		BNZ	AGAIN	No! Branch
0513	D3	RETURN	SEP	R3		056C	F8 07 A1 3 BYTE		LDI	07 PLO R1	Yes, check 3 byte
0514	86 52	FIX:	GLO R6	STR 2	Get destination			(ACT)			
					low address	056F	EA	MANY	SEX	RA	Opcode tables
0516	87		GLO	R7	Get fix start(low)	0570	07		LD7		Load from clock
0517	F5 AF		SD	PLO RF	Subtract and store	0571	F3		XOR		Check if 3 byte
					in F.0						opcode
0519	96 52		GHI R6	STR R2	Get destination	0572	3A 81		BNZ	CHECK4	No! Branch
					address (high)	0574	E7 17 17		INC R7	INC 17	Yes! Point to low
051B	97 75		GHI R7	SDB	Get fix start						address
					(high)	0577	8F F4 73		GLO RF	ADD	Add bias to it
051D	BF		PHI	RF	Subtract and store	057A	9F 74 57		GHI RF	ADC ST7	Add bias to high
					in F.1						and change it
051E	87 73		GLO R7	STX D	Push fix start on	057D	17 C4		SEX	R2	
0520	97 73		GHI R7	STX D	Stack	057F	30 2F		BR	BLOCKEND	
0522	F8 0F A1	CYCLE:	LDI 0F	PLO R1	Load number	0581	21 1A 81	CHECK4:	DEC R1	IN	
					affected 2 byte	0584	3A 6F		BNZ	MANY	
					ops	0586	17		INC	R7	
0525	FA	ANOTHER:	SEX	RA	RX is now A	0587	F8 D0 AA		INC	R7	Reset table
0526	07		LD7		Load from block	058A	30 22		BR	CYCLE	
0527	F3		XOR		Check if 2 byte						
					(Aff.) code						
0528	3A 44		BNZ	CHECK2	No, go check other						
					tables						
052A	E7 17		SEX R7	INC R7	Yes! Point to						
					branch value						
052C	8F		GLO	RF	Get bias value						
052D	F4 57		ADD	STR7	Add to value,						
					change value						
052F	E2	BLOCK END:	SEX	R2	R2-Index						
0530	98 52		GHI R8	STR R2	All block bytes						
0532	97 F5		GHI R7	SUB	Looked at?						
0534	33 3E		BNZ	MORE	*						
0536	88 52		GLO R8	STR 2	*						
0538	87 F5		GLO R7	XOR							
053A	33 3E		BNZ	MORE							
053C	30 13		BR	ENDFX	Yes, return from						
					routine						
053E	17	MORE:	INC	R7	Increment block						
					pointer						
053F	F8 D0 AA		LDI	PLO RA	Restore table						
					pointer						
0542	30 22		BR	CYCLE	Go process another						

Q*BUG

Welcome to the QUEST BASIC USERS GROUP.
(Here after known as QBUG)

Hopefully, this will be a regular feature of QUEST DATA devoted to users of the QUEST SUPER BASIC VERSION 5.0 program. Emphasis will be on machine language enhancements to SUPER BASIC. My aim will be to pass along any improvements that you, the readers of this column, contribute and a few of my own. Since this is a USERS group column, it is your input that will support future columns. Please send in any ideas, suggestions, questions, or what have you, so that we can keep the column rolling.

I am a self-taught machine language tinkerer and am not a real hotshot programmer. However, with a little patience and some hard disassembling of SUPER BASIC, I feel anyone can learn the fundamental workings of SUPER BASIC and come up with some useful gimmicks even if they only satisfy some personal whim.

First thing, let me explain the format in which I will write numbers in this and any future columns.

By now, hopefully, you know that the internal workings of the 1802 microprocessor are expressed in hexadecimal format numbers (hex). This means that any reference to register contents, memory contents, addresses, etc. should and will henceforth be in hex form. If I write "Page 3500" or "Address 2345", these will always be hex numbers. I will not show an "M" prefix for an address or an "H" suffix for a number.

Of course, any number within a Basic program, unless preceded by a # or a @, will be in decimal format.

Also, SUPER BASIC VER. 5.0 will henceforth be called simply "Super" which it surely is!

Because my setup consists of an ELF II with the Netronics Video Board and terminal, some of my changes to SUPER are made to satisfy the limitations imposed by the quirks in the ELF II equipment. I do not do much original programming in BASIC and usually concentrate on converting published programs for TRS or other computers to a format usable in SUPER or machine language programming.

Now, let me present a method for providing a little quicker start up for SUPER.

SUPER 5.0, as presently configured and written, requires that the user respond with a C/R or 'M' when first bringing up SUPER. This is to allow SUPER to measure the terminal time constants and 'stuff' them into work page 0000 at locations 00E7 and 00E8. This routine is included so that SUPER will be somewhat hardware independent and can be used on any terminal.

Once the user has run SUPER on his terminal, these constants are available for reuse and the initial C/R or 'M' response can be eliminated. Also, the initialization routine occupies memory location 3493 to 34CC and this program space can be used for other routines.

The key to eliminating the initialization routine is the inclusion of work page 0000 to 00FF in the taped master SUPER program. This will insure that the work page and the time constants and other data recorded on the work page will be loaded into memory when SUPER is loaded. Thus, SUPER, when first re-recorded to your backup tapes, should be recorded from memory location 0000 to the end of your particular version of SUPER. This will include the time constant location 00E7 and 00E8 and allow us to completely eliminate the initialization routine at 3493.

SUPER vectors to the Serial I/O initialization routine with a long branch at location 3300 to location 3400. The final long branch to the initialization routine is C0 34 93 at location 3400. For ELFII users, this should be changed to C0 31 48 (the actual CLS routine) to clear the screen and return to the C/W prompt. I presume that non ELFII owners can merely change location 3400 to a D5 instruction but cannot guarantee the results.

Finally, for this column, we should discuss procedures for providing cassette tape deck control on an ELF II using the Netronics motor control board.

Although the manual for SUPER 5.0 states that cassette tape deck control can only be accomplished with a hardware change, I find that a simple software change in SUPER will provide motor control without any hardware changes. Page 3200 of SUPER contains most of the cassette in/out routines. Simply stated, although not exactly step by step, non-ELF II deck control uses the byte 00 to turn off the input and output decks, byte 01 to turn on the input deck,

and byte 02 to turn on the output deck. The ELF II uses byte 00 to turn on both decks, byte 01 to turn on the output deck, and byte 02 to turn on the input deck. Additionally, byte 03 will turn off both decks.

The first change to be made will insure that both decks are turned off when SUPER is first entered. Since we will be using and saving work page 0000 as part of the SUPER program, we can put a simple little routine at location 0000 to turn the decks off and then jump to the Cold Start routine at location 0100. This change is:

```
0000 - E0 67 03 (Output byte 03, turn off decks)
0003 - C0 01 00 (Jump to Cold Start)
```

The next change is to the byte at location 32A0. This is the byte to turn off both decks after a Pload, Psave, Dload, or Dsave and is presently '00'. Change this byte to '03' and you now turn off the ELF II decks.

Next, we will change the bytes which turn on the input or output decks. This is presently controlled by a tricky routine at location 321E thru 3225.

Apparently, SUPER enters the cassette I/O routines with the DF register set to 1 if it is in the Dsave or Psave mode. DF is tested and if it is 1, execution jumps to location M 321EH. SUPER will then load D with 01 (F8 01 at 321E), add (7C) D, DF, and the 00 byte at 3221, and put the results in D and on the stack(52). D is then shifted to the right (F6) and DF is tested for 0.

If SUPER did come in with DF set to 1, adding the 01 in D and the 1 in DF and putting the result in D will make D=2. Shifting 02 (0000 0010 in binary) to the right would leave D=01 and force DF=0 (0000 0001(0 to DF)). The DF test at 3224 (3B) would be true and execution would branch to location 32B5. This is the cassette output routine and the byte 02 on the stack would eventually be sent to the output deck by the 63 instruction at location 32C1.

If SUPER entered the cassette I/O routines in the Pload or Dload mode, DF will be set to 0. The 01 at 321E would be added to DF (0) and the result put in D. Shifting 01 right would force DF=1 and the DF test at 3224 would fail and execution would continue at 3226. This is the cassette input routine and the 01 would be sent to the input deck by the 63 instruction at location 3226.

To make the changes necessary for the ELF II, we will simplify the routines somewhat. Since locations 3200 to 3205 are actually unused, we will use them for part of our changes. First, at location 321E, we will put a

short branch to location 3200 (33 00). This branch is conditional, based on the state of DF. If DF=1, the test is true and execution will branch to 3200. Thus, if SUPER enters in the Dsave or Psave mode, we will branch to 3200. At location 3200, we will load D with 01 (F8 01), put 01 on the stack (52) and unconditionally branch (30 B5) to location 32B5, where the 01 byte will be sent to the output deck and execution in the output mode will continue.

If SUPER entered in the input mode, the conditional branch at 320E will not take effect since DF will equal 0. We will then want to load D with 02 (F8 02) at location 3210, put 02 on the stack, and continue execution at 3226, the cassette input routine. The 02 in D will be sent to, and turn on, the input deck and execution in the input mode will continue.

Incidentally, ELF II owners, don't forget to change the 63 instructions at 3226, 32A2, and 32C1 to 67.

In summary, the cassette changes are:

```
0000  E0 67 03
0003  C0 01 00
3200  F8 01 52 30 B5 C4
321E  33 00
3220  F8 02 52 C4 C4 C4 67
32A0  03 52 67
32C1  67
```

EDITORS NOTE:

This will be a regular feature as we have 6 more ready to publish!

CONGRATULATIONS FRED

QUESTDATA
P.O. Box 4430
Santa Clara, CA 95054

Publisher.....Quest Electronics
Editor.....Paul Messinger
QBUG Editor.....Fred Hannan
Proof Reading.....Judy Pitkin
Production.....John Larimer

The contents of this publication are copyright and shall not be reproduced without permission of QUESTDATA. Permission is granted to quote short sections of articles when used in reviews of this publication. QUESTDATA welcomes contributions from its readers. Manuscripts will be returned only when accompanied by a self addressed stamped envelope. Articles or programs submitted will appear with the authors name unless the contributor wishes otherwise. Payment is at the rate of \$15 per published page. QUESTDATA exists for the purpose of exchanging information about the RCA 1802 microcomputer.

THE COSMAC KID

By Mark Wendell

It had been a great day. I had just finished killing off seventeen Klingons in the computer of a local college. When I got home, I checked the mail. Waiting for me was Popular Electronics and I read the article and was completely blown away, being relatively new to micros and the language, but my interest had been caught, the seed was planted. I read up as much as I could on micromputers in general, and I got out all of my back issues of Popular Electronics, Radio-Electronics, and Elementary Electronics, trying to find as much as I could about the elusive 1802.

Having just graduated from junior high, my finances were almost non-existent (have you ever seen a rich just-graduated junior high schooler?). So I had to start scrimping and saving, working my fingers to the bone, and weaseling as much as I could from my parents. And then came my birthday. Since I had been such a good kid all year (heh, heh), my dad decided to split the cost with me. I was almost there.

Now I had to figure out which kit to get. After price-comparing and writing some letters, I decided on Quest.

There was only one more obstacle to overcome: my mother, who hates machines with a passion. The following is a conversation between myself and the matriarch of the household on the day I finally had all the money raised.

"Yes, but what can it do? What is it good for?!"

"Well...er...it can count. And it can make sounds!" I gulped, the slow terror of rejection rising in my gut.

"It can count and make noise, and it costs over a hundred bucks!" Oh.

"Well, it also can...uh...make neat pictures on the TV!"

"I just don't know, it just doesn't sound like its worth it..."

And suddenly I had it, I'd stick her with education!

"Its also educational! It can teach me logic,

and Boolean algebra, and electronics, and number systems, and programming!" I had her by the... er...I sure had her now.

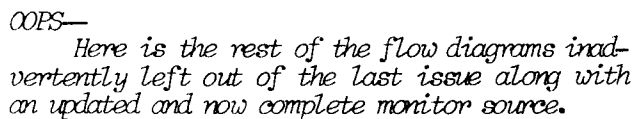
"Well, if you think its worth it, but...ah... what can it do?" You get the picture.

Three days later, weary and worn, but happy at my eventual victory, I sent out my order for a Super Elf kit.

A little less than a week later I got it via UPS and eagerly looked it over. After going through two rolls of solder, I viewed my creation and took the big step: I plugged it in. And...nothing happened. Completely crushed and at the point of suicide, I wrapped it up and sent it back the next day for repairs. Time munched onward.

A month later, my Elf came back home with a doctor's bill attached. I paid the bill and looked it over. Apparently, I had made a few construction errors (I'm only human), but it was better now. Again I plugged it in, only this time I saw the most glorious pair of red zeroes that I had ever seen in my whole life, and these were flanked by magnificent stars that shone brilliantly, expressing the 1802's mode and state of mind. Since I had read up on programming, I loaded my first program; 7B00! Boy! Another star blinked into life! Totally overjoyed, I ran the gamut of programs listed in Popular Electronics. When I came to the sound generators, I became ecstatic—it was the most incredibly fantastic thing in the whole world! But even that didn't last forever. My software was definitely sparse, so I began looking around. Suddenly, there was a glimmering light—a ray of hope befell my eyes as I received the first complimentary issue of QUESTDATA. This was where it was at! I readily subscribed, and am now happily feeding my Elf wondrous programs. The little Elf greedily accepts all programs with open RAM and churns out results perfectly. The COSMAC is a willing jinni and joyfully serves any lucky soul fortunate enough to own the microprocessor of microprocessors: the 1802.

PHILLIP LIESCHESKI



ADDRESS	INSTR	OPERAND	COMMENT
473A:	32A6	BZ	DUMP
473C:	FF01	SMI	#01
473E:	329E	BZ	EXEC
4740:	FF04	SMI	#04
4742:	328F	BZ	INSP
4744:	FF03	SMI	#03
4746:	3281	BZ	LOAD
4748:	FF01	SMI	#01
474A:	32C1	BZ	MODI
474C:	301E	BR	PROMP
474E:	E2	SCALL	* CALL SCRT ROUTINE
474F:	A6	SEX	R2
4750:	13	INC	R6
4751:	13	INC	R3
4752:	83	GLO	R3
4753:	73	STXD	R3
4754:	93	GMI	R3
4755:	73	STXD	R3
4756:	23	DEC	R3
4757:	03	LDN	R3
4758:	73	STXD	R3
4759:	23	DEC	R3
475A:	03	LDN	R3
475B:	73	STXD	R3
475C:	86	GLO	R6
475D:	D5	RETN	GO TO IT VIA SRE-M
475E:	304E	SCALL	
4760:	E2	SCRT ROUTINE	* RETURN SCRT ROUTINE
4761:	A6	SEX	R2
4762:	6C	IRX	R6
4763:	72	LDXA	R3
4764:	B3	PHI	R3
4765:	F0	LDX	R3
4766:	A3	PLO	R6
4767:	06	GLO	R3
4768:	D3	SEP	R3
4769:	3060	BR	SRETN
476A:	D4865	BRKP	* BREAKPOINT SET-UP ROUTINE
476B:	F847	CALL	IADR
476C:	B6	PHI	PAGE
476D:	BE	PHI	R6
476E:	F802	PAD	RE
476F:	A6	PLO	PAD
4770:	40	LDA	R0
4771:	20	DEC	R0
4772:	50	STR	R6
4773:	F8DE	LDI	R0
4774:	50	STR	R0
4775:	F8DA	LDI	BENT
4776:	AE	PLO	RE
4777:	C0470D	LBR	EBUG5
4778:	D4865	BRKP	* LOAD CODE ROUTINE
4779:	F847	CALL	IADR
4780:	B6	PHI	PAGE
4781:	BE	PHI	R6
4782:	F802	PAD	RE
4783:	A6	PLO	PAD
4784:	40	LDA	R0
4785:	20	DEC	R0
4786:	50	STR	R6
4787:	F8DE	LDI	R0
4788:	50	STR	R0
4789:	F8DA	LDI	BENT
4790:	AE	PLO	RE
4791:	C0470D	LBR	EBUG5
4792:	D4865	BRKP	* LOAD CODE ROUTINE
4793:	F847	CALL	IADR
4794:	B6	PHI	PAGE
4795:	BE	PHI	R6
4796:	F802	PAD	RE
4797:	A6	PLO	PAD
4798:	40	LDA	R0
4799:	20	DEC	R0
4800:	50	STR	R6
4801:	F8DE	LDI	R0
4802:	50	STR	R0
4803:	F8DA	LDI	BENT
4804:	AE	PLO	RE
4805:	C0470D	LBR	EBUG5
4806:	D4865	BRKP	* LOAD CODE ROUTINE
4807:	F847	CALL	IADR
4808:	B6	PHI	PAGE
4809:	BE	PHI	R6
4810:	F802	PAD	RE
4811:	A6	PLO	PAD
4812:	40	LDA	R0
4813:	20	DEC	R0
4814:	50	STR	R6
4815:	F8DE	LDI	R0
4816:	50	STR	R0
4817:	F8DA	LDI	BENT
4818:	AE	PLO	RE
4819:	C0470D	LBR	EBUG5
4820:	D4865	BRKP	* LOAD CODE ROUTINE
4821:	F847	CALL	IADR
4822:	B6	PHI	PAGE
4823:	BE	PHI	R6
4824:	F802	PAD	RE
4825:	A6	PLO	PAD
4826:	40	LDA	R0
4827:	20	DEC	R

```

4784: D44860 LOAD1      CALL      OADR      IADR      IADR
4787: D44824      CALL      IADR      IADR      IADR
478A: 61      OADR      R1      R1      R1
478B: 50      STR      R0      R0      R0
478C: 10      INC      R0      R0      R0
478D: 3084     BR      BR      BR      BR

* INSPECT CODE ROUTINE
478F: D44865      INSP      CALL      IADR      IADR
4792: D44860      INSP1     CALL      OADR      OADR
4795: 40      LDA      R0      R0      R0
4796: D44847      CALL      OADR      OADR
4799: D447E5      CALL      INCR      INCR
479C: 3092     BR      BR      BR      BR

* EXECUTE CODE ROUTINE
479E: D44865      EXEC      CALL      IADR      IADR
47A1: 80      GLO      R0      R0      R0
47A2: 73      STX0     R0      R0      R0
47A3: 90      GHI      R0      R0      R0
47A4: 73      STX0     R0      R0      R0
47A5: D5      RETN      RETN      RETN

* DUMP CODE ROUTINE
47A6: D44865      DUMP      CALL      IADR      IADR
47A9: F808     LOI      R08     R08     R08
47AB: AB      PLO      R0      R0      R0
47AC: D44860      DUMP2     CALL      OADR      OADR
47AD: 40      LDA      R0      R0      R0
47AE: D44847      CALL      OADR      OADR
47AF: F820     LOI      R08     R08     R08
47B0: 2B      STX0     R0      R0      R0
47B1: D44703      CALL      OADR      OADR
47B2: 2B      STX0     R0      R0      R0
47B3: 8B      DEC      R0      R0      R0
47B4: 3A4F     GLO      R0      R0      R0
47B5: D447E5      DUMP2     GLO      R0      R0
47B6: 30A9     BR      BR      BR      BR

* MODIFY CODE ROUTINE
47C1: D44865      MOD1      CALL      IADR      IADR
47C4: D447EC      MOD11     CALL      OADR      OADR
47C7: D44860      MOD12     CALL      OADR      OADR
47CA: 40      LDA      R0      R0      R0
47CB: D44847      CALL      OADR      OADR
47CC: D44707      CALL      OADR      OADR
47CD: 52      STR      R2      R2      R2
47CE: F80D     SMI      R2      R2      R2
47CF: 32C4     BZ      BZ      BZ      BZ
47D0: F0      LDX      R0      R0      R0
47D1: F07C     SMI      R0      R0      R0
47D2: CA470D      LBN2     LBN2     LBN2
47D3: D44824      CALL      OADR      OADR
47D4: 61      GLO      R1      R1      R1
47D5: 20      DEC      R0      R0      R0
47D6: 50      STR      R0      R0      R0
47D7: 10      INC      R0      R0      R0
47D8: 30C7     BR      BR      BR      BR

* INPUT CR SUBR
47E5: D44707      INCR      CALL      IADR      IADR

47E8: 47E8:      FF0D      SMI      CR      CR
47EA: 47EA:      JADD      EBUGS  EBUGS
47EC: 47EC:      F80A      LDI      LF      LF
47EE: 47EE:      D44703      CALL      OTT      OTT
47F1: 47F1:      D5      RETN      RETN      RETN

DISPLAY ADDRESS
GET DATA BYTE
STORE IN MEMORY

DISPLAY MEM CONTENTS
WAIT FOR A CR
TRY AGAIN

GET ADDR
STORE IT ON STACK

60 TO IT VIA SRETN

GET ADDR
PREP 8 CNTR

DISPLAY ADDR

DISPLAY 8 BYTES OF

WAIT FOR A CR

GET ADDR
OUTPUT A LINEFEED

DISPLAY MEM CONTENTS

CHECK FOR AN INSERT

ABORT OP
GET NEW BYTE
STORE IT IN MEMORY

WAIT FOR A CR

47F2: 47F2:      D44707      IMXD      CALL      IADR      IADR
47F5: 47F5:      52      STR      R2      R2
47F6: 47F6:      FF2E      SMI      PERIOD PERIOD
47F8: 47F8:      C2470D      LBN2     LBN2
47F9: 47F9:      F0      LDX      EBUGS  EBUGS
47FA: 47FA:      F80D      SMI      CR      CR
47FB: 47FB:      C24820      LBN2     LBN2
47FC: 47FC:      F0      LDX      IMXD3  IMXD3
47FD: 47FD:      801:      LDI      R01     R01
47FE: 47FE:      802:      LDI      R02     R02
47FF: 47FF:      803:      LDI      R03     R03
4800: 4800:      804:      LDI      R04     R04
4801: 4801:      805:      LDI      R05     R05
4802: 4802:      806:      LDI      R06     R06
4803: 4803:      807:      LDI      R07     R07
4804: 4804:      808:      LDI      R08     R08
4805: 4805:      809:      LDI      R09     R09
4806: 4806:      80A:      LDI      R0A     R0A
4807: 4807:      80B:      LDI      R0B     R0B
4808: 4808:      80C:      LDI      R0C     R0C
4809: 4809:      80D:      LDI      R0D     R0D
480A: 480A:      80E:      LDI      R0E     R0E
480B: 480B:      80F:      LDI      R0F     R0F
480C: 480C:      810:      LDI      R10     R10
480D: 480D:      811:      LDI      R11     R11
480E: 480E:      812:      LDI      R12     R12
480F: 480F:      813:      LDI      R13     R13
4810: 4810:      814:      LDI      R14     R14
4811: 4811:      815:      LDI      R15     R15
4812: 4812:      816:      LDI      R16     R16
4813: 4813:      817:      LDI      R17     R17
4814: 4814:      818:      LDI      R18     R18
4815: 4815:      819:      LDI      R19     R19
4816: 4816:      81A:      LDI      R1A     R1A
4817: 4817:      81B:      LDI      R1B     R1B
4818: 4818:      81C:      LDI      R1C     R1C
4819: 4819:      81D:      LDI      R1D     R1D
481A: 481A:      81E:      LDI      R1E     R1E
481B: 481B:      81F:      LDI      R1F     R1F
481C: 481C:      820:      LDI      R20     R20
481D: 481D:      821:      LDI      R21     R21
481E: 481E:      822:      LDI      R22     R22
481F: 481F:      823:      LDI      R23     R23
4820: 4820:      824:      LDI      R24     R24
4821: 4821:      825:      LDI      R25     R25
4822: 4822:      826:      LDI      R26     R26
4823: 4823:      827:      LDI      R27     R27
4824: 4824:      828:      LDI      R28     R28
4825: 4825:      829:      LDI      R29     R29
4826: 4826:      82A:      LDI      R2A     R2A
4827: 4827:      82B:      LDI      R2B     R2B
4828: 4828:      82C:      LDI      R2C     R2C
4829: 4829:      82D:      LDI      R2D     R2D
482A: 482A:      82E:      LDI      R2E     R2E
482B: 482B:      82F:      LDI      R2F     R2F
482C: 482C:      830:      LDI      R30     R30
482D: 482D:      831:      LDI      R31     R31
482E: 482E:      832:      LDI      R32     R32
482F: 482F:      833:      LDI      R33     R33
4830: 4830:      834:      LDI      R34     R34
4831: 4831:      835:      LDI      R35     R35
4832: 4832:      836:      LDI      R36     R36
4833: 4833:      837:      LDI      R37     R37
4834: 4834:      838:      LDI      R38     R38
4835: 4835:      839:      LDI      R39     R39
4836: 4836:      83A:      LDI      R3A     R3A
4837: 4837:      83B:      LDI      R3B     R3B
4838: 4838:      83C:      LDI      R3C     R3C
4839: 4839:      83D:      LDI      R3D     R3D
483A: 483A:      83E:      LDI      R3E     R3E
483B: 483B:      83F:      LDI      R3F     R3F
483C: 483C:      840:      LDI      R40     R40
483D: 483D:      841:      LDI      R41     R41
483E: 483E:      842:      LDI      R42     R42
483F: 483F:      843:      LDI      R43     R43
4840: 4840:      844:      LDI      R44     R44
4841: 4841:      845:      LDI      R45     R45

```

```

4842: 60      IRX
4843: F1      OR
4844: A1      PLO
4845: 3024    BR
                                     R1
                                     IMEX

      * OUTPUT HEX NUMBER SUBR
      OHEX      STXD
4847: 73      SMR
4848: F6      SMR
4849: F6      SMR
484A: F6      SMR
484B: F6      SMR
484C: F6      SMI
484E: C7      LSNF
484F: FC07    ADI
4851: FC3A    ADI
4853: D4703   CALL
4856: 60      IRX
4857: F0      LDX
4858: FA0F    ANI
485A: FFOA    SMI
485C: C7      LSNF
485D: FC07    ADI
485F: FC3A    ADI
4861: D4703   CALL
4864: D5      RETN

      * INPUT ADDRESS SUBR
      IADR      CALL
4865: D4324    GLO
4868: 81      PLO
4869: A0      GHI
486A: 91      PHI
486B: 00      RETN
486C: D5

      * OUTPUT ADDRESS SUBR
      OADR      GHI
486D: 50      CALL
486E: D4847    GLO
4871: 60      GLO
4872: D4847    CALL
4875: F83A    LDI
4877: D4703   CALL
487A: F820    LDI
487C: D4703   CALL
487F: D5      RETN

      * RE-ENTRY ROUTINE
      BENT1     PLC
4880: A1      PLO
4881: F847    LDI
4883: B6      PHI
4884: F802    LDI
4886: A6      PLO
4887: B6      LDM
4888: 23      DEC
4889: 53      STR
488A: 9E      GHI
488B: B3      PHI
488C: F88F    LDI
488E: A3      PLO
488F: D3      SEP
4890: D3      GLO
4891: 81      CALL
4892: D4847    LBP
4893: C0470D

```

CONVERT HEX IN ACCM INTO ASCII

PUSH CONTENT OF R1 INTO R0

SAVE ACCM IN R1.0
RESTORE CONTENTS OF MEMORY

RESTORE R3 AS PC

DISPLAY CONTENTS OF ACCM

QUESTDATA
P.O. Box 4430
Santa Clara, CA 95054

*A 12 issue subscription to QUESTDATA, the publication devoted entirely to the COSMAC 1802 is \$12.
(Add \$6.00 for airmail postage to all foreign countries except Canada and Mexico add \$2.00)
Your comments are always welcome and appreciated. We want to be your 1802's best friend.*

Payment.

- ☐ Check or Money Order Enclosed
Made payable to Quest Electronics
- ☐ Master Charge No
- ☐ Bank Americard No
- ☐ Visa Card No

Expiration Date: _____

Signature _____

☐ Renewal ☐ New Subscription

NAME _____

ADDRESS _____

CITY _____

STATE _____

ZIP _____

FROM THE PUBLISHER

SEND IN YOUR PROGRAMS

We have been very encouraged by the content, quality and quantity of programs submitted for publication to QUESTDATA. Please keep them coming. We are interested in all types of programs including software and hardware large and small, Basic and machine language covering all subjects. Programs of 256 bytes or less are particularly needed. Also we will be publishing more hardware oriented articles, with your support naturally. The format we would like you to use would include a typed write-up with annotated code listing and a flow chart. We will continue to pay at the rate of \$15.00 per published page. Programs submitted in machine readable form (Basic, Basic editor, or Editor-Assembler cassettes) and or "camera ready" will get higher payment and are likely to be published sooner. Write for our free "How to write for QUESTDATA" instructions. Please enclose a self addressed stamped business size envelope for your copy by return mail.

TIME TO RESUBSCRIBE

Since many of you began with issue #1 of volume II, many subscriptions are up for renewal. The price remains at \$12.00 (with the exception of Canada and Mexico) for 12 issues in spite of increased mailing costs. It is an extremely attractive value for any 1802 computer user. We expect to have some very interesting issues during 1982 that will make your computer more useful as well as entertaining. After several major staffing changes and production improvements it appears that issues can be published regularly and frequently with an objective of at least ten per year. An exciting new series on QUEST SUPER BASIC begins with this issue and will continue on through volume III. New subscriptions or renewals may be accomplished relatively painlessly by filling in the form at the end of this issue. If you haven't renewed yet this may be your last issue. Thank you for your support in the past.

With this issue we complete the second volume of QUESTDATA. This volume will be bound and offered as we have the first volume and will do again when we complete the succeeding volumes.

COSMAC CLUB COSMAC CLUB COSMAC CLUB COSMAC CLUB COSMAC CLUB COSMAC CLUB

24 QUESTDATA
P.O. Box 4430
Santa Clara, CA 95054

ADDRESS CORRECTION REQUESTED

BULK RATE
U.S. Postage Paid
QUEST
Electronics
Permit No. 549
Santa Clara, CA