CMOS Fabrication and Layout

- Transistors are fabricated on a thin silicon wafer that serve as both a mechanical support and electrical common point called substrate

- Fabrication process (a.k.a. Lithography) is similar to printing press

  - On each step, different materials are deposited or etched

- Easiest way to understand physical layout is to look at the wafer from two perspectives:

  - Top-section

  - Cross-section

1

Photo Lythography
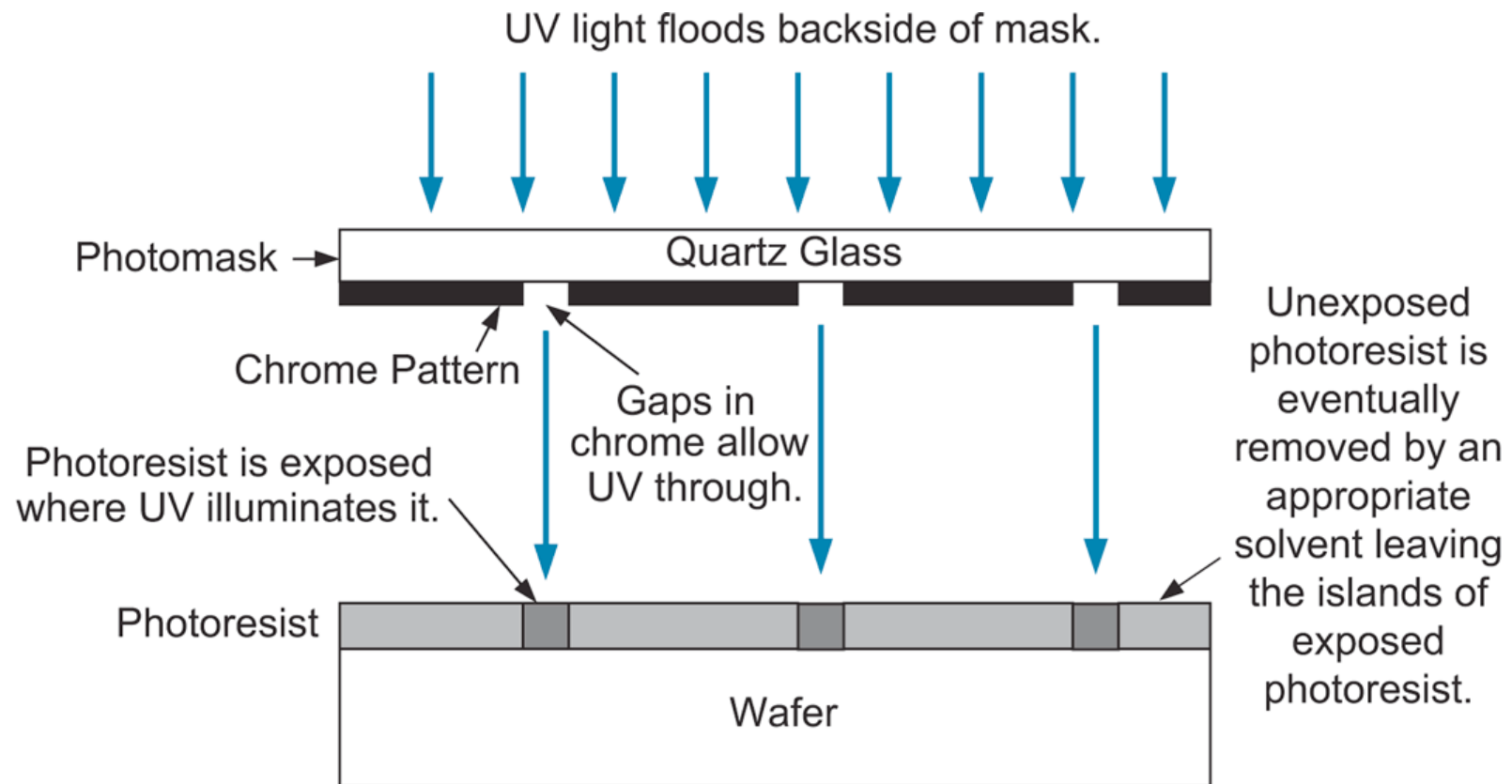
- "Carving pictures in stone using light"

UV light floods backside of mask.

Photomask → | Quartz Glass

Chrome Pattern

Gaps in chrome allow UV through.

Photoresist is exposed where UV illuminates it.

Photoresist

Wafer

Unexposed photoresist is eventually removed by an appropriate solvent leaving the islands of exposed photoresist.

FIG 3.1 Photomasking with a negative resist (lens system between mask and wafer omitted to improve clarity and avoid diffracting the reader ☺)

Inverter Cross Section

- Typically use p-type substrate for nMOS transistors

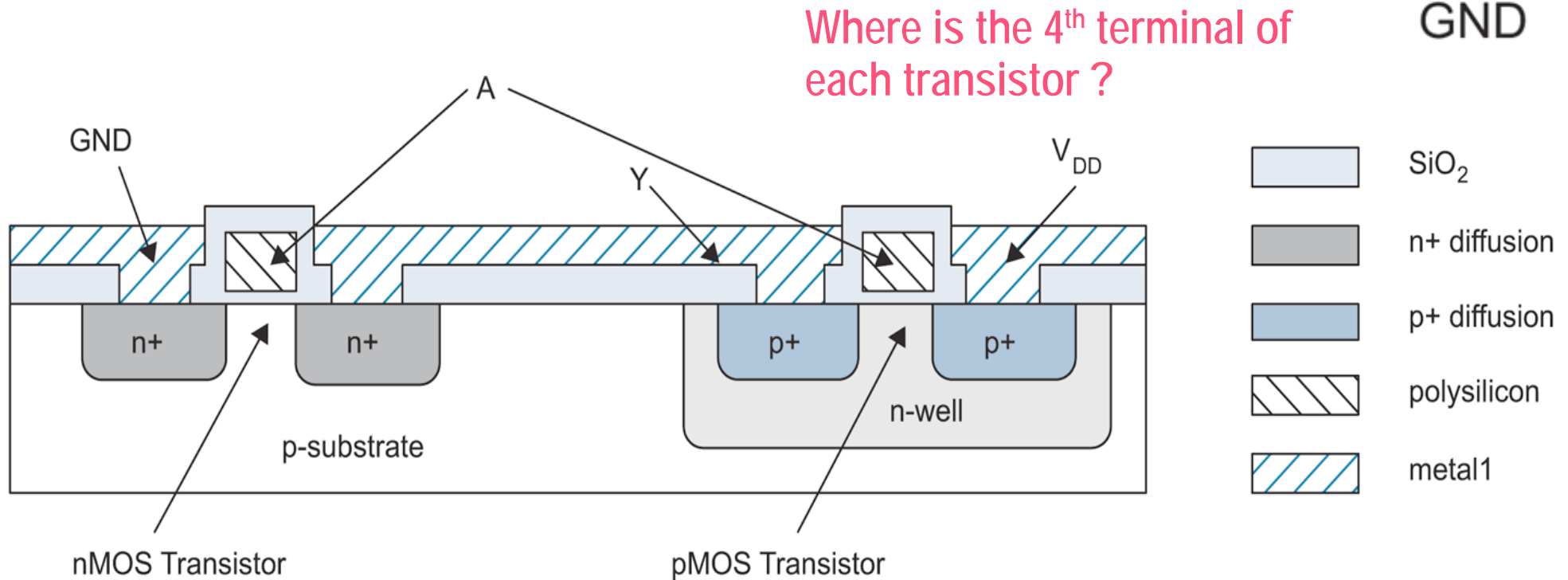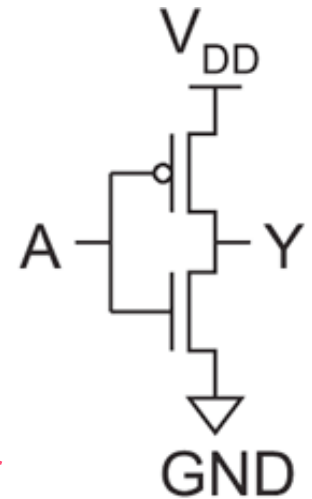- Requires n-well for body of pMOS transistors

Where is the 4th terminal of each transistor ?

FIG 1.33 Inverter cross-section

Well and Substrate Taps

- Substrate must be tied to GND and n-well to V_{DD}

- Metal to lightly-doped semiconductor forms poor connection (parasitic diode)

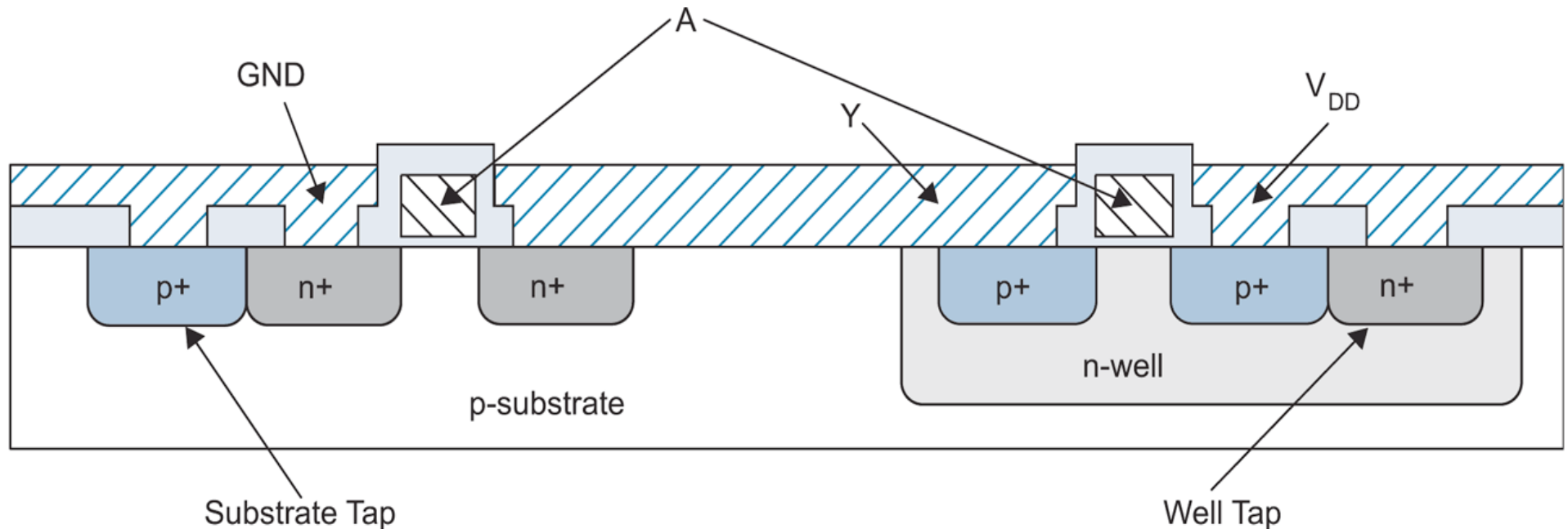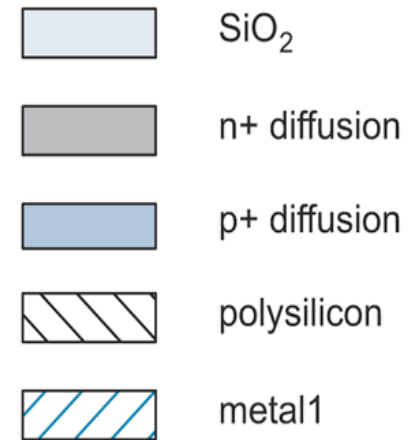- Use heavily doped well and substrate contacts

Legend:
- SiO$_2$
- n+ diffusion
- p+ diffusion
- polysilicon
- metal1

FIG 1.34 Inverter cross-section with well and substrate contacts. Color version on inside front cover.
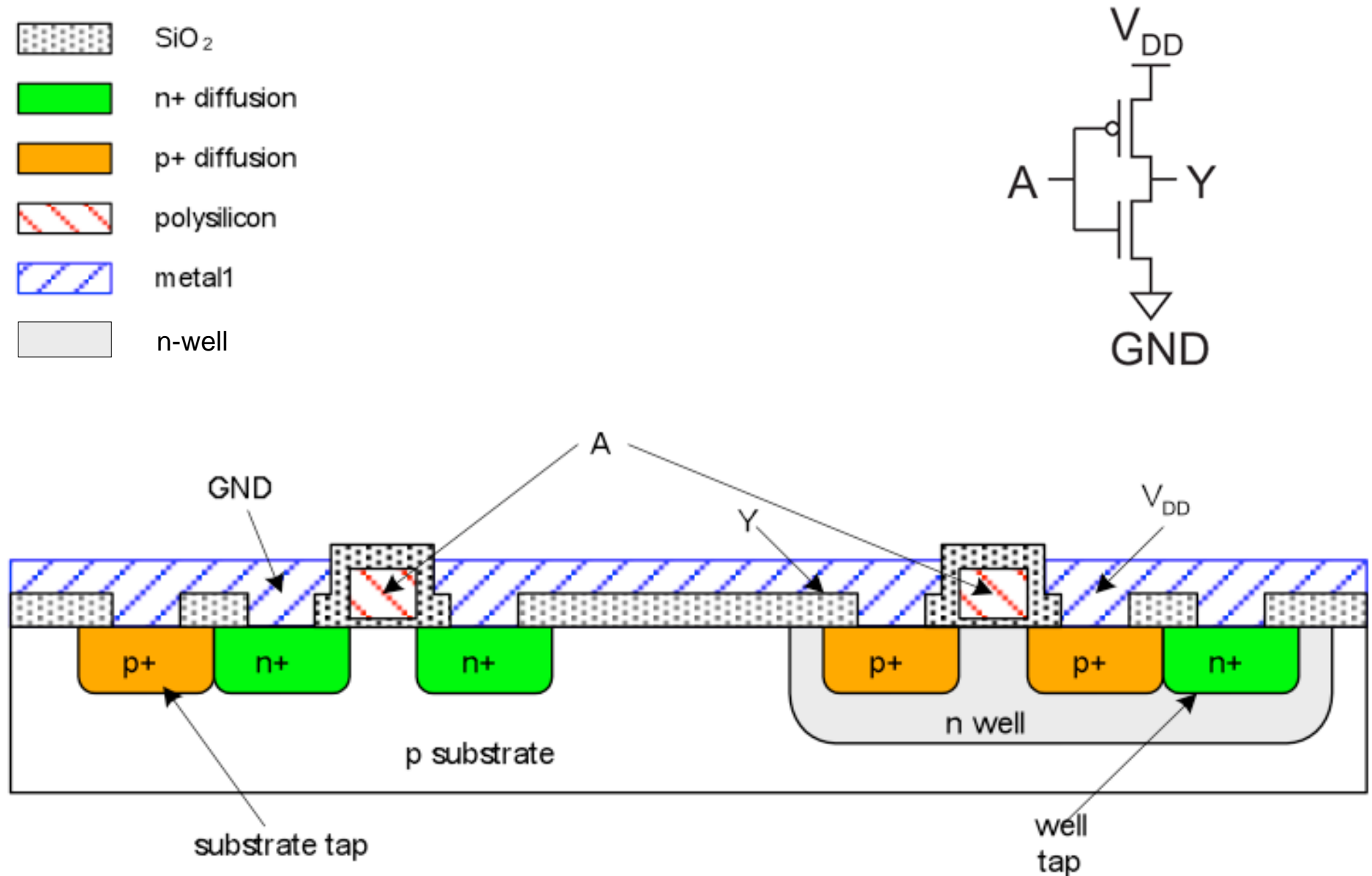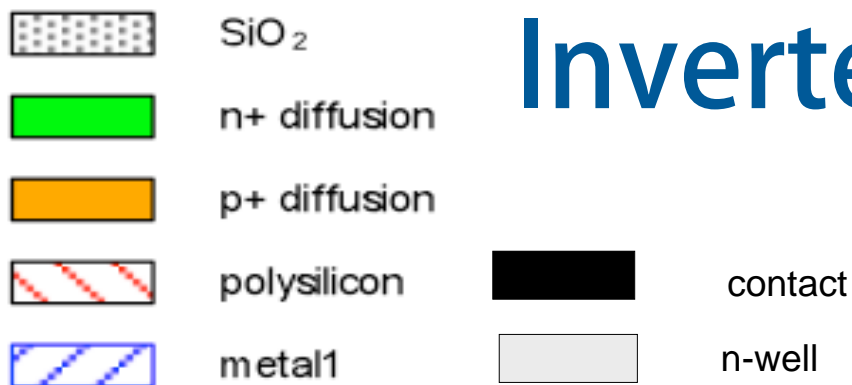
Let's add some color ...

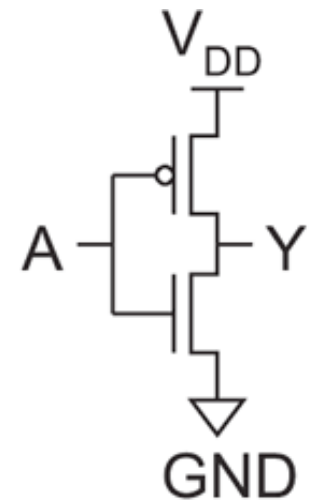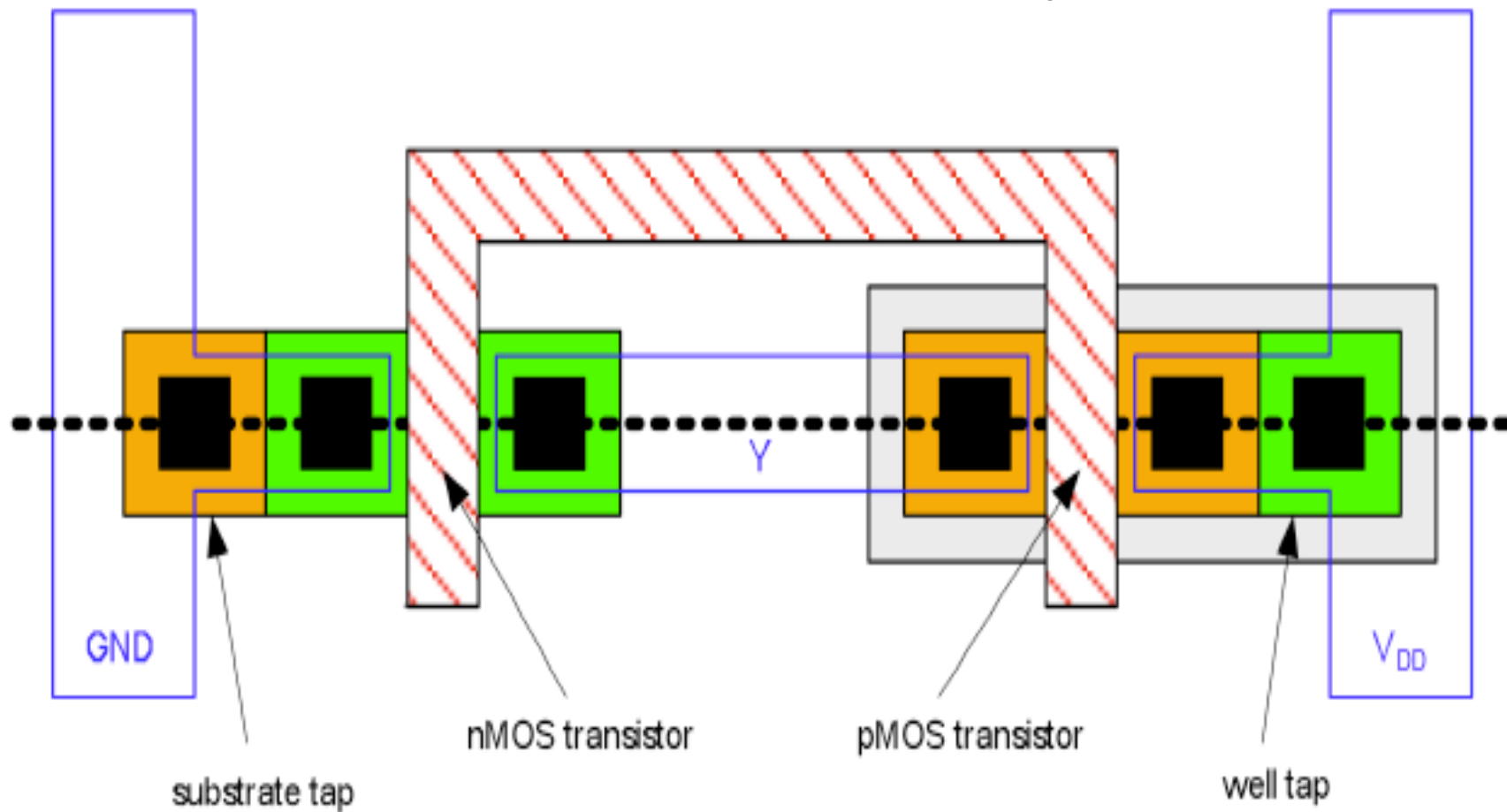FIG 1.34 Inverter cross-section with well and substrate contacts. Color version

Inverter Top View

Legend:
- SiO$_2$
- n+ diffusion
- p+ diffusion
- polysilicon
- metal1
- contact
- n-well

- Transistors and wires are defined by masks

GND

Y

V$_{DD}$

substrate tap

nMOS transistor

pMOS transistor

well tap

V$_{DD}$

A — Y

GND

Inverter Mask Set

Six masks:

- n-well
- poly silicon
- n+ diffusion
- p+ diffusion
- Contact
- Metal

7
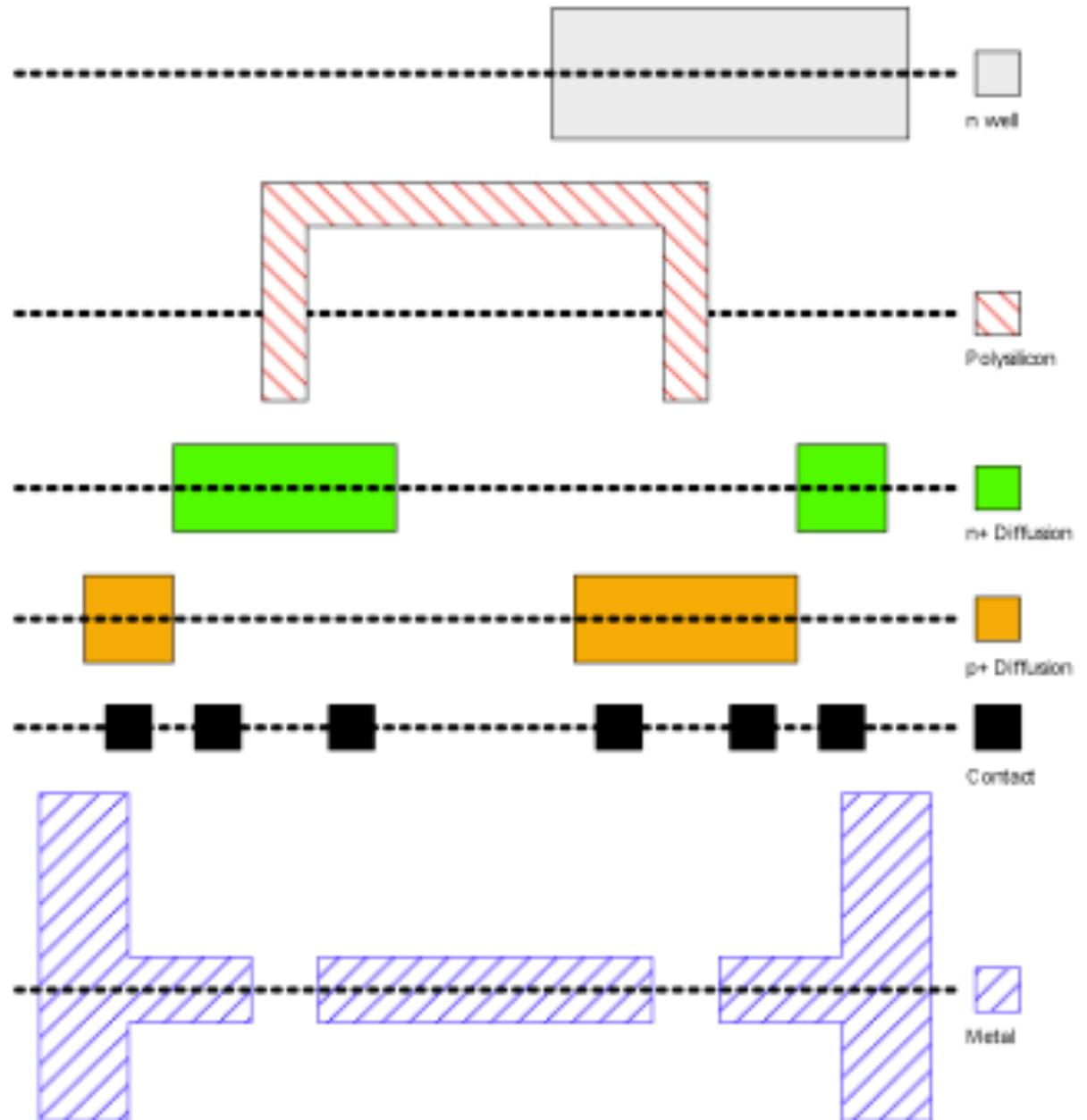
Fabrication Steps

- Start with blank wafer

- Build invert from bottom up

| |
|---|
| p substrate |

n-well Formation

- First step will be to form the n-well

  - Cover wafer with protective layer of SiO_2 (oxide)
    to grow SiO_2 on top of Si wafer put the Si with H_2O
    or O_2 in oxidation furnace at 900 – 1200 C

  - (Remove layer where n-well should be built)

 - (Implant or diffuse n dopants into exposed wafer)

  - (Strip off SiO_2)

SiO$_2$

p substrate

9

Deposit silicon-oxide and photoresist

- Photoresist is a light-sensitive organic polymer

- Softens where exposed to light

Photoresist

SiO$_2$

p substrate
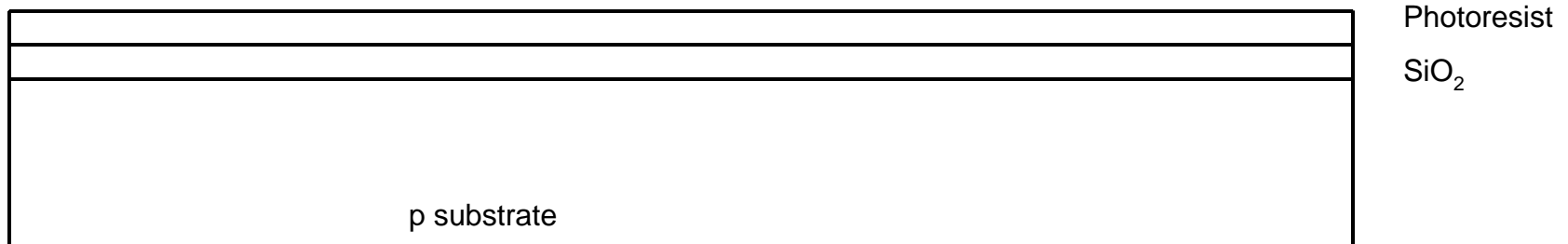
NOTE: The silicon oxide is just to protect the wafer

Photo-Lithography

- Expose photoresist through n-well mask

- Strip off exposed photoresist

Photoresist

SiO$_2$

p substrate
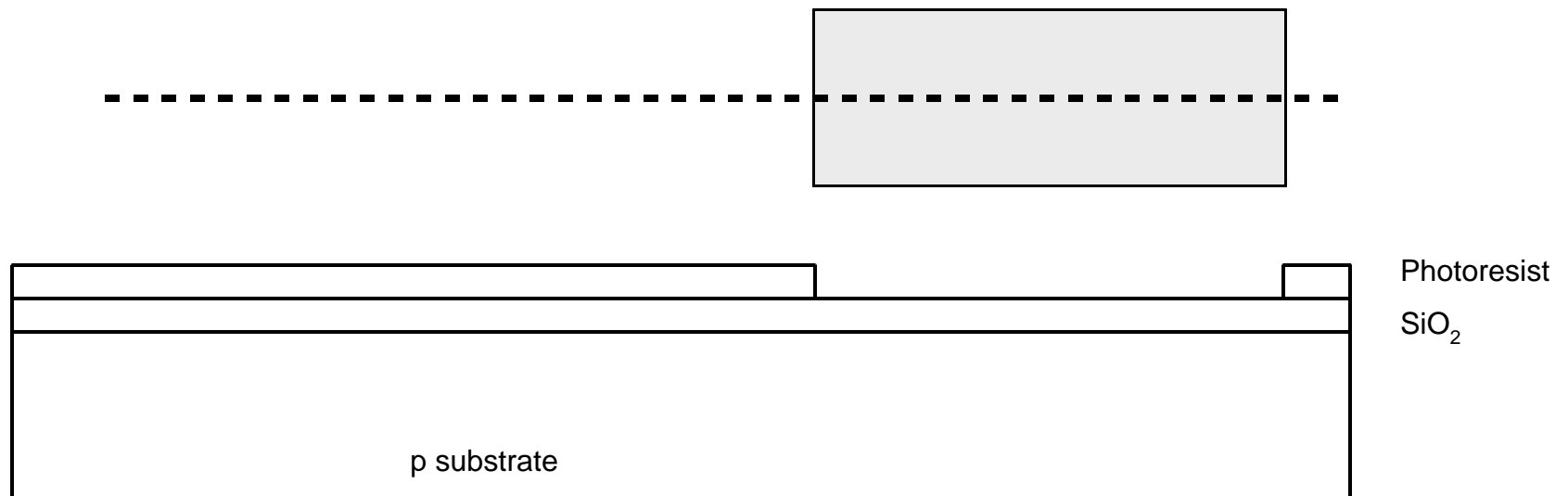
Etching

- Etch oxide with hydrofluoric acid (HF)
    - Seeps through skin and eats bone: nasty stuff!!!
- Only attacks oxide where resist has been exposed

Photoresist

SiO$_2$

p substrate
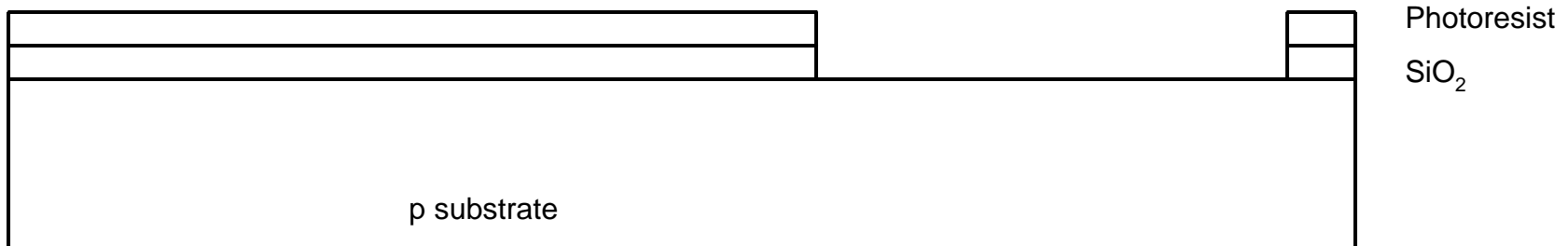
The n-well

- n-well is formed with diffusion or ion implantation

- Diffusion

  - Place wafer in furnace with arsenic gas

  - Heat until As atoms diffuse into exposed Si

- Ion Implantation

  - Blast wafer with beam of As ions

 - Ions blocked by SiO_2, only enter exposed Si

SiO$_2$

n well

13
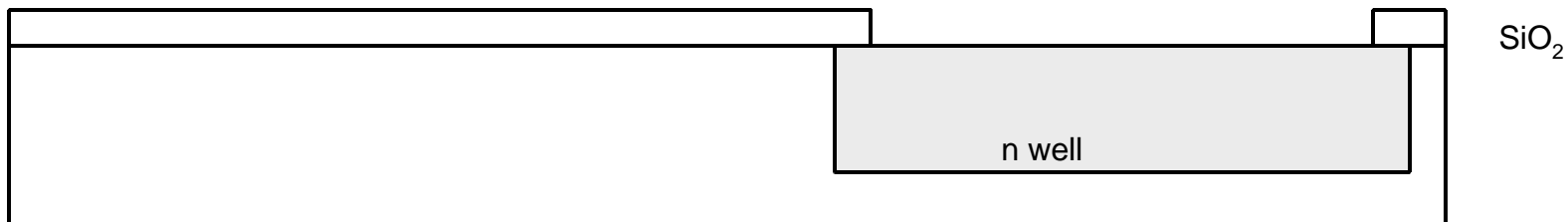
Strip protective oxide

- Strip off the remaining oxide using HF

- Back to bare wafer with n-well

- Subsequent steps involve similar series of steps

n well

p substrate

Gate oxide and Polysilicon

- Deposit very thin layer of gate oxide

    < 20 Å (6-7 atomic layers)

- Chemical Vapor Deposition (CVD) of silicon layer

    – Place wafer in furnace with Silane gas (SiH_4)

    – Forms many small crystals called polysilicon

    – Heavily doped to be good conductor

Polysilicon
Thin gate oxide

n well

p substrate
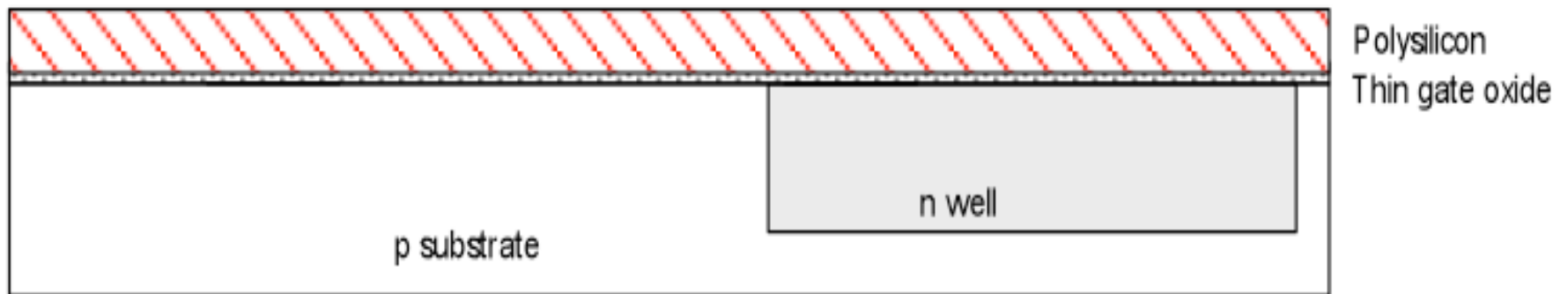
Polysilicon patterning

- Use same lithography process to pattern polysilicon

Polysilicon

Polysilicon
Thin gate oxide

n well

p substrate

16
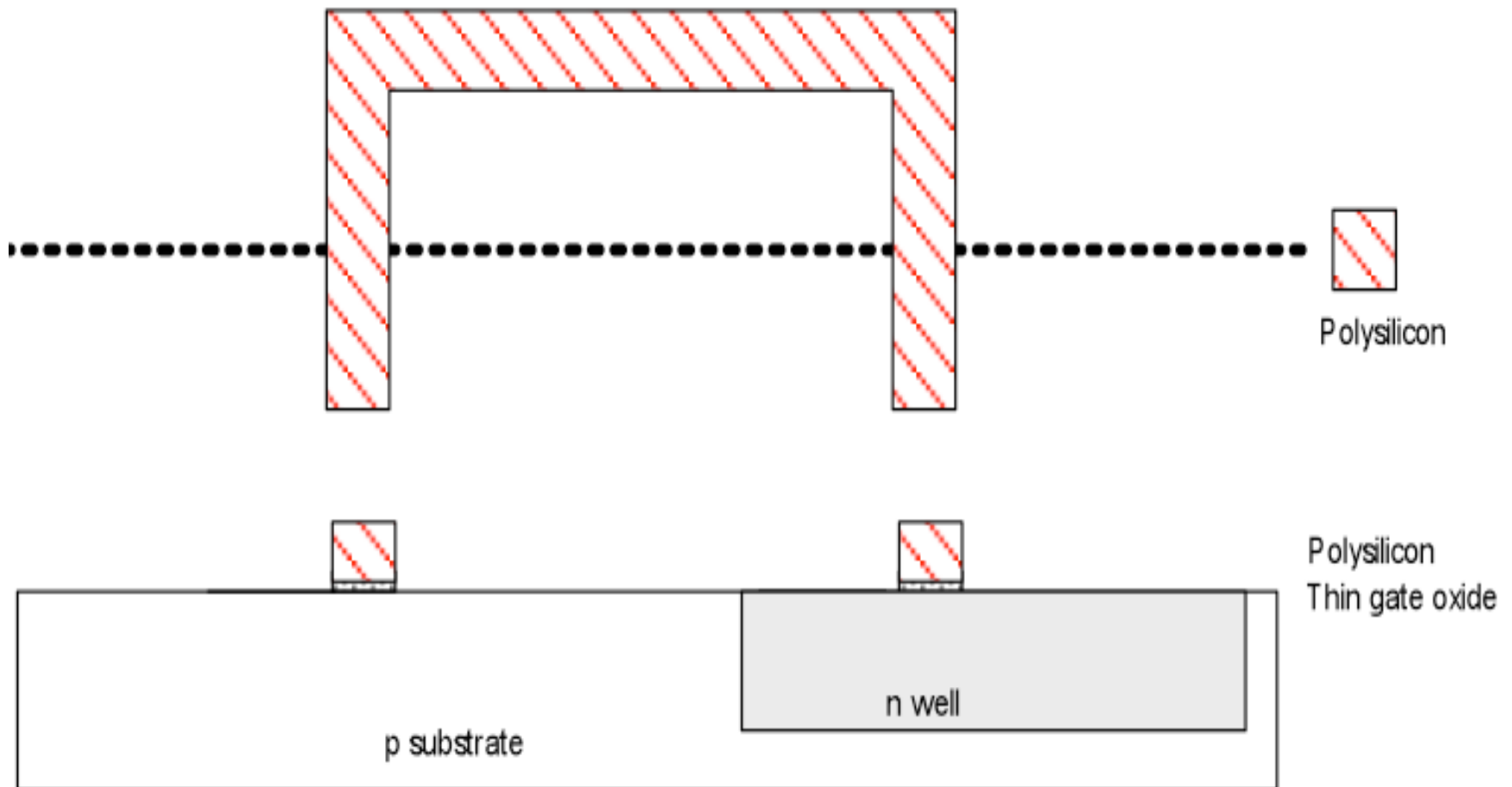
Self-aligned polysilicon gate process

- The polysilicon gate serves as a mask to allow precise alignment of the source and drain with the gate

- Use oxide and masking to expose where n+ dopants should be diffused or implanted

- n-diffusion forms nMOS source, drain, and n-well contact

protective layer of oxide

p substrate

n well

17
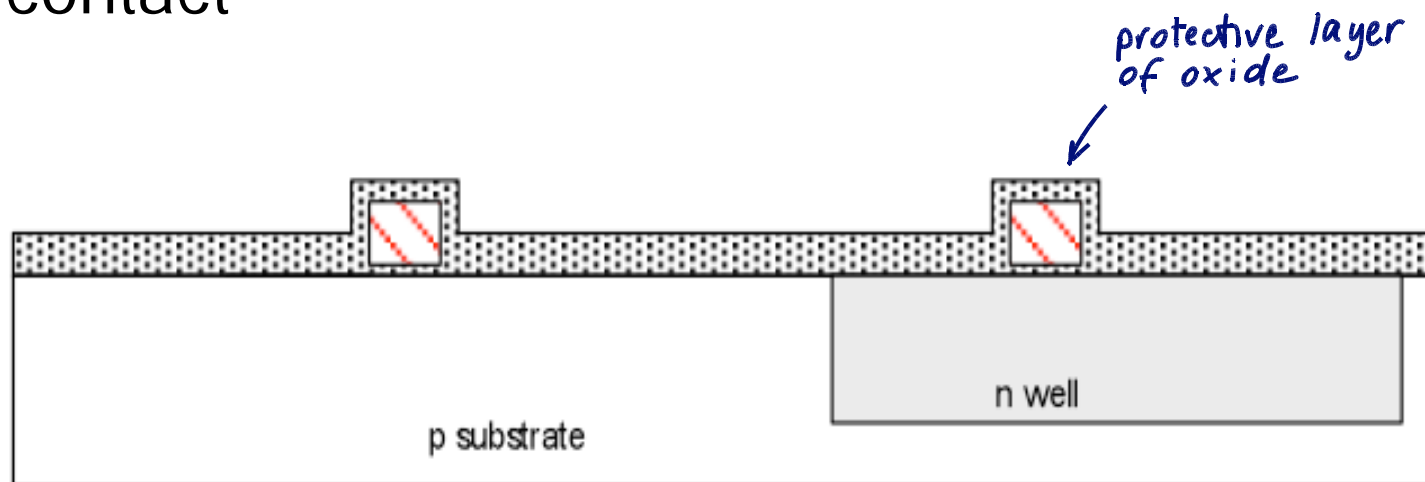
Formation of the n-diffusions

- Pattern oxide and form n+ regions

- *Self-aligned process* (poysilicon gate) "blocks" diffusion under the gate

- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing

n+ Diffusion

n well

p substrate

18
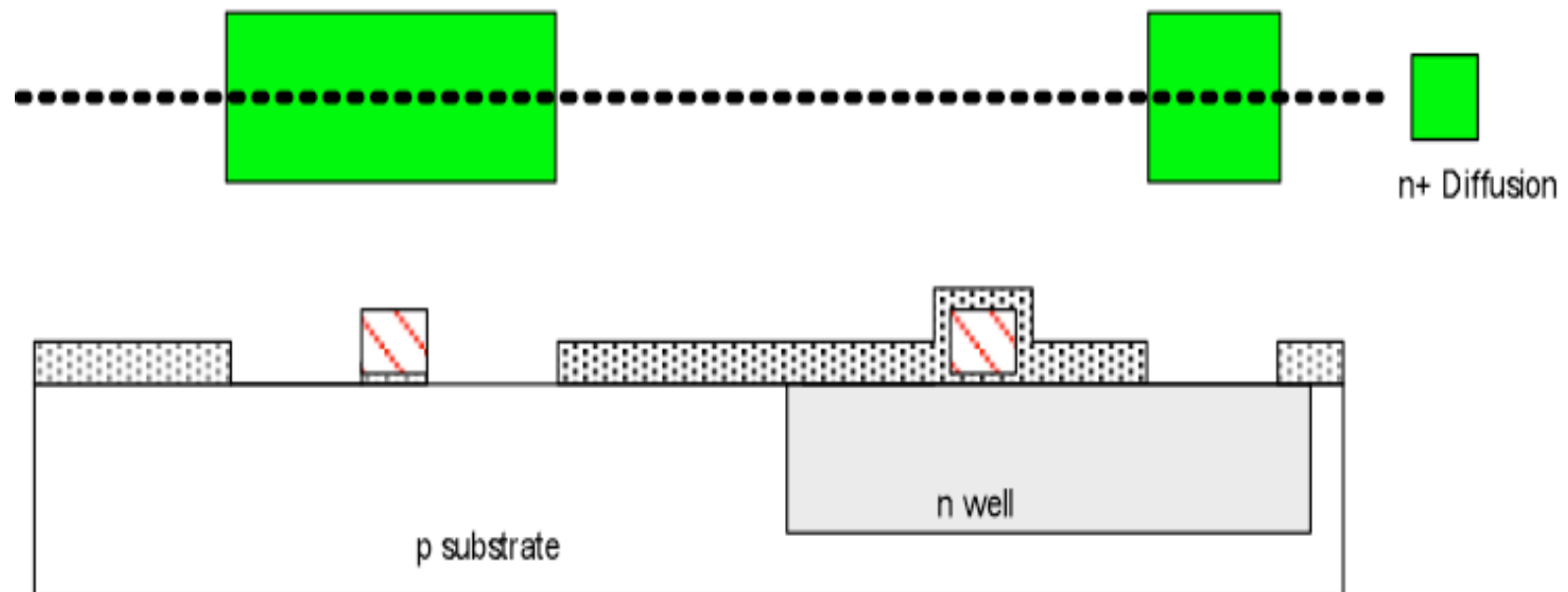
The n-diffusions

- Historically dopants were diffused

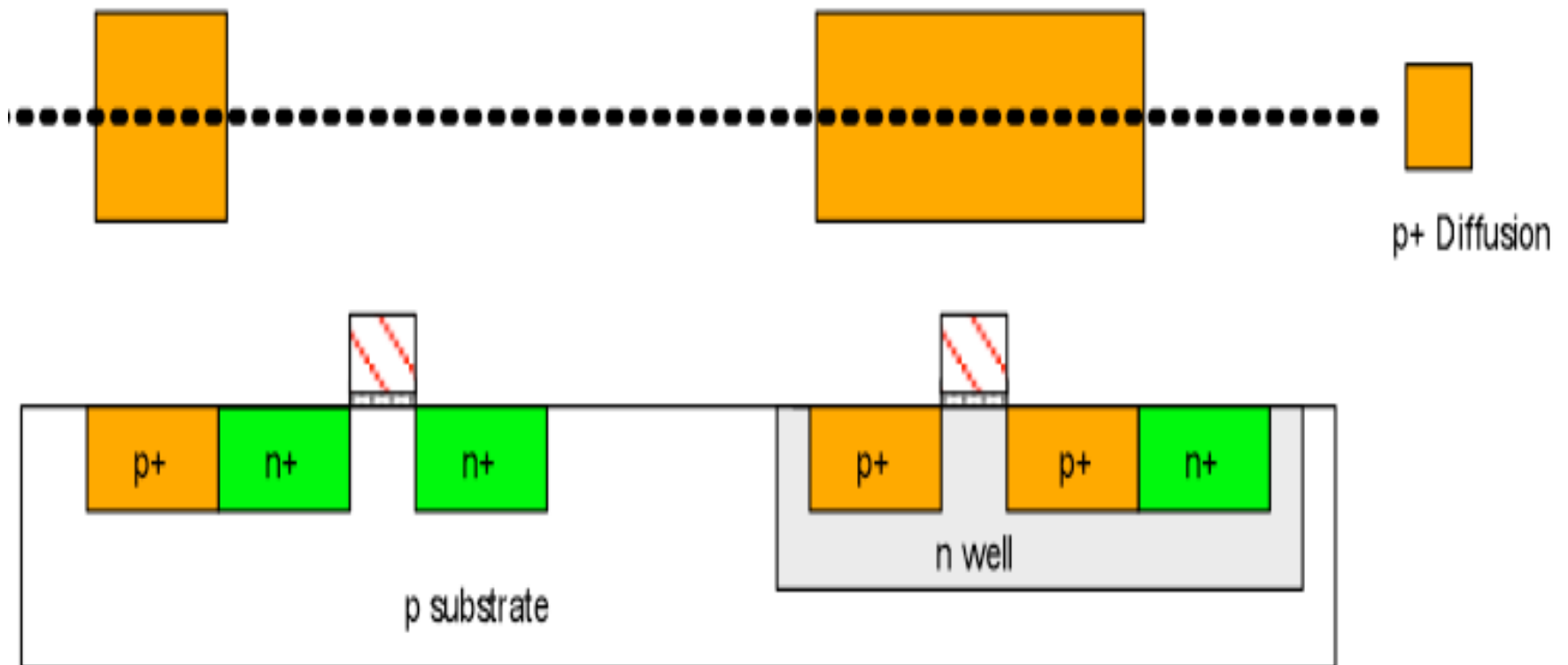- Usually ion implantation today (but regions are still called diffusion)
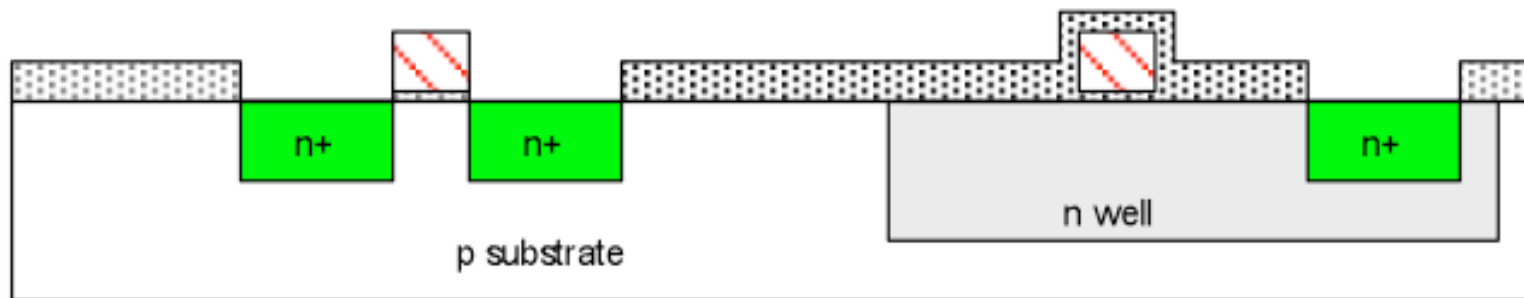
- Strip off oxide to complete patterning step

The p-diffusions

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact
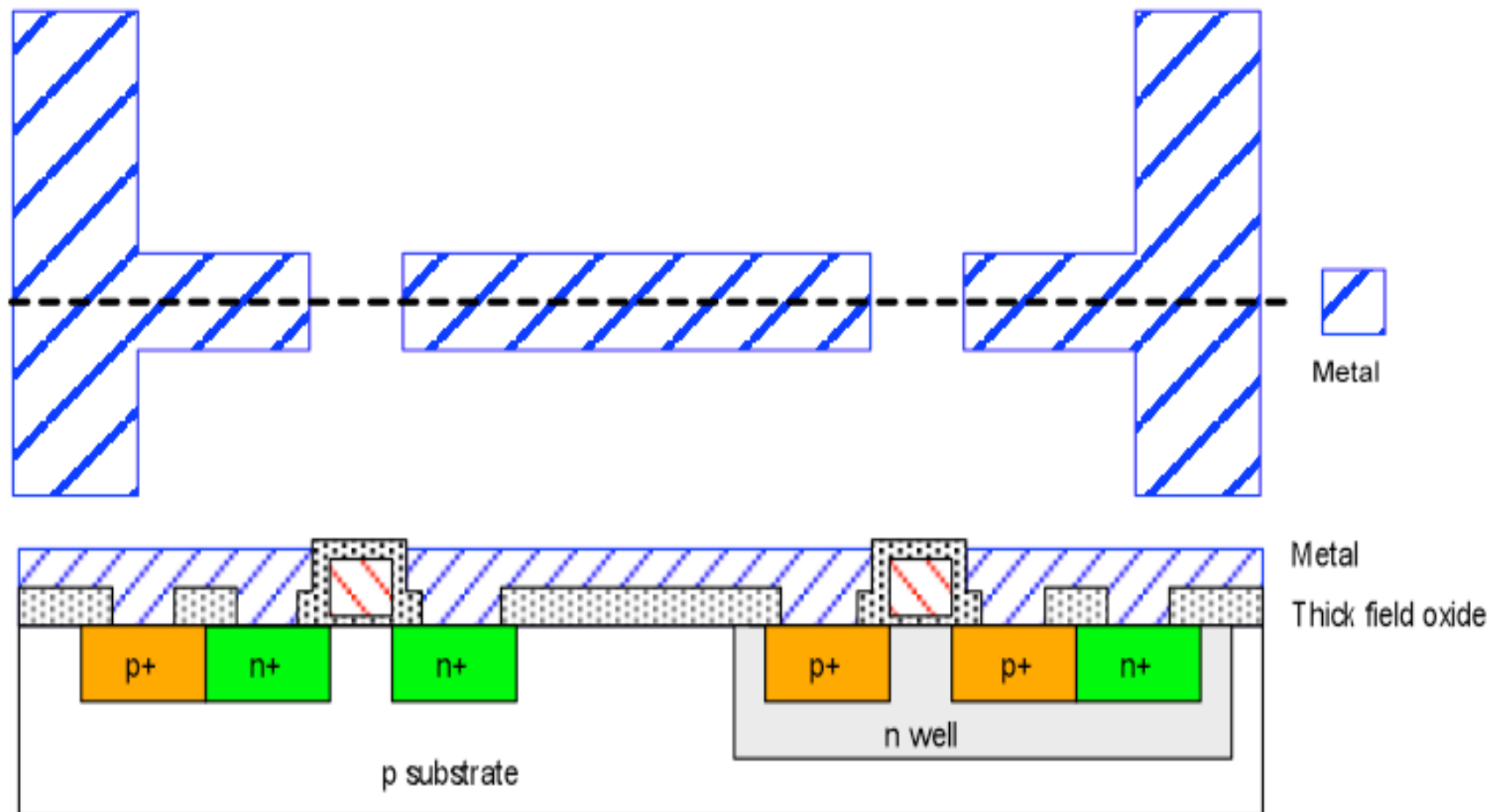

p+ Diffusion

p+   n+   n+

p+   p+   n+

n well

p substrate

Contacts

- Now we need to create the devices' terminals

- Cover chip with thick field oxide (FOX)

- Etch oxide where contact cuts are needed

Contact

Thick field oxide

p+ n+   n+   p+ p+ n+

n well

p substrate
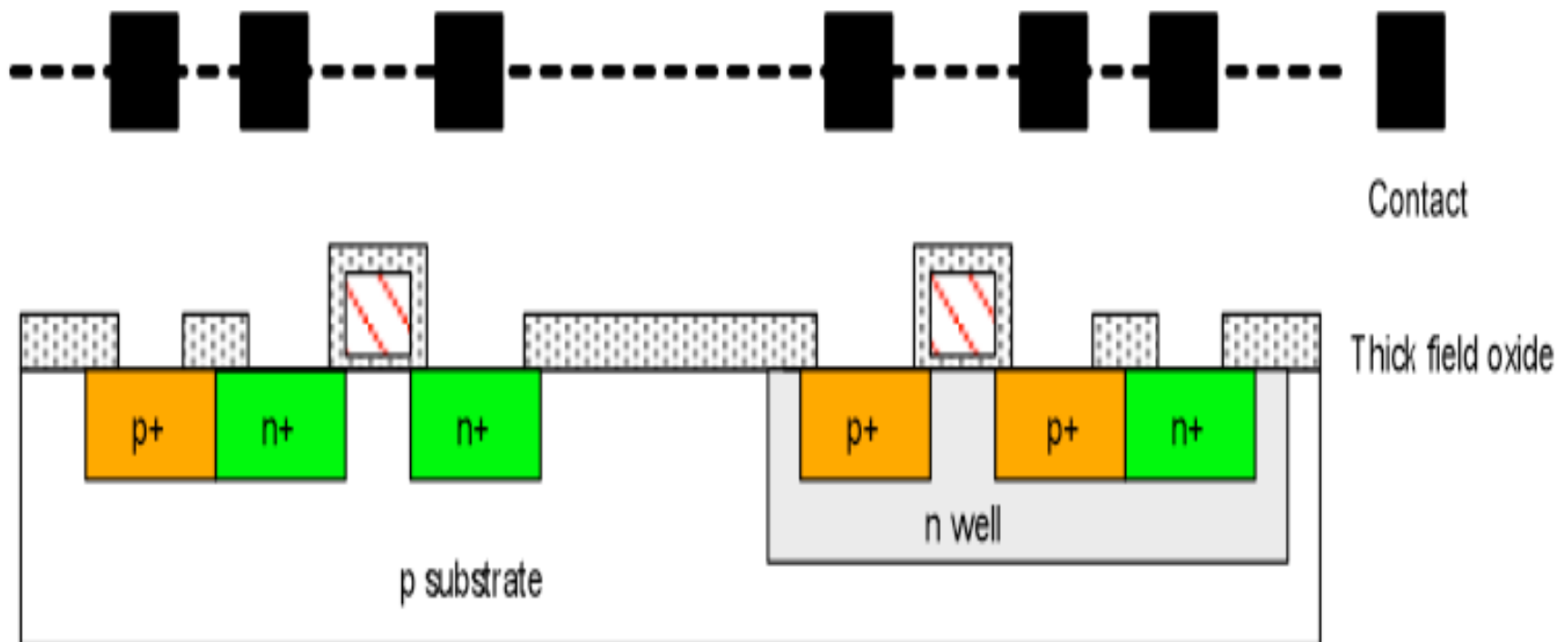
Metallization

- Sputter on aluminum over whole wafer, filling the contacts as well

- Pattern to remove excess metal, leaving wires

Metal

Metal

Thick field oxide

p+   n+   n+   p+   p+   n+

n well

p substrate
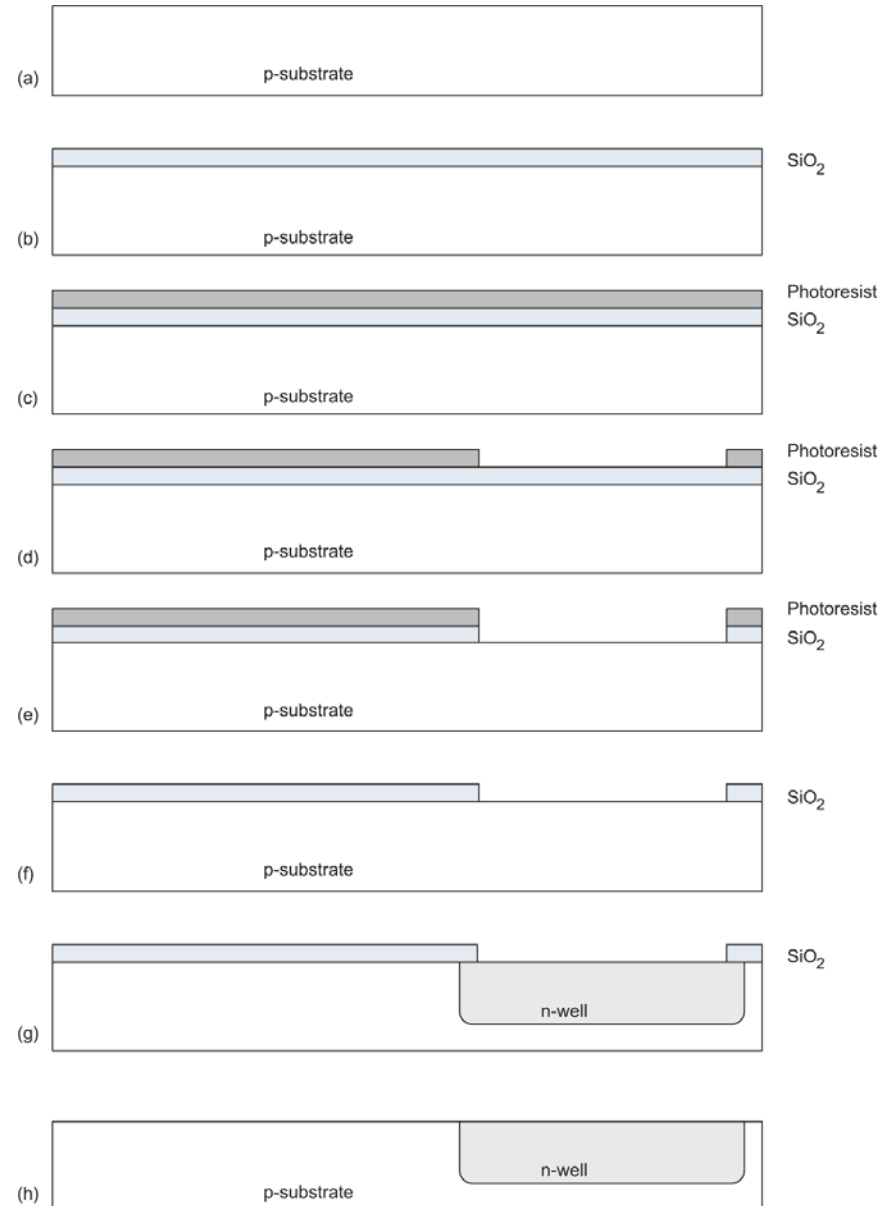
Fabrication Steps Summary (1/3)

FIG 1.36 Cross-sections while manufacturing the n-well

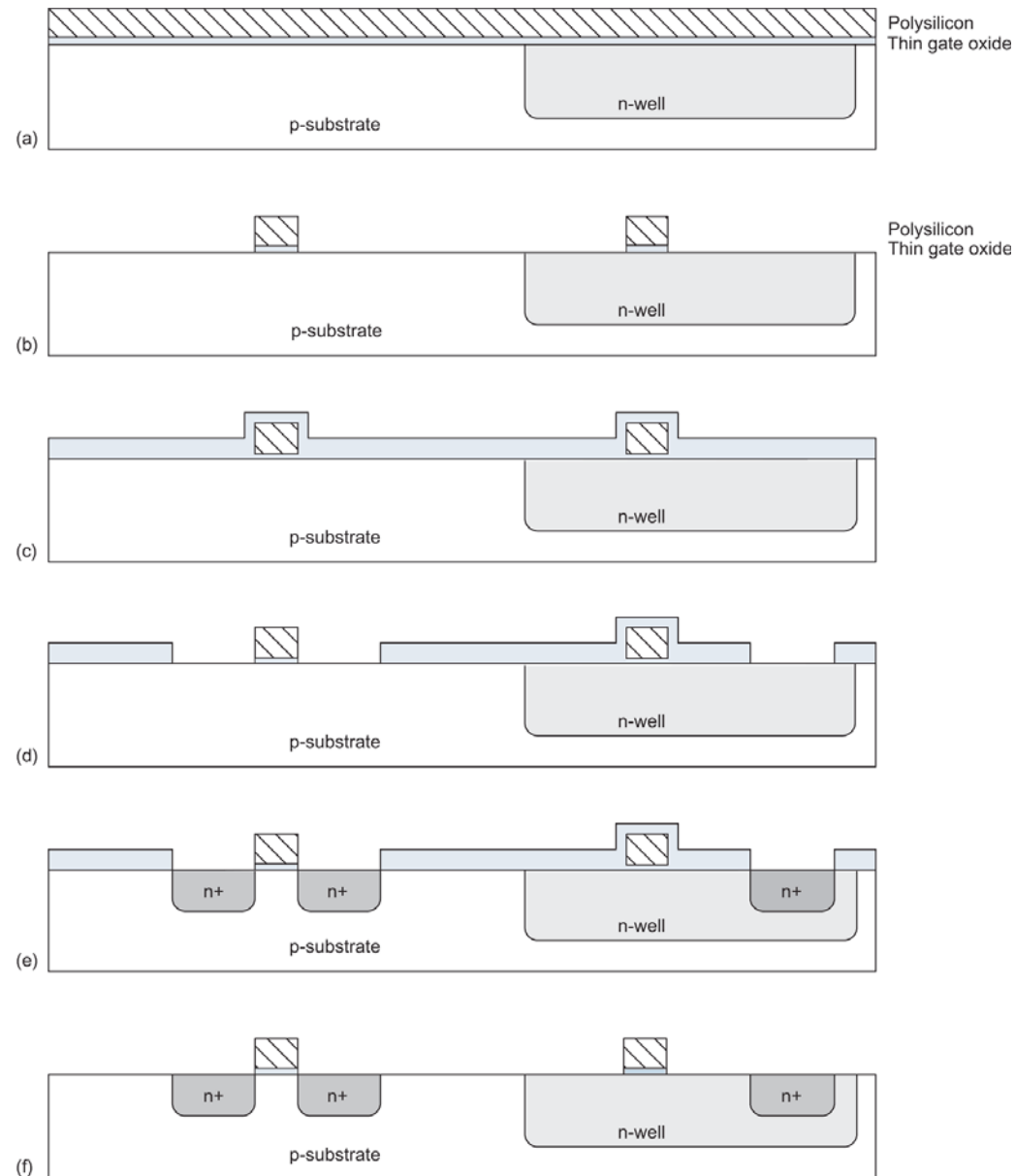# Fabrication Steps Summary (2/3)

FIG 1.37 Cross-sections while manufacturing polysilicon and n-diffusion
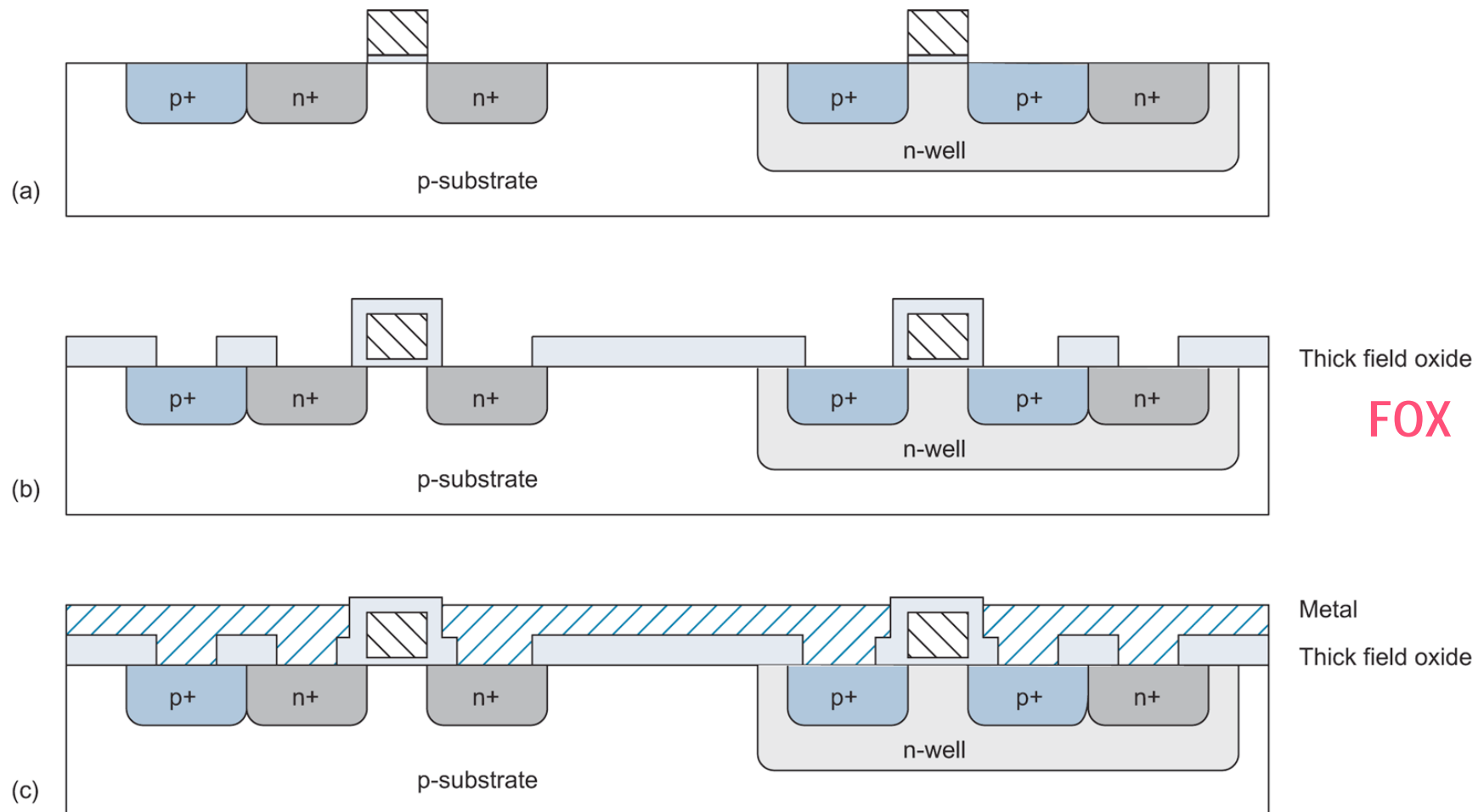
24

Fabrication Steps Summary (3/3)

FIG 1.38 Cross-sections while manufacturing p-diffusion, contacts, and metal

Basic Fabrication Steps in a nutshell

- Though a mask transfer an "image" of the design to the wafer

- Do something to imaged parts of the wafer

  - Implant – add impurities to change electrical properties

  - Deposit – deposit metal, insulator or other layers

  - Grow Oxide – place silicon in oxidizing ambient

  - Etch – Cut into surface of topmost layer(s)

  - Polish – Make surface of wafer flat

- Strip 0ff imaging material (resist) and proceed to next step

Layout Design

- Chips are specified with set of masks

- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)

- Feature size f = distance between source and drain

  – Set by minimum width of polysilicon

- Feature size improves 30% every 3 years or so

- Normalize for feature size when describing design rules

- Express rules in terms of λ = f/2

  – E.g. λ = 0.3 μm in 0.6 μm process

Layout Design Rules

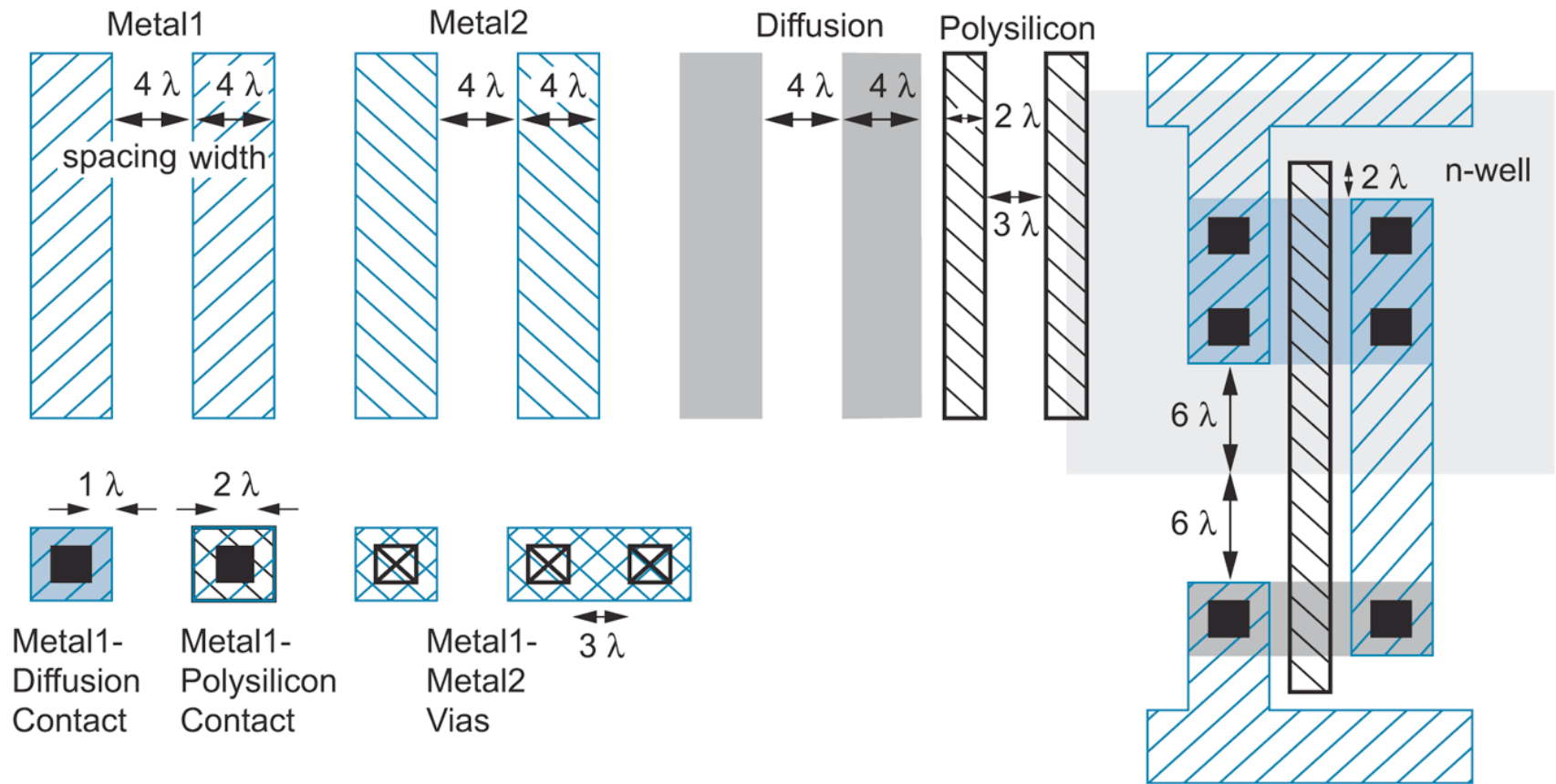Conservative rules to get started !

FIG 1.39 Simplified λ-based design rules *for layouts with 2-metal layers (MOSIS)*

Design Rules Summary

- Metal and diffusion have minimum width and spacing of 4λ

- Contacts are 2λ x 2λ and must be surrounded by 1λ on the layers above and below

- Polysilicon uses a width of 2λ

- Polysilicon overlaps diffusions by 2λ where a transistor is desired and has spacing or 1λ away where no transistor is desired

- Polysilicon and contacts have a spacing of 3λ from other polysilicon or contacts

- N-well surrounds pMOS transistors by 6λ and avoid nMOS transistors by 6λ

Logic Gates layout

- Layout can be very time consuming

- Design gates to fit together nicely

- Build a library of standard cells

- Standard cell design methodology
  - V_{DD} and GND should abut (standard height)
  - Adjacent gates should satisfy design rules
  - nMOS at bottom and pMOS at top
  - All gates include well and substrate contacts
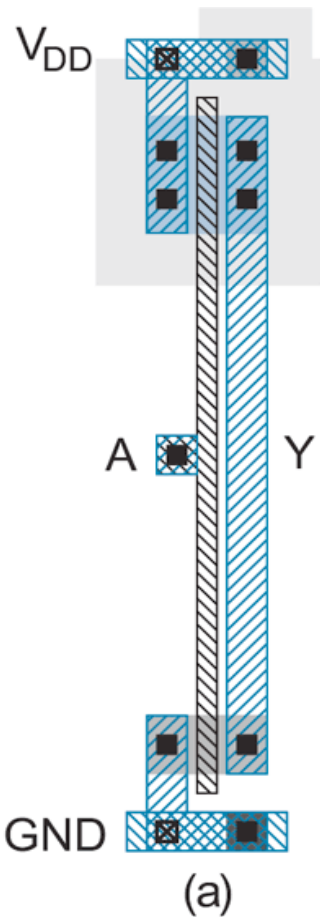
Inverter Layout

- Transistor dimensions specified as W / L ratio

- Minimum size is 4λ / 2λ, sometimes called 1 unit
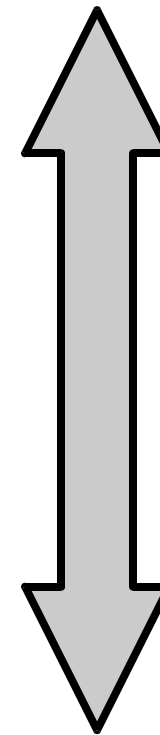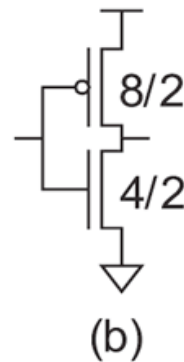
FIG 1.40 Inverter with dimensions labeled
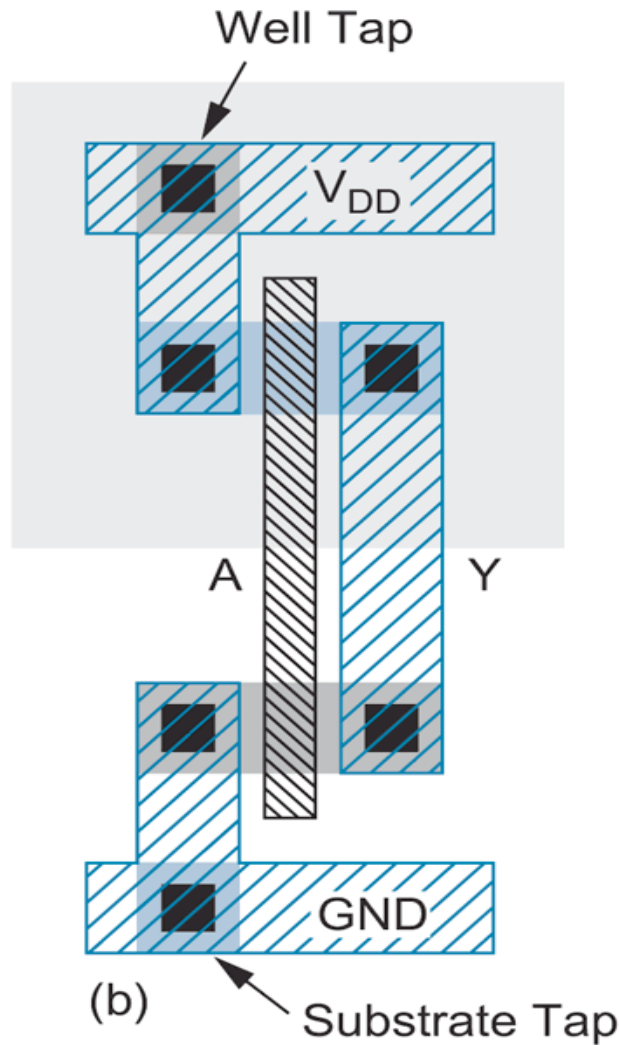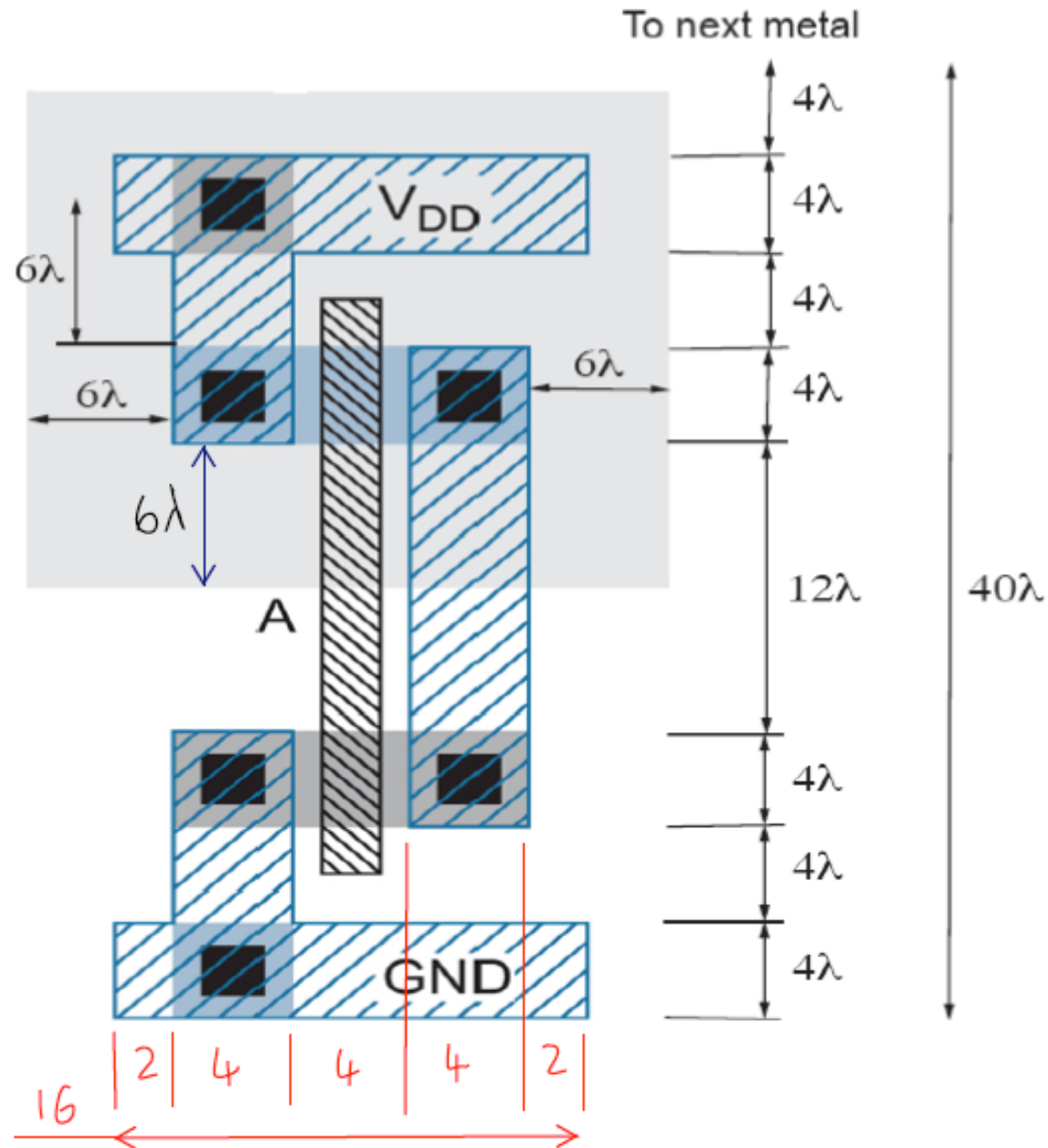
- In f = 0.6 μm process, this is 1.2 μm wide, 0.6 μm long

Inverter Standard Cell Layout

(b)

Well Tap

V_{DD}

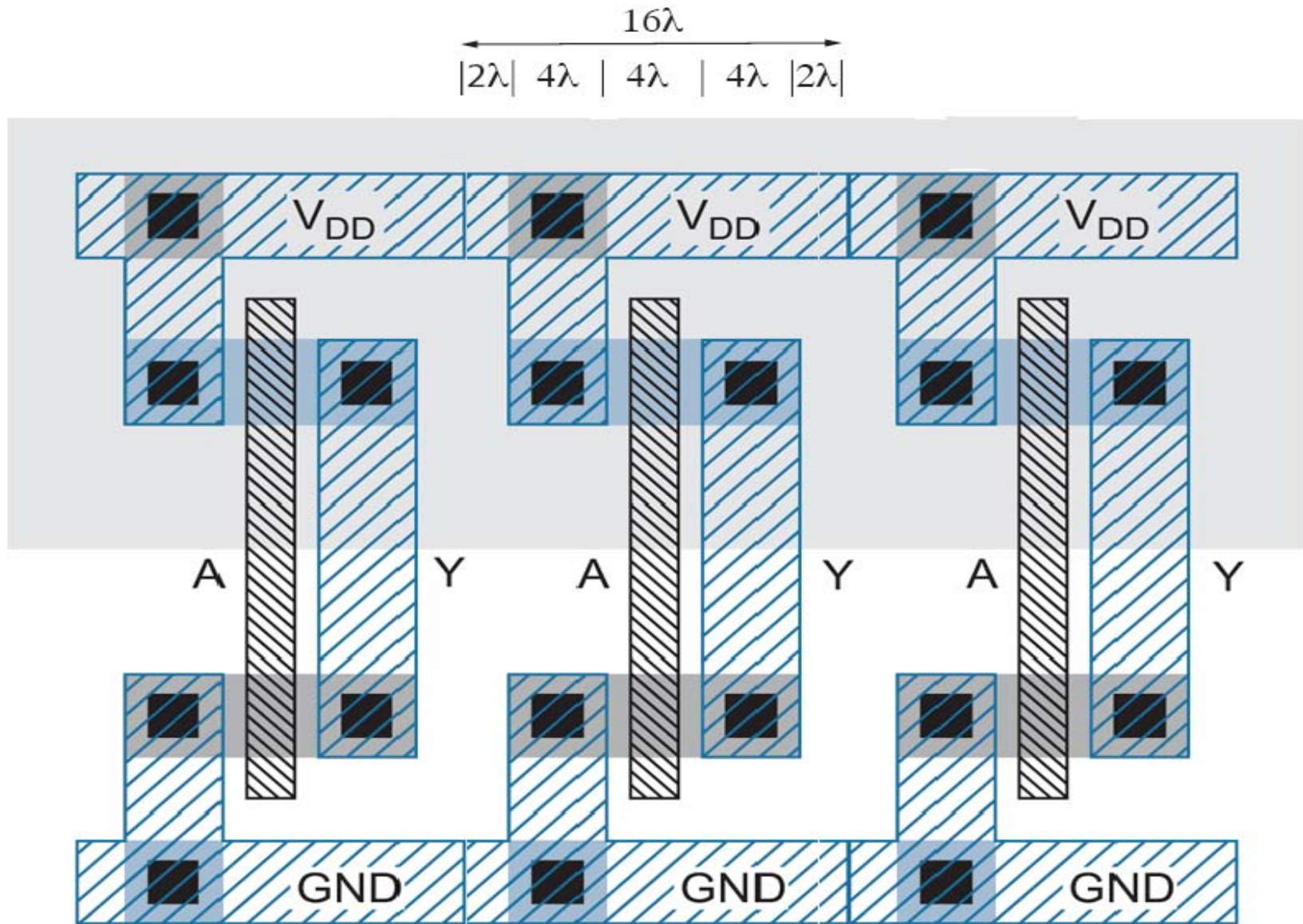A   Y

Substrate Tap

GND

Usually the pMOS has width 2 or 3 times the width of the nMOS

Inverter Standard Cell Area (1/2)

Inverter Standard Cell Area (2)

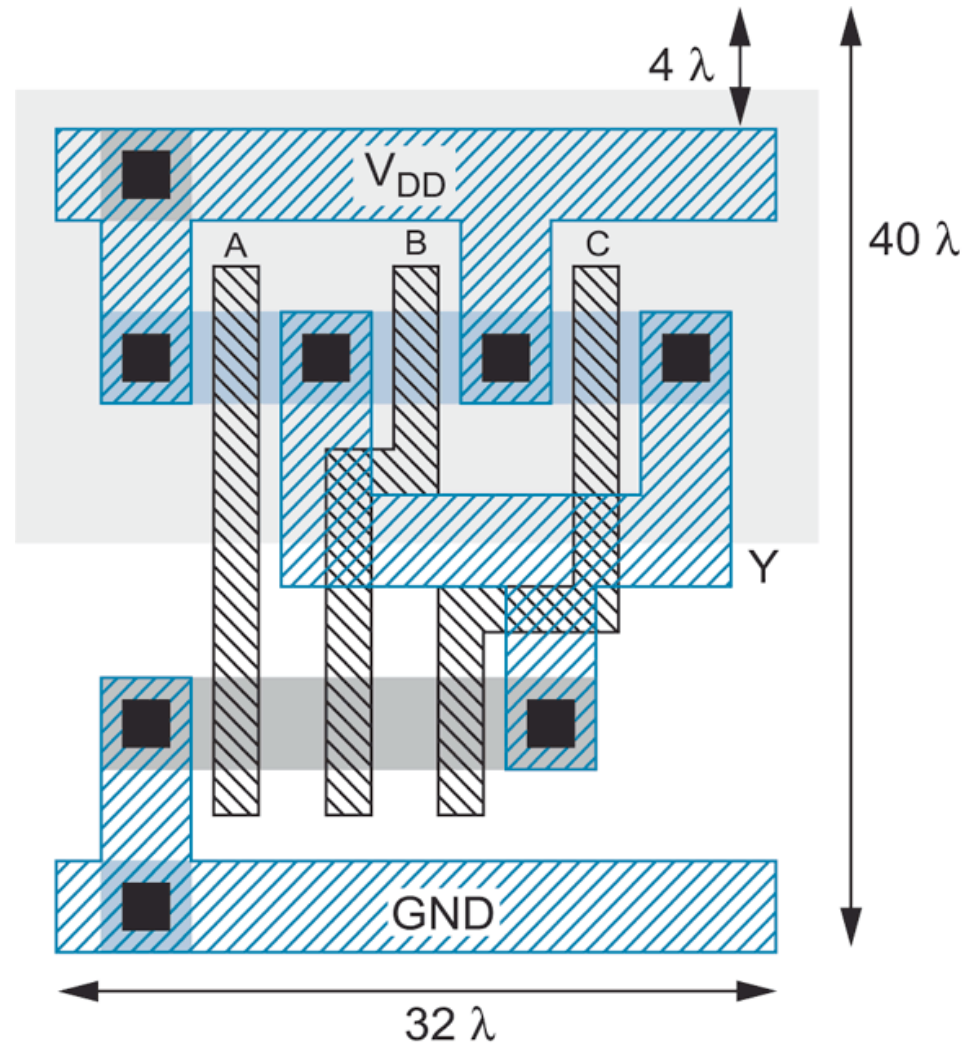Three abutted standard cell inverters

3-input Standard Cell NAND

FIG 1.42 3-input NAND standard cell gate layouts

35

Stick Diagrams

- **Stick diagrams** help plan layout quickly
  - Need not be to scale
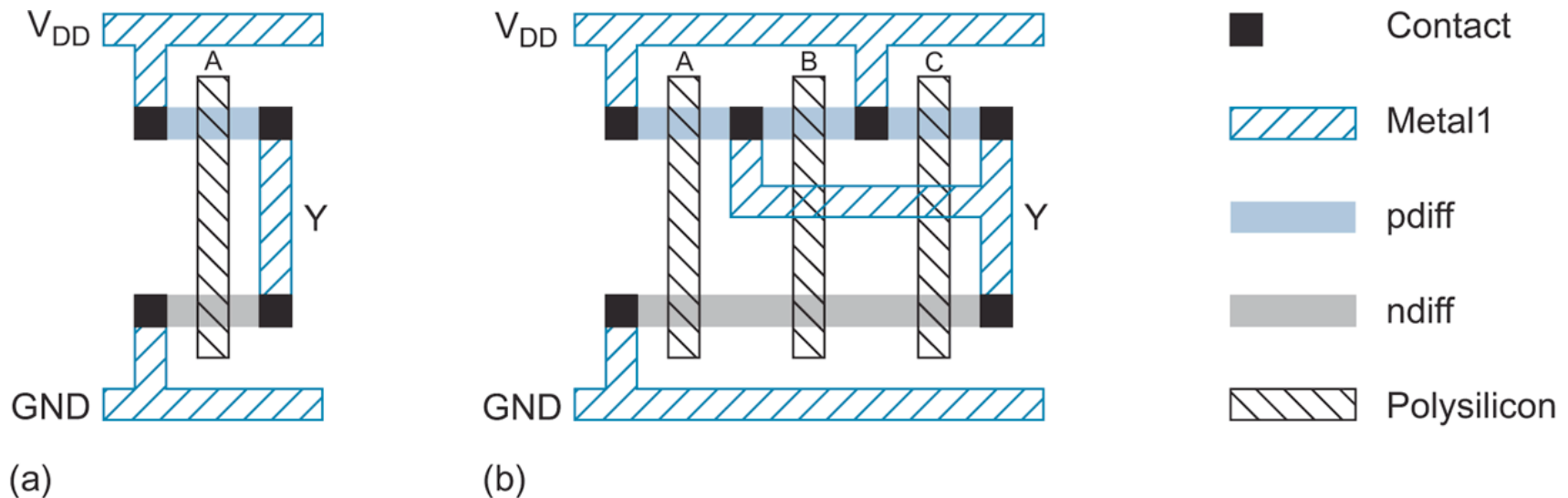 - Draw with color pencils or dry-erase markers

FIG 1.43 Stick diagrams of inverter and 3-input NAND gate. Color version on inside front cover.

36

Wiring Tracks

- A **wiring track** is the space required for a wire
  - 4λ width, 4λ spacing from neighbor = 8λ pitch
  - Transistors also consume one wiring track
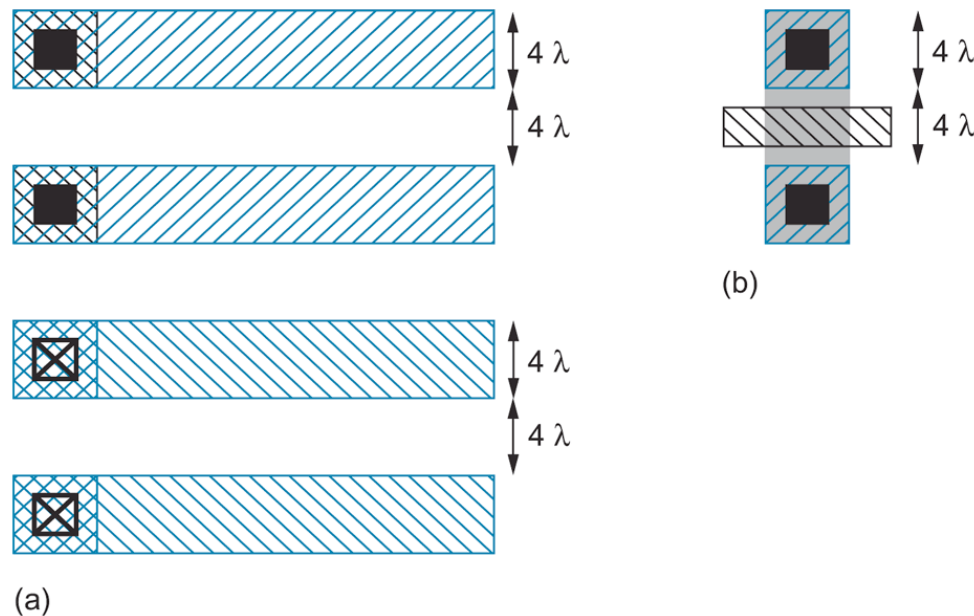

FIG 1.44 Pitch of routing tracks

Well Spacing

- Wells must surround transistors by 6λ
    - Implies 12λ between opposite transistor flavors
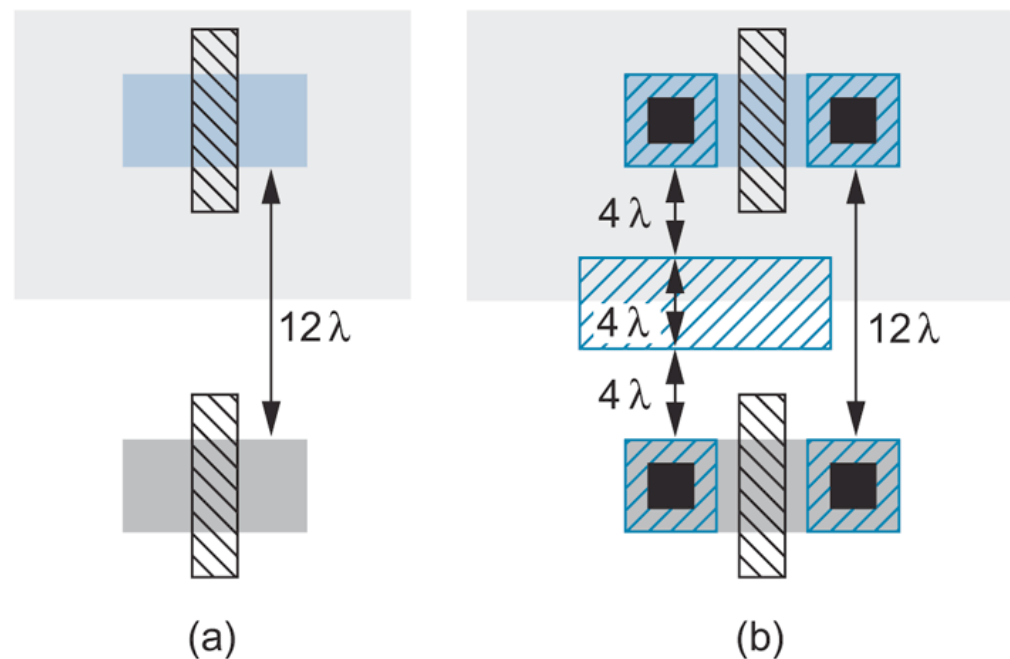   - Leaves room for one wire track

FIG 1.45 Spacing between nMOS and pMOS transistors

Area Estimation

Horizontal
4 × 8 = 32

Vertical
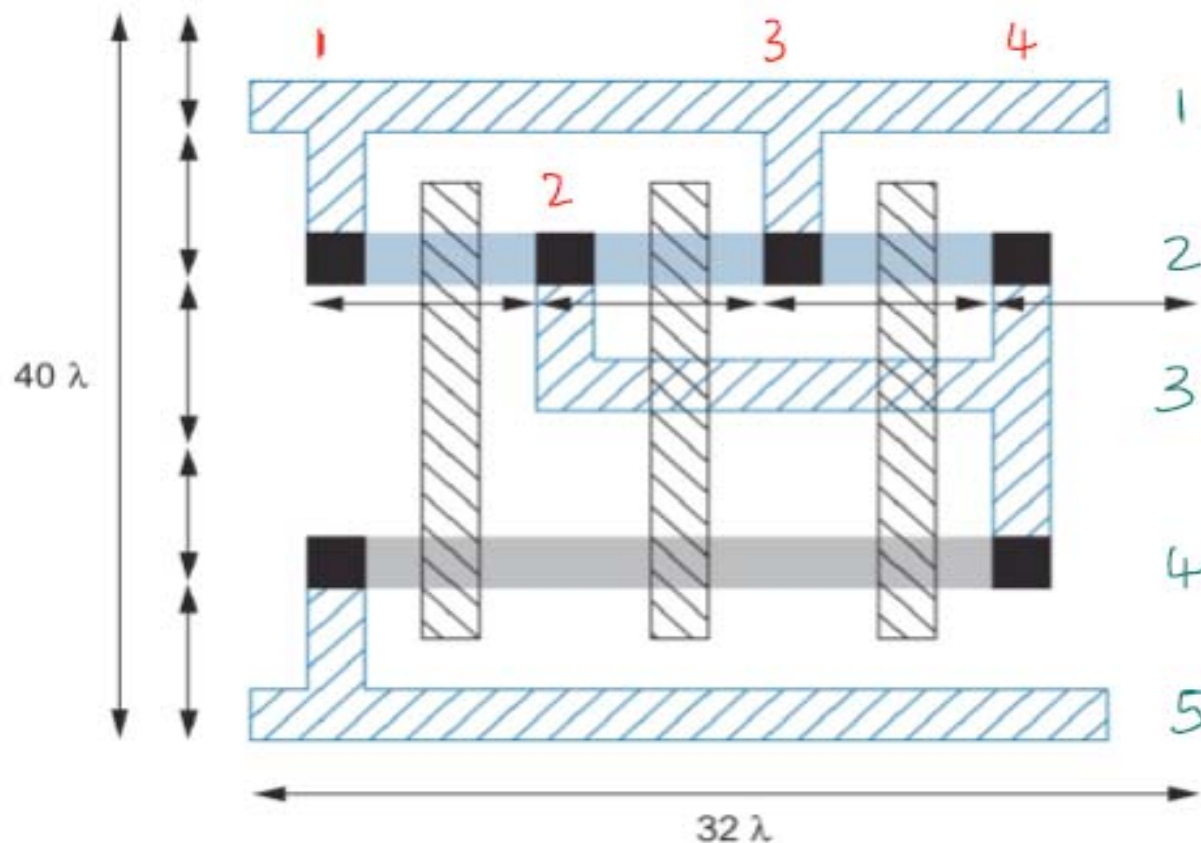5 × 8 = 40

- Estimate area by counting wiring tracks
    - Multiply by 8 to express in λ

FIG 1.46 3-input NAND gate area estimation