

Design Assignment 1

Zurizadae Soto Maya [1010229548]

Zarah Mathew [1009961720]

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I. Engineering Specification and Background Research

The objective of this design assignment is to sense load current using a low-side 0.1 Ω sense resistor and convert it into a voltage signal suitable for a microcontroller ADC to read. As voltage across the sense resistor is very small (0-0.35 V for 0-3.5A respectively), the signal must be conditioned before it can be accurately read. Hence, this conditioning requires two operations: amplification and offset shifting.

Op-amps prove apt for this function, as its primary purpose is to amplify a signal, making it easier for a microcontroller to read and process information. They are also useful for filtering and extracting specific frequencies while minimizing any noise that might be found on the signal. The following potential building-block circuits are considered:

1. Non-Inverting Amplifier

A non-inverting amplifier (Figure 1) outputs a signal that is in phase with the input voltage input signal and multiplies its amplitude by the gain determined by resistor ratios. Thus, output voltage is calculated as

$$V_{out} = Gain \times V_{in} \quad (1)$$

$$\text{where } Gain = 1 + \frac{R_{feedback}}{R_{ground}}$$

This op-amp provides the required gain to scale V_{sense} (0-0.35V) to nearly the full ADC range (0-3.3V). Its high input impedance prevents loading from the sense resistor and it has linear predictable scaling. However, it can not provide the 0.25V output offset alone so additional circuitry is required.

2. Summing Amplifier

A summing amplifier (Figure 2) produces a voltage output that is equivalent to the sum of two or more input voltages. In this application, the circuit can be utilized to add a constant 0.25V to the amplified signal, ensuring that V_{out} remains within the usable ADC range and avoids op-amp saturation. However, it is sensitive to resistor tolerances, as small deviations in resistance ratios can distort gain or offset.

3. Voltage Divider

A voltage divider reduces a large input voltage to a smaller, proportional output voltage. This configuration into the circuit can help reduce the voltage supply from 19V to 0.25V However, without buffering, divider accuracy may decrease and noise may be present in results through discrepancies.

Given these points, our chosen design approach intends to adapt these circuit blocks to amplify the voltage input and shift it to a correct baseline level. This approach meets the design goals while leaving us additional op-amps available for future filtering stages. Practical design considerations during iterations include single-supply operation, resistor tolerances, linear range with offset, and noise and sensitivity of components.

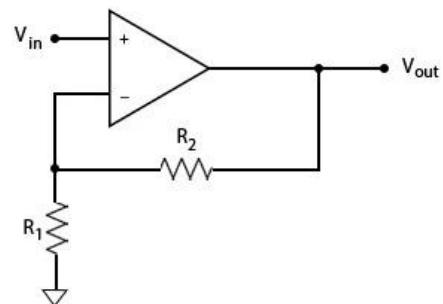


Figure 1: Non-Inverting Op-Amp [1]

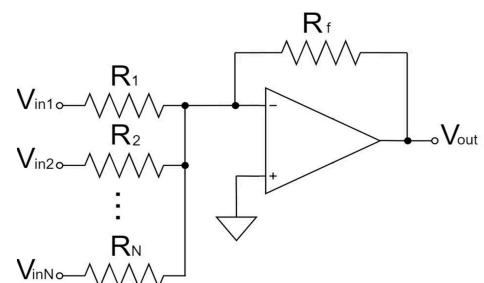


Figure 2: Summing Amplifier [2]

II. Candidate Design Iterations

Candidate 1: Two-Stage Non-Inverting Op Amps

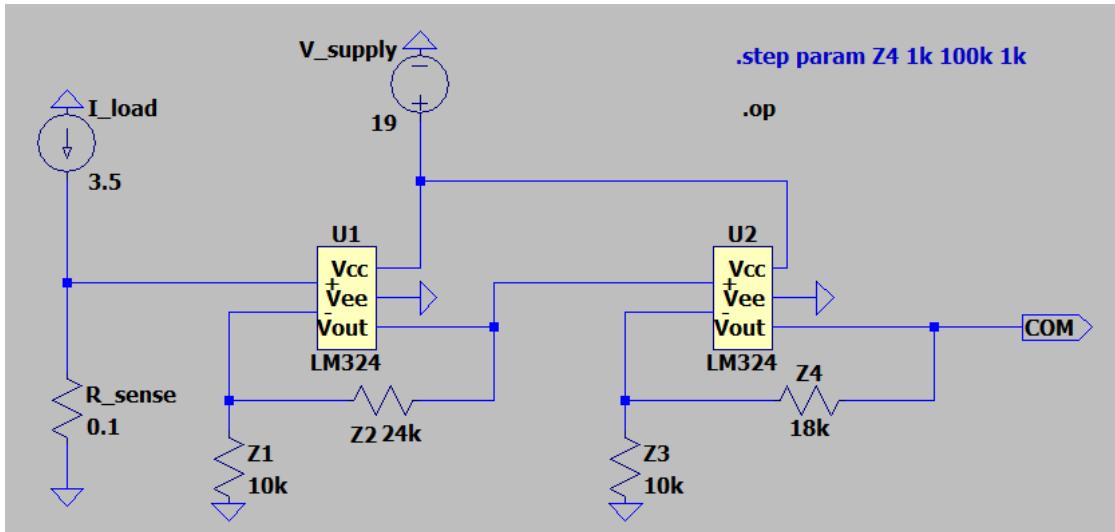


Figure 3: LTSpice Circuit Schematic of Candidate 1 Design

In this approach, we explored using two non-inverting op-amps in this circuit, as shown in Figure 3. The non-inverting topology was used to preserve the polarity and maximize the input impedance. Resistor values were found by fixing convenient reference resistances of $10\text{ k}\Omega$ and then solving standard non-inverting gain equations using nodal analysis. The stages are as follows:

- Stage 1 (Primary Non-Inverting Amplifier):* Amplifies the small voltage across the 0.1Ω sense resistor into a large range. The gain $A_1 = 1 + \frac{Z_2}{Z_1} = 1 + \frac{24k}{10k} = 3.4$.
- Stage 2 (Secondary Non-Inverting Amplifier):* Takes in the voltage to further scale the final output voltage. The gain $A_2 = 1 + \frac{Z_4}{Z_3} = 1 + \frac{18k}{10k} = 2.8$.

Thus, the total product gain $A = A_1 \times A_2 = 3.4 \times 2.8 = 9.52$.

$$\text{So, } V_{com} = 0.35 \times 9.52 = 3.33 \text{ V at } 3.5 \text{ A}$$

This design focused mainly on meeting the upper limit requirement of 3.3V at a maximum current of 3.5A and was assumed that the lower limits would fail into place naturally. This caused the offset of 0.25V to not be taken into account. Performing a DC Sweep confirmed that:

- When current = 3.5A, $V_{sense} = 0.35\text{V}$, $V_{out} = 3.33\text{V}$, satisfying one of the design goals and confirming the calculation above.
- When current = 0A, $V_{sense} = 1.01 \times 10^{-9}\text{V}$, $V_{out} = 0.03\text{ V}$ instead of the desired offset of 0.25V.

Adjusting resistor values in this circuit could not resolve this issue because the op-amp is powered by a single supply; with no additional voltage source, the output can not increase to produce the required offset.

Main Takeaway: While the circuit successfully handled the upper limit requirement, offset behaviour was not considered. This motivated a redesign to explicitly incorporate offset and meet the low-current output requirement.

Candidate 2: Single Summing Non-Inverting Op Amp with Buffer

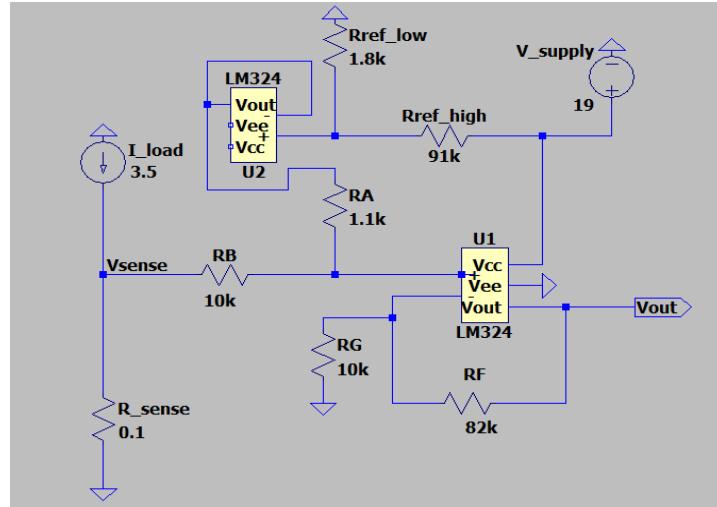


Figure 4: LTSpice Circuit Schematic of Candidate 2 Design

In this approach, we explored adding a buffer to a circuit and introducing a voltage divider as shown in Figure 4. To obtain the resistor values, we first defined the target gain as $A = 8.714$ (A_1) and offset as 0.25V. To obtain the resistor values, we first set the values of R_B , R_A and R_G to be $10\text{ k}\Omega$ and computed the value of R_F by $G = 1 + \frac{R_F}{R_G}$ which give us a value of $82\text{ k}\Omega$. From this, we calculated the values for R_{Ref_low} and R_{Ref_high} using the voltage divider equation to obtain the offset. (A similar math process as in A_1 is followed). The nearest standard values were picked and adjusted in LTSpice. The stages are as follows:

1. *Stage 1 (Voltage Divider + Buffer)*: A pair of resistors divided the 19V supply to create a 0.25V offset. The voltage is passed through an op-amp buffer to prevent loading effects.
2. *Stage 2 (Non-Inverting Amplifier)*: V_{sense} is amplified by a gain of 8.714 and summed with the buffered 0.25V reference, producing the required shifted output.

While this iteration addressed the offset, the circuit was highly sensitive to resistor ratios. A DC sweep revealed a “hockey-stick” shaped curve (Graph 1) as well rather than an expected straight line. When

- Current = 3.5A, $V_{sense} = 0.35\text{V}$, $V_{out} = 3.21\text{V}$
- Current = 0A, $V_{sense} = 988.16\text{ pV}$, $V_{out} = 13.71\text{ mV}$

This suggested that the offset was not properly set and was not maintained throughout. Additionally, tuning resistor ratios was time-consuming because of the interdependence between gain and offset in the selection of resistors.



Graph 1: Current vs V_{out}

Major Takeaway: While more robust than candidate 1, this design felt more complex than necessary and did not properly consider the offset.

III. Final Candidate Design

Final Candidate Design: Single Op-Amp Non-Inverting Summing Amplifier

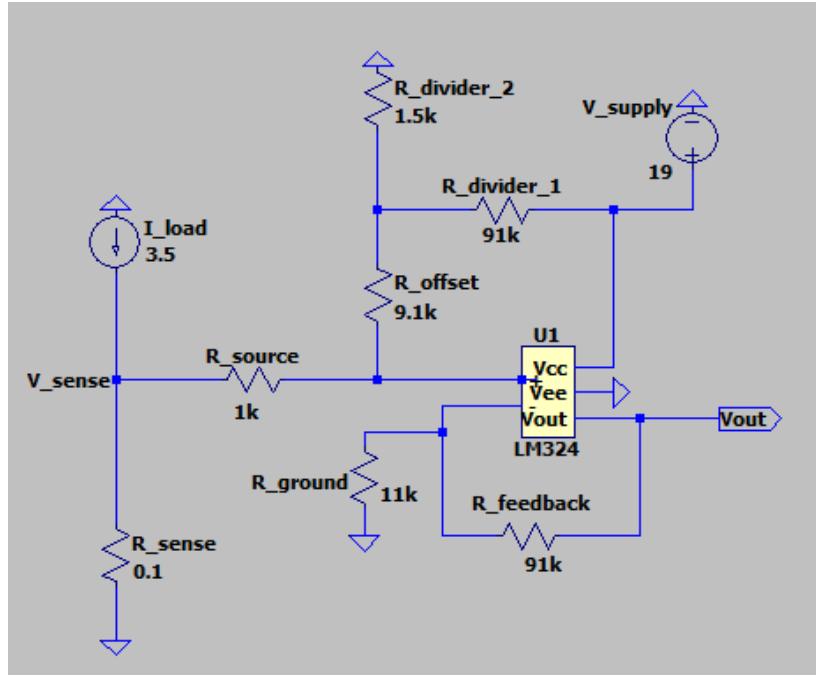


Figure 5: LTSpice Circuit Schematic of the Final Design

The final candidate design builds off of Design Candidate 2 where the buffer is removed as shown in Figure 5. Instead, a single op-amp solution is developed that achieves both amplification and offset in one stage. This minimizes circuit complexity, preserves components, and makes the design inexpensive. The final circuit consists of one LM324 op-amp, one DC current source, one 19V Voltage supply, and seven resistors. To obtain the values of the resistors, we did a mathematical analysis based on 4 main equations (A2). Further details of calculations are demonstrated in A1.

For this design, we were able to properly incorporate the offset. Compared to Design Iteration 2, we opted to eliminate the buffer, which gave more stability to our design and made it easier to determine the resistor ratio. Moreover, by eliminating the buffer, three op-amps are left free to use in future stages, especially for designing the filter, reducing the complexity of the circuit. This makes the signal path more direct, which can lead to fewer potential points of failure and a more straightforward analysis of the circuit, which will come in handy during the debugging process. Furthermore, the overall power consumption of the circuit is reduced, making it more efficient and cost-effective. The final design is simpler than candidate 2 and avoids the offset issue found in candidate 1. This design has 4 main stages:

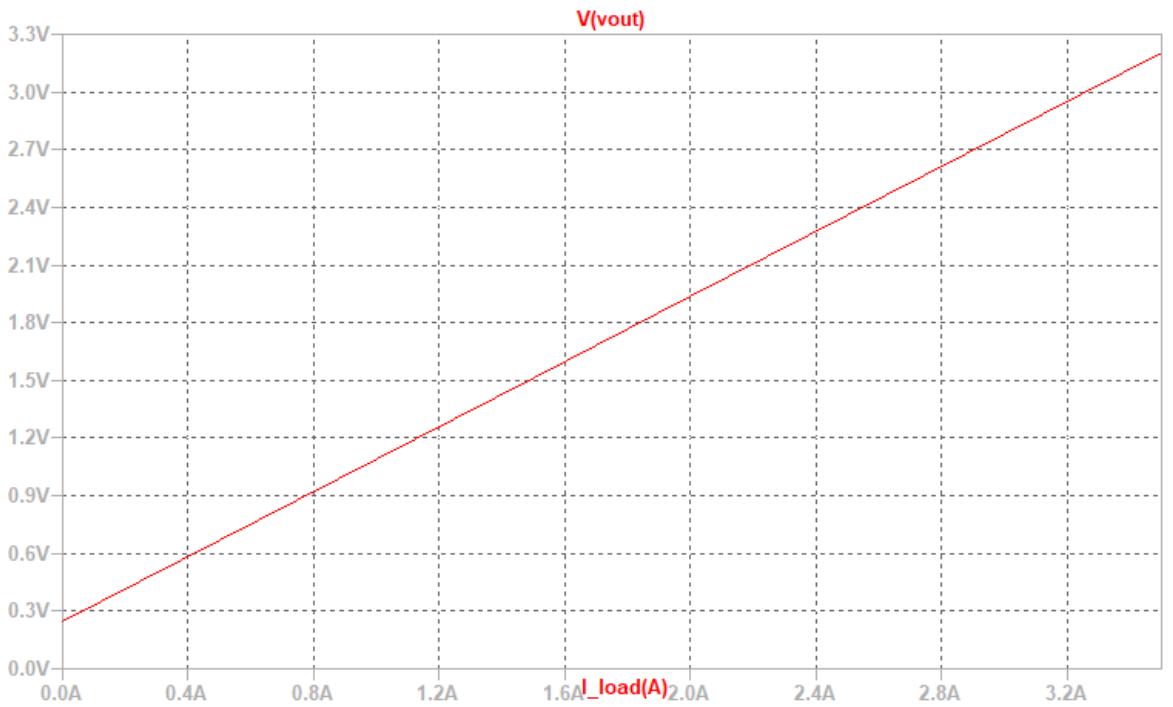
1. *Stage 1 (Current Source)*: The current source passes a load current through a small sense resistor $R_{sense} = 0.1 \Omega$ which is connected to ground, producing a voltage $V_{sense} = I_{load} \times R_{sense}$. At $I_{load} = 3.5A$, $V_{sense} = 0.35V$.
2. *Stage 2 (Input Network)*: The voltage across R_{sense} is passed through a $1 k\Omega$ resistor R_{source} directly to the non-inverting input of the op-amp, where it is combined with the voltage of the offset. This resistor serves as an input resistor and does not attenuate the signal significantly.

3. *Stage 3 (Gain & Feedback):* The op-amp is utilized as a non-inverting summing amplifier. Two resistors $R_{ground} = 11\text{k}\Omega$ and $R_{feedback} = 91\text{k}\Omega$ are connected to the inverting input of the op-amp to produce the closed-loop gain by the circuit according to

$$G = 1 + \frac{R_{feedback}}{R_{ground}} \approx 1 + \frac{91k}{11k} \approx 9.27$$

Therefore, the small voltage from R_{sense} is amplified, increasing V_{sense} into the required output range for V_{out} :

4. *Stage 4 (Voltage Divider):* To shift the output, a voltage divider is utilized to produce a reference voltage from the 19V supply ($R_{divider_1} = 91\text{k}\Omega$ and $R_{divider_2} = 1.5\text{k}\Omega$). This divider produces 0.31V. A resistor $R_{offset} = 9.1\text{k}\Omega$ supplies this voltage into the summing node of the op-amp's non-inverting input. This creates the DC offset so that at $I_{load} = 0\text{A}$, the output is near 0.25V instead of 0V.



Graph 2: DC Sweep Simulation of V_{out} vs I_{load} for Final Design Candidate

The simulation results displayed in Graph 2 indicate that the circuit produces a voltage output that is linearly related to the current load, which closely matches the values expected for the circuit given the input current. In comparison to Design Iteration 1, at 0 A, we have an offset ≈ 0.25 V. In comparison to Design Iteration 2, we have a more stable behaviour which suggests that the circuit can maintain a constant behaviour along the range of values making it more reliable.

I_{load}	Expected V_{sense}	Measured V_{sense}	% Error	Expected V_{out}	Measured V_{out}	% Error
0A	0V	2.66 μ V	0	0.25V	0.243 V	2.8
100mA	0.01V	10.06 mV	0.6	0.337V	0.328 V	2.7
1A	0.1V	100 mV	0	1.121V	1.09 V	2.8
3.5A	0.35V	350 mV	0	3.3V	3.21V	2.7

Table 1: Comparison of Measured and Expected V_{sense} and V_{out} across load current range

Table 1 shows the simulated performance of the final candidate design over the intended I_{load} . The measured V_{sense} is almost exact to the expected values by $\leq 0.6\%$ errors at all points. The measured output voltage also follows the expected values, but is consistently $\approx 2.8\%$ lower than the target across all test currents. This discrepancy is expected as we may not be able to get the exact resistor values as we calculated and had to get the closest standard resistors available. Given that the resistors have a 5% tolerance each, the observed error is within what would be predicted. In real-world circuit design, tighter tolerances may be more reliable in achieving the 0.25 V offset and a gain of 8.417. Despite this, the results still demonstrate that the circuit design is functional.

It is important to note that during the resistor calculation, while we were able to get V_{out} close to the expected value, some calculated values were not available as standard resistor components. Thus, resistor values had to be rounded up. Additionally, after simulating the circuit on LTSpice, we experimented with the values of the resistors and adjusted it accordingly to the DC sweep values to improve the accuracy of our design. This explains some of the discrepancies between the calculations and the actual resistors values (A3). The nearest resistor and capacitor standard values were used, which led to a slightly higher gain of 9.27 compared to the target gain of 8.417. This $\approx 10\%$ deviation is acceptable because the output falls within the design specifications. In real-world circuit design, exact resistor ratios are nearly impossible as standard component specifications and error tolerances need to be considered. Thus, selecting the nearest standard values and verifying our results through simulation ensures efficiency and feasibility of our design.

Overall, the single op-amp non-inverting summing amplifier as our final design candidate proves stable and efficient in meeting the design goals than both Candidate 1 and Candidate 2. The functional requirements are verified through LTSpice simulation, illustrating the effectiveness of this design approach.

IV. Sources

[1] Analog Device, Inc., <> Analog Devices Technical Glossary>>, Analog Devices, Inc.
<https://www.analog.com/en/resources/glossary/non-inverting-op-amp.html>

[2] Spiceman, <>Op-Amp Summing Amplifier circuit>>, Specimen, <https://spiceman.net/adder-circuit/>

V. Appendix

A1. Rough Math Derivations

From the design requirements, our transfer function must fulfill this equation:

$$V_{out} = A \cdot V_{sense} + V_{offset} \quad (1)$$

Where the total gain is defined by

$$A = \frac{V_{out, max} - V_{out, min}}{V_{sense, max} - V_{sense, min}} = \left(\frac{3.3 - 0.25}{0.35 - 0} \right) = 8.714 \quad (2)$$

$$V_{out} = 8.714 V_{sense} + 0.25 \quad (3)$$

Because, the design uses a non-inverting summing op-amp the total output voltage is defined [1] as

$$V_{out} = G \cdot V_{node(-)} \quad (4)$$

The total gain with respect to the desire gain can be defined by

$$A = G \left(\frac{R_{offset}}{R_{offset} + R_{source}} \right) \quad (5)$$

Note that in gain A the offset is taken into account, however we want to find the desire gain for the feedback loop

$$V_{offset} = G \left(\frac{R_{source}}{R_{source} + R_{offset}} \right) V_{div} \quad (6)$$

From these relationships and by selecting $R_{offset} = 10 k\Omega$ and $R_{source} = 1 k\Omega$

$$\frac{R_{offset}}{R_{offset} + R_{source}} = \frac{10 k\Omega}{10 k\Omega + 1 k\Omega} = 0.909 \quad (7)$$

$$\frac{R_{source}}{R_{source} + R_{offset}} = \frac{1 k\Omega}{10 k\Omega + 1 k\Omega} = 0.091 \quad (8)$$

We are now able to calculate the gain (G)

$$G = \frac{A}{0.909} = 9.586 \quad (9)$$

The values for $R_{feedback}$ and R_{ground} can be found by using the gain relationship for a non-inverting amplifier

$$G = 1 + \frac{R_{feedback}}{R_{Ground}} \quad (10)$$

$$\frac{R_{feedback}}{R_{Ground}} = 8.586 \quad (11)$$

Choosing $R_{feedback} = 10 k\Omega$

$$R_{feedback} = 85.86 k \quad (12)$$

According to assignment considerations, we select $R_{feedback} = 82 k\Omega$. Because this value changes, we have to recompute the gain value.

$$G = \frac{R_{feedback}}{R_{Ground}} + 1 = \frac{82}{10} + 1 = 9.2 \quad (13)$$

Using this “True” gain value, we can calculate the required the divider voltage (V_{div}) so we can obtain the desired offset

$$V_{offset} = G \left(\frac{R_{source}}{R_{source} + R_{offset}} \right) V_{div} \quad (14)$$

$$0.25 = 9.2 \left(\frac{1}{11} \right) V_{div} \quad (15)$$

$$V_{div} = 0.299 V \quad (16)$$

Using the voltage divider equation, we can obtain the required resistors to achieve this

$$V_{offset} = V_{supply} \left(\frac{R_{divider2}}{R_{divider1} + R_{divider2}} \right) \quad (17)$$

$$\frac{V_{div}}{V_{supply}} = \frac{R_{divider2}}{R_{divider1} + R_{divider2}} \quad (18)$$

$$\frac{0.299}{19} = \frac{R_{divider2}}{R_{divider1} + R_{divider2}} \quad (19)$$

Choosing $R_{divider1} = 91 k\Omega$

$$\frac{R_{\text{divider}2}}{91+R_{\text{divider}2}} = 0.0157 \quad (20)$$

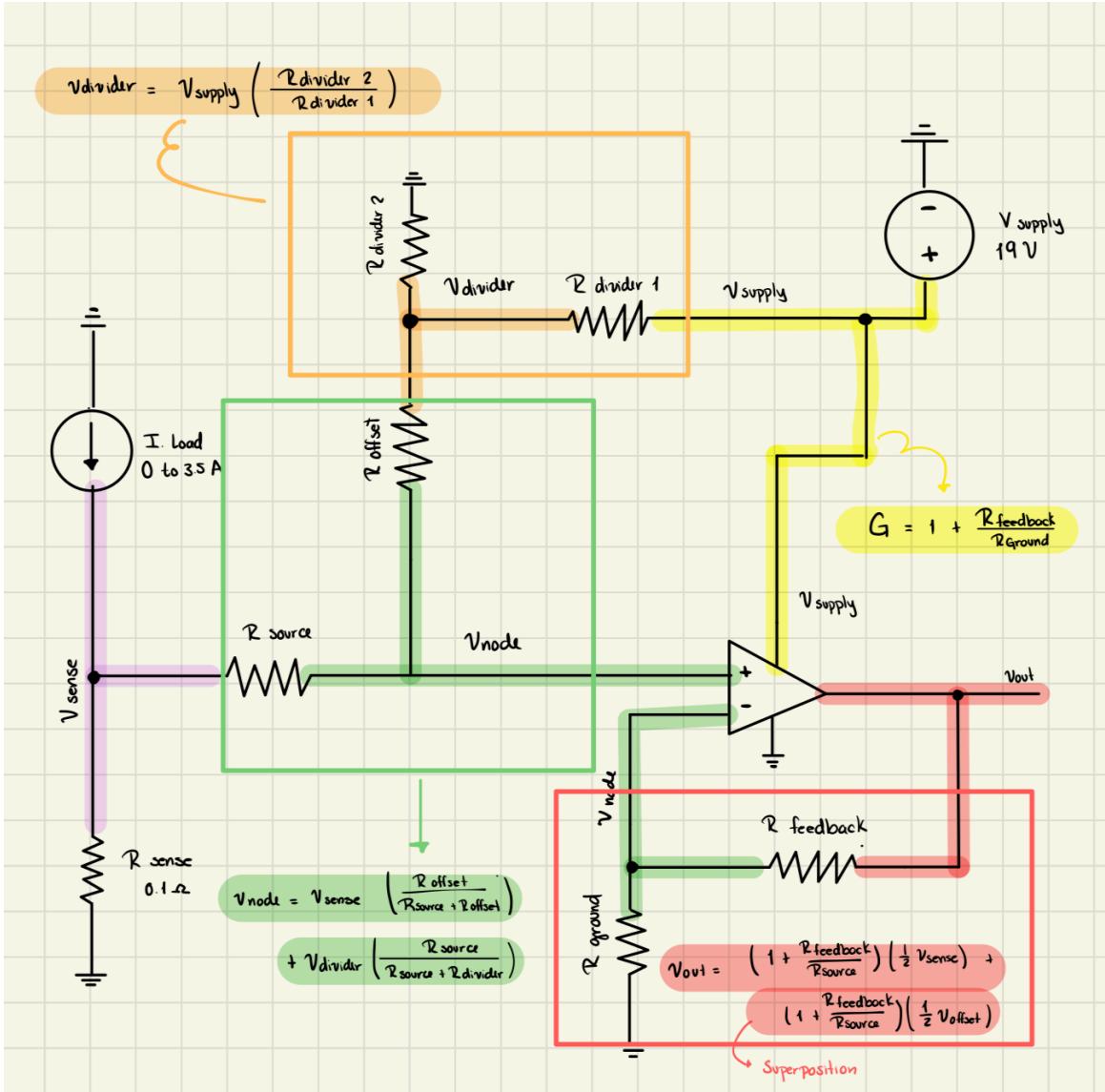
$$R_{\text{divider}2} = 1.45 \text{ k}\Omega \quad (21)$$

According to assignment considerations, we select $R_{\text{feedback}} = 1.5 \text{ k}\Omega$.

[1] OP-AMPS. 1995. [Online]. Available on:

<https://www.analog.com/media/en/training-seminars/design-handbooks/op-amp-applications/section1.pdf>

A2. Sketch Plan of Mathematical Analysis



A3. Resistors Calculated vs Circuit Value

Component	Calculated Value	Circuit Value
R_{Sense}	0.1 Ω (Given)	0.1 Ω (Given)
$R_{divider2}$	1.5 kΩ	1.5 kΩ
$R_{divider1}$	91 kΩ	91 kΩ
R_{Source}	1 kΩ	1 kΩ
R_{offset}	10 kΩ	9.1 kΩ
R_{ground}	10 kΩ	11 kΩ
$R_{feedback}$	82 kΩ	91 kΩ