Design Assignment 3

Zurizadae Soto Maya [1010229548]
Zarah Mathew [1009961720]

November 14th, 2025

I. Deliverable 1: Table of measured output voltage

I_{sense} (A)	$V_{expected}$ (V)	V_{out1} (V)	V_{out2} (V)
0.000	0.25	0.23	0.22
0.010	0.26	0.24	0.24
0.020	0.27	0.26	0.25
0.030	0.28	0.27	0.27
0.050	0.29	0.30	0.30
0.100	0.34	0.38	0.38
0.150	0.38	0.46	0.46
0.200	0.42	0.54	0.54
0.300	0.51	0.70	0.69
0.400	0.60	0.86	0.85
0.500	0.69	1.02	1.01
1.000	1.12	1.08	1.08
2.000	1.99	2.17	2.17
2.500	2.43	2.82	2.81
3.000	2.86	3.48	3.47
3.250	3.08	4.09	4.07
3.500	3.30	4.11	4.10

The measured unfiltered output V_{out1} ≈ measured filtered output V_{out2} and increases linearly with current, demonstrating that the circuit achieves its intended linear voltage-current behaviour. This confirms a correct candidate design and functional PCB construction. Additionally, the amplifier reproduced the intended expected values for voltage. It is important to note that at low currents (0-1A), the measured and expected values match within a 5-10% tolerance whereas for high current (2-3.5A), the measured voltage is consistently higher than the expected voltage. This can be due to the following:

1. **Resistor Tolerances of 5%:** The amplifier gain is set as G = 1 + $\frac{R_f}{R_f}$. Since all the resistors have a ±5% tolerance, the actual gain ratio deviates from the ideal value. For

example, for the first stage of our circuit, we measured 89.7kΩ instead of 91kΩ and 10.7k Ω instead of 11kΩ. Additionally, the measured R_{sense} is 0.11Ω compared to the ideal 0.1Ω allowing the amplifier to perceive more current than what was actually passing through, creating an upward shift in output voltage.

2. **Different Capacitor Value:** Our design in the low-pass filter used a 15nF capacitor, but we were given a 12nF capacitor. While this does not majorly cause any discrepancies, it contributes to small discrepancies between measured output V_{out1} and V_{out2}.
3. **Power Supply Variability:** The power supply provided fluctuating voltage (18.7V ~ 19.4V), possibly introducing variations in output and introducing noise.
4. **Possible Thermal Drift:** At higher currents, the components and nearby PCB copper may have warmed up, resulting in increased deviation in the data. This can also explain the shape of the graph towards higher current.

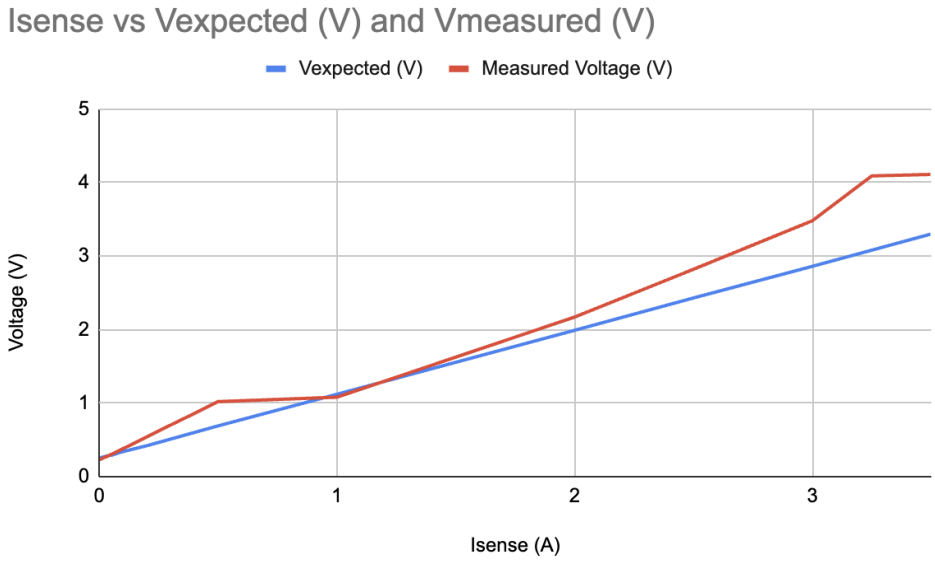
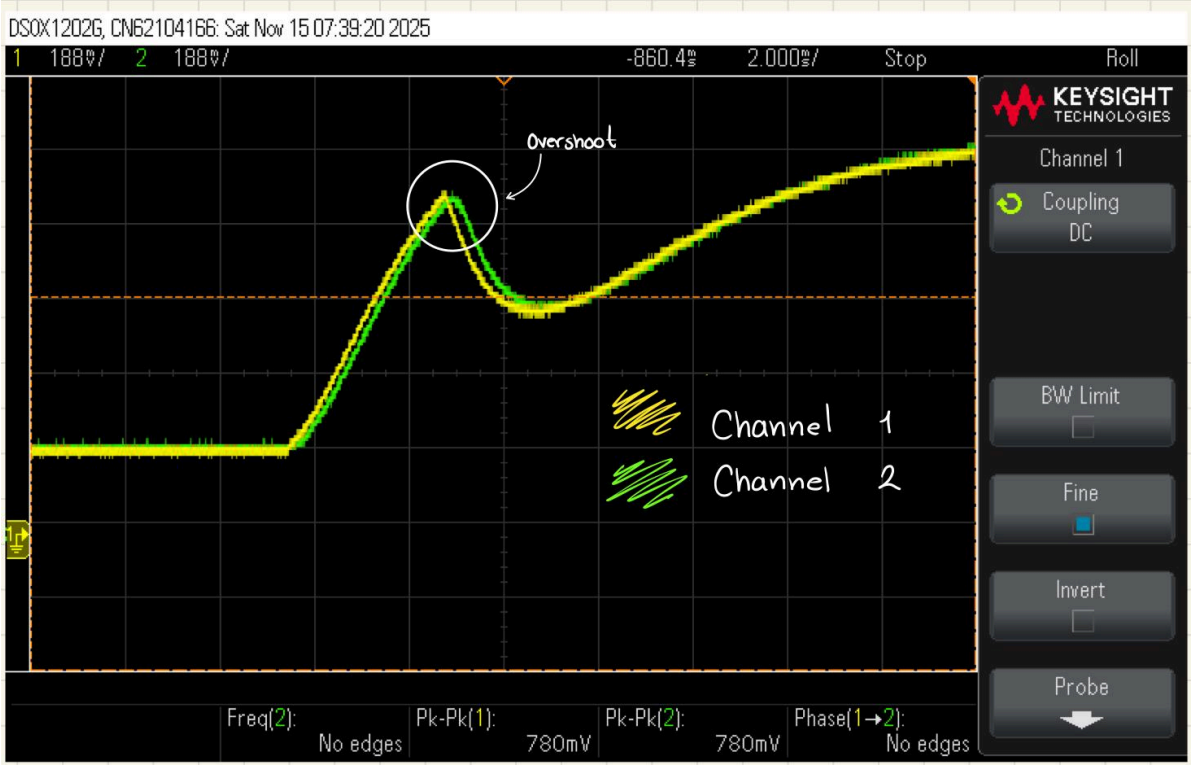


Figure 1: Linear Relationship between I_{sense} and measured voltage

Overall, the PCB functions correctly, and the observed errors fall within the expected component tolerances.

II. Deliverable 2: Comparison of non-filtered vs filtered output



The image above compares the unfiltered (V_{out1}) and the filtered (V_{out2}) output from our PCB.

- Channel 1(Yellow) shows the unfiltered output (V_{out1})
- Channel 2 (Green) shows the filtered output (V_{out2})

As it can be seen, the unfiltered signal has a high frequency response which has a sharp overshoot and a drastic decay. The filtered signal (Green) has a smoother change, where there are not any visible sharp values, creating a much more stable response. This indicates that our filtering is actually working, as the overshoot seen on the unfitter signal is removed.

III. Deliverable 3: Soldered PCB Images

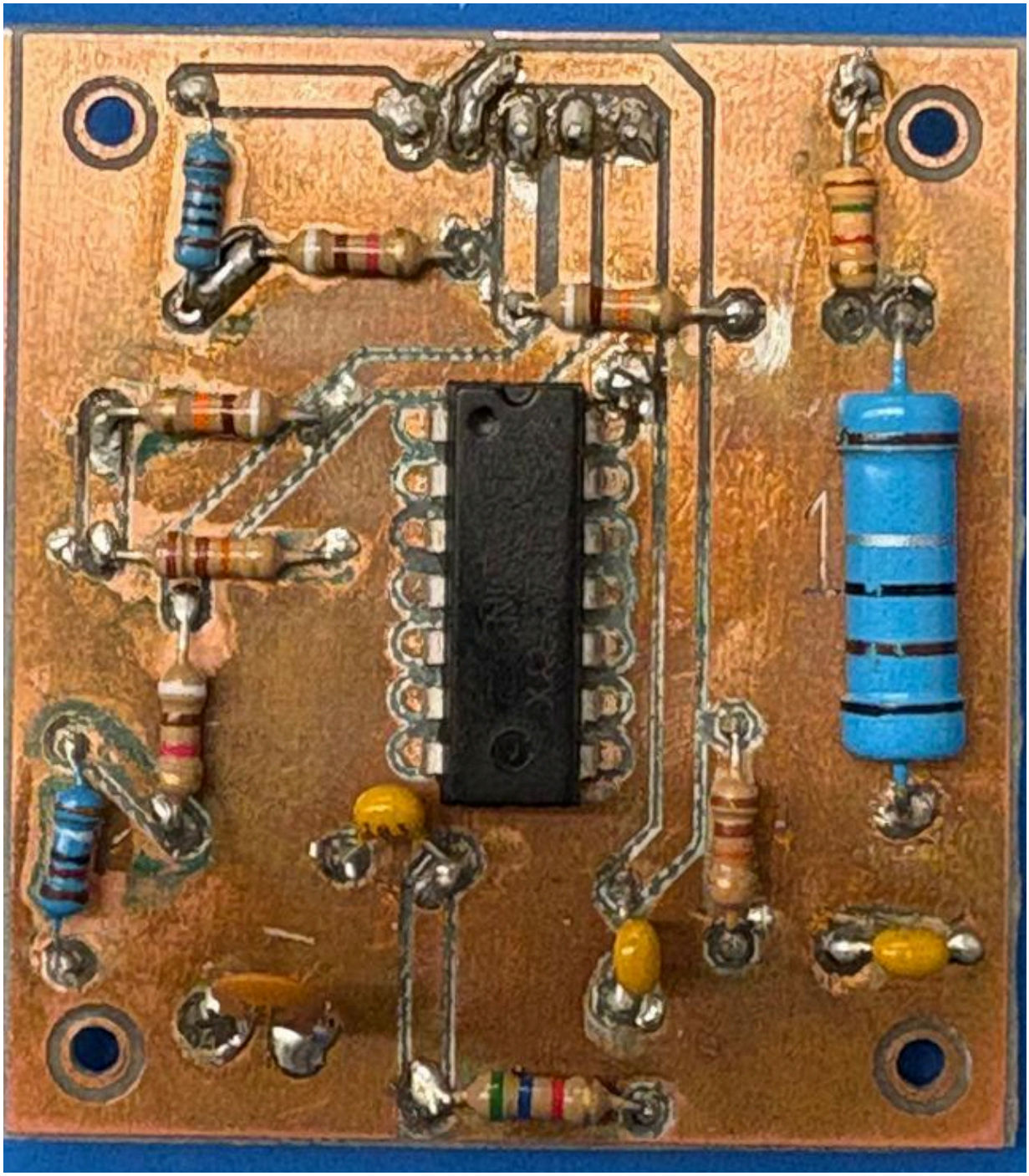


Figure 2: Top View of PCB

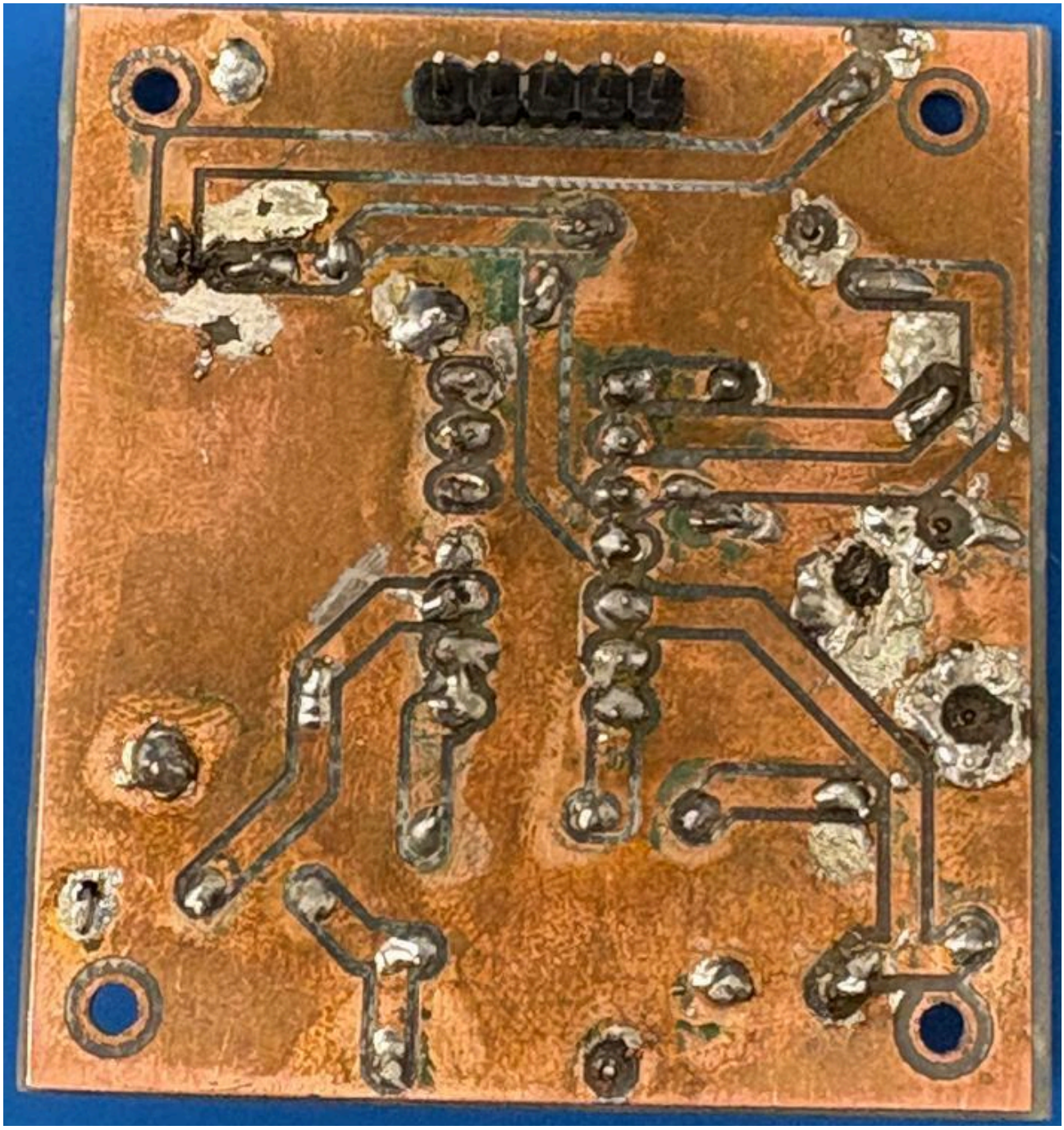
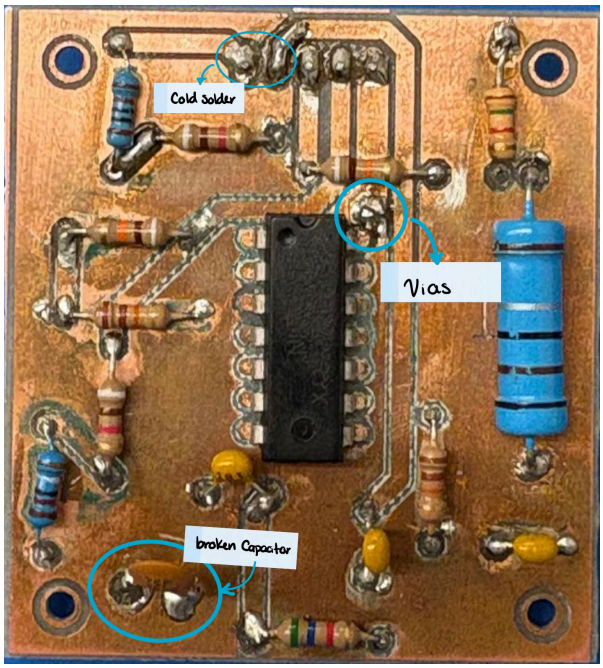


Figure 3: Bottom view of PCB

Our PCB contains one via which is connected by soldering wires through the board. The main issues during testing that we found were due to soldering issues.

Description of main issues	Annotated PCB
• The I_{sense} and V_{out1} pins had cold solder joints, preventing current from flowing through these connections. This was resolved to restore proper electrical continuity. • The capacitor on the lower left broke while testing. Repairments were made by soldering additional legs to extend its lead and then reinstalled securely on the PCB.	
• Some areas on the bottom side of the PCB were overheated during soldering, thus, got burned. This caused the copper pour to lift and prevent soldering. While this did not affect the majority of the PCB because no critical traces were connected in this region, one trace on the top left was affected. The component lead was bent to reach an intact trace and soldered to restore connectivity. • Several bridges were found on the PCB, creating short circuits and prevented V_{out1} to receive the signal. These bridges were removed with a solder wick and pump.