

1. 00110101 11001010

a) To clear all odd bit positions to 0, we must AND with 01010101 01010101:

$$00110101 \quad 11001010 \quad \text{AND} \quad 01010101 \quad 01010101 =$$

$$00010101 \quad 01000000$$

b) To set the rightmost 4 bits to 1, we must OR with 00000000 00001111:

$$00110101 \quad 11001010 \quad \text{OR} \quad 00000000 \quad 00001111 =$$

$$00110101 \quad 11001111$$

c) To complement the most significant 8 bits, we must XOR with 11111111 00000000:

$$00110101 \quad 11001010 \quad \text{XOR} \quad 11111111 \quad 00000000 =$$

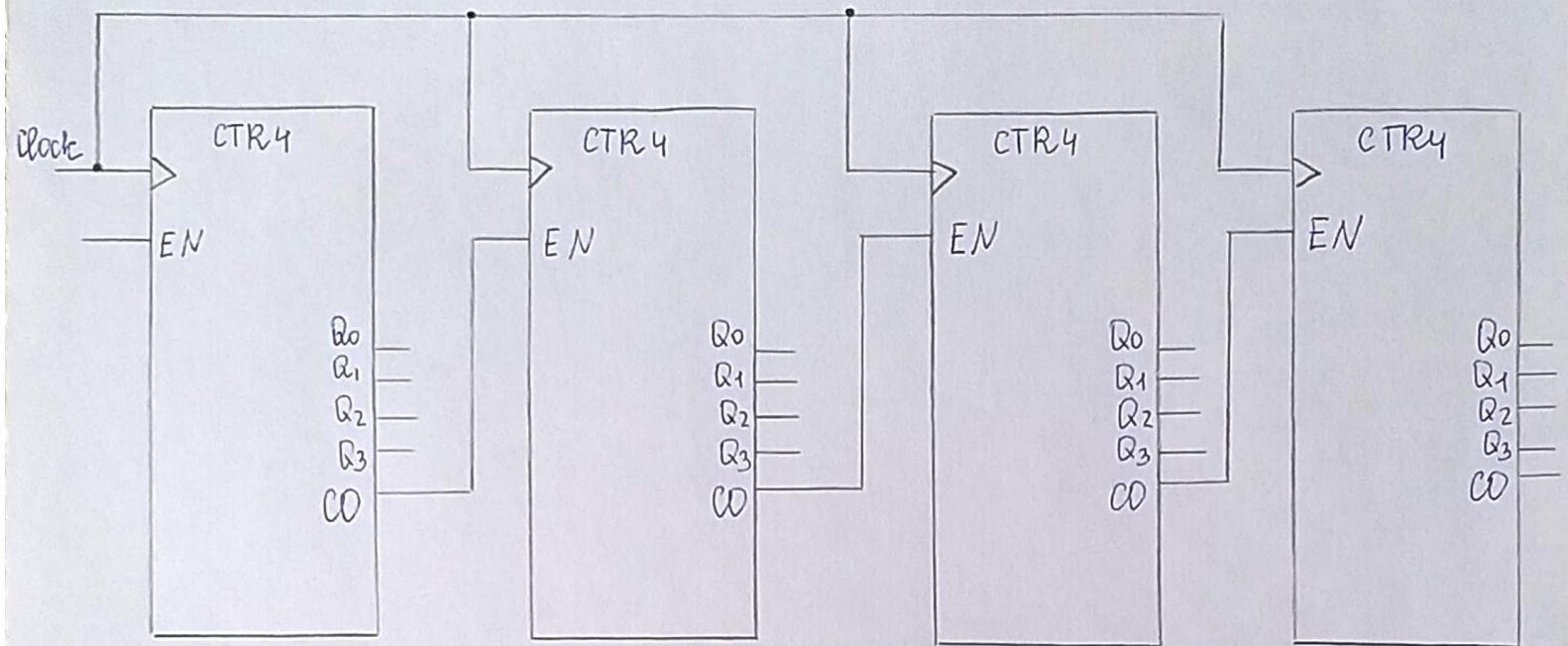
$$11001010 \quad 11001010$$

2. 11001010

Shift left: 10010100

Shift right: 01100101

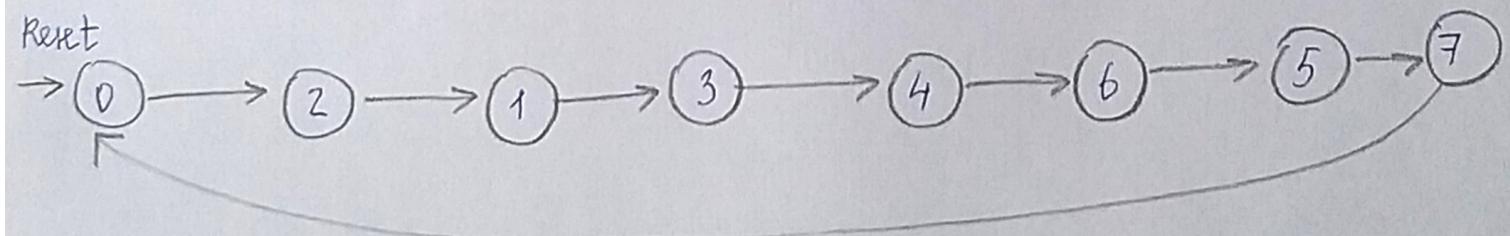
3.



The maximum number of AND gates in a chain that a signal must propagate through is 4: one AND gate for each 4-bit parallel counter

4. D, 2, 1, 3, 4, 6, 5, 7

State diagram:



State table:

Current state			Next state		
A(t)	B(t)	C(t)	A(t+1)	B(t+1)	C(t+1)
0	0	0	0	1	0
0	0	1	0	1	1
0	1	0	0	0	1
0	1	1	1	0	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	0	0	0

Inputs: A, BC

Outputs: B

$$\mathcal{D}A = A\bar{B} + A\bar{C} + \bar{A}BC$$

Inputs: A, BC

Outputs: B

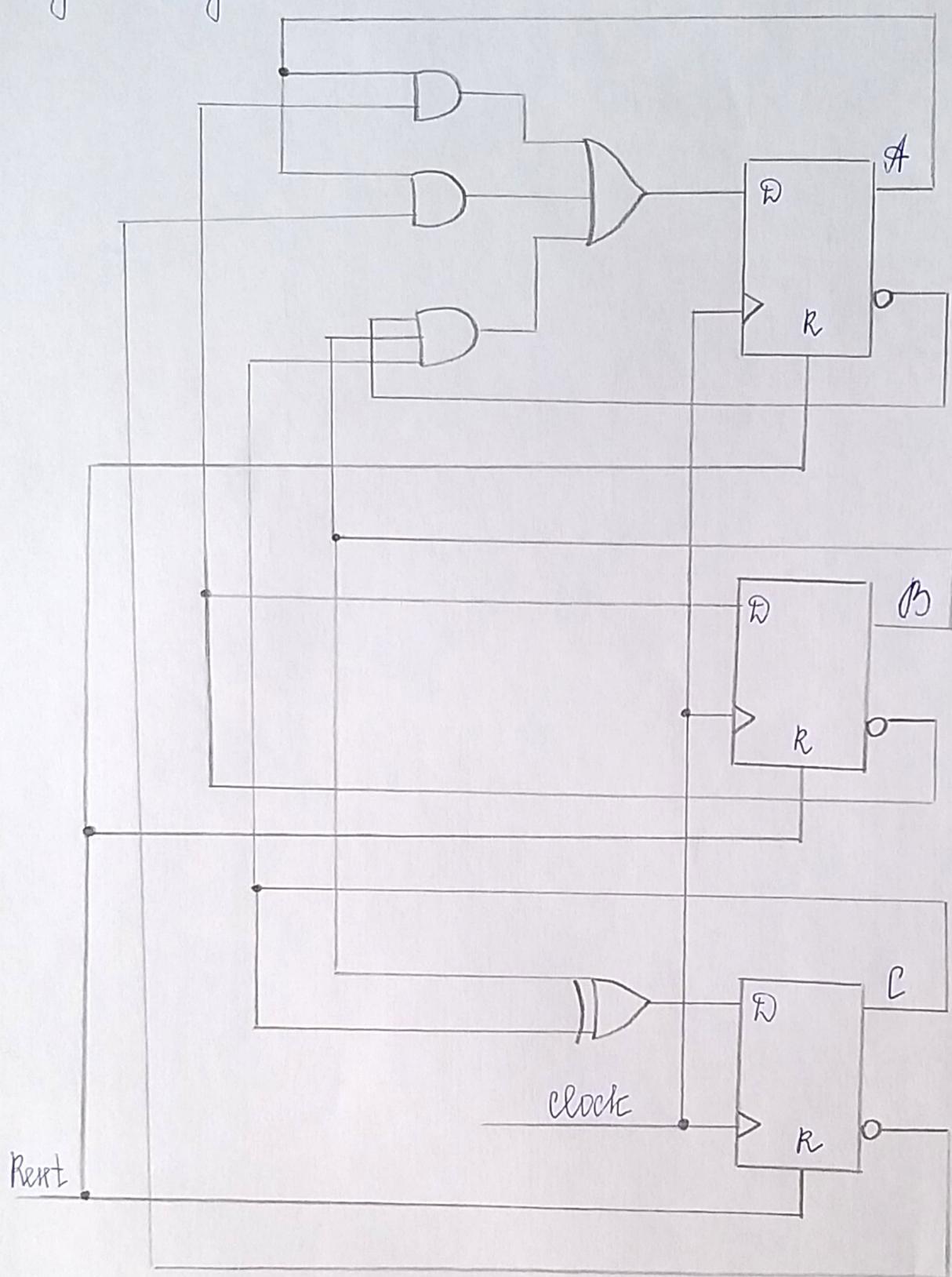
$$\mathcal{D}B = \bar{B}$$

Inputs: A, BC

Outputs: B

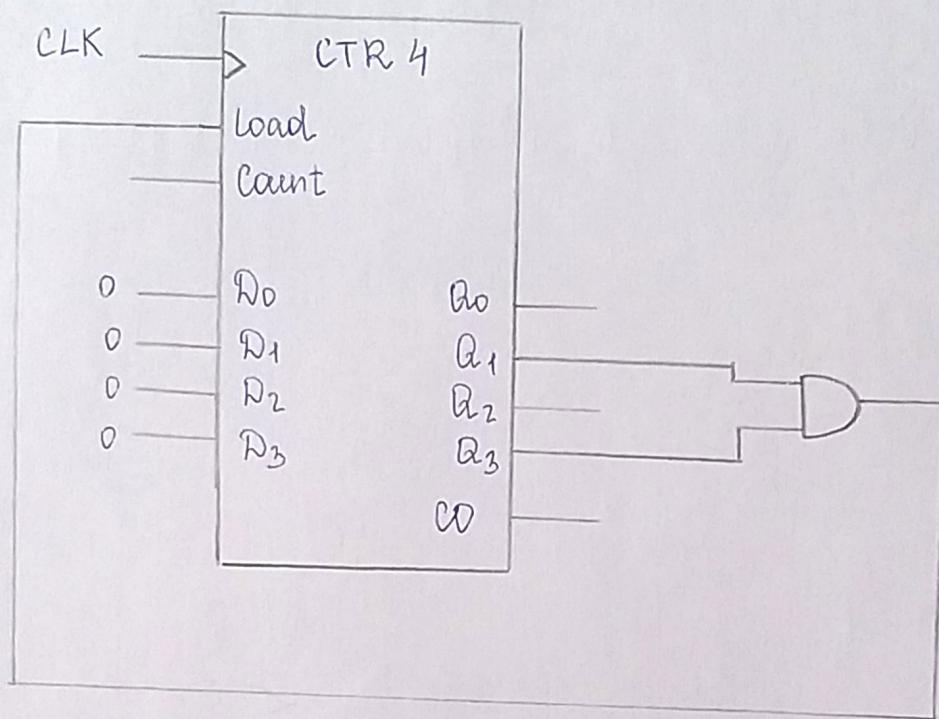
$$\mathcal{D}C = \bar{B}\bar{C} + B\bar{C} = B \oplus C$$

Logic diagram:

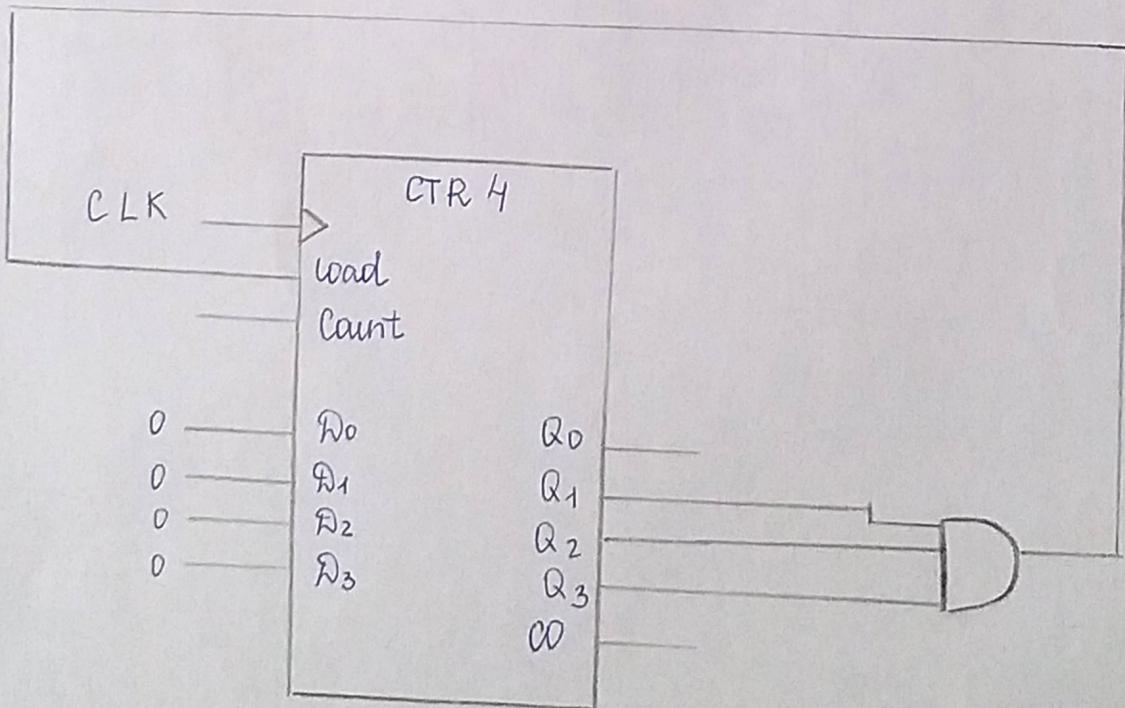


5.

a) from 0000 to 1010



b) from 0000 to 1110



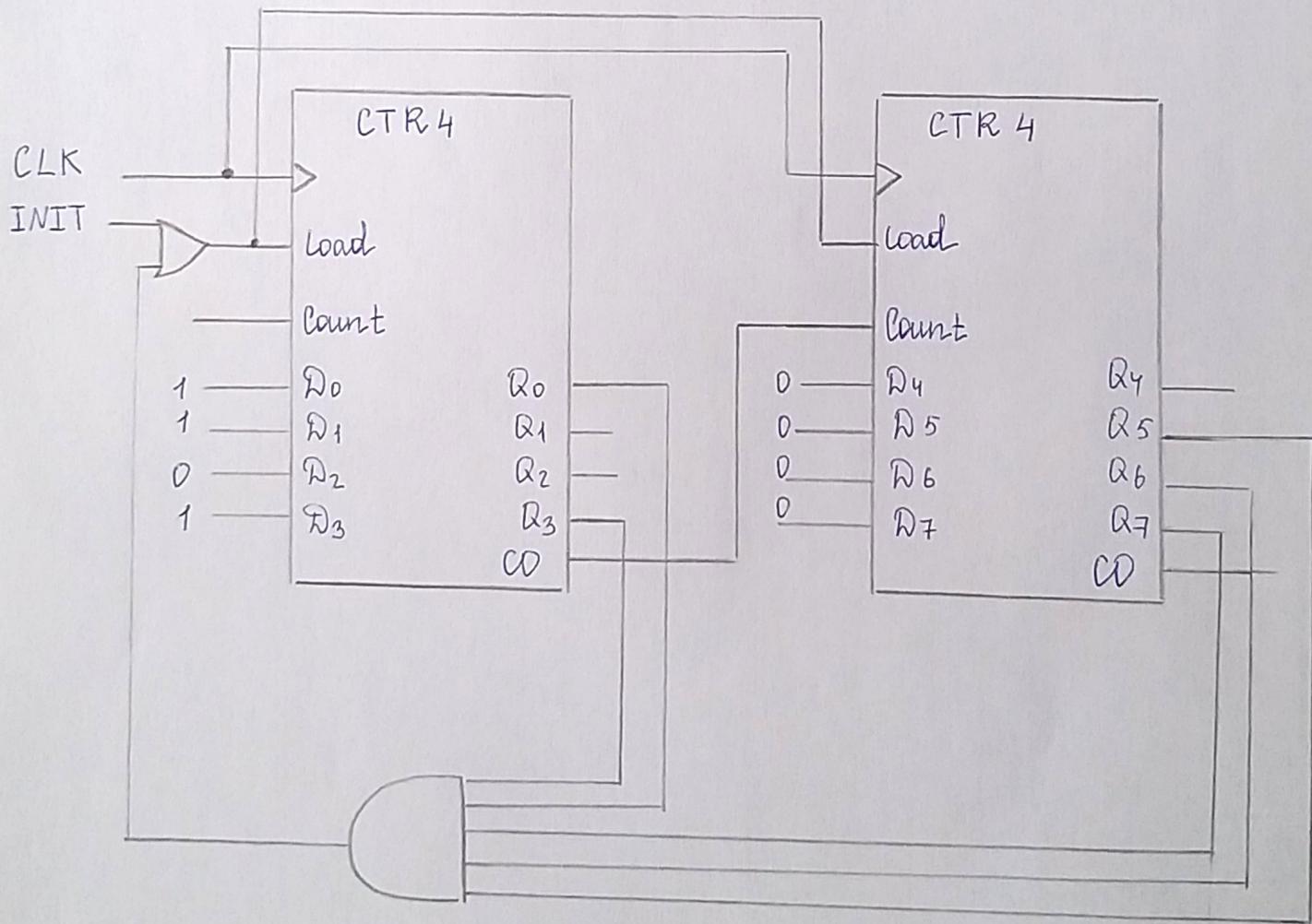
6. from 11 to 233

$$233 = 128 + 64 + 32 + 9$$

$$(233)_2 = (128)_2 + (64)_2 + (32)_2 + (9)_2 = 10000000 +$$

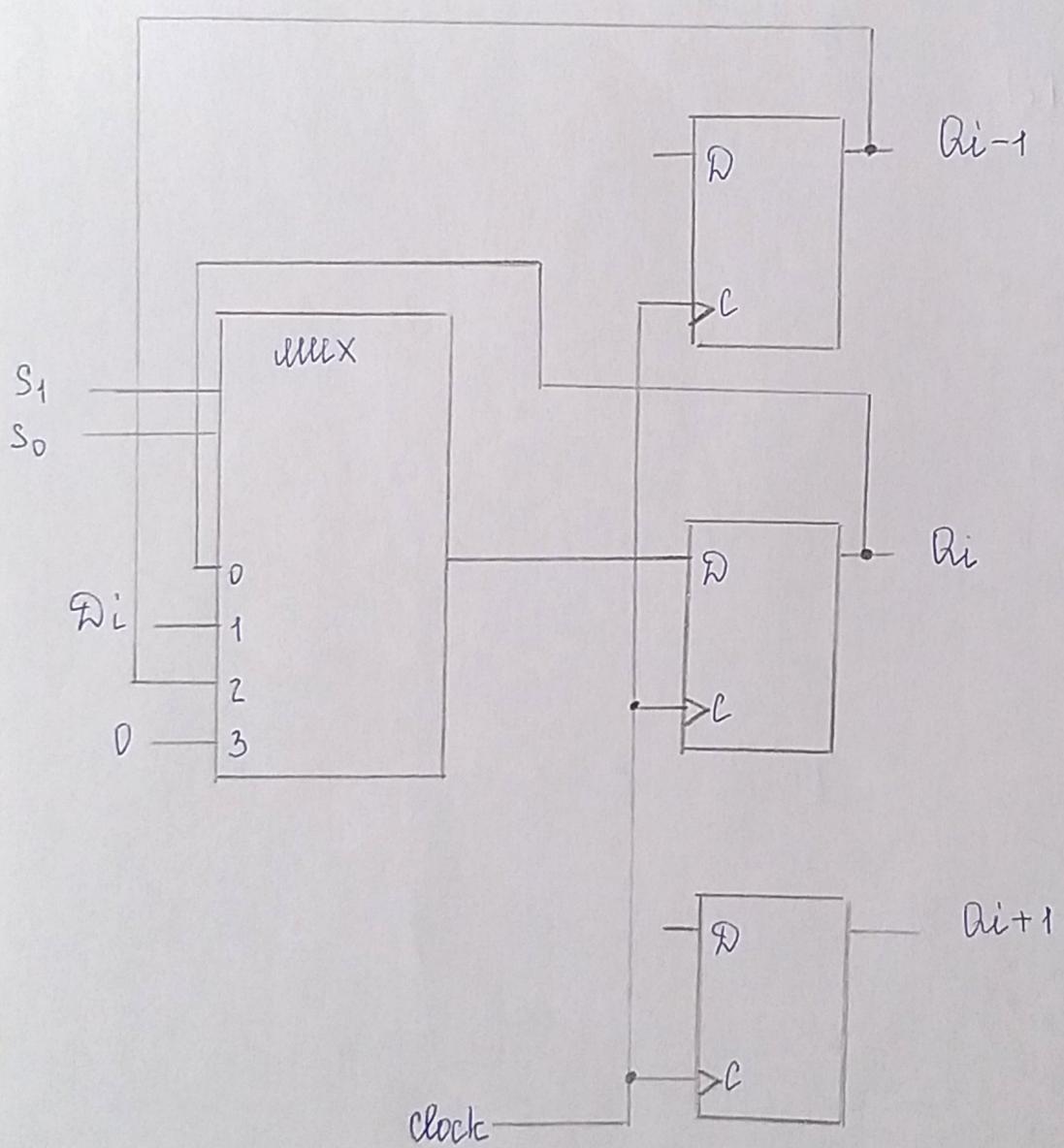
$$1000000 + 100000 + 1001 = 11101001$$

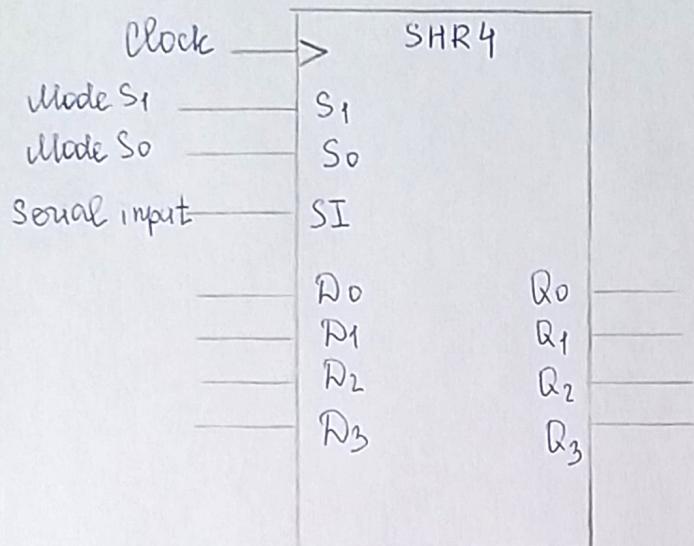
$$(11)_2 = 00001011$$



7.

S_1	S_0	Register operation
0	0	no change
0	1	load parallel data
1	0	shift down
1	1	clear register to 0



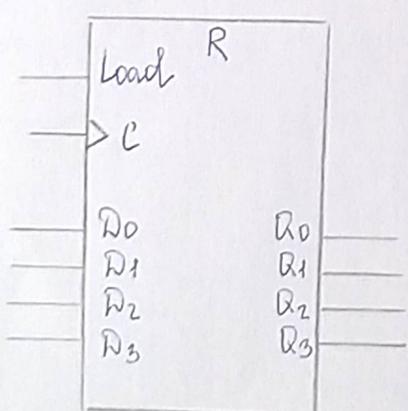


$$8. \quad C_0 : R_2 \leftarrow 0$$

$$C_1 : R_2 \leftarrow \bar{R}_2$$

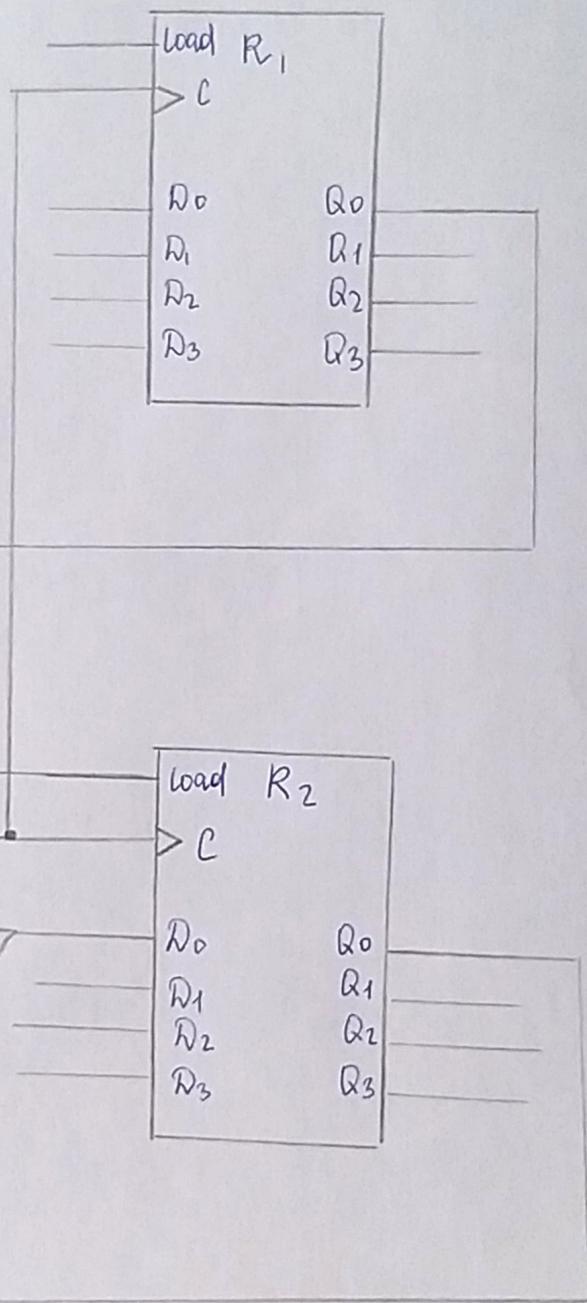
$$C_2 : R_2 \leftarrow R_1$$

4-bit register:



$$\text{Load} = C_0 + C_1 + C_2$$

$$D_i = R_2(t+1)_i = C_0 \cdot 0 + C_1 \bar{R}_{2i} + C_2 R_{1i} = \\ 0 + C_1 \bar{R}_{2i} + C_2 R_{1i} = C_1 \bar{R}_{2i} + C_2 R_{1i}$$



The same can be implemented for other bits

$$g. \quad S_1: B \leftarrow B + A$$

$$S_0: B \leftarrow B + 1$$

We assume that only one of S_1, S_0 is equal to 1; for all S_1 and S_0 equal to 0, the content of B remains unchanged

$$D_i = \bar{S}_1 \cdot \bar{S}_0 \cdot B_i + S_1 (\underbrace{B_i \oplus A_i \oplus C_i}_{\overline{B_i}}) + S_0 (\underbrace{B_i \oplus 1 \oplus C_i}_{\overline{B_i}}) =$$

$$\bar{S}_1 \cdot \bar{S}_0 \cdot B_i + S_1 (B_i \oplus A_i \oplus C_i) + S_0 (\overline{B_i \oplus C_i}) =$$

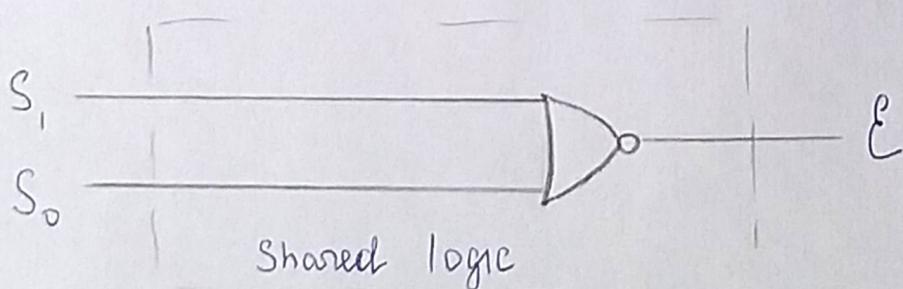
$$\bar{S}_1 \cdot \bar{S}_0 \cdot B_i + S_1 ((B_i \oplus C_i) \oplus A_i) + S_0 (\overline{B_i \oplus C_i})$$

$$C_{i+1} = S_1 ((B_i \oplus A_i) C_i + B_i A_i) + S_0 ((\underbrace{(B_i \oplus 1) C_i}_{\overline{B_i}}) + \underbrace{B_i \cdot 1}_{B_i}) =$$

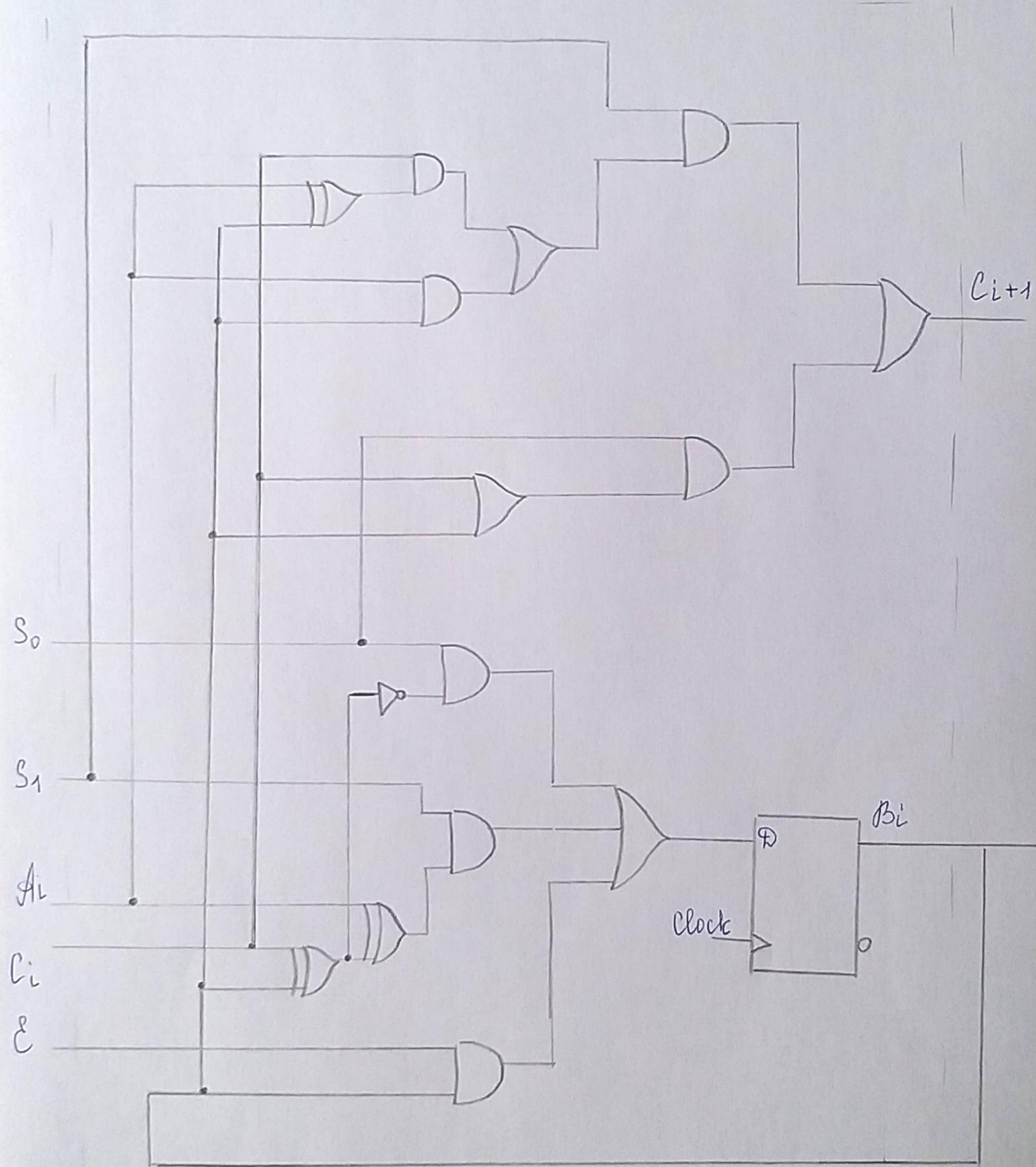
$$S_1 ((B_i \oplus A_i) C_i + B_i A_i) + S_0 ((\underbrace{B_i + \overline{B_i}}_1) (B_i + C_i)) =$$

$$S_1 ((B_i \oplus A_i) C_i + B_i A_i) + S_0 (B_i + C_i)$$

$$\text{Let } E = \bar{S}_1 \cdot \bar{S}_0 = \overline{S_1 + S_0}$$



Register cell



$$10. \quad R_0 \leftarrow R_1$$

$$R_5 \leftarrow R_1$$

$$R_6 \leftarrow R_2$$

$$R_7 \leftarrow R_3$$

$$R_8 \leftarrow R_3$$

$$R_9 \leftarrow R_4$$

$$R_{10} \leftarrow R_4$$

$$R_{11} \leftarrow R_1$$

a) As for a single-bus system, simultaneous transfers with different sources in a single clock cycle are impossible, the minimum number of buses to execute the transfers in, at most, two clock cycles is 2 because there are 4 different sources

B)

