



СОЗДАНИЕ КОМПОНЕНТА (IP)

Проектирование цифровой
техники с применением ПЛИС
и аппаратного языка разработки
System Verilog

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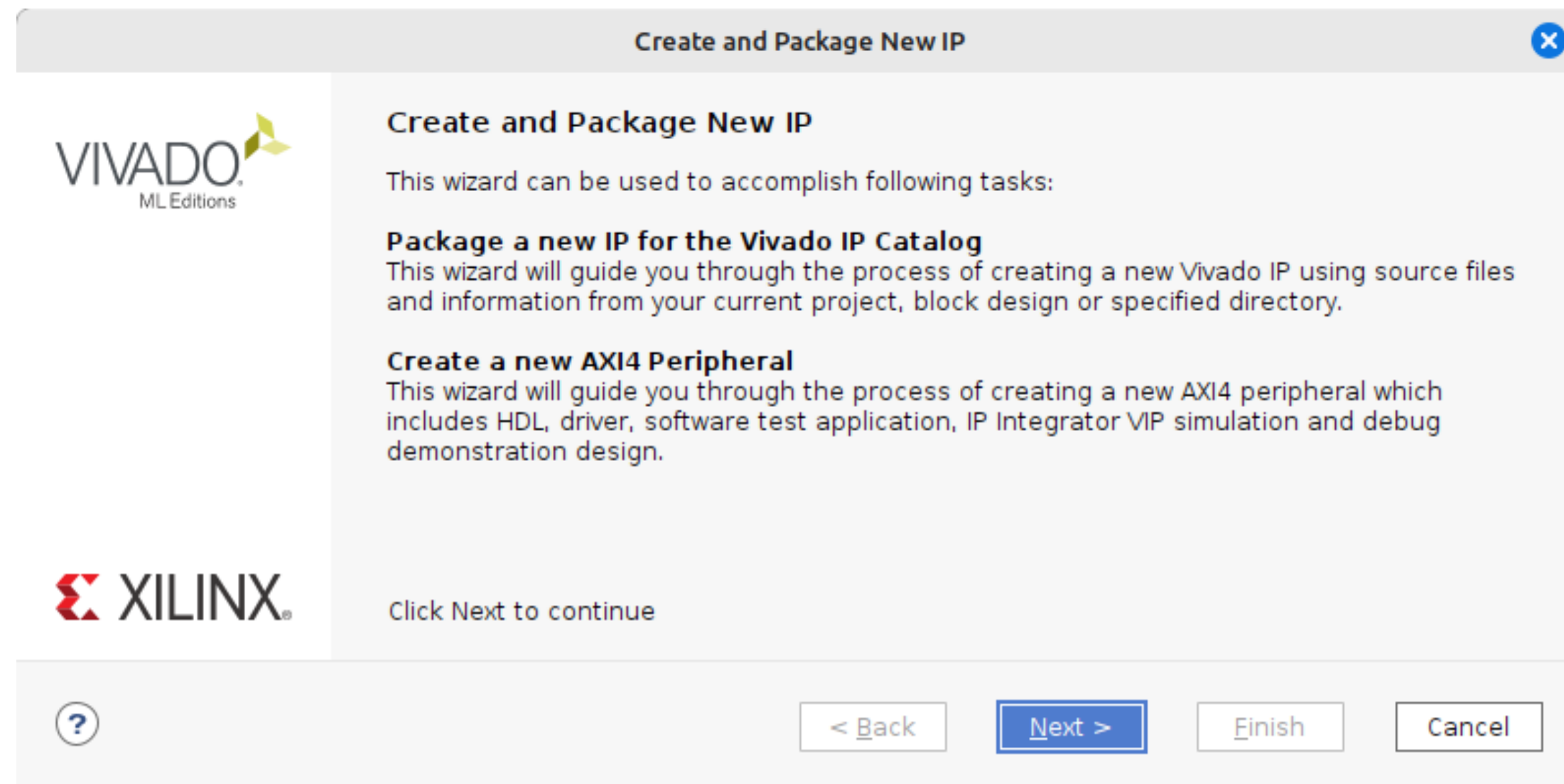
Пример



IP – Intellectual Property

<https://digilent.com/reference/learn/programmable-logic/tutorials/zybo-creating-custom-ip-cores/start>

Создание компонента (IP)



Создание компонента (IP)



Create and Package New IP

Create Peripheral, Package IP or Package a Block Design

Please select one of the following tasks.

Packaging Options

☐ Package your current project
Use the project as the source for creating a new IP Definition.

☐ Package a block design from the current project
Choose a block design as the source for creating a new IP Definition.
Select a block design:

system

☐ Package a specified directory
Choose a directory as the source for creating a new IP Definition.

Create AXI4 Peripheral

☒ Create a new AXI4 peripheral
Create an AXI4 IP, driver, software test application, IP Integrator AXI4 VIP simulation and debug demonstration design.

?

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Finish

Cancel

Создание компонента (IP)



Create and Package New IP

Peripheral Details

Specify name, version and description for the new peripheral

Name:

axi_pwm

Version:

1.0

Display name:

axi_pwm_v1.0

Description:

My new AXI IP

IP location:

/home/neya/tmp/ip_repo

☐ Overwrite existing

?

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Finish

Cancel

Создание компонента (IP)



Create and Package New IP

Add Interfaces

Add AXI4 interfaces supported by your peripheral

Enable Interrupt Support

S00_AXI

axi_pwm_v1.0

+

-

Interfaces

S00_AXI

Name

S00_AXI

Interface Type

Lite

Interface Mode

Slave

Data Width (Bits)

32

Memory Size (Bytes)

64

Number of Registers

4

[4..512]

?

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Finish

Cancel

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Создание компонента (IP)





Create and Package New IP

Create Peripheral

Peripheral Generation Summary


1. IP (user.org:user:axi_pwm:1.0) with [1 interface\(s\)](#)
2. Driver(v1_00_a) and testapp [more info](#)
3. AXI4 VIP Simulation demonstration design [more info](#)
4. AXI4 Debug Hardware Simulation demonstration design [more info](#)

Peripheral created will be available in the catalog :
/home/neya/tmp/ip_repo

Next Steps:

- ☒ Add IP to the repository
- ☐ Edit IP
- ☐ Verify Peripheral IP using AXI4 VIP
- ☐ Verify peripheral IP using JTAG interface

Click Finish to continue



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Finish

Cancel

Создание компонента (IP)





Create and Package New IP

Create Peripheral

Peripheral Generation Summary


1. IP (user.org:user:axi_pwm:1.0) with 1 [interface\(s\)](#)
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Next Steps:

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- ☒ Edit IP
- ☐ Verify Peripheral IP using AXI4 VIP
- ☐ Verify peripheral IP using JTAG interface

Click Finish to continue



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Finish

Cancel

Создание компонента (IP)



Create Source File

Create a new source file and add it to your project.

File type:

SystemVerilog

File name:

pwm.sv

File location:

repo/axi_pwm_1_0/hdl

?

OK

Cancel

Создание компонента (IP)



Add Sources

Создание компонента (IP)



Define Module

Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

Module name:

I/O Port Definitions

+ - ↑ ↓

Port Name	Direction		Bus	MSB	LSB
i_clk	input	▼	<input type="checkbox"/>	0	0
i_period	input	▼	<input checked="" type="checkbox"/>	31	0
i_width	input	▼	<input checked="" type="checkbox"/>	31	0
i_set	input	▼	<input type="checkbox"/>	0	0
o_pulse	output	▼	<input type="checkbox"/>	0	0

?

OK

Cancel

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Создание компонента (IP)



PROJECT MANAGER - edit_axi_pwm_v1_0

Sources

- Design Sources (3)
 - axi_pwm_v1_0 (axi_pwm_v1_0.v) (1)
 - pwm (pwm.sv)
 - IP-XACT (1)
- Constraints
- Simulation Sources (2)
- Utility Sources

Source File Properties

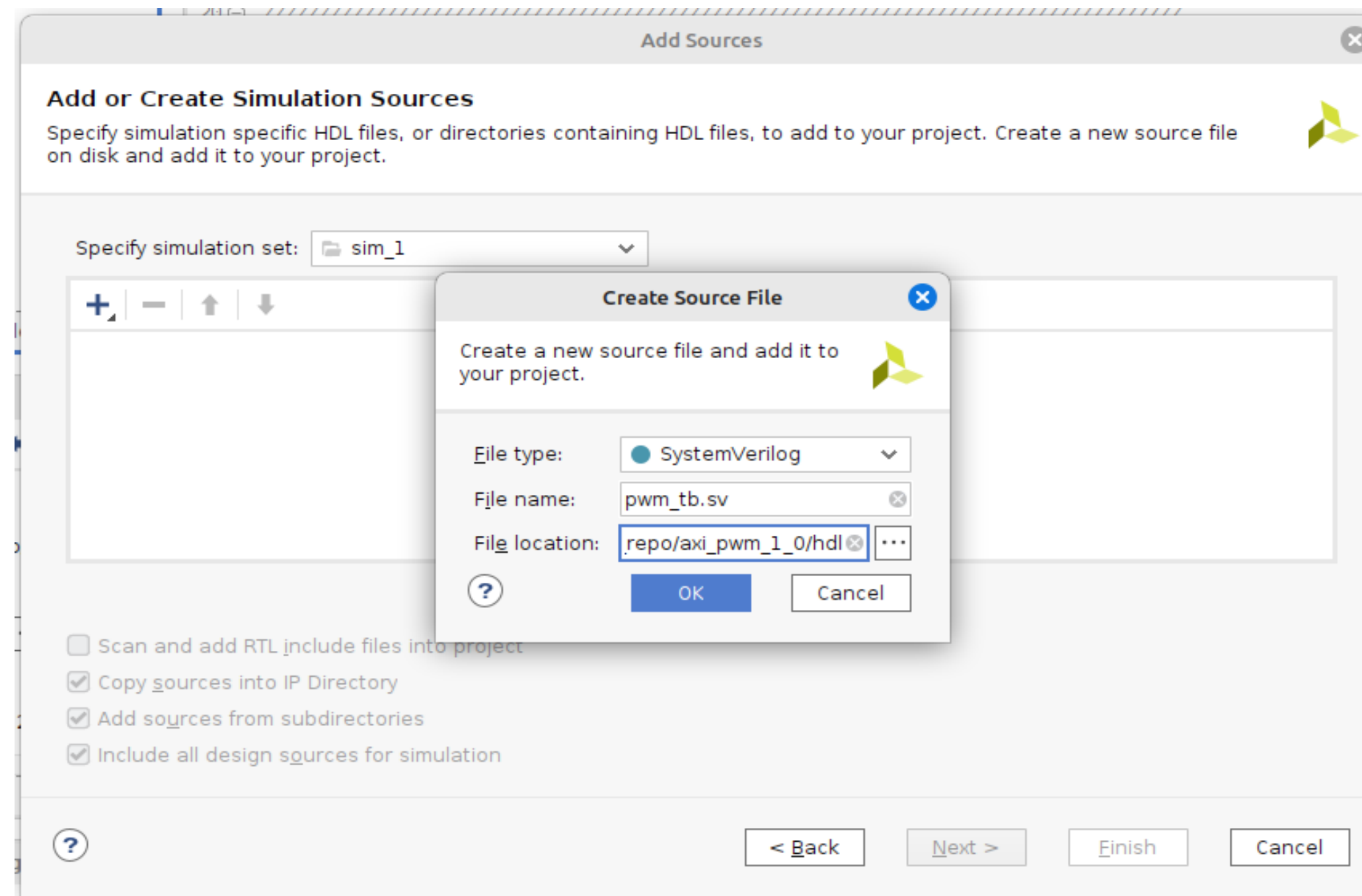
pwm.sv

- ☒ Enabled
- Location: /home/neya/tmp/ip_repo/axi
- Type: SystemVerilog
- Library: xil_defaultlib
- Size: 0.6 KB
- Modified: Today at 13:13:05 PM

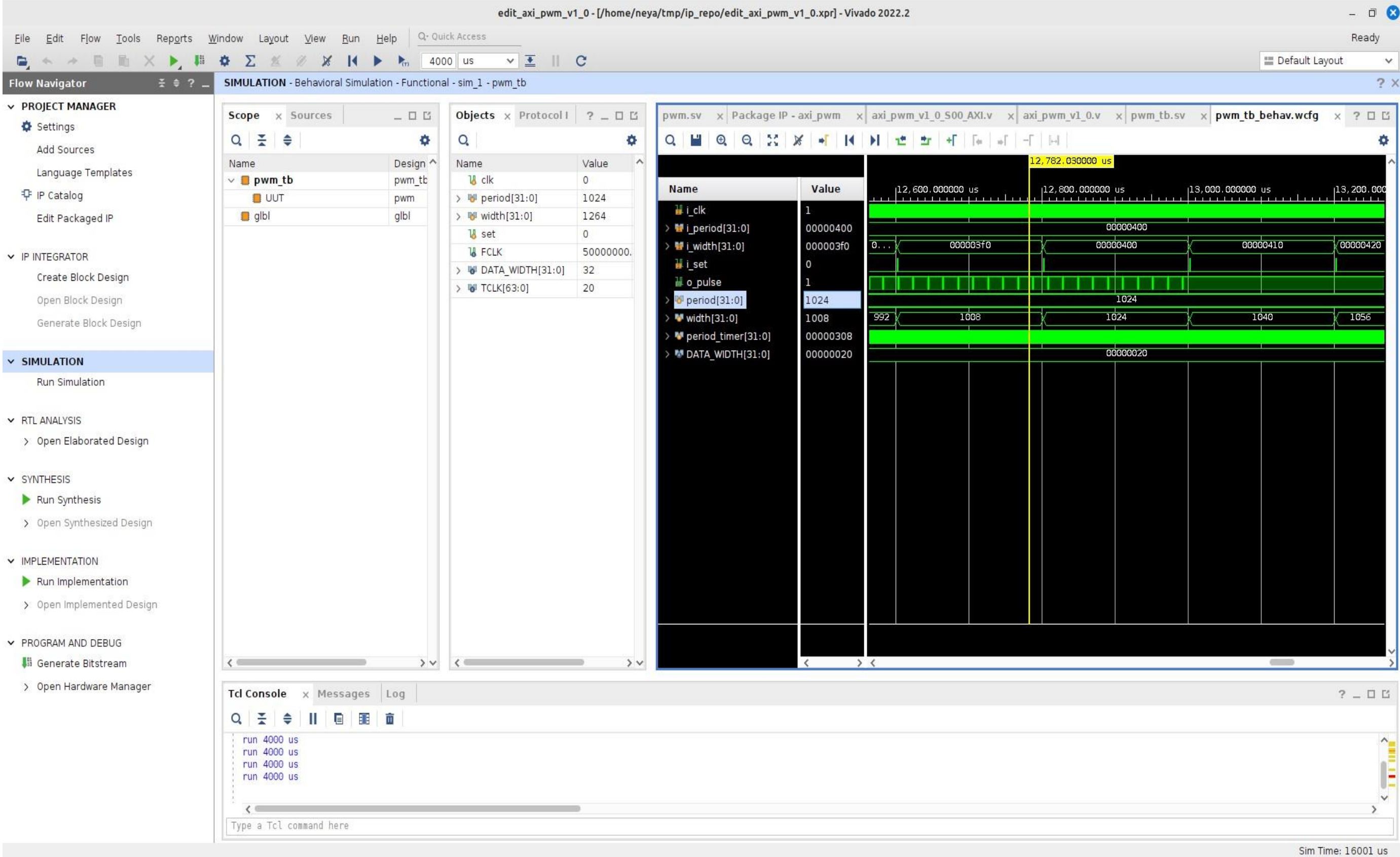
pwm.sv

```
1 timescale 1ns / 1ps
2 //////////////////////////////////////////////////
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 09/19/2024 01:09:08 PM
7 // Design Name:
8 // Module Name: pwm
9 // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////
21
22
23 module pwm
24   #(parameter int DATA_WIDTH = 32)
25   (
26     input i_clk,
27     input [DATA_WIDTH -1:0] i_period,
28     input [DATA_WIDTH -1:0] i_width,
29     input i_set,
30     output o_pulse
31   );
32 endmodule
33
```

Создание компонента (IP)



Создание компонента (IP)



Создание компонента (IP)



pwm.sv x Package IP - axi_pwm x axi_pwm_v1_0_S00_AXI.v x axi_pwm_v1_0.v x pwm_tb.sv x pwm_tb_be

Packaging Steps

- ✓ Identification
- ✓ Compatibility
- File Groups**
- Customization Parameters
- Ports and Interfaces
- ✓ Addressing and Memory
- Customization GUI
- Review and Package

File Groups

! Merge changes from File Groups Wizard

Q | [Icons] | + | C

Name	Library Name	Type	Is Include	File Group Name	Model Name
Standard			<input type="checkbox"/>		
Advanced			<input type="checkbox"/>		
> Verilog Synthesis (2)			<input type="checkbox"/>		axi_pwm_v1_0
> Verilog Simulation (2)			<input type="checkbox"/>		axi_pwm_v1_0
> Software Driver (6)			<input type="checkbox"/>		
> UI Layout (1)			<input type="checkbox"/>		
> Block Diagram (1)			<input type="checkbox"/>		

Создание компонента (IP)



pwm.sv x Package IP - axi_pwm x axi_pwm_v1_0_S00_AXI.v x axi_pwm_v1_0.v x pwm_tb.sv x pwm_tb_behav.wcfg x

Packaging Steps

- ✓ Identification
- ✓ Compatibility
- ⚠ File Groups
- ✓ Customization Parameters
- ✓ Ports and Interfaces
- ✓ Addressing and Memory
- ✓ Customization GUI
- Review and Package**

Review and Package

⚠ 1 warning 2 info messages

Summary

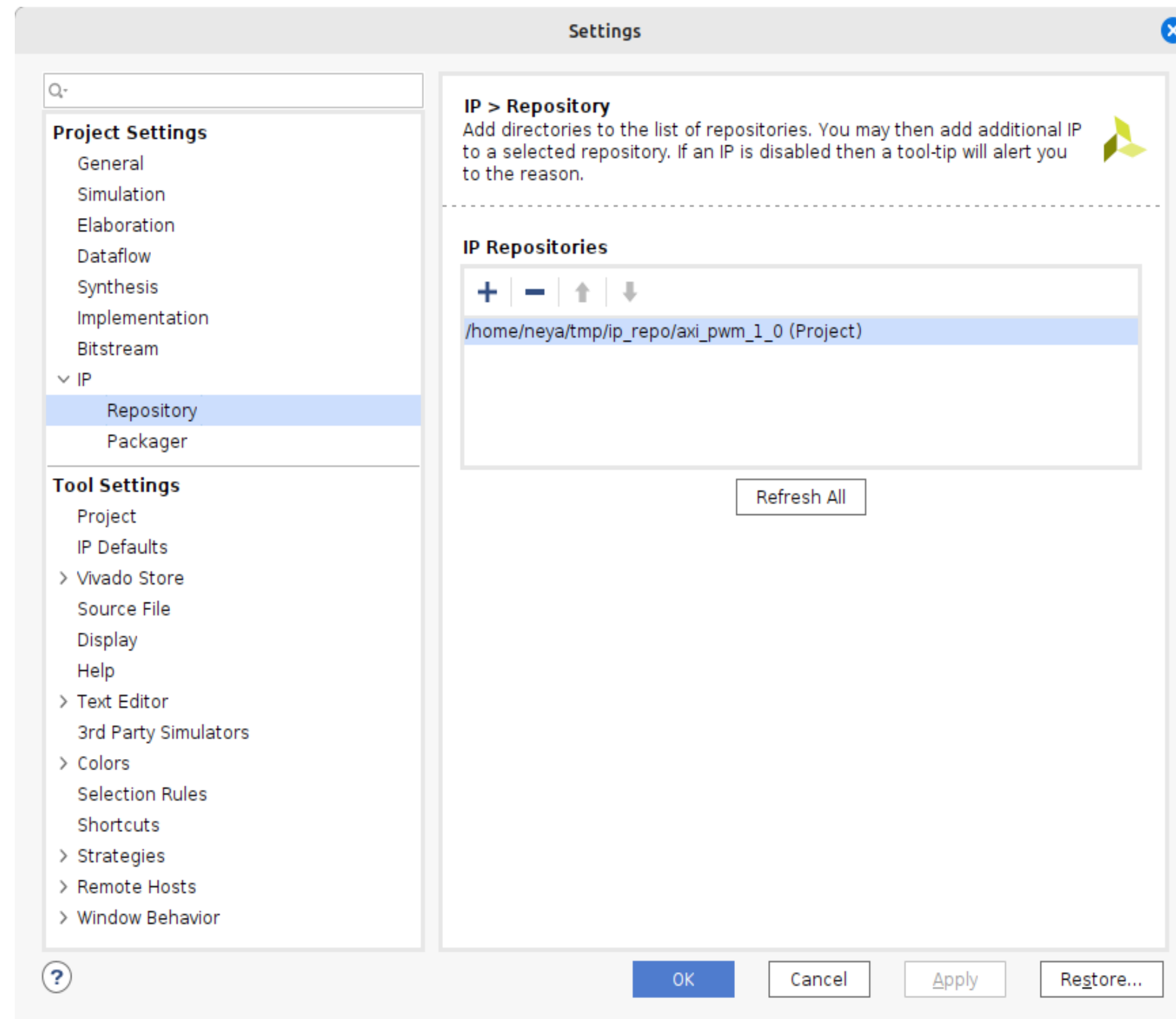
Display name: axi_pwm_v1.0
Description: My new AXI IP
Root directory: /home/neya/tmp/ip_repo/axi_pwm_1_0

After Packaging

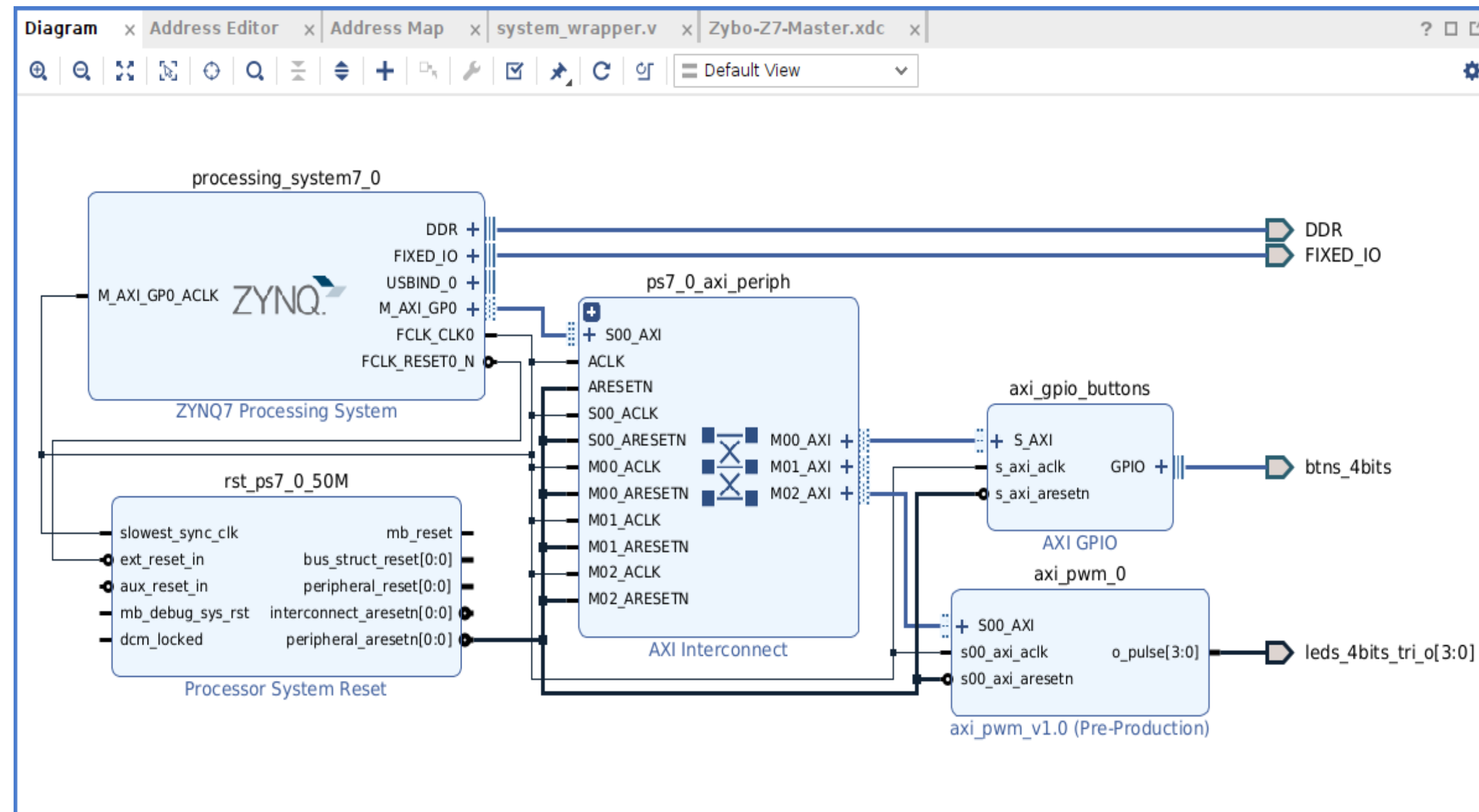
An archive will not be generated. Use the settings link below to change your preference
Project will be removed after completion
[Edit packaging settings](#)

Re-Package IP

Создание компонента (IP)



Создание компонента (IP)



Создание компонента (IP)



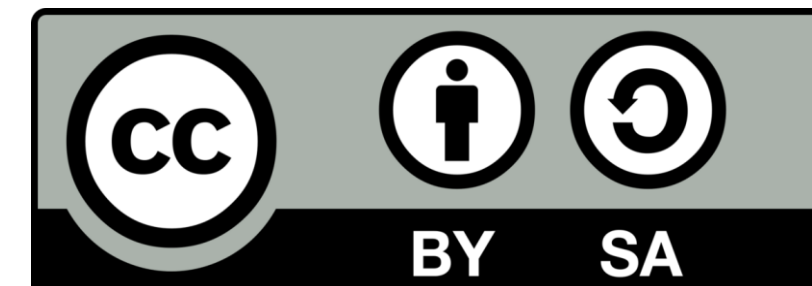
Diagram x Address Editor x Address Map x system_wrapper.v x Zybo-Z7-Master.xdc x

</

Создание компонента (IP)



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Спасибо за внимание!