



СОЗДАНИЕ КОМПОНЕНТА (IP)

**Проектирование цифровой
техники с применением ПЛИС
и аппаратного языка разработки
System Verilog**

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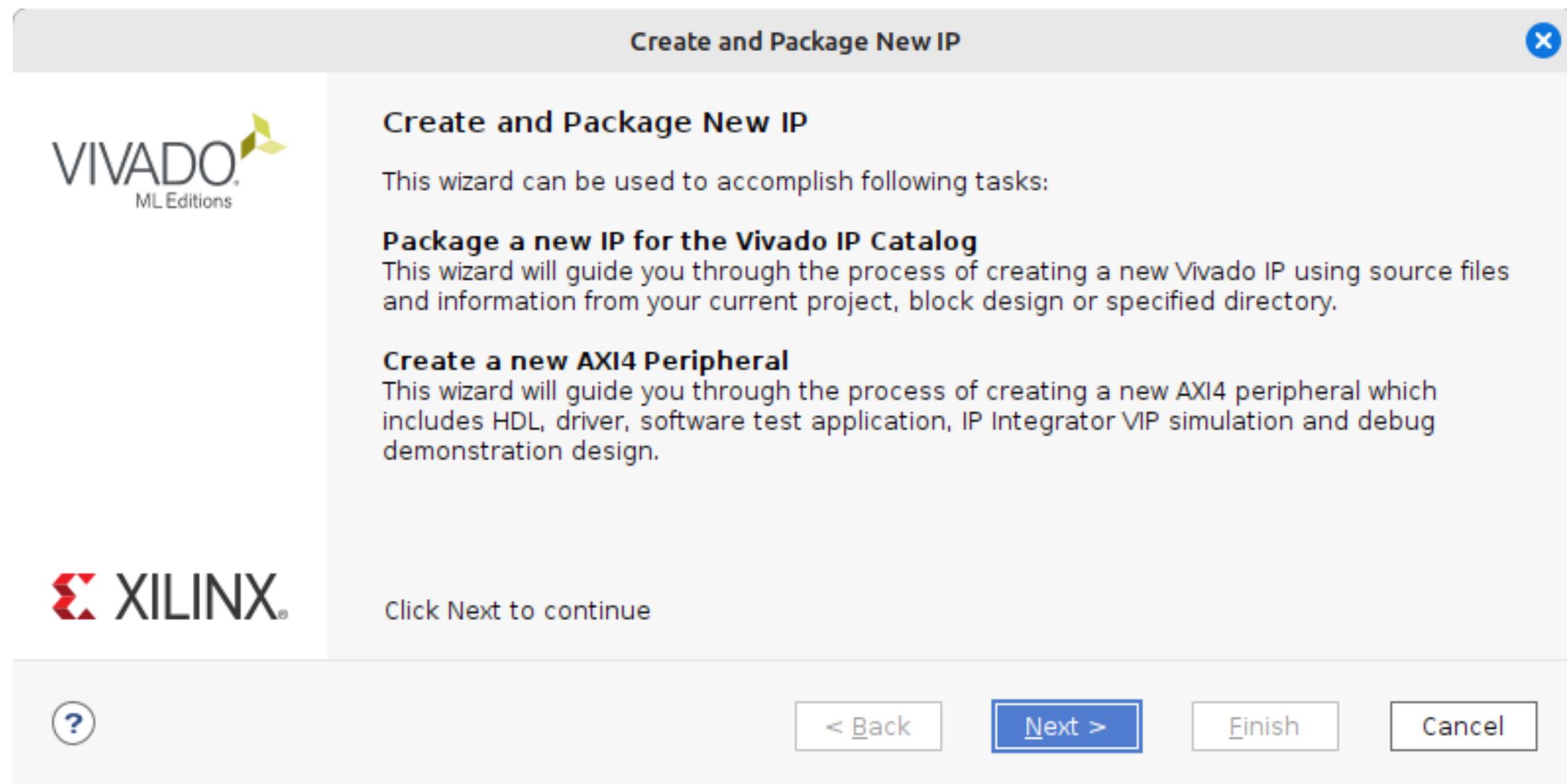
Пример



IP – Intellectual Property

<https://digilent.com/reference/learn/programmable-logic/tutorials/zybo-creating-custom-ip-cores/start>

Создание компонента (IP)



Создание компонента (IP)



Create and Package New IP ×

Create Peripheral, Package IP or Package a Block Design

Please select one of the following tasks.



Packaging Options

- Package your current project
Use the project as the source for creating a new IP Definition.
- Package a block design from the current project
Choose a block design as the source for creating a new IP Definition.
Select a block design:
- Package a specified directory
Choose a directory as the source for creating a new IP Definition.

Create AXI4 Peripheral

- Create a new AXI4 peripheral
Create an AXI4 IP, driver, software test application, IP Integrator AXI4 VIP simulation and debug demonstration design.

? < Back Next > Finish Cancel

Создание компонента (IP)



Create and Package New IP X

Peripheral Details
Specify name, version and description for the new peripheral

Name:	axi_pwm	<input type="button" value="X"/>
Version:	1.0	<input type="button" value="X"/>
Display name:	axi_pwm_v1.0	<input type="button" value="X"/>
Description:	My new AXI IP	<input type="button" value="X"/>
IP location:	/home/neya/tmp/ip_repo	<input type="button" value="X"/> ...

Overwrite existing

? < Back Next > Finish Cancel

Создание компонента (IP)



Create and Package New IP

Add Interfaces
Add AXI4 interfaces supported by your peripheral

The dialog shows the following configuration for the 'S00_AXI' interface:

- Enable Interrupt Support
- + - Interfaces:
 - S00_AXI
 - axi_pwm_v1.0
- Name: S00_AXI
- Interface Type: Lite
- Interface Mode: Slave
- Data Width (Bits): 32
- Memory Size (Bytes): 64
- Number of Registers: 4 [4..512]

Buttons at the bottom: ? < Back Next > Finish Cancel

Создание компонента (IP)



Create and Package New IP

VIVADO
ML Editions

Create Peripheral

Peripheral Generation Summary

1. IP (user.org:user:axi_pwm:1.0) with 1 interface(s)
2. Driver(vl_00_a) and testapp [more info](#)
3. AXI4 VIP Simulation demonstration design [more info](#)
4. AXI4 Debug Hardware Simulation demonstration design [more info](#)

Peripheral created will be available in the catalog :
`/home/neya/tmp/ip_repo`

Next Steps:

Add IP to the repository

Edit IP

Verify Peripheral IP using AXI4 VIP

Verify peripheral IP using JTAG interface

Click Finish to continue

< Back Next > **Finish** Cancel

Создание компонента (IP)



Create and Package New IP

VIVADO
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Peripheral Generation Summary

1. IP (user.org:user:axi_pwm:1.0) with 1 interface(s)
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Peripheral created will be available in the catalog :
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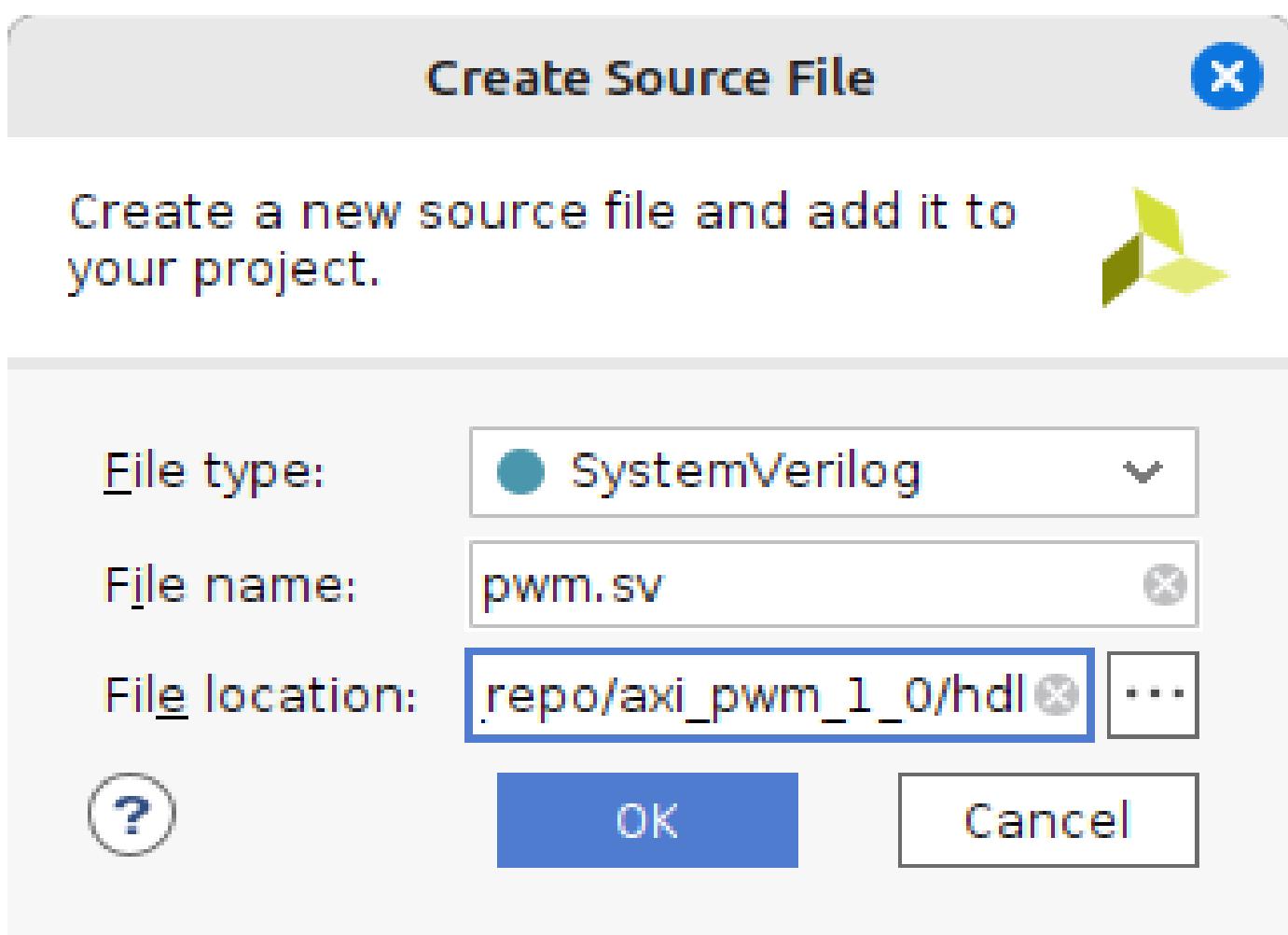
Next Steps:

Add IP to the repository
 Edit IP
 Verify Peripheral IP using AXI4 VIP
 Verify peripheral IP using JTAG interface

Click Finish to continue

< Back Next > **Finish** Cancel

Создание компонента (IP)



Создание компонента (IP)



Add Sources

Add or Create Design Sources

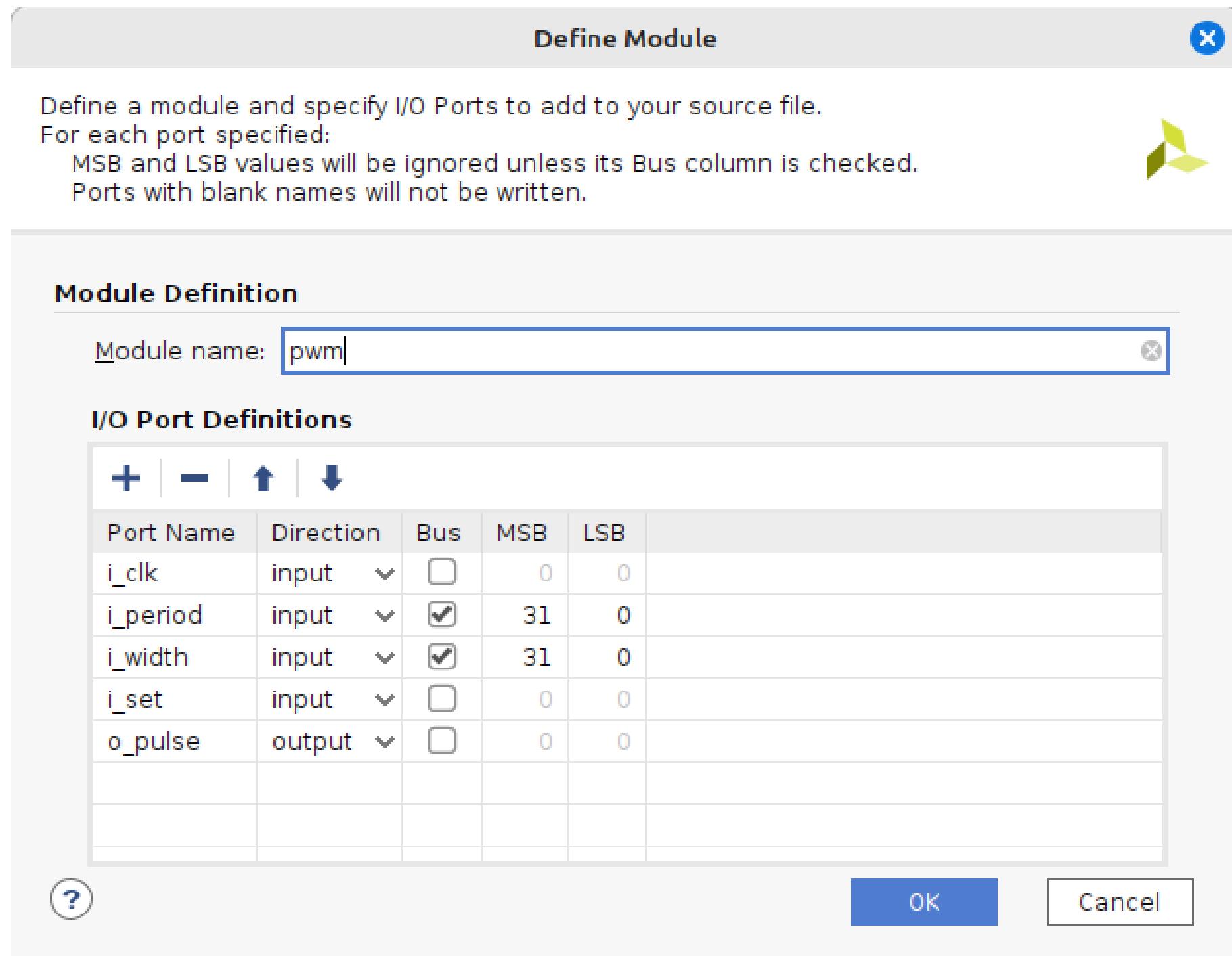
Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.

The dialog box displays a table of design sources:

	Index	Name	Library	Location
●	1	pwm.sv	xil_defaultlib	/home/neya/tmp/ip_repo/axi_pwm_1_0/hdl

Buttons at the bottom include: Add Files (disabled), Create File (highlighted), Scan and add RTL include files into project (unchecked), Copy sources into IP Directory (checked), Add sources from subdirectories (checked), Help (?), Back (< Back), Next >, Finish, and Cancel.

Создание компонента (IP)



Создание компонента (IP)



PROJECT MANAGER - edit_axi_pwm_v1_0

Sources ? _ □ X

Design Sources (3)
axi_pwm_v1_0 (axi_pwm_v1_0.v) (1)
pwm (pwm.sv)
IP-XACT (1)
Constraints
Simulation Sources (2)
Utility Sources

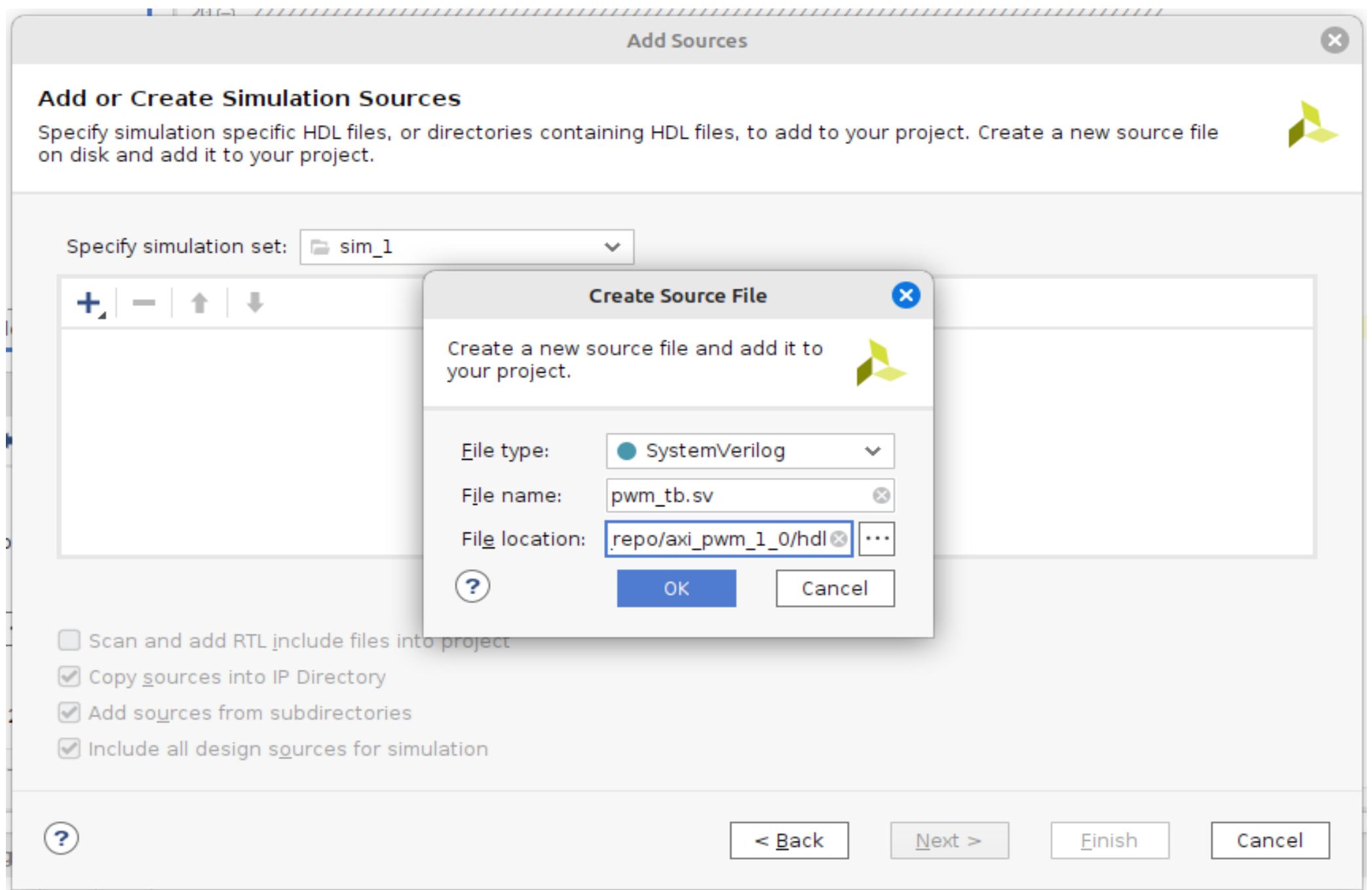
Hierarchy Libraries Compile Order

pwm.sv * Project Summary Package IP - axi_pwm

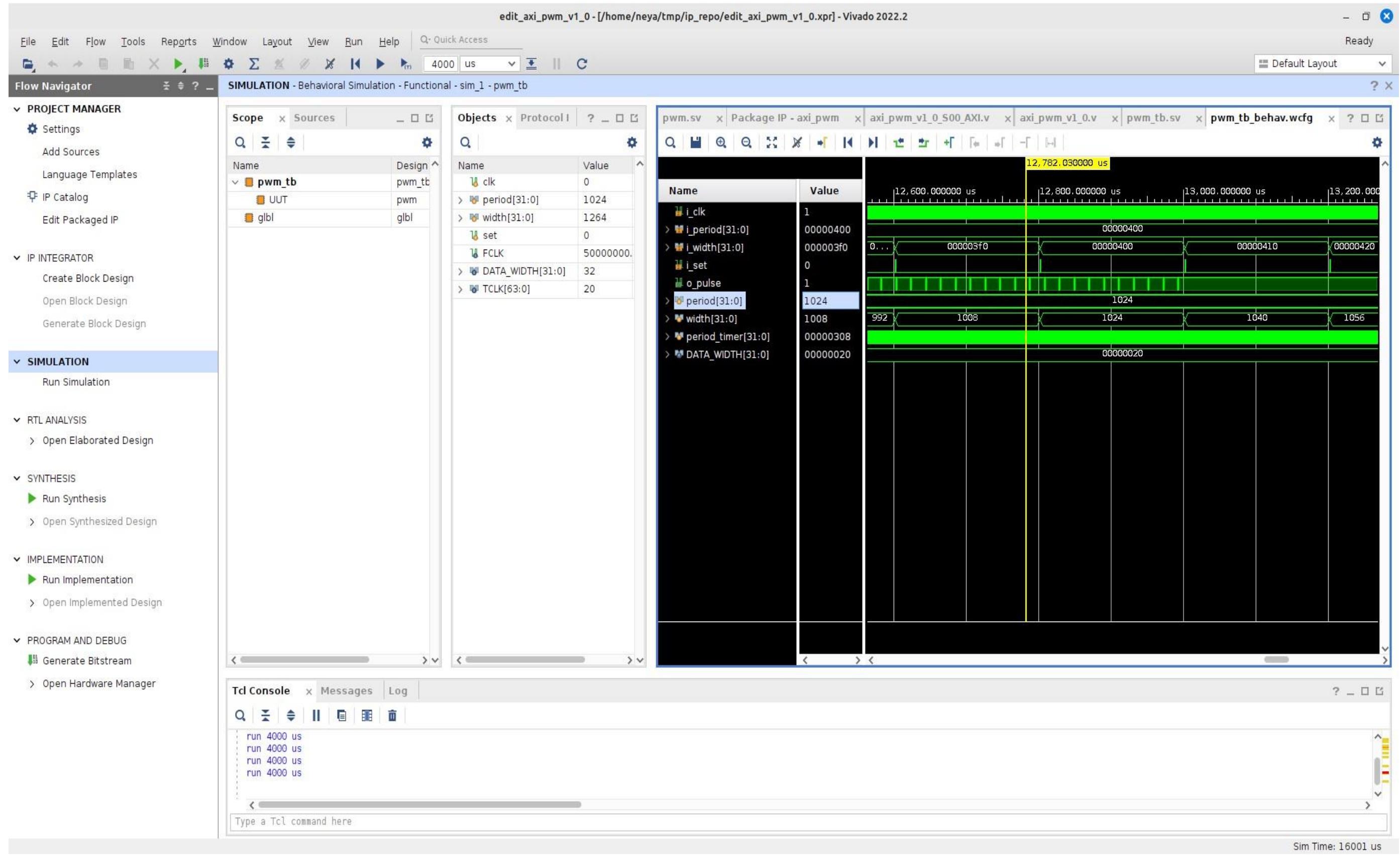
/home/neya/tmp/ip_repo/axi_pwm_1_0/hdl/pwm.sv

```
1 `timescale 1ns / 1ps
2 // Company:
3 // Engineer:
4 //
5 //
6 // Create Date: 09/19/2024 01:09:08 PM
7 // Design Name:
8 // Module Name: pwm
9 // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 //
22 module pwm
23 #(parameter int DATA_WIDTH = 32)
24 (
25     input i_clk,
26     input [DATA_WIDTH -1:0] i_period,
27     input [DATA_WIDTH -1:0] i_width,
28     input i_set,
29     output o_pulse
30 );
31 endmodule
32
33 
```

Создание компонента (IP)



Создание компонента (IP)



Создание компонента (IP)



The screenshot shows the Vivado IP Packager interface with the following details:

Top tabs: pwm.sv, Package IP - axi_pwm, axi_pwm_v1_0_S00_AXI.v, axi_pwm_v1_0.v, pwm_tb.sv, pwm_tb_be

Left sidebar: Packaging Steps (Identification, Compatibility, File Groups, Customization Parameters, Ports and Interfaces, Addressing and Memory, Customization GUI, Review and Package). The "File Groups" step is selected.

Main area: File Groups table with the following data:

Name	Library Name	Type	Is Include	File Group Name	Model Name
Standard			<input checked="" type="checkbox"/>		
Advanced			<input type="checkbox"/>		
Verilog Synthesis (2)			<input type="checkbox"/>	axi_pwm_v1_0	
Verilog Simulation (2)			<input type="checkbox"/>	axi_pwm_v1_0	
Software Driver (6)			<input type="checkbox"/>		
UI Layout (1)			<input type="checkbox"/>		
Block Diagram (1)			<input type="checkbox"/>		

Message bar: ! Merge changes from File Groups Wizard

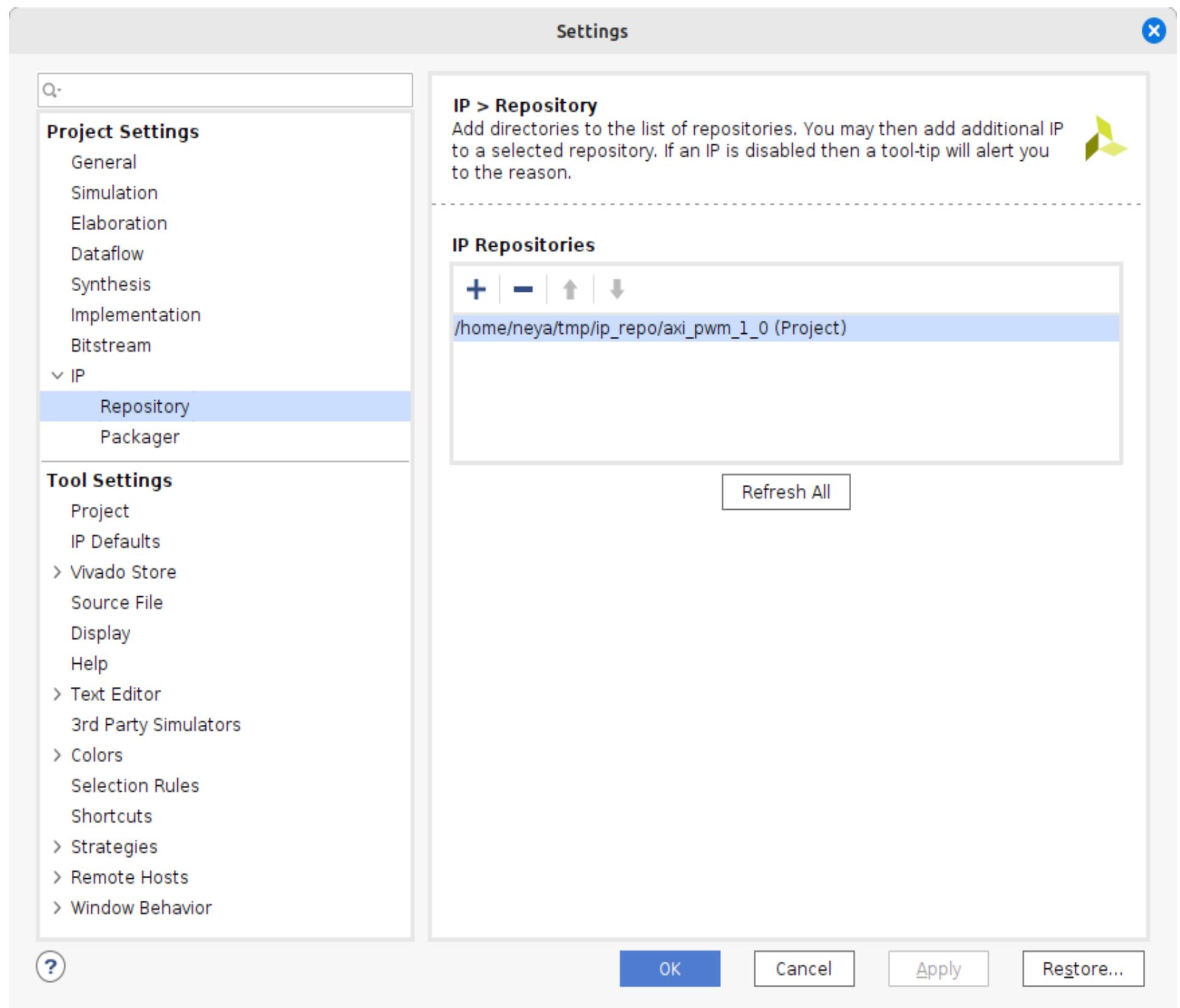
Создание компонента (IP)



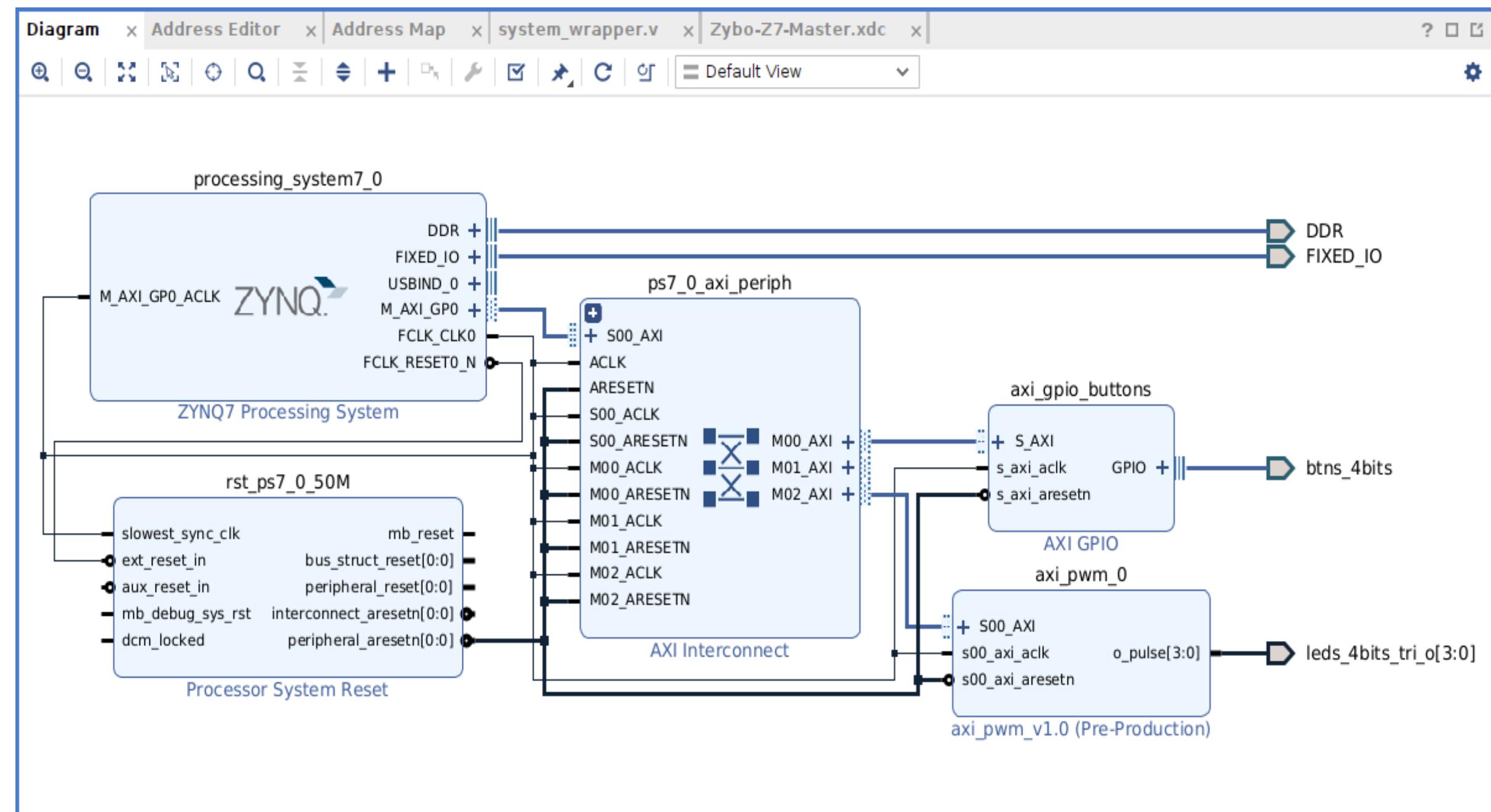
The screenshot shows the Vivado IP Packager interface with the following details:

- Project Title:** Package IP - axi_pwm
- Packaging Steps:**
 - ✓ Identification
 - ✓ Compatibility
 - ⚠ File Groups
 - ✓ Customization Parameters
 - ✓ Ports and Interfaces
 - ✓ Addressing and Memory
 - ✓ Customization GUI
- Review and Package:**
 - 1 warning 2 info messages
 - Summary:**
 - Display name: axi_pwm_v1.0
 - Description: My new AXI IP
 - Root directory: /home/neya/tmp/ip_repo/axi_pwm_1_0
 - After Packaging:**
 - An archive will not be generated. Use the settings link below to change your preference
 - Project will be removed after completion
 - [Edit packaging settings](#)
- Buttons:**
 - Re-Package IP

Создание компонента (IP)



Создание компонента (IP)



Создание компонента (IP)



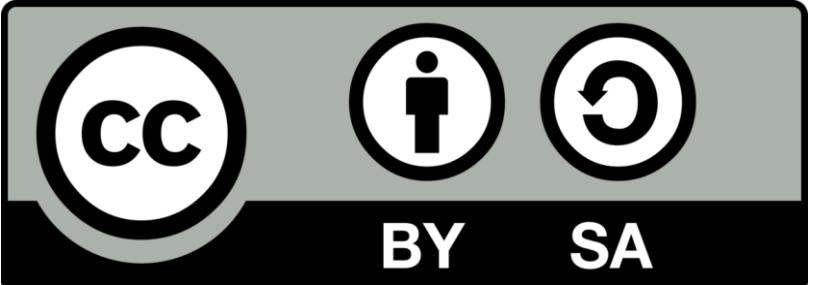
The screenshot shows the Vivado Address Editor interface with the following tabs: Diagram, Address Editor (selected), Address Map, system_wrapper.v, and Zybo-Z7-Master.xdc. The Address Editor tab has filters for Assigned (2), Unassigned (0), Excluded (0), and Incomplete (1). The main table displays memory assignments:

Name	Interface	Slave Segment	Master Base Address	Range	Master High Address
Network 0					
/processing_system7_0					
/processing_system7_0/Data (32 address bits : 0x40000000 [1G])					
/axi_gpio_buttons/S_AXI	S_AXI	Reg	0x4120_0000	64K	0x4120_FFFF
/axi_pwm_0/S00_AXI	S00_AXI	S00_AXI_reg	0x43C0_0000	128	0x43C0_007F
Incomplete Paths (1)					

Создание компонента (IP)



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Спасибо за внимание!