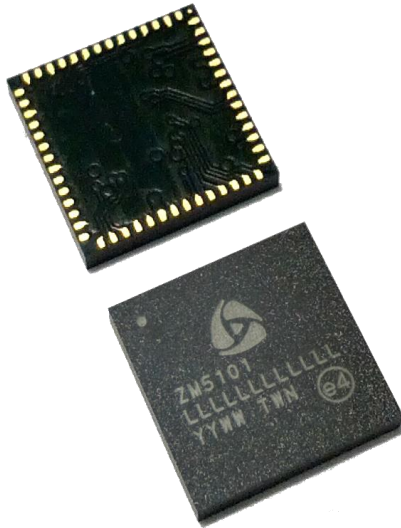


FULLY INTEGRATED Z-WAVE® WIRELESS SYSTEM-IN-PACKAGE



The Sigma Designs ZM5101 System-in-Package is a fully integrated Z-Wave module in a small 8mm x 8mm x 1.2mm form factor. It is an ideal solution for home control applications such as access control, appliance control, AV control, building automation, energy management, lighting, security, and sensor networks in the “Internet of Things”.

A baseband controller, sub-1 GHz radio transceiver, crystal, decoupling, and matching is included to provide a complete Z-Wave system requiring only an external SAW filter and antenna. The ZM5101 SiP remains pad and pin compatible with the 400 series ZM4101 SiP.

The ZM5101 SiP is based on an 8-bit 8051 CPU core, which is optimized to handle the data and link management requirements of a Z-Wave node. The patented Z-Wave protocol supports automatic retransmissions, collision avoidance mechanisms, frame acknowledgements, frame CRCs, frequency agility, and full mesh routing to ensure a highly reliable and robust wireless communication solution.

The integrated baseband controller, sub-1 GHz radio transceiver, a comprehensive set of hardware peripherals, 16kB of SRAM, and 128kB of Flash memory is available for OEM applications and the Z-Wave protocol stack.

Features

- Pad and pin compatible with the ZM4101
- ITU G.9959 compliant

SiP

- Optimized 8051 CPU Core
- 128kB Flash
- 16kB SRAM
- Two UARTs with speed up to 230.4kbps
- Two SPIs with speed up to 8MHz
- USB 2.0 full speed
- 4-channel 12/8-bit rail-to-rail ADC with VDD/internal/external voltage reference
- 4-channel 16-bit LED PWM
- 30 GPIOs
- Hardware AES-128 security engine
- 1000 step dimmer (TRIAC/FET)
- Keypad Scan controller for up to 128 keys
- Infra-red RX/TX controller with learning
- Power-On-Reset/Brown-out Detection
- Supply voltage range from 2.3V to 3.6V for optional battery operation
- TX mode current typ. 34mA@0dBm
- RX mode current typ. 32mA
- Normal mode current typ. 15mA
- Sleep mode current typ. 1µA
- Wake-up timer current typ. 700nA
- Less than 1ms cold start-up time

Radio Transceiver

- Receiver sensitivity without SAW filter down to -105dBm@9.6kbps
- Transmit power without SAW filter up to +6dBm
- Z-Wave 9.6/40/100kbps data rates
- Supports all Z-Wave sub-1 GHz frequency bands (865.2MHz to 926.3 MHz)
- Supports multi-channel frequency agility and listen before talk
- Regulatory Compliance
 - ACMA: AS/NZS 4268
 - CE: EN 300 220/489
 - FCC: CFR 47 Part 15
 - IC: RSS-GEN/210
 - MIC: ARIB STD-T108

1 CONTENT

| | | |
|----------|---|-----------|
| 2 | OVERVIEW | 4 |
| 2.1 | CPU..... | 4 |
| 2.2 | PERIPHERALS..... | 5 |
| 2.2.1 | Advanced Encryption Standard Security Processor | 5 |
| 2.2.2 | Analog-to-Digital Converter | 5 |
| 2.2.3 | Brown-Out Detector / Power-On-Reset..... | 6 |
| 2.2.4 | Crystal Driver and System Clock..... | 6 |
| 2.2.5 | Dimmer..... | 6 |
| 2.2.6 | General Purpose Input/Output..... | 7 |
| 2.2.7 | General Purpose Timer / Pulse Width Modulator | 7 |
| 2.2.8 | Infra-Red Controller..... | 8 |
| 2.2.9 | Interrupt Controller | 8 |
| 2.2.10 | Keypad Scan Controller | 9 |
| 2.2.11 | Light-Emitting Diode Contoller..... | 9 |
| 2.2.12 | Reset Controller..... | 10 |
| 2.2.13 | Serial Peripheral Interface..... | 10 |
| 2.2.14 | Special Function Registers..... | 11 |
| 2.2.15 | Timers..... | 11 |
| 2.2.16 | Universal Asynchronous Receiver / Transmitter | 12 |
| 2.2.17 | Universal Serial Bus..... | 12 |
| 2.2.18 | Wake-Up Timer | 12 |
| 2.2.19 | Watchdog..... | 13 |
| 2.2.20 | Wireless Transceiver..... | 13 |
| 2.3 | MEMORY MAP..... | 13 |
| 2.4 | MODULE PROGRAMMING..... | 14 |
| 2.4.1 | Entering In-System Programming Mode | 14 |
| 2.4.2 | Entering Auto Programming Mode | 14 |
| 2.5 | POWER SUPPLY REGULATOR | 14 |
| 3 | TYPICAL APPLICATION | 15 |
| 4 | PIN CONFIGURATION | 16 |
| 4.1 | PIN FUNCTIONALITY..... | 16 |
| 5 | ELECTRICAL CHARACTERISTICS..... | 22 |
| 5.1 | TEST CONDITIONS | 22 |
| 5.1.1 | Typical Values..... | 22 |
| 5.1.2 | Minimum and Maximum Values..... | 22 |
| 5.2 | ABSOLUTE MAXIMUM RATINGS | 23 |
| 5.3 | GENERAL OPERATING RATINGS..... | 23 |
| 5.4 | CURRENT CONSUMPTION | 23 |
| 5.5 | SYSTEM TIMING..... | 25 |
| 5.6 | NON-VOLATILE MEMORY RELIABILITY | 25 |
| 5.7 | ANALOG-TO-DIGITAL CONVERTER | 26 |
| 5.8 | DC CHARACTERISTICS | 26 |
| 5.9 | RF CHARACTERISTICS..... | 28 |
| 5.9.1 | Transmitter..... | 28 |
| 5.9.2 | Receiver..... | 29 |

| | | |
|-----------|--|-----------|
| 5.9.3 | Regulatory Compliance | 32 |
| 6 | Z-WAVE FREQUENCIES | 33 |
| 7 | MODULE INFORMATION..... | 34 |
| 7.1 | MODULE MARKING..... | 34 |
| 7.2 | MODULE DIMENSIONS..... | 35 |
| 8 | PROCESS SPECIFICATION..... | 36 |
| 9 | PCB MOUNTING AND SOLDERING..... | 36 |
| 9.1 | RECOMMENDED PCB MOUNTING PATTERN..... | 36 |
| 9.2 | SOLDERING INFORMATION | 37 |
| 10 | ORDERING INFORMATION | 38 |
| 10.1 | TAPE AND REEL INFORMATION | 39 |
| 11 | ABBREVIATIONS..... | 42 |
| 12 | REVISION HISTORY | 44 |
| 13 | REFERENCES | 46 |

2 OVERVIEW

The ZM5101 SiP is a fully integrated SiP containing all the hardware required to add Z-Wave functionality to OEM products. The ZM5101 SiP contains the ZW0501 die along with a 32MHz crystal, power supply decoupling, and matching circuit as illustrated in Figure 2.1. The module only requires a stable DC supply, an external SAW filter, and an antenna matched to 50Ω for operation.

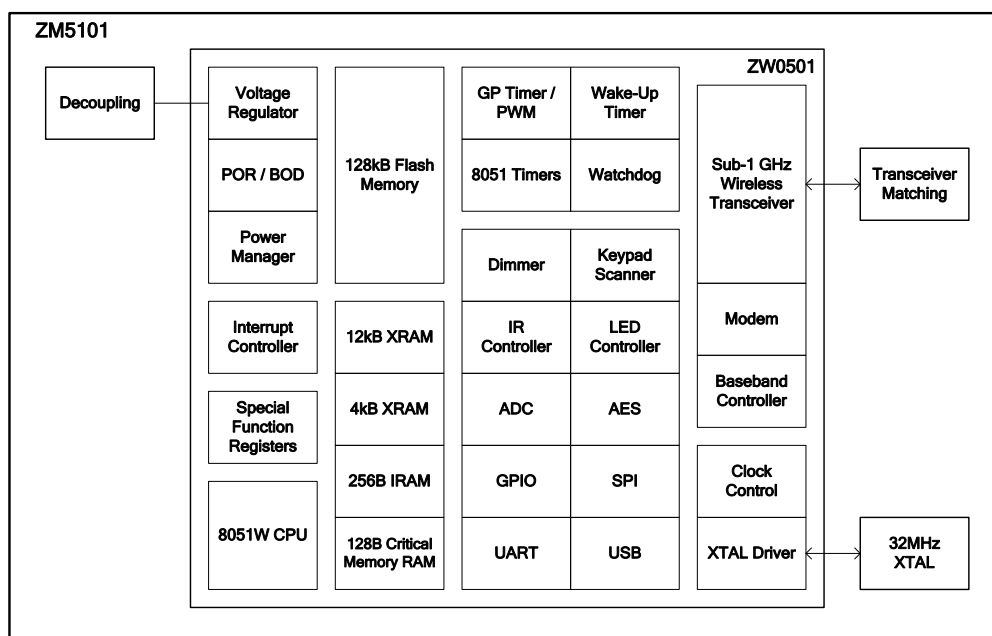


Figure 2.1: Functional block diagram

The ZM5101 SiP is verified to pass regulatory requirements and qualified to meet Z-Wave specifications. It is fully backwards compatible with the ZM4101 SiP in terms of the available GPIOs, hardware peripherals, and footprint. Unlike the ZM4101 SiP, it does not require a higher voltage during programming.

2.1 CPU

The CPU is binary compatible with the industry standard 803x/805x CPU and is operated at 32MHz. Its cycle performance is improved by six times relative to the standard 8051 implementation.

The CPU can be placed in the main modes as described in Table 2.1.

Table 2.1: CPU modes

| Mode | Description |
|---|---|
| ACTIVE | <ul style="list-style-type: none"> Code is executed Peripherals are available All I/O's are resistively pulled high Use a short (up to 4ms) reset-low pulse to enter the reset of active state |
| SLEEP | <ul style="list-style-type: none"> Wake-up timer available Critical memory retention available I/O's states according to user configuration Use API call to enter from ACTIVE mode |
| PROGRAMMING DURING SUSTAINED RESET | <ul style="list-style-type: none"> Used to program the internal FLASH via UART or SPI Code is not executed All I/O's are resistively pulled high Programming requires external control of the RESET pin plus either the UART or the SPI port |
| APM PROGRAMMING | <ul style="list-style-type: none"> Used to program the internal FLASH via USB, UART, or SPI, often initiated from an API call All I/O's are resistively pulled high Access to the RESET pin is not required The chip can be configured to reset into this state either using an API call or instructed via the programming interface. |
| EXTERNAL NVM PROGRAMMING | <ul style="list-style-type: none"> Used to program an external NVM (FLASH/EPROM) (optionally) wired to the SPI port Code is not executed All I/O's are resistively pulled high External NVM programming requires external control of the RESET pin (plus the NVM-SPI port) |

2.2 PERIPHERALS

2.2.1 ADVANCED ENCRYPTION STANDARD SECURITY PROCESSOR

The Z-Wave protocol specifies the use of Advanced Encryption Standard (AES) 128-bit block encryption for secure applications. The built-in Security Processor is a hardware accelerator that encrypts and decrypts data at a rate of 1 byte per 1.5μs. It encodes the frame payload and the message authentication code to ensure privacy and authenticity of messages. The processor supports Output FeedBack (OFB), Cipher-Block Chaining (CBC), and Electronic CodeBook (ECB) modes to target variable length messages. Payload data is streamed in OFB mode, and authentication data is processed in CBC mode as required by the Z-Wave protocol. The processor implements two efficient access methods: Direct Memory Access (DMA) and streaming through Special Function Register (SFR) ports. The processor functionality is exposed via the Z-Wave API for application use.

2.2.2 ANALOG-TO-DIGITAL CONVERTER

The Analog-to-Digital Converter (ADC) is capable of sampling one of the five available input voltage sources and returns an 8 or 12-bit unsigned representation of the selected input scaled relative to the selected reference voltage, as described by the formula below.

$$ADC_{OUT} = \frac{V_{IN}}{V_{REF+} - V_{REF-}}, \quad V_{REF-} \leq V_{IN} \leq V_{REF+}$$

The ADC is capable of operating rail to rail, while the following input configurations apply (V_{BG} = built-in band-gap 1.25V, V_{DD} = supply voltage, V_{IN} = Pin 15 to pin 18):

Table 2.2: ADC source configuration

| Source | Description | Pin |
|------------|--|--|
| V_{IN} | The sampling input voltage | Pin 15, pin 16, pin 17, pin 18, V_{BG} |
| V_{REF+} | The positive node of the reference voltage | Pin 15, V_{BG} , V_{DD} |
| V_{REF-} | The negative node of the reference voltage | Pin 16, GND |

If the sampling input voltage crosses a predefined lower or upper voltage threshold, an interrupt is triggered. Setting $V_{IN} = V_{BG}$ and $V_{REF+} = V_{DD}$ implements a battery monitor. All inputs (V_{IN} , V_{REF+} , V_{REF-}) must be driven by low impedance (R_{source}) voltage sources, to suppress offsets caused by GPIO input leakage of up to 10 μ A.

$$R_{source} \leq \frac{V_{REF+} - V_{REF-}}{2 * |I_{INADC}| * 2^{No. of bits}}, \text{ where } I_{INADC} = \pm 10\mu A$$

If the output impedance of the signal source is larger than R_{source} , an external buffer must be used.

2.2.3 BROWN-OUT DETECTOR / POWER-ON-RESET

When a cold start-up occurs, an internal Power-On-Reset (POR) circuit ensures that code execution does not begin unless the supply voltage is sufficient. After which, an internal Brown-Out Detector (BOD) circuit guarantees that faulty code execution does not occur by entering the reset state, if the supply voltage drops below the minimum operating level. These guarantees apply equally in both the active and sleep modes.

2.2.4 CRYSTAL DRIVER AND SYSTEM CLOCK

The system clock and RF frequencies are derived from an external 32MHz crystal (XTAL) which is factory trimmed to guarantee initial frequency precision. The temperature and 5 years aging margin for the 32MHz crystal is 15 ppm.

2.2.5 DIMMER

The Dimmer allows you to build *leading edge* or *trailing edge* dimmers to cover dimming applications with electronic transformers, halogen or incandescent lamps, wire-wound transformers, etc. The classic leading edge method requires an external TRIAC while the more versatile and electronic transformer friendly trailing edge method requires external Field Effect Transistors (FET) or Insulated-Gate Bipolar Transistors (IGBT). The Dimmer regulates the power-on duration with a precision of 1000 steps in each 50 Hz or 60 Hz half-period. Once the Dimmer has been initialized, it will run at the requested power setting without any assistance from the MCU.

2.2.5.1 LEADING EDGE MODE

This is the classic TRIAC mode. Based on the dim-level requested, the Dimmer determines *when* and *how* the power is switched on. To ensure reliable handling in presence of inductive loads, multiple trigger pulses are automatically appended when needed.

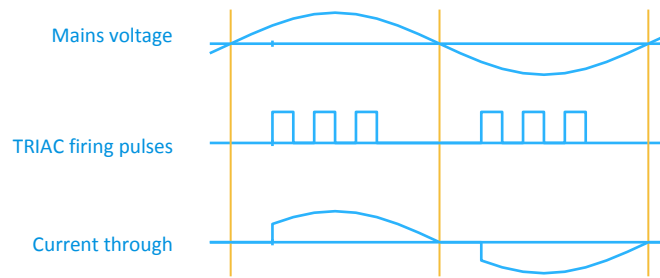


Figure 2.2: Leading edge mode (TRIAC)

2.2.5.2 TRAILING EDGE MODE

When FET/IGBT Mode is enabled, the Dimmer allows power to grow softly after each voltage zero crossing event. The Dimmer controls the turn-off time (or angle) by switching off the FET/IGBT.

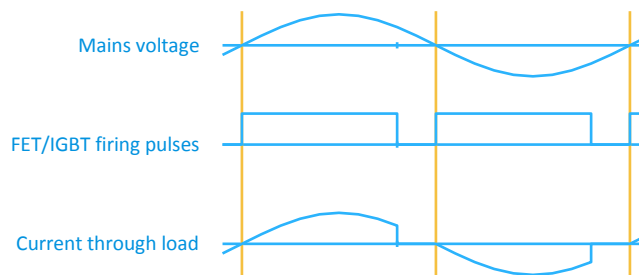


Figure 2.3: Trailing edge mode (FET/IGBT)

2.2.5.3 ZERO CROSSING SYNCHRONIZATION

The Dimmer detects and synchronizes to the AC voltage via a zero-crossing acquisition signal provided by the dimming application. This signal must be connected to pin 15 and be GPIO input level compliant. Multiple single and dual event-per-cycle formats are supported. Fixed phase delays are accepted and easily compensated for through the Z-Wave API.

2.2.6 GENERAL PURPOSE INPUT/OUTPUT

There are 30 General Purpose Input/Output (GPIO) pins grouped into four ports. These pins can be configured individually as Schmitt triggered inputs with/without internal pull-up or open-drain/push-pull outputs. The GPIO pins can be overridden by peripheral functions and each pin is able to drive loads with a minimum of 8mA.

2.2.7 GENERAL PURPOSE TIMER / PULSE WIDTH MODULATOR

A 16-bit General Purpose (GP) auto-reload timer could be provided with either an accurate 4MHz clock or an approximate 32kHz clock. It can be configured to auto-reload a predefined value and may be polled or programmed to generate an interrupt when

the register wraps around. It also serves as a Pulse Width Modulated (PWM) signal generator on pin 15. A simple low frequency Digital-to-Analog Converter (DAC) could be designed using a few external passive components.

2.2.8 INFRA-RED CONTROLLER

The Infra-Red (IR) controller is capable of generating and detecting/learning most coding formats used in A/V equipment. It uses the DMA to minimize the load on the CPU.

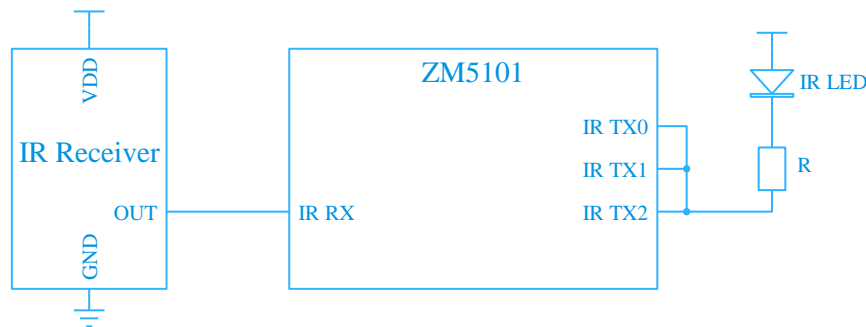


Figure 2.4: IR transmitter and receiver devices

The IR transmitter generates a carrier modulated with a data and streams it to an external LED driver or directly drives an IR LED via 3 pins. The IR receiver is capable of learning the properties of an incoming signal and stores the base-band data.

2.2.9 INTERRUPT CONTROLLER

Fifteen interrupt sources are supported, including external interrupt sources. The interrupts are shared between the user application and the Z-Wave protocol. Priorities for the interrupts are pre-assigned by the Z-Wave protocol implementation. Therefore, constraints for the user application apply.

Table 2.3: Interrupt vector table

| Vector | Interrupt Name | Priority | Resources served |
|--------|-----------------------|----------|---|
| 00 | INT0 | 01 | External interrupt 0 via pin 36 |
| 01 | Timer 0 | 02 | Timer 0 overflow |
| 02 | INT1 | 03 | External interrupt 1 via either pin 37 or pin 36, 37, 38, 39, 41, 42, 43, and 44. Wake-up |
| 03 | Timer 1 | 04 | Timer 1 overflow |
| 04 | UART0 | 05 | UART0 end of RX or TX |
| 05 | Multi | 06 | AES, SPI1, and many more reserved resources |
| 06 | Dimmer | 07 | External interrupt via ZEROX pin 15. Supported by the Dimmer API |
| 07 | General Purpose Timer | 08 | General Purpose Timer overflow |
| 08 | ADC | 09 | Battery monitor, ADC low and high monitor |
| 09 | RF | 10 | RF DMA |
| 10 | UART1 | 11 | UART1 end of RX or TX |
| 11 | USB | 12 | USB data ready |
| 12 | IR | 13 | IR RX data ready/TX done. Supported by the IR API |
| 13 | SPI0 | 14 | SPI0 end of TX |
| 14 | NMI | 00 | Non-Maskable Interrupt for debugger and more |

2.2.10 KEYPAD SCAN CONTROLLER

The chip includes a key scanner to service up to 128 keys. 16 GPIO outputs and 8 GPIO inputs provide all the pull-up resistors and Schmitt trigger inputs required by the full setup.

Table 2.4: Properties of the keypad scan controller

| Property | Description |
|---|--|
| Key matrix size | 8 rows x 16 columns |
| No. of concurrent key press detections | 2 to 8 |
| Hardware setup | 8 horizontal wires (rows) are resistively pulled high by 8 inputs, and are always enabled. 16 vertical wires (columns) are either driven-low by 16 outputs, of which 1 is always enabled and 2 to 16 are optional, or resistively pulled high by 8 inputs. |
| Detection method | An output driven-low will be detected at an input when a key press shorts an intersection point. |
| Interrupts | Supported for key pressed and released events. |
| De-bouncing | Glitches and rapid state changes can be discarded by configuring the minimum key press duration. |
| Wakeup | The controller can be configured to wake up the CPU from the sleep mode after a key press. |

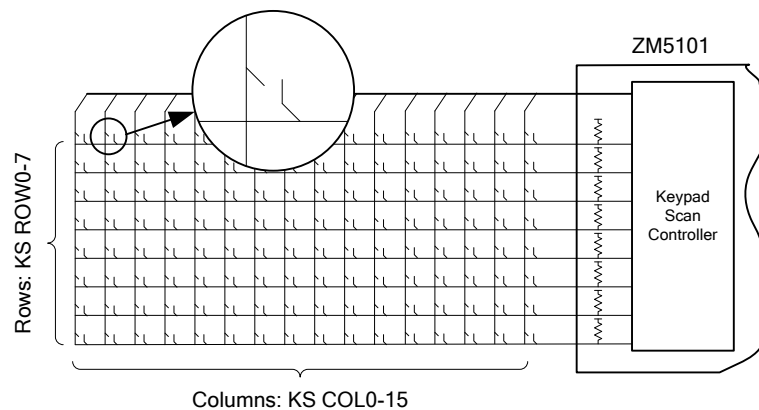


Figure 2.5: Keypad with 8x16 keys

2.2.11 LIGHT-EMITTING DIODE CONTROLLER

The Light-Emitting Diode (LED) controller provides a four-channel PWM generator that can be used to control the current drawn through an LED.

Table 2.5: Properties of the LED controller

| Property | Description |
|--|--|
| Pulse width resolution | 16-bit |
| Frequency | 488 Hz |
| No. of channels | 4 |
| Placement of the pulse within a single period | Normal mode (Pulses of all channels are synchronized to the beginning of a period) Skewed mode (In each consecutive channel, pulses are shifted 25% of the period relative to the previous channel) |
| Drive strength | 8mA |

2.2.12 RESET CONTROLLER

After a reset event, the MCU is reinitialized in less than 1ms. This delay is mostly due to the charge time of the internal and external supply capacitances, and bringing the XTAL clock into a stable oscillation. Multiple events may cause a reset. Therefore, the actual cause is latched by hardware and may be retrieved via software when the system resumes operation. Some reset methods deliberately leave the state of GPIO pins unchanged, while other GPIO pins are set to high impedance with an internal pull-up.

Table 2.6: Supported reset methods

| Reset Cause | Description | GPIO state | Maskable |
|-------------------------------|---|-----------------------------|----------|
| BOR | Reset request generated by Brown-Out-Reset hardware | High impedance with pull-up | No |
| INT1 | Reset request generated when a signal is received on pin INT1, when the chip is in power down mode | Unchanged | Yes |
| Keypad Scan Controller | Reset request generated when any of the KS_ROW pins are being held low, and the chip is in power down mode. This happens when a key is pressed. | Unchanged | Yes |
| POR | Reset request generated by Power-On-Reset hardware | High impedance with pull-up | No |
| RESET_N | Reset request generated by the RESET_N pin being de-asserted | High impedance with pull-up | No |
| Software | Reset request generated in software. | Unchanged | Yes |
| WATCHDOG | Reset request generated by the WATCHDOG Timer timing out | High impedance with pull-up | Yes |
| WUT | Reset request generated by the Wake-Up-Timer timing out | Unchanged | Yes |

2.2.13 SERIAL PERIPHERAL INTERFACE

SPI0 and SPI1 Serial Peripheral Interfaces enable synchronous data transfers between devices.

Table 2.7: SPI signal modes

| SPI Signal | SPI Function, master | SPI Function, slave |
|-------------|----------------------|---------------------|
| MOSI | Data output | Data input |
| MISO | Data input | Data output |
| SCK | Clock output | Clock input |
| SS_N | None | Slave select |

During data transmission, SCK acts as a clock, while 8-bits of data are exchanged between the two devices within 8 cycles of SCK.

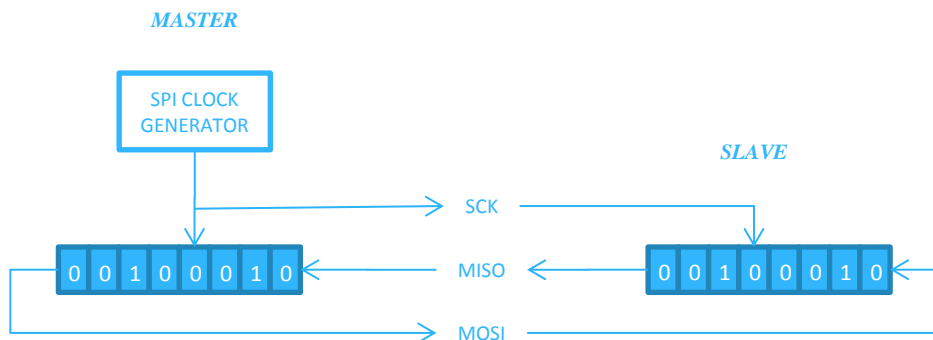


Figure 2.6: Flow of data between SPI master and slave

The module acts as a SPI master when controlling an external device such as an external Non-Volatile Memory (NVM). The slave select (or chip select) of the external NVM could be driven by an available GPIO. SPI0 can be used as both a master and a slave, while SPI1 can only be used as a master. SPI1 slave mode is reserved for In-System Programming (ISP) mode.

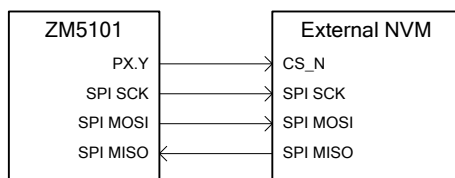


Figure 2.7: Typical interface to slave device

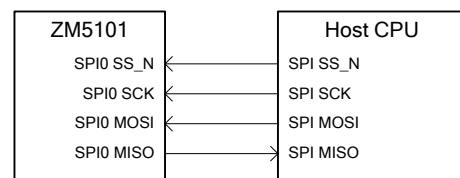


Figure 2.8: Typical interface from master device

2.2.14 SPECIAL FUNCTION REGISTERS

Similar to the 8051 architecture, all the built-in peripherals are configured and controlled with Special Function Register (SFR) circuits that are exposed to the application via the Z-Wave API.

2.2.15 TIMERS

Timer 0 and Timer 1 are 16-bit counters that can be clocked from a fixed internal source or an external source. Except for the use of external gating signals, the complete set of classic 8051 T0/T1 features is available.

Table 2.8: Timer sources

| Timer | Fixed Internal Source | External Source |
|----------------|-----------------------|-----------------|
| Timer 0 | 16 MHz | Pin 18 |
| Timer 1 | 16 MHz | Pin 17 |

2.2.16 UNIVERSAL ASYNCHRONOUS RECEIVER / TRANSMITTER

The Universal Asynchronous Receiver / Transmitter (UART) is a hardware block operating independently of the 8051 CPU. It offers full-duplex data exchange, up to 230.4kbps, with an external host microcontroller requiring an industry standard NRZ asynchronous serial data format. The UART0 interface is available over pin 53 and 54, and UART1 interface over pin 19 and 20 (refer section 4). A data byte is shifted as a start bit, 8 data bits (lsb first), and a stop bit, respectively, with no parity and hardware handshaking. Figure 2.9 shows the waveform of a single serial byte. The UART is compliant with RS-232 when an external level converter is used.



Figure 2.9: UART waveform

2.2.17 UNIVERSAL SERIAL BUS

A Universal Serial Bus (USB) 2.0 full speed interface is available over pin 2 and 3 (refer section 4). The Communication Device Class / Abstract Control Mode (CDC/ACM) provides an emulated virtual COM port to a host. This makes it easy to migrate from legacy RS-232 communication to USB communication. Figure 2.10 shows the two termination resistors necessary to maintain signal integrity of the differential pair and a single pull-up resistor on USB_DP, which indicates a full speed device to the host.

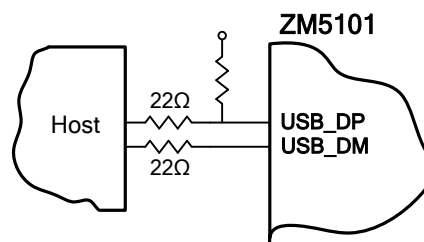


Figure 2.10: USB interface

The controller supports USB suspend mode and remote wakeup. During suspend mode, except for the crystal oscillator clocking at a slower rate and the active USB controller, the entire CPU is powered off. The USB controller uses the DMA for fast data transfer and automatic data retransmissions/CRC to maintain data integrity.

2.2.18 WAKE-UP TIMER

The Wake-Up Timer (WUT) plays an important role in maximizing battery life of applications like Frequently Listening Routing Slave (FLIRS) Z-Wave nodes. It is available to customer applications via the Z-Wave API, and can be configured to wake a sleeping node after 1 to 256 seconds. The programming resolution equals 8-bit fractions of 2 seconds, alternatively 8-bit fractions of 256 seconds. The WUT is automatically calibrated to the system clock when it is operational, maintaining an accuracy of <2%.

2.2.19 WATCHDOG

The watchdog helps prevent the CPU from entering a deadlock state. A timer that is enabled by default achieves this by triggering a reset event in case it overflows. The timer overflows in 1 second, therefore it is essential that the software clear the timer periodically. The watchdog is disabled when the chip is in power down mode, and automatically restarts with a cleared timer when waking up to the active mode.

2.2.20 WIRELESS TRANSCEIVER

The wireless transceiver is a sub-1 GHz ISM narrowband FSK radio, a modem, and a baseband controller. This architecture provides an all-digital direct synthesis transmitter and a low IF digital receiver. The Z-Wave protocol currently utilizes 2-key FSK/GFSK modulation schemes at 9.6/40/100 kbps data rates throughout a span of carrier frequencies from 865.2 to 926.3MHz.

The output power of the transmitter is configurable in the range -24dBm to +6dBm ($V_{DD} = +2.3V$ to $+3.6V$, $T_A = -40$ to $+85^{\circ}C$). An external front-end could be used to further increase the link budget if necessary.

2.3 MEMORY MAP

Figure 2.11 shows an illustration of the byte wise addressable memories that are shared between the user application and the Z-Wave protocol stack. Additional ROM and NVR areas are used for boot code, calibration data, production data, and lock bytes.

Table 2.9: Description of memory blocks

| ID | Memory | Address Method | Exposed during Programming | Description |
|-------|-------------|----------------|----------------------------|--|
| M1-M4 | 128kB Flash | Program Memory | Yes | Flash memory, mapped in 3 banks of 32kB slices over a 32kB common block, one read access per 2 clock cycles. |
| M5-M6 | 16kB RAM | XRAM | Yes | SRAM's split into 4kB and 12kB contiguous blocks |
| M7 | 256B RAM | IRAM | No | Bit addressable SRAM |
| M8 | 128B RAM | XRAM | No | Critical SRAM for data persistency during sleep mode |
| M9 | 256B NVM | (API) | No | Cached high endurance non-volatile data registers |
| M10 | 256B NVR | (API) | Yes | Flash area reserved for the Z-Wave protocol, calibration data, production data, and lock bytes |

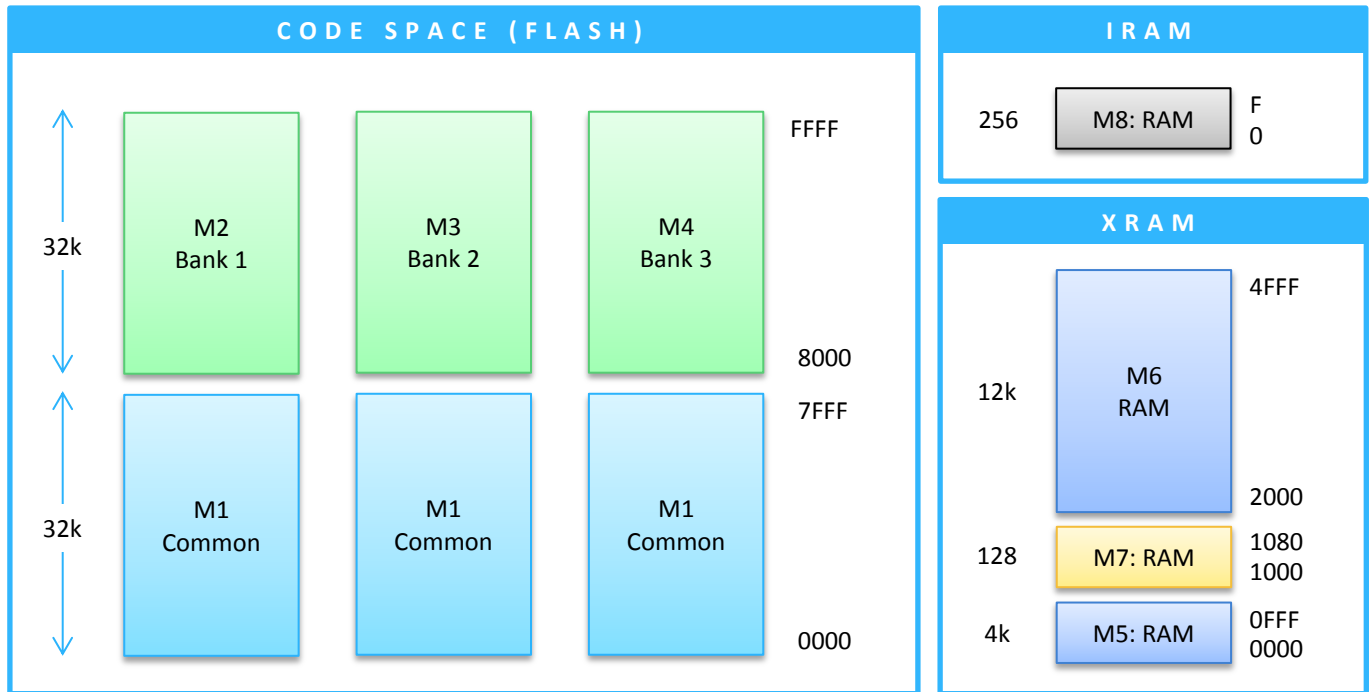


Figure 2.11: Non-API addressable memory blocks

2.4 MODULE PROGRAMMING

The firmware of the ZM5101 SiP can be upgraded wither via SPI1, UART0, or USB interface. [1] In-System Programming is the default mode delivered from the factory.

2.4.1 ENTERING IN-SYSTEM PROGRAMMING MODE

The module can be placed into the In-System Programming (ISP) mode by asserting the active low RESET_N signal for 5.2ms. The programming unit of the module then waits for the “Interface Enable” serial command before activating the ISP mode over either the SPI1 or UART0.

2.4.2 ENTERING AUTO PROGRAMMING MODE

Alternatively, the module can be placed into the Auto Programming Mode (APM) by calling an API function. The programming unit of the module will enter APM immediately after a hardware or software reset. Once the module is in APM, the firmware can be written to the internal flash using the SPI1, UART0 or USB interface.

2.5 POWER SUPPLY REGULATOR

While the supply to the digital I/O circuits is unregulated, on-chip low-dropout regulators derive all the 1.5 V and 2.5 V internal supplies required by the Micro-Controller Unit (MCU) core logic, non-volatile data registers, flash, and the analogue circuitry.

An illustration of an application example using the ZM5101 SiP implementation is shown in Figure 3.1. It is strongly recommended that the power supply is decoupled sufficiently.

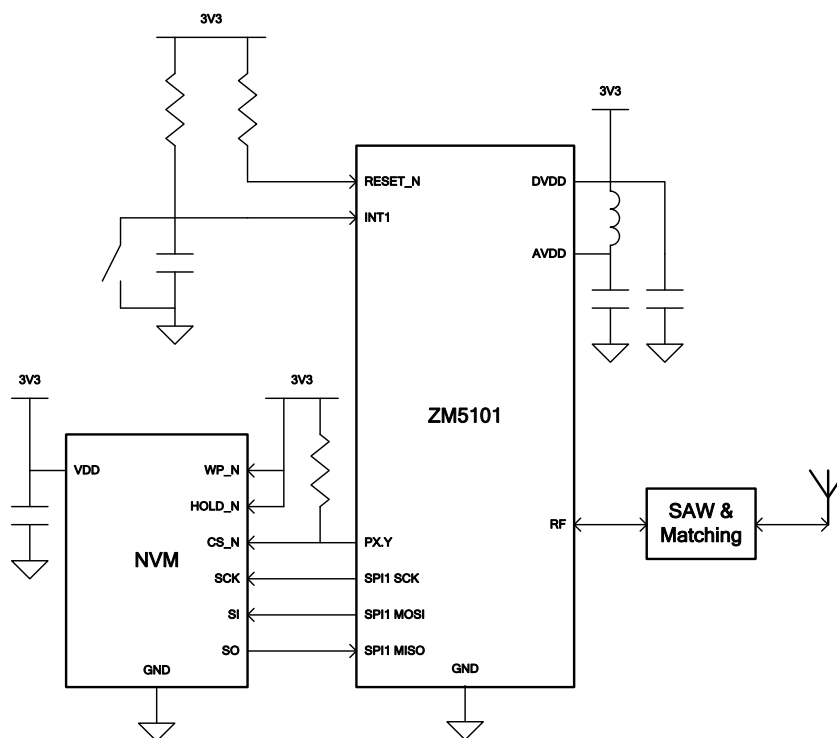


Figure 3.1: Example of a standalone application with an external antenna

4 PIN CONFIGURATION

The layout of the pins on the ZM5101 SiP is shown in Figure 4.1.

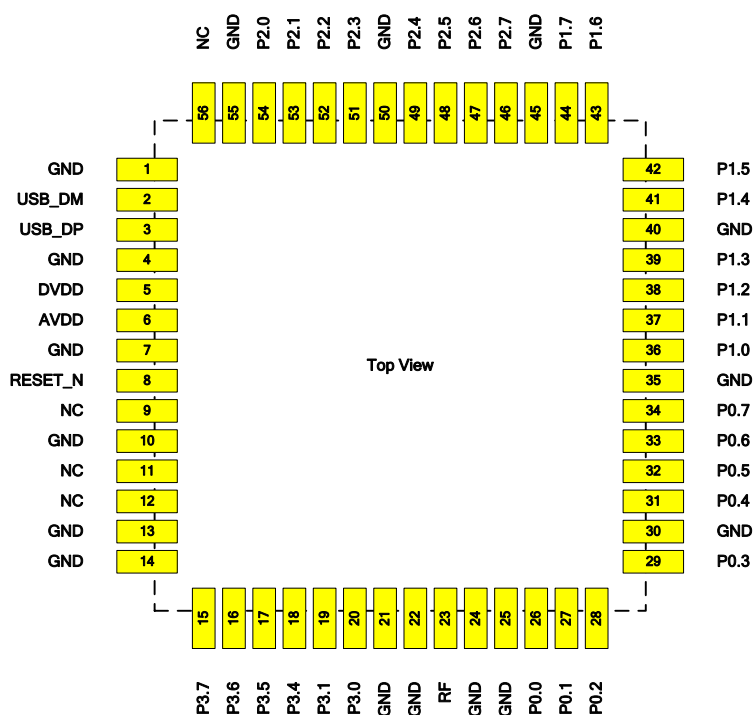


Figure 4.1: Pin layout (top view)

4.1 PIN FUNCTIONALITY

Table 4.1: Power, ground, and no connect signals

| Pin Name | Pin Location | Type ¹ | Function |
|------------------------|---|-------------------|--|
| AV_{DD} | 6 | S | Module analog power supply. |
| DV_{DD} | 5 | S | Module digital power supply. |
| GND | 1, 4, 7, 10, 13, 14, 21, 22, 24, 25, 30, 35, 40, 45, 50, 55 | S | Ground. Must be connected to the ground plane. |
| NC | 9, 11, 12, 56 | - | Leave electrically unconnected. |

Table 4.2: Module control signals

| Pin Name | Pin Location | Type | Function |
|----------------|--------------|------|--|
| RESET_N | 8 | I | Active low signal that places the module in a reset state. |

¹ I = Input, O = Output, D+ = Differential Plus, D- = Differential Minus, S = Supply

Table 4.3: SPI0 interface signals

| Pin Name | Pin Location | Type | Function in Reset State | Function in Active State |
|------------------|--------------|------|---------------------------------------|--|
| SPI0 SS_N | 20 | I | High impedance with internal pull-up. | SPI0 Slave Select. Can be optionally used as a chip select input when configured as a slave. |
| SPI0 SCK | 46 | I/O | High impedance with internal pull-up. | SPI0 Clock. Output in master mode and input in slave mode. Can be remapped to pin 53. |
| SPI0 MISO | 47 | I/O | High impedance with internal pull-up. | Master-In-Slave-Out serial data. Input in master mode and output in slave mode. Can be remapped to pin 54. |
| SPI0 MOSI | 48 | I/O | High impedance with internal pull-up. | Master-Out-Slave-In serial data. Output in master mode and input in slave mode. |

Table 4.4: SPI1 interface signals

| Pin Name | Pin Location | Type | Function in Reset State | Function in Active State |
|------------------|--------------|------|--|---|
| SPI1 SCK | 49 | I/O | SPI1 Clock input with internal pull-up. | SPI1 Clock. Output in master mode. |
| SPI1 MISO | 51 | I/O | Serial data transmit when in SPI1 ISP mode, high impedance otherwise with internal pull-up. | Master-In-Slave-Out serial data. Input in master mode. |
| SPI1 MOSI | 52 | I/O | Waits for the "Interface Enable" serial command after 5.2ms. Enters SPI1 ISP mode after command is received from the host. | Master-Out-Slave-In serial data. Output in master mode. |

Table 4.5: UART0 interface signals

| Pin Name | Pin Location | Type | Function in Reset State | Function in Active State |
|-----------------|--------------|------|---|--|
| UART0 RX | 54 | I | Waits for the "Interface Enable" serial command after 5.2ms. Enters UART0 ISP mode after command is received from the host. | Receive data from host serial port. Can be remapped to pin 18. |
| UART0 TX | 53 | O | Serial data transmit when in UART0 ISP mode, high impedance otherwise. | Transmit data to host serial port. Can be remapped to pin 17. |

Table 4.6: UART1 interface signals

| Pin Name | Pin Location | Type | Function in Reset State | Function in Active State |
|-----------------|--------------|------|---------------------------------------|-------------------------------------|
| UART1 RX | 20 | I | High impedance with internal pull-up. | Receive data from host serial port. |
| UART1 TX | 19 | O | High impedance with internal pull-up. | Transmit data to host serial port. |

Table 4.7: USB interface signals

| Pin Name | Pin Location | Type | Function in Reset State | Function in Active State |
|---------------|--------------|------|---|--|
| USB_DP | 3 | D | ISP when in APM mode, high impedance with internal pull-up otherwise. | USB 2.0 full-speed positive differential signal. |
| USB_DM | 2 | D | ISP when in APM mode, high impedance with internal pull-up otherwise. | USB 2.0 full-speed negative differential signal. |

Table 4.8: ADC interface signals

| Pin Name | Pin Location | Type | Function in Reset State | Function in Active State |
|-------------|--------------|------|---------------------------------------|--|
| ADC0 | 18 | I | High impedance with internal pull-up. | Analog-to-Digital converter input. |
| ADC1 | 17 | I | High impedance with internal pull-up. | Analog-to-Digital converter input. |
| ADC2 | 16 | I | High impedance with internal pull-up. | Analog-to-Digital converter input or lower reference voltage. |
| ADC3 | 15 | I | High impedance with internal pull-up. | Analog-to-Digital converter input or higher reference voltage. |

Table 4.9: External interrupt interface signals

| Pin Name | Pin Location | Type | Function in Reset State | Function in Active State |
|-------------|-----------------------------------|------|---------------------------------------|--|
| INT0 | 36 | I | High impedance with internal pull-up. | External interrupt 0 input. High priority. |
| INT1 | 36, 37, 38, 39, 41, 42, 43, 44 | I | High impedance with internal pull-up. | External interrupt 1 input. Low priority. |

Table 4.10: Timer interface signals

| Pin Name | Pin Location | Type | Function in Reset State | Function in Active State |
|-------------------|--------------|------|---------------------------------------|-------------------------------|
| T0 EXT CLK | 18 | I | High impedance with internal pull-up. | Timer 0 external clock input. |
| T1 EXT CLK | 17 | I | High impedance with internal pull-up. | Timer 1 external clock input. |

Table 4.11: IR interface signals

| Pin Name | Pin Location | Type | Function in Reset State | Function in Active State |
|---------------|--------------|------|---------------------------------------|--|
| IR RX | 19 | I | High impedance with internal pull-up. | Infra-Red receiver input for learning mode. |
| IR TX0 | 18 | O | High impedance with internal pull-up. | Infra-Red transmitter 0 output with 16mA driver. |
| IR TX1 | 17 | O | High impedance with internal pull-up. | Infra-Red transmitter 1 output with 16mA driver. |
| IR TX2 | 16 | O | High impedance with internal pull-up. | Infra-Red transmitter 2 output with 16mA driver. |

Table 4.12: PWM interface signals

| Pin Name | Pin Location | Type | Function in Reset State | Function in Active State |
|------------|--------------|------|---------------------------------------|--|
| PWM | 15 | O | High impedance with internal pull-up. | Pulse width modulator output. Can be remapped to pin 36. |

Table 4.13: LED controller interface signals

| Pin Name | Pin Location | Type | Function in Reset State | Function in Active State |
|-----------------|--------------|------|---------------------------------------|--------------------------|
| PWM LED0 | 31 | O | High impedance with internal pull-up. | LED controller output. |
| PWM LED1 | 32 | O | High impedance with internal pull-up. | LED controller output. |
| PWM LED2 | 33 | O | High impedance with internal pull-up. | LED controller output. |
| PWM LED3 | 34 | O | High impedance with internal pull-up. | LED controller output. |

Table 4.14: Dimmer interface signals

| Pin Name | Pin Location | Type | Function in Reset State | Function in Active State |
|--------------|--------------|------|---------------------------------------|--|
| TRIAC | 16 | O | High impedance with internal pull-up. | Dimmer output. Firing pulse to TRIAC/FET/IGBT. |
| ZEROX | 15 | I | High impedance with internal pull-up. | Zero-cross detection input. |

Table 4.15: RF interface signals

| Pin Name | Pin Location | Type | Function in Reset State | Function in Active State |
|-----------|--------------|------|---------------------------------------|--------------------------|
| RF | 23 | I/O | High impedance with internal pull-up. | RF input and output. |

Table 4.16: Keypad scanner interface signals

| Pin Name | Pin Location | Type | Function in Reset State | Function in Active State |
|----------|--------------|------|---|----------------------------------|
| KS COL0 | 26 | O | High impedance with internal pull-up. | Keypad Scanner Column 0 output. |
| KS COL1 | 27 | O | High impedance with internal pull-up. | Keypad Scanner Column 1 output. |
| KS COL2 | 28 | O | High impedance with internal pull-up. | Keypad Scanner Column 2 output. |
| KS COL3 | 29 | O | High impedance with internal pull-up. | Keypad Scanner Column 3 output. |
| KS COL4 | 31 | O | High impedance with internal pull-up. | Keypad Scanner Column 4 output. |
| KS COL5 | 32 | O | High impedance with internal pull-up. | Keypad Scanner Column 5 output. |
| KS COL6 | 33 | O | High impedance with internal pull-up. | Keypad Scanner Column 6 output. |
| KS COL7 | 34 | O | High impedance with internal pull-up. | Keypad Scanner Column 7 output. |
| KS COL8 | 15 | O | High impedance with internal pull-up. | Keypad Scanner Column 8 output. |
| KS COL9 | 16 | O | High impedance with internal pull-up. | Keypad Scanner Column 9 output. |
| KS COL10 | 17 | O | High impedance with internal pull-up. | Keypad Scanner Column 10 output. |
| KS COL11 | 18 | O | High impedance with internal pull-up. | Keypad Scanner Column 11 output. |
| KS COL12 | 19 | O | High impedance with internal pull-up. | Keypad Scanner Column 12 output. |
| KS COL13 | 20 | O | High impedance with internal pull-up. | Keypad Scanner Column 13 output. |
| KS COL14 | 53 | O | Serial data transmit when in UART0 ISP mode, high impedance with internal pull-up otherwise. | Keypad Scanner Column 14 output. |
| KS COL15 | 54 | O | Waits for the "Interface Enable" serial command after 5.2ms. Enters UART0 ISP mode after command is received from the host. | Keypad Scanner Column 15 output. |
| KS ROW0 | 36 | I | High impedance with internal pull-up. | Keypad Scanner Row 0 input. |
| KS ROW1 | 37 | I | High impedance with internal pull-up. | Keypad Scanner Row 1 input. |
| KS ROW2 | 38 | I | High impedance with internal pull-up. | Keypad Scanner Row 2 input. |
| KS ROW3 | 39 | I | High impedance with internal pull-up. | Keypad Scanner Row 3 input. |
| KS ROW4 | 41 | I | High impedance with internal pull-up. | Keypad Scanner Row 4 input. |
| KS ROW5 | 42 | I | High impedance with internal pull-up. | Keypad Scanner Row 5 input. |
| KS ROW6 | 43 | I | High impedance with internal pull-up. | Keypad Scanner Row 6 input. |
| KS ROW7 | 44 | I | High impedance with internal pull-up. | Keypad Scanner Row 7 input. |

Table 4.17: GPIO interface signals

| Pin Name | Pin Location | Type | Function in Reset State | Function in Active State |
|----------|--------------|------|---|-----------------------------------|
| P0.0 | 26 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P0.1 | 27 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P0.2 | 28 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P0.3 | 29 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P0.4 | 31 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P0.5 | 32 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P0.6 | 33 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P0.7 | 34 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P1.0 | 36 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P1.1 | 37 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P1.2 | 38 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P1.3 | 39 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P1.4 | 41 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P1.5 | 42 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P1.6 | 43 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P1.7 | 44 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P2.0 | 54 | I/O | Waits for the "Interface Enable" serial command after 5.2ms. Enters UART0 ISP mode after command is received from the host. | General purpose input and output. |
| P2.1 | 53 | I/O | Serial data transmit when in UART0 ISP mode, high impedance with internal pull-up otherwise. | General purpose input and output. |
| P2.2 | 52 | I/O | Waits for the "Interface Enable" serial command after 5.2ms. Enters SPI1 ISP mode after command is received from the host. | General purpose input and output. |
| P2.3 | 51 | I/O | Serial data transmit when in SPI1 ISP mode, high impedance with internal pull-up otherwise. | General purpose input and output. |
| P2.4 | 49 | I/O | SPI1 Clock input with internal pull-up. | General purpose input and output. |
| P2.5 | 48 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P2.6 | 47 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P2.7 | 46 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P3.0 | 20 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P3.1 | 19 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P3.4 | 18 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P3.5 | 17 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P3.6 | 16 | I/O | High impedance with internal pull-up. | General purpose input and output. |
| P3.7 | 15 | I/O | High impedance with internal pull-up. | General purpose input and output. |

5 ELECTRICAL CHARACTERISTICS

This section describes the electrical parameters of the ZM5101 SiP module.

5.1 TEST CONDITIONS

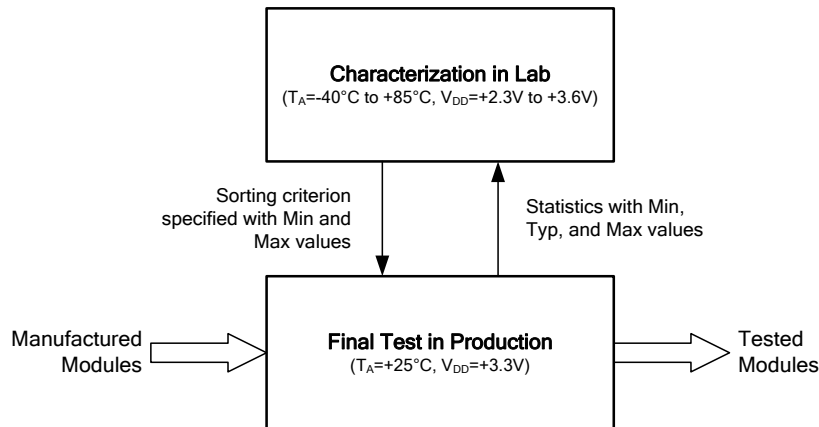


Figure 5.1: Testing flow

The following conditions apply for characterization in the lab, unless otherwise noted.

1. Ambient temperature $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
2. Supply voltage $V_{DD} = +2.3\text{V}$ to $+3.6\text{V}$
3. All tests are carried out on the ZDB5101 Z-Wave Development Board. [2]
4. Conducted transmission power is measured with no SAW filter for 868.4, 908.4, and 921.4MHz at 50Ω
5. Conducted receiver sensitivity is measured with no SAW filter for 868.4, 908.4, and 921.4MHz at 50Ω

The following conditions apply for the final test in production, unless otherwise noted.

1. Ambient temperature $T_A = +25^{\circ}\text{C}$
2. Supply voltage $V_{DD} = +3.3\text{V}$
3. Conducted transmission power is measured with no SAW filter for 868.4, 908.4, and 921.4MHz at 50Ω
4. Conducted receiver sensitivity is measured with no SAW filter for 868.4, 908.4, and 921.4MHz at 50Ω

5.1.1 TYPICAL VALUES

Unless otherwise specified, typical data refer to the mean of a data set measured at an ambient temperature of $T_A = 25^{\circ}\text{C}$ and supply voltage of $V_{DD} = +3.3\text{V}$.

5.1.2 MINIMUM AND MAXIMUM VALUES

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by a final test in production on 100% of the devices at an ambient temperature of $T_A = 25^{\circ}\text{C}$ and supply voltage of $V_{DD} = +3.3\text{V}$.

For data based on measurements, the minimum and maximum values represent the mean value plus or minus three times the standard deviation ($\mu \pm 3\sigma$).

5.2 ABSOLUTE MAXIMUM RATINGS

The absolute ratings specify the limits beyond which the module may not be functional. Exposure to absolute maximum conditions for extended periods may cause permanent damage to the module.

Table 5.1: Voltage characteristics

| Symbol | Description | Min | Max | Unit |
|-------------|---|------|---------|------|
| V_{DD} | Main supply voltage | -0.3 | +3.6 | V |
| V_{IN} | Voltage applied on any input pin | -0.3 | +3.6 | V |
| I_{IN} | Current limit when over driving the input ($V_{IN-GND} > V_{DD-GND}$) | - | +20.0 | mA |
| P_{RF-IN} | Radio receiver input power | - | +10.0 | dBm |
| ESD_{HBM} | JEDEC JESD22-A114F Human Body Model | - | +2000.0 | V |
| ESD_{MM} | JEDEC JESD22-A115C Machine Model | - | +200.0 | V |
| ESD_{CDM} | JEDEC JESD22-C101E Field-Induced Charged-Device Model | - | +500.0 | V |

Table 5.2: Current characteristics

| Symbol | Description | Min | Max | Unit |
|-----------|---|------|------|------|
| I_{VDD} | Sum of current into all VDD power supply pins | - | +120 | mA |
| I_{GND} | Sum of the current out of all GND ground pins | -120 | - | mA |

Table 5.3: Thermal characteristics

| Symbol | Description | Min | Max | Unit |
|---------------|---------------------------|-----|------|------|
| T_J | Junction temperature | -55 | +125 | °C |
| $T_{STORAGE}$ | Storage temperature range | -40 | +85 | °C |

5.3 GENERAL OPERATING RATINGS

The operating ratings indicate the conditions where the module is guaranteed to be functional.

Table 5.4: Recommended operating conditions

| Symbol | Description | Min | Typ | Max | Unit |
|---------------|--|-------|-------|-------|------|
| V_{DD} | Standard operating supply voltage | +2.3 | +3.3 | +3.6 | V |
| V_{DD_USB} | Standard operating supply voltage when USB PHY is used | +3.0 | +3.3 | +3.6 | V |
| f_{SYS} | Internal clock frequency | - | 32.0 | - | MHz |
| T_A | Ambient operating temperature | -40.0 | +25.0 | +85.0 | °C |

5.4 CURRENT CONSUMPTION

Measured at an ambient temperature of $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ and a supply voltage of $V_{DD} = +2.3\text{V}$ to $+3.6\text{V}$.

Table 5.5: Current consumption in active modes

| Symbol | Description | Min | Typ | Max | Unit |
|------------------|--|-----|------|------|------|
| I_{DD_ACTIVE} | MCU running at 32MHz | - | 14.9 | 16.0 | mA |
| I_{DD_RX} | MCU and radio receiver active | - | 32.4 | 35.5 | mA |
| $I_{DD_TX_24}$ | MCU and radio transmitter active, -24dBm | - | 27.7 | - | mA |
| $I_{DD_TX_6}$ | MCU and radio transmitter active, +6dBm | - | 45.4 | - | mA |

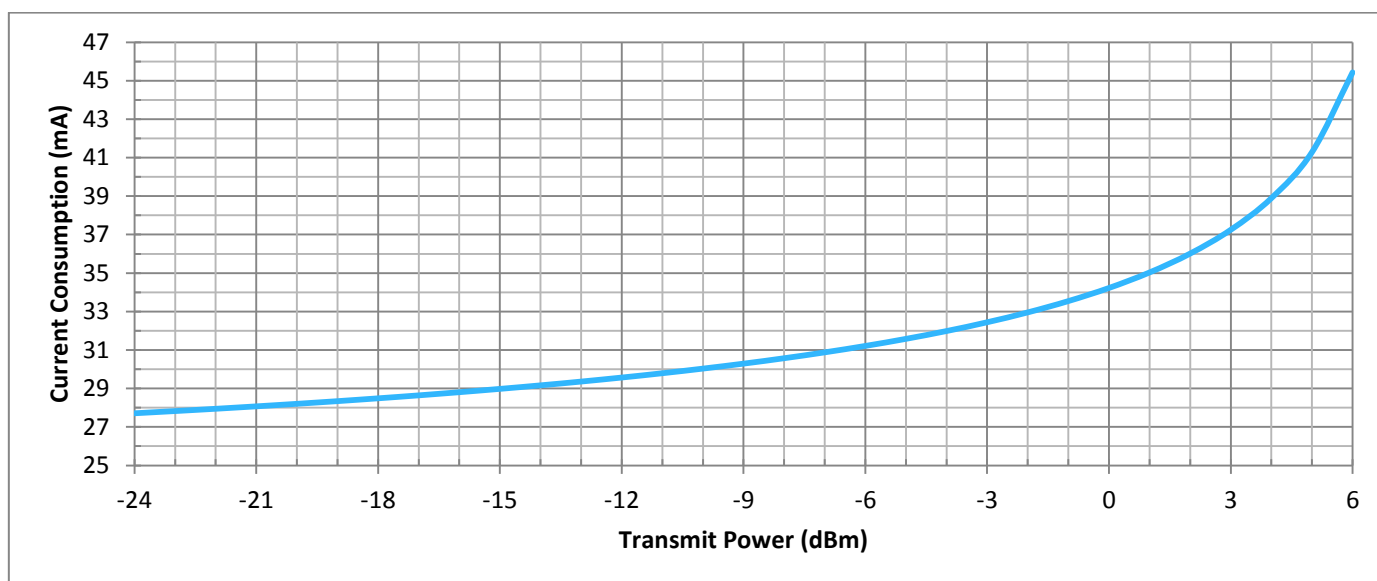


Figure 5.2: Typical current consumption vs. transmit power

Table 5.6: Current consumption in power saving modes

| Symbol | Description | Min | Typ | Max | Unit |
|--------------------|---|-----|-----|-----|---------|
| I_{DD_SLEEP} | Module in sleep state | - | 1.0 | 1.6 | μ A |
| I_{USB_SLEEP} | USB suspend mode with state persistency, and system clock | - | 2.0 | 2.3 | mA |
| I_{DD_WUT} | Module in sleep state with wake-up timer active | - | 2.0 | - | μ A |
| $I_{DD_WUT_RAM}$ | Module in sleep state with wake-up timer and 128 bytes of critical RAM active | - | 2.1 | - | μ A |

Table 5.7: Current consumption during programming

| Symbol | Description | Min | Typ | Max | Unit |
|---------------------|-----------------------|-----|-----|-----|------|
| $I_{DD_PGM_SPI}$ | Programming via SPI1 | - | 15 | - | mA |
| $I_{DD_PGM_UART}$ | Programming via UART0 | - | 15 | - | mA |
| $I_{DD_PGM_USB}$ | Programming via USB | - | 15 | - | mA |

5.5 SYSTEM TIMING

Measured at an ambient temperature of $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ and a supply voltage of $V_{DD} = +2.3\text{V}$ to $+3.6\text{V}$.

Table 5.8: Transition between operating modes

| Symbol | Description | Min | Typ | Max | Unit |
|----------------------------|--|-----|-----|-----|---------------|
| $t_{\text{ACTIVE_SLEEP}}$ | Transition time from the active state to the sleep state | - | - | 125 | ns |
| $t_{\text{SLEEP_ACTIVE}}$ | Transition time from the sleep state to the active state ready to execute code | - | - | 160 | μs |

Table 5.9: System start-up time

| Symbol | Description | Min | Typ | Max | Unit |
|----------------------------|---|-----|-----|------|------|
| V_{POR} | Power-on-Reset (POR) threshold on rising supply voltage at which the reset signal is deasserted | - | - | +2.3 | V |
| $t_{\text{RESET_ACTIVE}}$ | Transition time from the reset state to the active state ready to execute code with a power rise time not exceeding $10\mu\text{s}$ | - | - | 1.0 | ms |

Table 5.10: Wake-up timer accuracy

| Symbol | Description | Min | Typ | Max | Unit |
|--------------------------|--|-----|-----|-----|------|
| $t_{\text{WUT_OFFSET}}$ | Wake-up timer offset, Y-axis intercept of time vs. setting curve | - | - | 40 | ms |
| $t_{\text{WUT_SCALE}}$ | Wake-up timer absolute error | - | - | 2 | % |

Table 5.11: Reset timing requirements

| Symbol | Description | Min | Typ | Max | Unit |
|-------------------------|---|-----|-----|-----|------|
| $t_{\text{RST_PULSE}}$ | Duration to assert RESET_N to guarantee a full system reset | 20 | - | - | ns |

Table 5.12: Programming time

| Symbol | Description | Min | Typ | Max | Unit |
|--------------------------|--|-----|-----|------|------|
| $t_{\text{ERASE_FULL}}$ | Time taken to erase the entire flash memory | - | - | 44.1 | ms |
| $t_{\text{PGM_FULL}}$ | Time taken to program the entire flash memory over SPI1 at 4MHz including a full erase | - | - | 1.4 | s |

5.6 NON-VOLATILE MEMORY RELIABILITY

Qualified for an ambient temperature of $T_A = +25^{\circ}\text{C}$ and a supply voltage of $V_{DD} = +3.3\text{V}$. The on-chip memory is based on SuperFlash® technology.

Table 5.13: On-chip flash

| Symbol | Description | Min | Typ | Max | Unit |
|--------------------------------|--|-------|-----|-----|--------|
| END _{FLASH} | Endurance, erase cycles before failure | 10000 | - | - | cycles |
| RET _{FLASH-LT} | Data retention | 100 | - | - | years |
| RET _{FLASH-HT} | Data retention (<i>Qualified for a junction temperature of $T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$</i>) | 10 | - | - | years |

Table 5.14: On-chip M9 high endurance NVM

| Symbol | Description | Min | Typ | Max | Unit |
|------------------------------|--|--------|-----|-----|--------|
| END _{NVM} | Endurance, erase cycles before failure | 100000 | - | - | cycles |
| RET _{NVM-LT} | Data retention | 100 | - | - | years |
| RET _{NVM-HT} | Data retention (<i>Qualified for a junction temperature of $T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$</i>) | 10 | - | - | years |

5.7 ANALOG-TO-DIGITAL CONVERTER

Measured at an ambient temperature of $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ and a supply voltage of $V_{DD} = +2.3\text{V}$ to $+3.6\text{V}$.

Table 5.15: 12-bit ADC characteristics

| Symbol | Description | Min | Max | Unit |
|---------------------------|--|-----------------|----------|-------|
| V _{BG} | Internal reference voltage | +1.20 | +1.30 | V |
| V _{REF+} | Upper reference input voltage | $V_{DD} - 0.90$ | V_{DD} | V |
| V _{REF-} | Lower reference input voltage | 0.00 | +1.20 | V |
| DNL _{ADC} | Differential non-linearity | -1.00 | +1.00 | LSB |
| ACC _{8b} | Accuracy when sampling 20ksps with 8-bit resolution | -2.00 | 2.00 | LSB |
| ACC _{12b} | Accuracy when sampling 10ksps with 12-bit resolution | -5.00 | 5.00 | LSB |
| f _{S-8b} | 8-bit sampling rate | - | 0.02 | Msp/s |
| f _{S-12b} | 12-bit sampling rate | - | 0.01 | Msp/s |

5.8 DC CHARACTERISTICS

Measured at an ambient temperature of $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

Table 5.16: Digital input characteristics, supply voltage of $V_{DD}=+2.3V$ to $+3.0V$

| Symbol | Description | Min | Max | Unit |
|--------------|---|--------|--------|------------|
| V_{IH} | Logical 1 input voltage high level | +1.85 | - | V |
| V_{IL} | Logical 0 input voltage low level | - | +0.75 | V |
| V_{IF} | Falling input trigger threshold | +0.75 | +1.05 | V |
| V_{IR} | Rising edge trigger threshold | +1.35 | +1.85 | V |
| V_{HYS} | Schmitt trigger voltage hysteresis | +0.55 | +0.85 | V |
| I_{IH} | Logical 1 input high level current leakage | - | +7.00 | μA |
| I_{IL-NPU} | Logical 0 input low level current leakage (<i>no internal pull-up resistor</i>) | -7.00 | - | μA |
| I_{IL-PU} | Logical 0 input low level current leakage (<i>with internal pull-up resistor</i>) | +35.00 | +90.00 | μA |
| PU_{IN} | Internal pull-up resistance ($T_A=+25^\circ C$) | 20.00 | 30.00 | k Ω |
| C_{IN} | Pin input capacitance | - | 15.00 | pF |

Table 5.17: Digital output characteristics, supply voltage of $V_{DD}=+2.3V$ to $+3.0V$

| Symbol | Description | Min | Max | Unit |
|-------------|---|-------|-------|------|
| V_{OH} | Logical 1 output voltage high level | +1.9 | - | V |
| V_{OL} | Logical 0 output voltage low level | - | +0.4 | V |
| I_{OH-LP} | Logical 1 output high level current sourcing | - | +6.0 | mA |
| I_{OL-LP} | Logical 0 output low level current sinking | -6.0 | - | mA |
| I_{OH-HP} | Logical 1 output high level current sourcing (<i>Pin15 to pin 18</i>) | - | +12.0 | mA |
| I_{OL-HP} | Logical 0 output low level current sinking (<i>Pin15 to pin 18</i>) | -12.0 | - | mA |

Table 5.18: Digital input characteristics, supply voltage of $V_{DD}=+3.0V$ to $+3.6V$

| Symbol | Description | Min | Max | Unit |
|--------------|---|--------|---------|------------|
| V_{IH} | Logical 1 input voltage high level | +2.10 | - | V |
| V_{IL} | Logical 0 input voltage low level | - | +0.90 | V |
| V_{IF} | Falling input trigger threshold | +0.90 | +1.30 | V |
| V_{IR} | Rising edge trigger threshold | +1.60 | +2.10 | V |
| V_{HYS} | Schmitt trigger voltage hysteresis | +0.65 | +0.95 | V |
| I_{IH} | Logical 1 input high level current leakage | - | +10.00 | μA |
| I_{IL-NPU} | Logical 0 input low level current leakage (<i>no internal pull-up resistor</i>) | -10.00 | - | μA |
| I_{IL-PU} | Logical 0 input low level current leakage (<i>with internal pull-up resistor</i>) | +40.00 | +120.00 | μA |
| PU_{IN} | Internal pull-up resistance ($T_A=+25^\circ C$) | 15.00 | 20.00 | k Ω |
| C_{IN} | Pin input capacitance | - | 15.00 | pF |

Table 5.19: Digital output characteristics, supply voltage of $V_{DD}=+3.0V$ to $+3.6V$

| Symbol | Description | Min | Max | Unit |
|-------------|---|-------|-------|------|
| V_{OH} | Logical 1 output voltage high level | +2.4 | - | V |
| V_{OL} | Logical 0 output voltage low level | - | +0.4 | V |
| I_{OH-LP} | Logical 1 output high level current sourcing | - | +8.0 | mA |
| I_{OL-LP} | Logical 0 output low level current sinking | -8.0 | - | mA |
| I_{OH-HP} | Logical 1 output high level current sourcing (<i>Pin15 to pin 18</i>) | - | +16.0 | mA |
| I_{OL-HP} | Logical 0 output low level current sinking (<i>Pin15 to pin 18</i>) | -16.0 | - | mA |

5.9 RF CHARACTERISTICS

5.9.1 TRANSMITTER

Measured at an ambient temperature of $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ and a supply voltage of $V_{DD} = +2.3\text{V}$ to $+3.6\text{V}$. The transmission power is adjusted by setting the value of the RFPOW register.

Table 5.20: Transmit performance

| Symbol | Description | Min | Typ | Max | Unit |
|----------------------------|--|-------|--------|-----|--------|
| P₆₃ | RF output power delivered to the antenna, RFPOW=63 | +5.3 | +5.9 | - | dBm |
| P₀₁ | RF output power delivered to the antenna, RFPOW=01 | -24.8 | -23.7 | - | dBm |
| P_{H2-63} | 2 nd harmonic, RFPOW=63 | - | -25.7 | - | dBc |
| P_{H2-48} | 2 nd harmonic, RFPOW=48 | - | -28.0 | - | dBc |
| P_{H2-32} | 2 nd harmonic, RFPOW=32 | - | -32.2 | - | dBc |
| P_{H2-20} | 2 nd harmonic, RFPOW=20 | - | -38.1 | - | dBc |
| P_{H2-8} | 2 nd harmonic, RFPOW=8 | - | -39.8 | - | dBc |
| P_{H3-63} | 3 rd harmonic, RFPOW=63 | - | -37.9 | - | dBc |
| P_{H3-48} | 3 rd harmonic, RFPOW=48 | - | -39.5 | - | dBc |
| P_{H3-32} | 3 rd harmonic, RFPOW=32 | - | -40.8 | - | dBc |
| P_{H3-20} | 3 rd harmonic, RFPOW=20 | - | -43.4 | - | dBc |
| P_{H3-8} | 3 rd harmonic, RFPOW=8 | - | -42.9 | - | dBc |
| PN_{30kHz} | Phase noise at 30kHz | - | -88.7 | - | dBc/Hz |
| PN_{100kHz} | Phase noise at 100kHz | - | -96.9 | - | dBc/Hz |
| PN_{1MHz} | Phase noise at 1MHz | - | -107.9 | - | dBc/Hz |
| PN_{10MHz} | Phase noise at 10MHz | - | -115.1 | - | dBc/Hz |
| PN_{20MHz} | Phase noise at 100MHz | - | -115.7 | - | dBc/Hz |
| BW_{9.6} | Channel bandwidth, 9.6kbps | - | 90.0 | - | kHz |
| BW₄₀ | Channel bandwidth, 40kbps | - | 90.0 | - | kHz |
| BW₁₀₀ | Channel bandwidth, 100kbps | - | 110.0 | - | kHz |

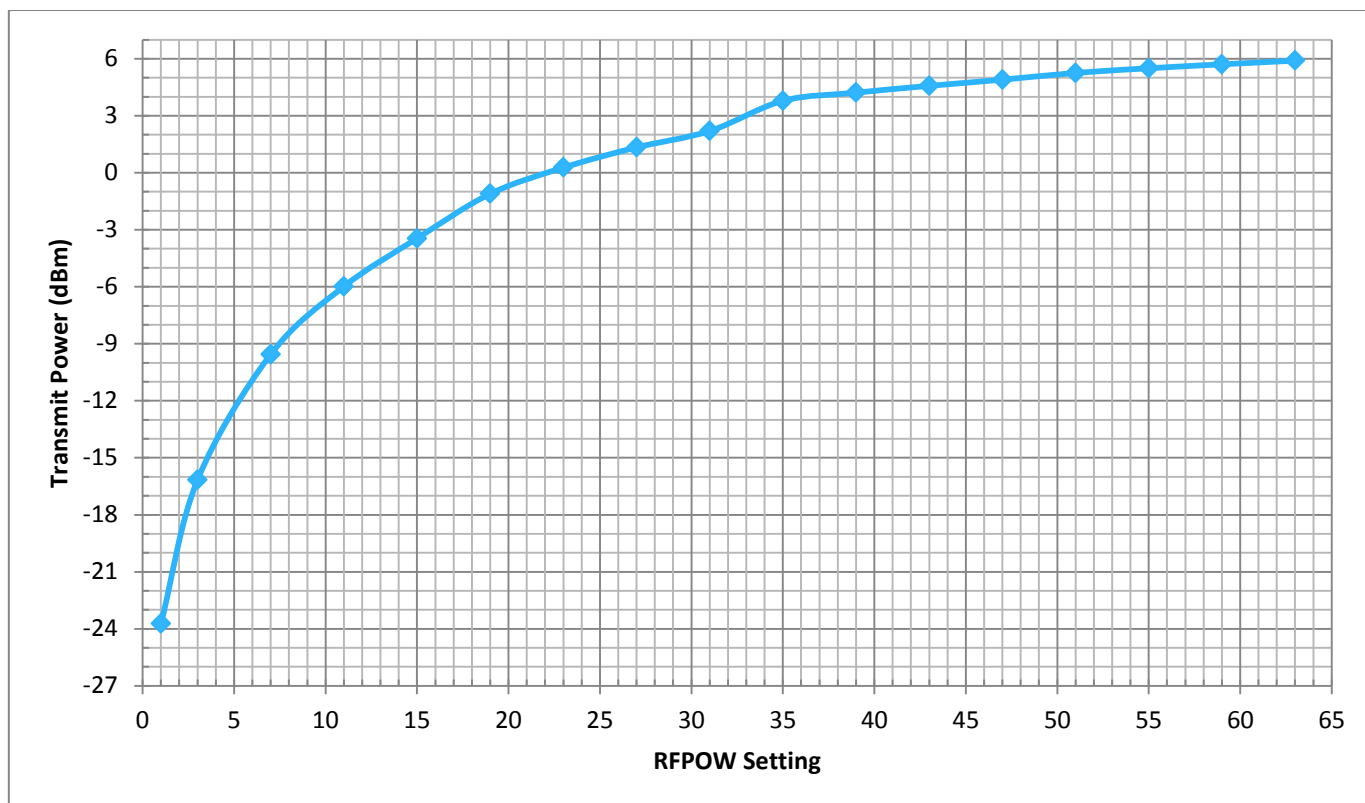


Figure 5.3: Typical transmit power vs. RFPOW setting

It is mandatory to calibrate the transmitter in production. Refer to [3] for more information.

5.9.2 RECEIVER

Measured over an ambient temperature of $T_A=+25^{\circ}\text{C}$ and a supply voltage of $V_{DD}=+2.3\text{V}$ to $+3.6\text{V}$.

Table 5.21: Receiver sensitivity

| Symbol | Description | Min | Typ | Max | Unit |
|-----------|--|-----|--------|--------|------|
| $P_{9.6}$ | Sensitivity at 9.6kbps, received power, FER < 1% | - | -104.5 | -101.9 | dBm |
| P_{40} | Sensitivity at 40kbps, received power, FER < 1% | - | -100.6 | -98.0 | dBm |
| P_{100} | Sensitivity at 100kbps, received power, FER < 1% | - | -94.3 | -91.5 | dBm |

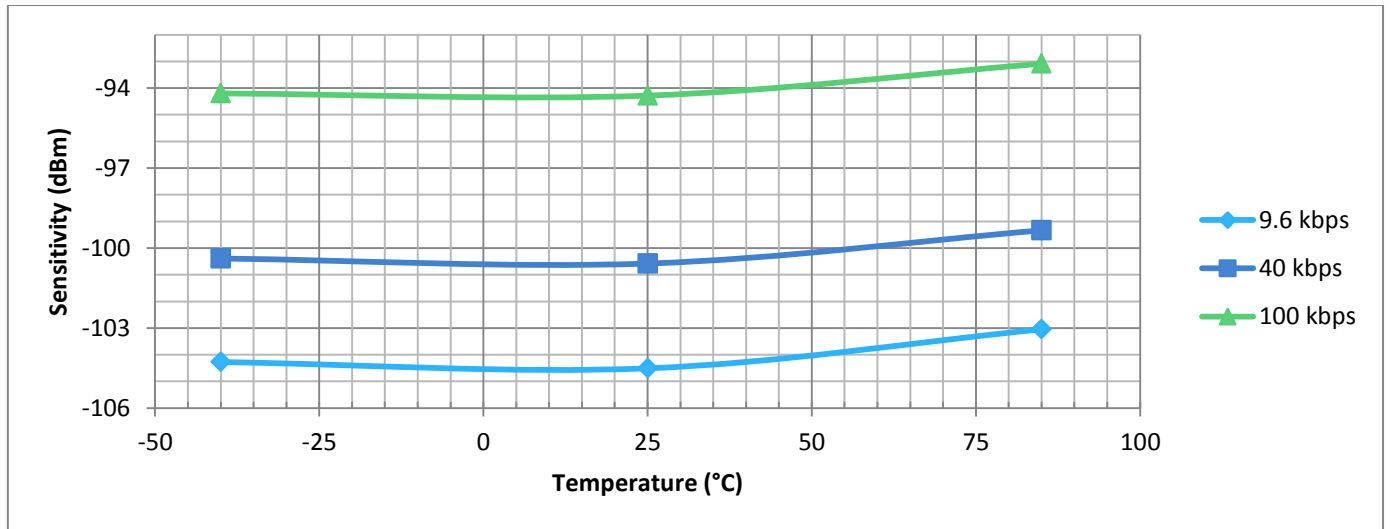


Figure 5.4: Typical sensitivity vs. temperature

Table 5.22: Receiver performance

| Symbol | Description | Min | Typ | Max | Unit |
|--------------------------------|---|-----|-------|-------|------|
| CCR_{9.6} | Co-channel rejection, 9.6kbps | - | -4.4 | - | dBc |
| BI_{1MHz-9.6} | Blocking immunity ² at $\Delta f=1\text{MHz}$, 9.6kbps | - | 45.0 | - | dBc |
| BI_{2MHz-9.6} | Blocking immunity at $\Delta f=2\text{MHz}$, 9.6kbps | - | 51.8 | - | dBc |
| BI_{5MHz-9.6} | Blocking immunity at $\Delta f=5\text{MHz}$, 9.6kbps | - | 69.8 | - | dBc |
| BI_{10MHz-9.6} | Blocking immunity at $\Delta f=10\text{MHz}$, 9.6kbps | - | 74.1 | - | dBc |
| BI_{100MHz-9.6} | Blocking immunity at $\Delta f=100\text{MHz}$, 9.6kbps | - | 80.9 | - | dBc |
| CCR₄₀ | Co-channel rejection, 40kbps | - | -9.3 | - | dBc |
| BI_{1MHz-40} | Blocking immunity at $\Delta f=1\text{MHz}$, 40kbps | - | 41.0 | - | dBc |
| BI_{2MHz-40} | Blocking immunity at $\Delta f=2\text{MHz}$, 40kbps | - | 47.4 | - | dBc |
| BI_{5MHz-40} | Blocking immunity at $\Delta f=5\text{MHz}$, 40kbps | - | 64.8 | - | dBc |
| BI_{10MHz-40} | Blocking immunity at $\Delta f=10\text{MHz}$, 40kbps | - | 68.6 | - | dBc |
| BI_{100MHz-40} | Blocking immunity at $\Delta f=100\text{MHz}$, 40kbps | - | 75.6 | - | dBc |
| CCR₁₀₀ | Co-channel rejection, 100kbps | - | -8.1 | - | dBc |
| BI_{1MHz-100} | Blocking immunity at $\Delta f=1\text{MHz}$, 100kbps | - | 35.1 | - | dBc |
| BI_{2MHz-100} | Blocking immunity at $\Delta f=2\text{MHz}$, 100kbps | - | 43.3 | - | dBc |
| BI_{5MHz-100} | Blocking immunity at $\Delta f=5\text{MHz}$, 100kbps | - | 57.9 | - | dBc |
| BI_{10MHz-100} | Blocking immunity at $\Delta f=10\text{MHz}$, 100kbps | - | 63.1 | - | dBc |
| BI_{100MHz-100} | Blocking immunity at $\Delta f=100\text{MHz}$, 100kbps | - | 68.9 | - | dBc |
| RSSI_{RANGE} | Dynamic range of the RSSI measurement | - | 70.0 | - | dB |
| RSSI_{LSB} | Resolution of the RSSI measurement | - | 1.5 | - | dB |
| P_{LO} | LO leakage at $\Delta f=200\text{kHz}$ and $\Delta f=325\text{kHz}$ | - | -80.4 | -76.1 | dBm |
| IIP3 | Input 3 rd order intercept point | - | -12.0 | - | dBm |
| BW_{9.6} | Intermediate frequency filter bandwidth, 9.6kbps | - | 300.0 | - | kHz |
| BW₄₀ | Intermediate frequency filter bandwidth, 40kbps | - | 300.0 | - | kHz |
| BW₁₀₀ | Intermediate frequency filter bandwidth, 100kbps | - | 600.0 | - | kHz |

² Blocker level is defined relative to the wanted receiving signal and measured with the wanted receiving signal 3dB above the sensitivity level

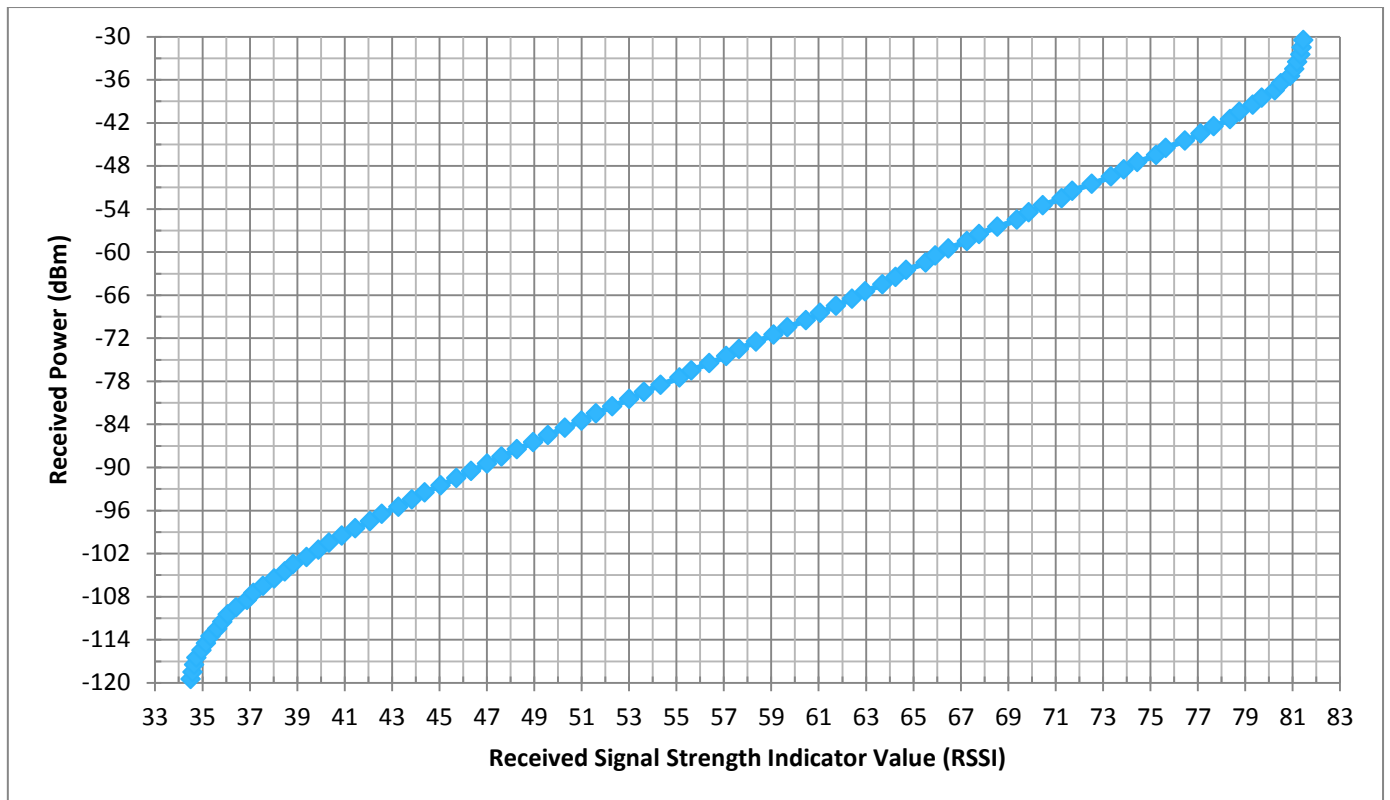


Figure 5.5: Typical input power vs. RSSI value

First-order approximation:

$$\text{Received Power [dBm]} \approx 1.55 \times \text{RSSI} - 162.69, \quad \text{where RSSI} \in [40, 80]$$

5.9.3 REGULATORY COMPLIANCE

The ZM5101 SiP has been tested on the ZDP03A Z-Wave Development Platform to be compliant with the following regulatory standards. [4]

- **ACMA COMPLIANCE**
 - AS/NZS 4268
 - CISPR 22
- **CE COMPLIANCE**
 - EN 300 220-1/2
 - EN 301 489-1/3
 - EN 55022
 - EN 60950-1
 - EN 61000-4-2/3
 - EN 62479
- **FCC COMPLIANCE**
 - FCC CFR 47 Part 15 Subpart C §15.249
- **IC COMPLIANCE**
 - RSS-GEN
 - RSS-210
 - ANSI C63.10
- **MIC COMPLIANCE**
 - ARIB STD-T108

6 Z-WAVE FREQUENCIES

Table 6.1: Z-Wave RF specification

| Data rate | 9.6kbps | 40kbps | 100kbps | |
|----------------------|------------------------------|--------------------------|--|---|
| Modulation | Frequency Shift Keying (FSK) | FSK | Gaussian Frequency Shift Keying (GFSK) | |
| Frequency deviation | $f_c \pm 20\text{kHz}$ | $f_c \pm 20\text{kHz}$ | $f_c \pm 29.3\text{kHz}$ | |
| Coding | Manchester encoded | Non-return to Zero (NRZ) | NRZ | |
| United Arab Emirates | 868.42 MHz | 868.40 MHz | 869.85 MHz | E |
| Australia | 921.42 MHz | 921.40 MHz | 919.80 MHz | H |
| Brazil | 921.42 MHz | 921.40 MHz | 919.80 MHz | H |
| Canada | 908.42 MHz | 908.40 MHz | 916.00 MHz | U |
| Chile | 908.42 MHz | 908.40 MHz | 916.00 MHz | U |
| China | 868.42 MHz | 868.40 MHz | 869.85 MHz | E |
| European Union | 868.42 MHz | 868.40 MHz | 869.85 MHz | E |
| Hong Kong | 919.82 MHz | 919.80 MHz | 919.80 MHz | H |
| Israel | 916.02 MHz | 916.00 MHz | - | U |
| India | 865.20 MHz | 865.20 MHz | 865.20 MHz | E |
| Japan | - | - | 922.50 MHz | H |
| | - | - | 923.90 MHz | H |
| | - | - | 926.30 MHz | H |
| Korea | - | - | 919.70 MHz | H |
| | - | - | 921.70 MHz | H |
| | - | - | 923.10 MHz | H |
| Mexico | 908.42 MHz | 908.40 MHz | 916.00 MHz | U |
| Malaysia | 868.12 MHz | 868.10 MHz | 868.10 MHz | E |
| New Zealand | 921.42 MHz | 921.40 MHz | 919.80 MHz | H |
| Russia | 869.02 MHz | 869.00 MHz | - | E |
| Singapore | 868.42 MHz | 868.40 MHz | 869.85 MHz | E |
| Taiwan | - | - | 922.50 MHz | H |
| | - | - | 923.90 MHz | H |
| | - | - | 926.30 MHz | H |
| United States | 908.42 MHz | 908.40 MHz | 916.00 MHz | U |
| South Africa | 868.42 MHz | 868.40 MHz | 869.85 MHz | E |

7 MODULE INFORMATION

7.1 MODULE MARKING



Figure 7.1: Marking placement

Table 7.1: Marking description

| | |
|--------------------------------|--------------------------------------|
| Device name | ZM5101 |
| Production code and lot number | LLLLLLLLLLLLL |
| Date | YY: Year WW: Week TWN: Country |

8 PROCESS SPECIFICATION

| Specification | Description |
|---------------|---|
| MSL 3 | Moisture Sensitivity Level tested according to JEDEC J-STD-020C |
| REACH | REACH is a European Community Regulation on chemicals and their safe use (EC 1907/2006). It deals with the Registration, Evaluation, Authorisation and Restriction of Chemical substances |
| RoHS | Designed in compliance with The Restriction of Hazardous Substances Directive (RoHS) |

9 PCB MOUNTING AND SOLDERING

9.1 RECOMMENDED PCB MOUNTING PATTERN

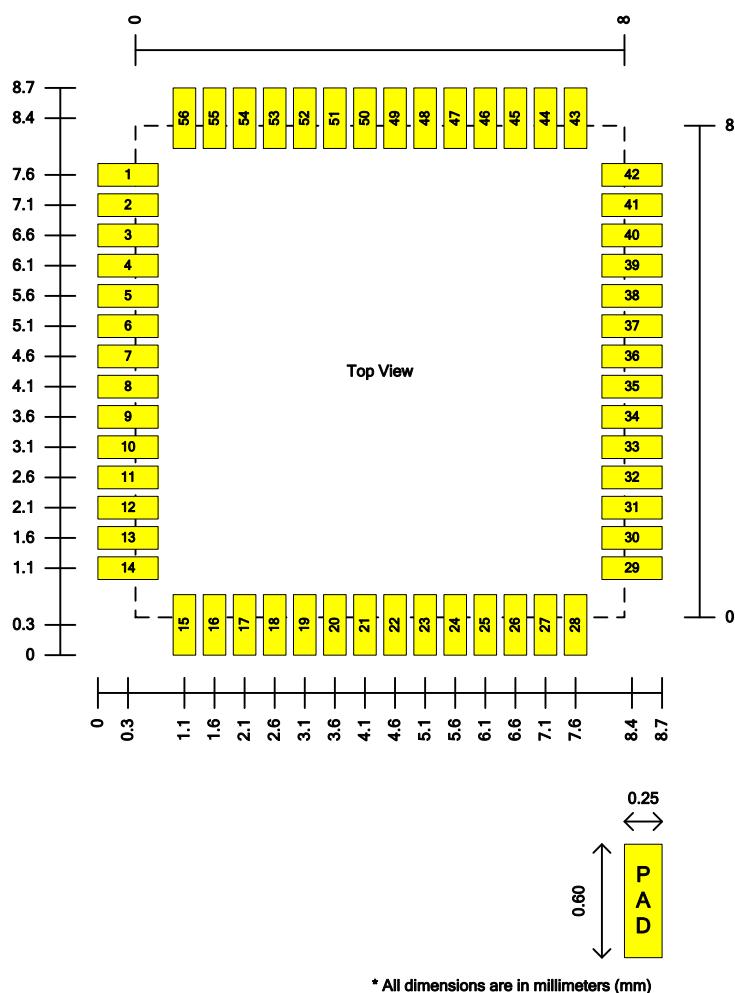


Figure 9.1: Top view of land pattern

9.2 SOLDERING INFORMATION

The soldering details to properly solder the ZM5101 module on standard PCBs are described below. The information provided is intended only as a guideline and Sigma Designs is not liable if a selected profile does not work.

See IPC/JEDEC J-STD-020D.1 for more information.

Table 9.1: Soldering details

| | |
|--|---|
| PCB solder mask expansion from landing pad edge | 0.1 mm |
| PCB paste mask expansion from landing pad edge | 0.0 mm |
| PCB process | Pb-free (Lead free for RoHS ³ compliance) |
| PCB finish | Defined by the manufacturing facility (EMS) or customer |
| Stencil aperture | Defined by the manufacturing facility (EMS) or customer |
| Stencil thickness | Defined by the manufacturing facility (EMS) or customer |
| Solder paste used | Defined by the manufacturing facility (EMS) or customer |
| Flux cleaning process | Defined by the manufacturing facility (EMS) or customer |

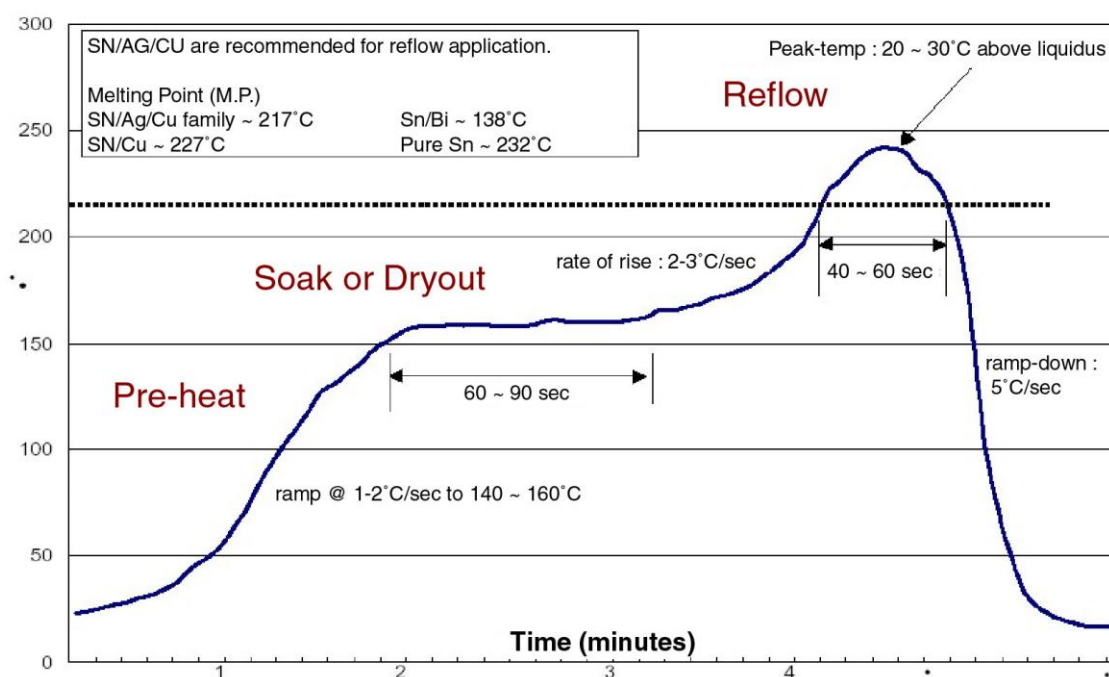


Figure 9.2: Typical reflow profile

³ RoHS = Restriction of Hazardous Substances Directive, EU

10 ORDERING INFORMATION**Table 10.1: Ordering codes**

| Orderable Device | Status | Package Type | Pins | Minimum Order Quantity | Description |
|----------------------|--------|--------------|------|------------------------|--|
| ZM5101A-CME3R | ACTIVE | SiP | 56 | 2000 pcs. | ZM5101 SiP Module, RevA, Tape and Reel |

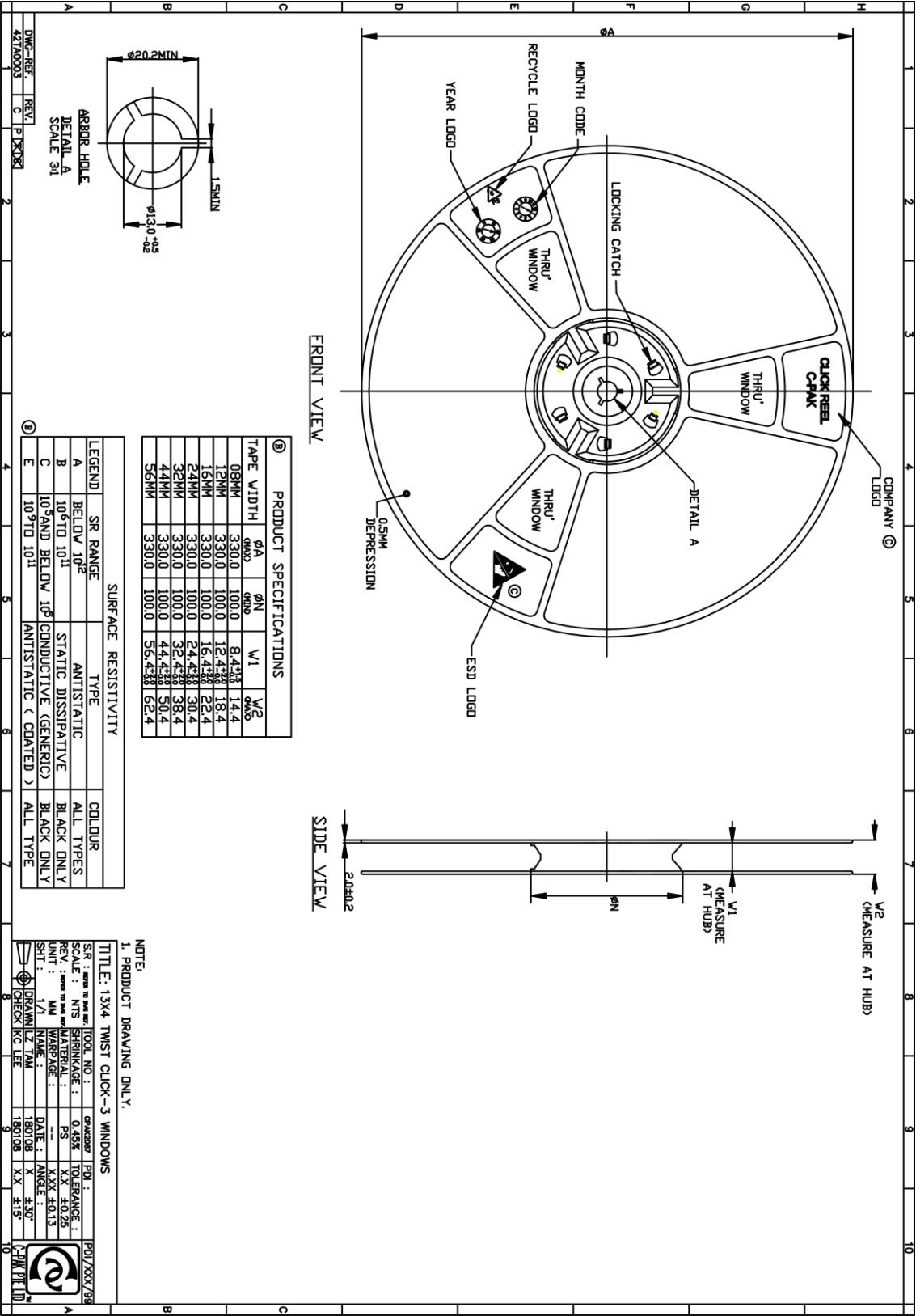
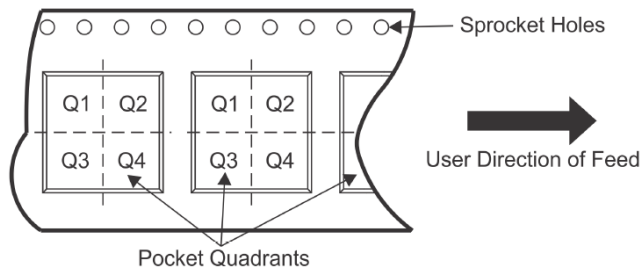


Figure 10.2: Reel Information

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



| Parameter | Value |
|----------------|--------------------|
| Pin 1 Quadrant | Pocket Quadrant Q1 |

11 ABBREVIATIONS

| Abbreviation | Description |
|--------------|--|
| 2FSK | 2-key Frequency Shift Keying |
| 2GFSK | 2-key Gaussian Frequency Shift Keying |
| ACM | Abstract Control Model |
| ACMA | Australian Communications and Media Authority |
| ADC | Analog-to-Digital Converter |
| AES | Advanced Encryption Standard |
| API | Application Programming Interface |
| APM | Auto Programming Mode |
| AV | Audio Video |
| BOD | Brown-Out Detector |
| CBC | Cipher-Block Chaining |
| CDC | Communications Device Class |
| CE | Conformité Européenne |
| COM | Communication |
| CPU | Central Processing Unit |
| CRC | Cyclic Redundancy Check |
| D | Differential |
| D- | Differential Minus |
| D+ | Differential Plus |
| DAC | Digital-to-Analog Converter |
| DC | Direct Current |
| DMA | Direct Memory Access |
| ECB | Electronic CodeBook |
| EMS | Electronic Manufacturing Services |
| FCC | Federal Communications Commission |
| FER | Frame Error Rate |
| FET | Field Effect Transistor |
| FLIRS | Frequently Listening Routing Slave |
| FSK | Frequency Shift Keying |
| GFSK | Gaussian Frequency Shift Keying |
| GP | General Purpose |
| GPIO | General Purpose Input Output |
| I | Input |
| I/O | Input / Output |
| IC | Integrated Circuit |
| IF | Intermediate Frequency |
| IGBT | Insulated-Gate Bipolar Transistor |
| INT | Interrupt |
| IPC | Interconnecting and Packaging Circuits |
| IR | Infrared |
| IRAM | Indirectly addressable Random Access Memory |
| ISM | Industrial, Scientific, and Medical |
| ISP | In-System Programming |
| ITU | International Telecommunications Union |
| JEDEC | Joint Electron Device Engineering Council |
| LED | Light-Emitting Diode |
| lsb | Least Significant Bit |
| LSB | Least Significant Byte |
| MCU | Micro-Controller Unit |
| MIC | Ministry of Internal affairs and Communications, Japan |
| MISO | Master In, Slave Out |

| Abbreviation | Description |
|--------------|---|
| MOSI | Master Out, Slave In |
| msb | Most Significant Bit |
| MSB | Most Significant Byte |
| NMI | Non-Maskable Interrupt |
| NRZ | Non-Return-to-Zero |
| NVM | Non-Volatile Memory |
| NVR | Non-Volatile Registers |
| O | Output |
| OEM | Original Equipment Manufacturer |
| OFB | Output FeedBack |
| Pb | Lead |
| PCB | Printed Circuit Board |
| POR | Power-On Reset |
| PWM | Pulse Width Modulator |
| RAM | Random Access Memory |
| RF | Radio Frequency |
| RoHS | Restriction of Hazardous Substances |
| ROM | Read Only Memory |
| RS-232 | Recommended Standard 232 |
| RX | Receive |
| S | Supply |
| SAW | Surface Acoustic Wave |
| SCK | Serial Clock |
| SFR | Special Function Register |
| SiP | System-in-Package |
| SPI | Serial Peripheral Interface |
| SRAM | Static Random Access Memory |
| T0 | Timer 0 |
| T1 | Timer 1 |
| TX | Transmit |
| UART | Universal Asynchronous Receiver Transmitter |
| USB | Universal Serial Bus |
| WUT | Wake-Up Timer |
| XRAM | External Random Access Memory |
| XTAL | Crystal |
| ZEROX | Zero Crossing |

12 REVISION HISTORY

| Date | Version | Affected | Revision |
|------------|---------|------------------------------------|--|
| 2016/12/21 | 8 | Table 5.5 | Cleaned up “TBD” values |
| 1015/07/27 | 7 | Figure 9.1 | Updated to align with assembly manufactures recommendation. |
| | | Table 9.2 | Removed – information included in updated Figure 9.1 |
| | | §8 | Added section Process Specification |
| | | §10.1 | Added orientation of component in tape |
| | | Table 5.6 | Max $I_{DD_SLEEP} = 1.6 \mu A$ added |
| | | Table 5.3 | $T_{STORAGE}$ added |
| 2013/12/13 | 6 | Table 2.1 | Entries in table of CPU modes rephrased |
| 2013/12/12 | 5A | Table 2.1, | Reduced the reset high period |
| | | §2.4.1 | Increased the RESET_N low period |
| 2013/11/27 | 4A | Table 10.1, | Changed to tape and reel only |
| | | §10.1 | Added the tape and reel information |
| 2013/10/31 | 3A | §Cover, | Updated performance values |
| | | Table 2.1, | Added method of entering reset mode |
| | | Table 2.3, | Updated INT1 pins |
| | | Figure 2.10, | Added termination resistor value |
| | | Figure 2.11, | Updated caption |
| | | Table 4.10, | Added timer pins |
| | | §5.1, | Updated final test description |
| | | Table 5.20, | Updated TX performance values |
| | | Figure 5.3, | Updated TX power curve |
| | | Table 5.22, | Updated LO leakage values |
| | | §5.9.2 | Updated equation for 1 st -order approximation |
| 2013/10/29 | 2D | Table 5.5, | Updated limits of current consumption |
| | | Table 5.20, Table 5.21, Table 5.22 | Updated limits of the transmitter and receiver |
| 2013/10/28 | 2C | §Cover, | Corrected the transmit power inconsistency |
| | | Figure 5.2 | |
| 2013/10/22 | 2B | §Cover, | Updated picture of ZM5101, adjusted the heading width, fixed typo |
| | | §2.1, | Added statement to link to CPU modes |
| | | Figure 2.4, Table 2.3, | Changed to using “pin” for non GPIOs, corrected the INT1 pins |
| | | § 2.2.10, | Changed to 128 keys, updated table and diagram to show 16 columns |
| | | Table 2.5, | Corrected the drive strength |
| | | Table 2.6, | Changed the GPIO state of INT1 and Keypad Scan Controller |
| | | Table 2.7, | Added Slave Select |
| | | Figure 2.7, Figure 2.8, | Changed GPIO to PX.Y, added diagram with ZM5101 as slave |
| | | §2.2.18, | Updated the precision of the WUT |
| | | §2.4.2, | Removed the word serial |
| | | Figure 3.1, | Changed GPIO to PX.Y |
| | | §4.1, | Added the peripheral name to reset state of pins 51, 52, 53, and 54, changed TRIAC to dimmer in the active state |
| | | Figure 5.2, | Corrected the decimal places |
| | | §7.1, | Updated the with picture of the marking |
| | | §9.2 | Corrected the precision and symbols |
| 2013/10/21 | 2A | §2.1, | Added CPU modes |
| | | Figure 2.1, | Changed matching block to transceiver matching |
| | | Table 5.1, | Added maximum RF input power |
| | | §5.4, | Updated the temperature and voltage range |

| Date | Version | Affected | Revision |
|------------|---------|---|---|
| | | Table 5.5, Figure 5.2, Table 5.12, Table 5.16, Table 5.18, Table 5.20, Figure 5.3, Table 5.21, Figure 5.4, Table 5.22, Figure 5.5, §5.9.1, §5.9.3, Table 5.17, Table 5.19, §13 | Update with measurement values of current consumption Update graph of TX current consumption Added full Flash programming time Added internal pull-up resistor values Added harmonic power levels Updated TX power graph Updated sensitivity with measurement values Updated sensitivity graph Added blocking power levels for different bit-rates Updated RSSI graph Added mandatory TX calibration Updated regulatory standards Added high power pin information Removed invalid references and changed format |
| 2013/08/06 | 1C | §All | Fixed front page description and minor corrections in the tables |
| 2013/08/05 | 1B | §All | Added list of abbreviations |
| 2013/08/02 | 1A | §All | Made minor corrections throughout the document Initial draft |

13 REFERENCES

- [1] INS11681, Instruction, "500 Series Z-Wave Single Chip Programming Mode"
- [2] DSH12571, Datasheet, "ZDB5101 Z-Wave Development Board"
- [3] INS12213, Instruction, "500 Series Hardware Integration Guide"
- [4] DSH11243, Datasheet, "ZDP03A, Z-Wave Development Platform"

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HEADQUARTERS

Sigma Designs, Inc.

1778 McCarthy Blvd. Milpitas, CA 95035

Tel: +1.408.262.9003 Fax: +1.408.957.9740

www.sigmadesigns.com

sales@sigmadesigns.com