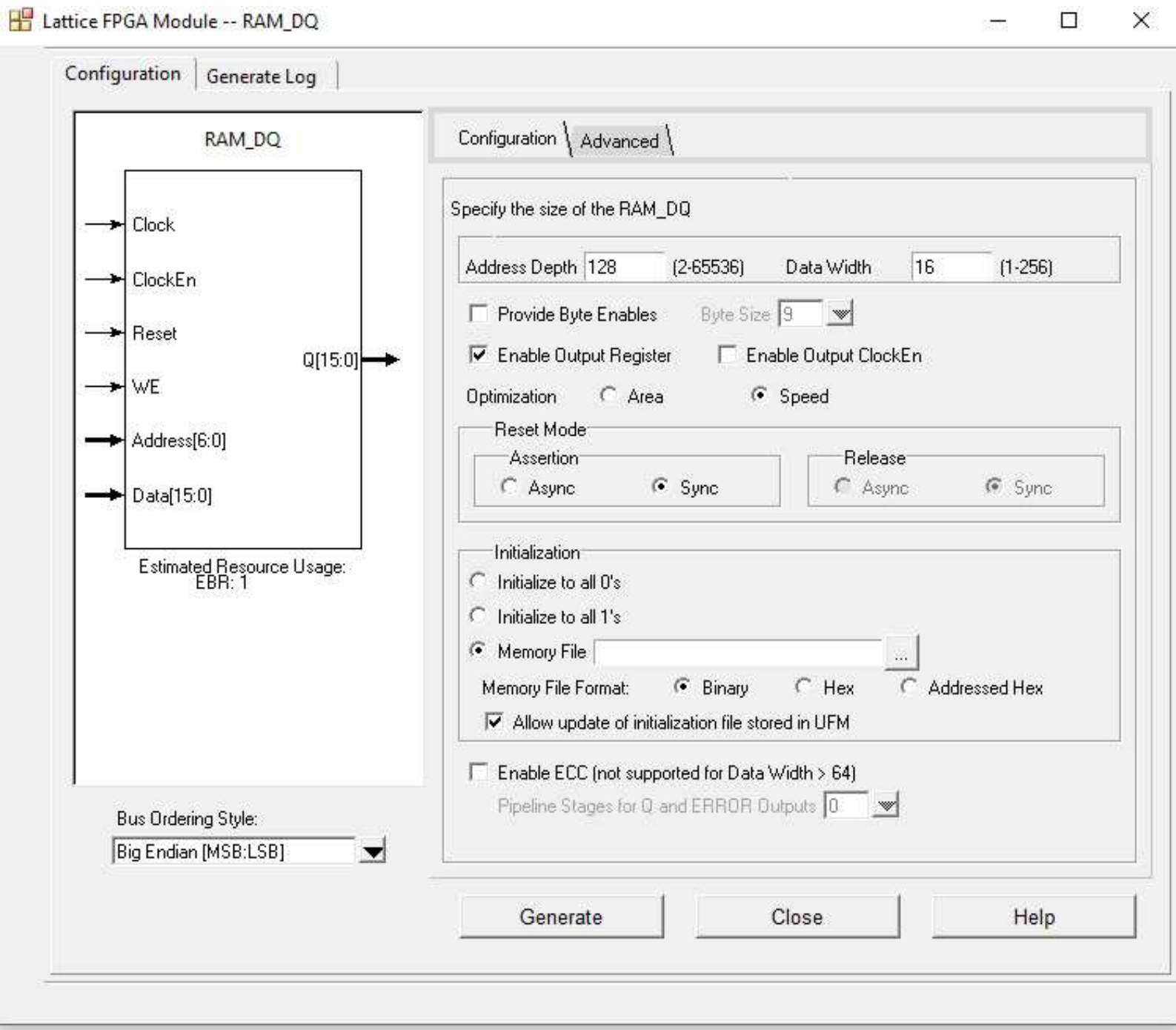
Lattice FPGA Module -- RAM_DQ
Configuration
Generate Log
RAM_DQ
Clock
ClockEn
Reset
WE
Address[6:0]
Data[15:0]
Q[15:0]
Estimated Resource Usage:
EBR: 1
Bus Ordering Style:
Big Endian [MSB:LSB]
Configuration
Advanced
Specify the size of the RAM_DQ
Address Depth 128 (2-65536)
Data Width 16 (1-256)
Provide Byte Enables
Byte Size 9
Enable Output Register
Enable Output ClockEn
Optimization
Area
Speed
Reset Mode
Assertion
Async
Sync
Release
Async
Sync
Initialization
Initialize to all 0's
Initialize to all 1's
Memory File
...
Memory File Format:
Binary
Hex
Addressed Hex
Allow update of initialization file stored in UFM
Enable ECC (not supported for Data Width > 64)
Pipeline Stages for Q and ERROR Outputs 0
Generate
Close
Help